3 A, 36 V, Synchronous Step-Down DC-to-DC Regulator

Data Sheet

ADP2443

FEATURES

- Continuous output current: 3 A
- Input voltage: 4.5 V to 36 V
- Integrated MOSFETs: 98 mΩ/35 mΩ
- Reference voltage: 0.6 V ± 1%
- Fast minimum on time: 50 ns
- Programmable switching frequency: 200 kHz to 1.8 MHz
- Synchronizes to external clock: 200 kHz to 1.8 MHz
- Precision enable and power good
- Cycle-by-cycle current limit with hiccup protection
- External compensation
- Programmable soft start time
- Startup into a precharged output
- Supported by ADIsimPower design tool

APPLICATIONS

- Intermediate power rail conversion
- Multicell battery powered systems
- Process control and industrial automation
- Healthcare and medical
- Networking and servers

TYPICAL APPLICATION CIRCUIT

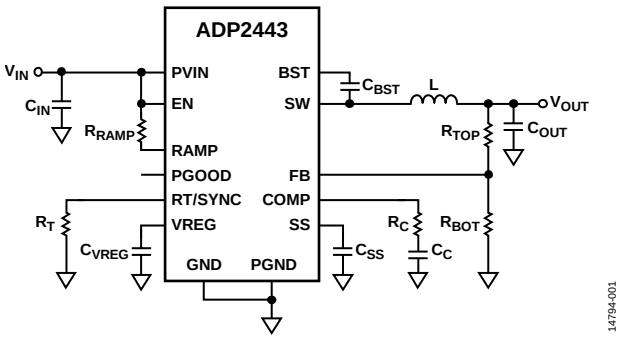

Figure 1.

GENERAL DESCRIPTION

The ADP2443 is synchronous step-down, dc-to-dc regulator with an integrated 98 mΩ, high-side power metal oxide semiconductor field effect transistor (MOSFET) and a 35 mΩ, synchronous rectifier MOSFET to provide a high efficiency solution in a compact 4 mm × 4 mm LFCSP package. The regulators operate from an input voltage range of 4.5 V to 36 V. The output voltage can be adjusted down to 0.6 V and deliver up to 3 A of continuous current. The fast 50 ns minimum on time allows the regulators convert high input voltage to low output voltage at high frequency.

The ADP2443 uses an emulated current mode, constant frequency pulse-width modulation (PWM) control scheme for excellent stability and transient response. The switching frequency of the ADP2443 can be programmed from 200 kHz to 1.8 MHz. The synchronization function allows the switching frequency be synchronized with an external clock to minimize the system noise.

The ADP2443 targets high performance applications that require high efficiency and design flexibility. External compensation and an adjustable soft start function provide design flexibility. The power-good output and precision enable input provide simple and reliable power sequencing.

Other key features include undervoltage lockout (UVLO), overvoltage protection (OVP), overcurrent protection (OCP), short-circuit protection (SCP), and thermal shutdown (TSD).

The ADP2443 operates over the −40°C to +125°C operating junction temperature range and is available in a 24-lead, 4 mm × 4 mm LFCSP package.

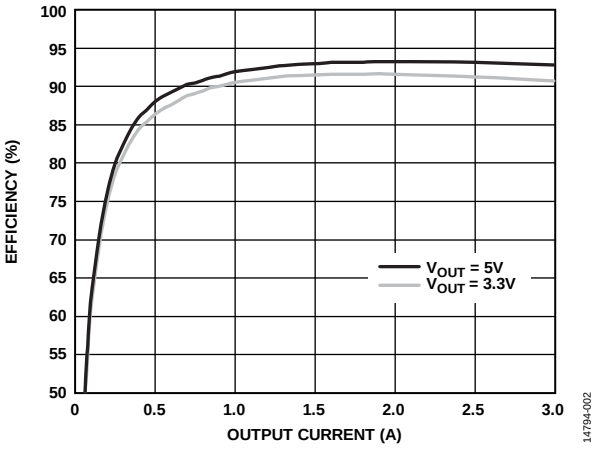

Figure 2. Efficiency vs. Output Current, V_{IN} = 24 V, f_{SW} = 300 kHz

Rev. 0 Document Feedback

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REVISION HISTORY

9/2016—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

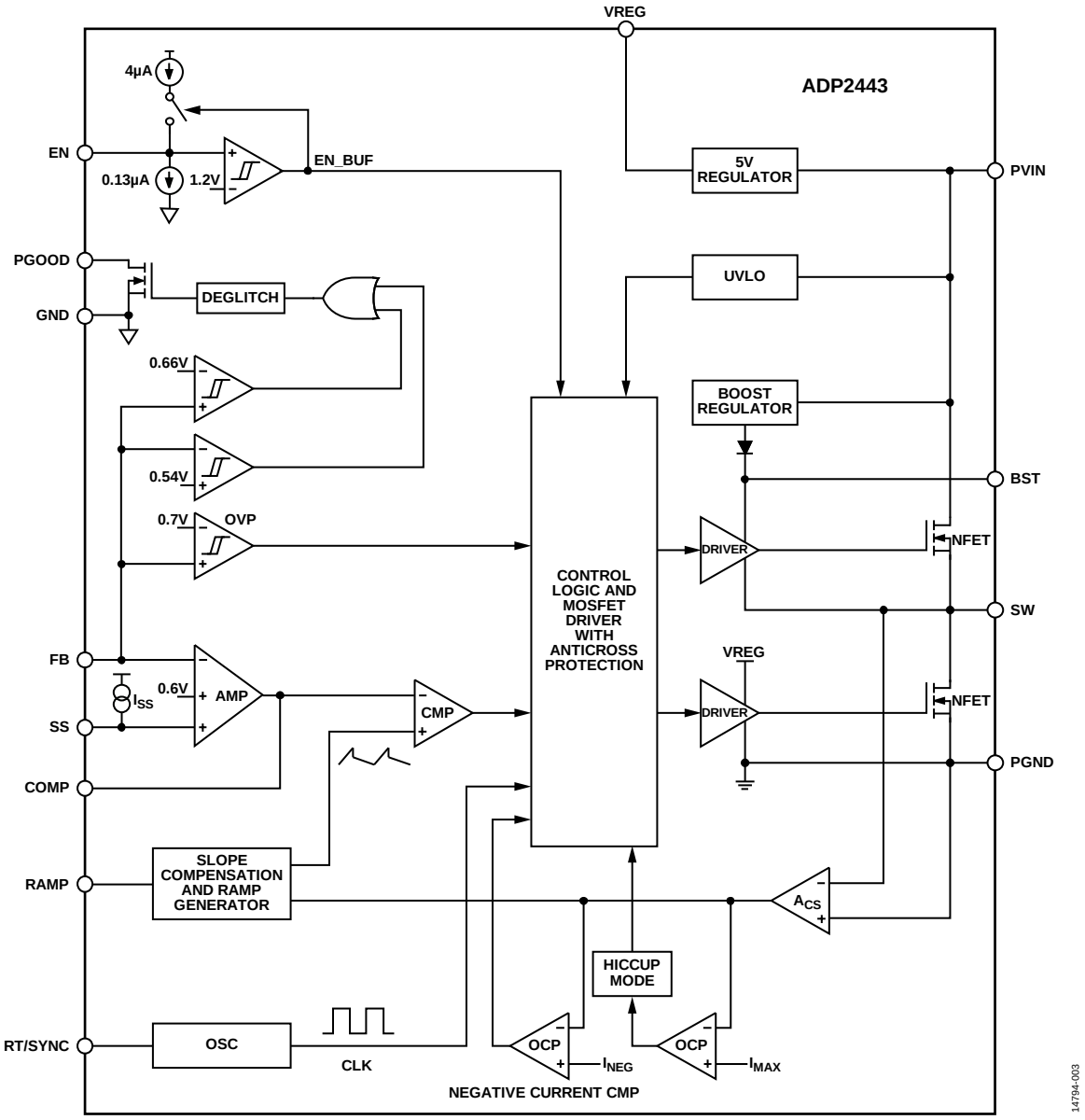

Figure 3.

SPECIFICATIONS

V_{PVIN} = 12 V, T_J = −40°C to +125°C for minimum/maximum specifications, T_A = 25°C for typical specifications, unless otherwise noted.

Table 1.

Parameters	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
PVIN						
PVIN Voltage Range	V_{PVIN}		4.5		36	V
Quiescent Current	I_Q	No switching, RAMP connected to PVIN through a resistor		0.868	1.1	mA
Shutdown Current	I_{SHDN}	EN = GND		28	57	µA
PVIN Undervoltage Lockout Threshold		PVIN rising		4.3	4.45	V
		PVIN falling	3.8	3.9		V
FB						
Regulation Voltage	V_{FB}	−40°C < T_J < +125°C	0.594	0.6	0.606	V
Bias Current	I_{FB}			0.05	0.2	µA
ERROR AMPLIFIER (EA)						
Transconductance	g_m		485	515	545	µS
Source Current	I_{SOURCE}	V_{FB} = 0.45 V		50		µA
Sink Current	I_{SINK}	V_{FB} = 0.75 V		50		µA
INTERNAL REGULATOR (VREG)						
VREG Voltage	V_{VREG}	V_{PVIN} = 12 V, I_{VREG} = 10 mA	4.9	5	5.1	V
Dropout Voltage		V_{PVIN} = 12 V, I_{VREG} = 30 mA		320		mV
Regulator Current Limit				100		mA
SW						
High-Side On Resistance[1]	R_{DSON_HS}	BST pin voltage (V_{BST}) − V_{SW} = 5 V		98	147	mΩ
Low-Side On Resistance[1]	R_{DSON_LS}	V_{VREG} = 5 V		35	58	mΩ
Low-Side Valley Current Limit			3.9	4.7	5.1	A
Low-Side Negative Current Limit			2	2.5	3	A
Leakage Current		V_{SW} = 0 V, EN = GND		1.5	7.9	µA
SW Minimum On Time	t_{MIN_ON}			50	65	ns
SW Minimum Off Time	t_{MIN_OFF}			200	235	ns
BST						
Bootstrap Voltage	V_{BOOT}		4.65	5	5.2	V
OSCILLATOR (RT/SYNC)						
Switching Frequency	f_{SW}	R_T = 280 kΩ	540	600	660	kHz
Switching Frequency Range			200		1800	kHz
Synchronization Range			200		1800	kHz
SYNC Minimum Pulse Width			100			ns
SYNC Minimum Off Time			100			ns
SYNC Input Voltage						
High			1.3			V
Low					0.4	V
SS						
SS Pin Pull-Up Current	I_{SS}		3.0	3.4	3.8	µA
PGOOD						
Power-Good Range						
FB Rising Threshold			108	110	112	%
FB Rising Hysteresis				5		%
FB Falling Threshold			88	90	92	%
FB Falling Hysteresis				5		%
Power-Good Deglitch Time		Both rising and falling		16		Clock cycles
Power-Good Leakage Current		V_{PGOOD} = 5 V		0.1	1	µA
Power-Good Output Low Voltage		I_{PGOOD} = 1 mA		220	300	mV

Parameters	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
EN						
EN Rising Threshold			1.16	1.2	1.24	V
EN Input Hysteresis				100		mV
EN Current		EN voltage < 1.1 V, sink current		0.13		µA
		EN voltage > 1.2 V, source current		4		µA
THERMAL SHUTDOWN						
Threshold				150		°C
Hysteresis				25		°C

[1] Pin to pin measurement.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
PVIN, EN, PGOOD, RAMP	−0.3 V to +40 V
SW	−1 V to +40 V
BST	V_{SW} + 6 V
FB, SS, COMP, RT/SYNC	−0.3 V to +6 V
VREG	−0.3 V to +6 V
PGND to GND	−0.3 V to +0.3 V
Operating Junction Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Soldering Conditions	JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-24-12[1]	42.6	6.8	°C/W

[1] Thermal impedance simulated value is based on a 4-layer, JEDEC standard board.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

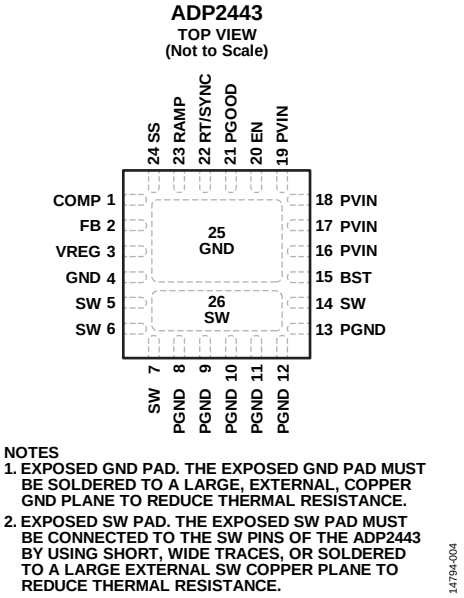

Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	COMP	Error Amplifier Output. Connect an RC network from COMP to GND.
2	FB	Feedback Voltage Sense Input. Connect this pin to a resistor divider from the output voltage (V_{OUT}).
3	VREG	Output of the Internal 5 V Regulator. The control circuits are powered from the voltage on this pin. Place a 1 µF, X7R or X5R ceramic capacitor between this pin and GND.
4	GND	Analog Ground. Return of internal control circuit.
5, 6, 7, 14	SW	Switch Node Output. Connect these pins to the output inductor.
8 to 13	PGND	Power Ground. Return of low-side power MOSFET.
15	BST	Supply Rail for the High-Side Gate Drive. Place a 0.1 µF, X7R or X5R capacitor between SW and BST.
16 to 19	PVIN	Power Input. Connect these pins to the input power source and connect a bypass capacitor between these pins and PGND.
20	EN	Precision Enable Pin. An external resistor divider can be used to set the turn-on threshold. To enable the device automatically, connect the EN pin to the PVIN pin.
21	PGOOD	Power-Good Output (Open-Drain). A pull-up resistor of 10 kΩ to 100 kΩ is recommended.
22	RT/SYNC	Frequency Setting (RT). Connect a resistor between RT and GND to program the switching frequency between 200 kHz to 1.8 MHz. Synchronization Input (SYNC). Connect this pin to an external clock to synchronize the switching frequency between 200 kHz and 1.8 MHz. See the Oscillator section and the Synchronization section for more information.
23	RAMP	Slope Compensation Setting. Connect a resistor from RAMP to PVIN to set the slope compensation.
24	SS	Soft Start Control. Connect a capacitor from SS to GND to program the soft start time.
25	EP, GND	Exposed GND Pad. The exposed GND pad must be soldered to a large, external, copper GND plane to reduce thermal resistance.
26	EP, SW	Exposed SW Pad. The exposed SW pad must be connected to the SW pins of the ADP2443 by using short, wide traces, or soldered to a large external SW copper plane to reduce thermal resistance.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 24 V, V_{OUT} = 5 V, L = 6.8 µH, C_{OUT} = 47 µF × 2, f_{SW} = 600 kHz, unless otherwise noted.

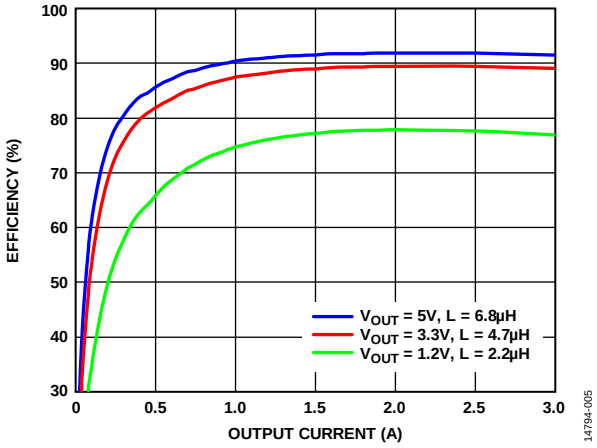

Figure 5. Efficiency at V_{IN} = 24 V, f_{SW} = 600 kHz

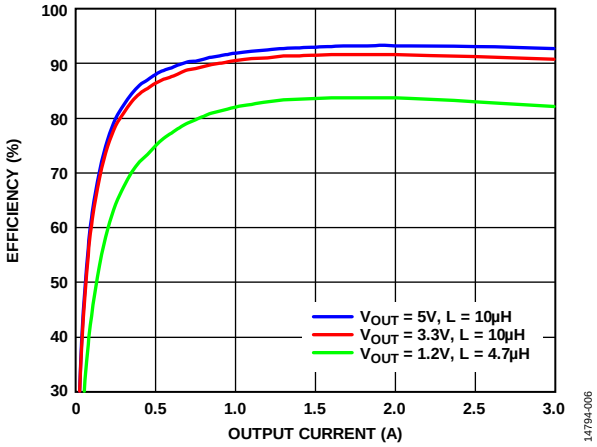

Figure 6. Efficiency at V_{IN} = 24 V, f_{SW} = 300 kHz

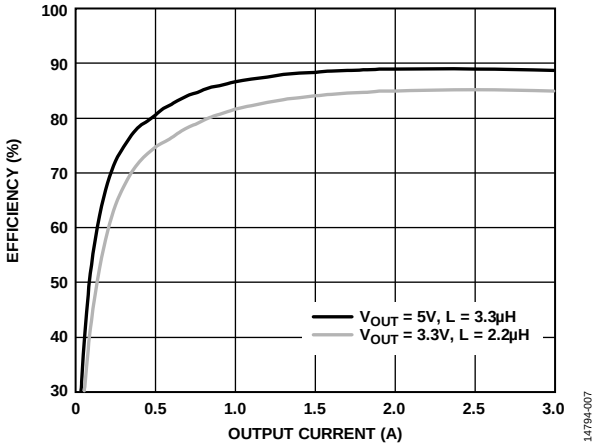

Figure 7. Efficiency at V_{IN} = 24 V, f_{SW} = 1.2 MHz

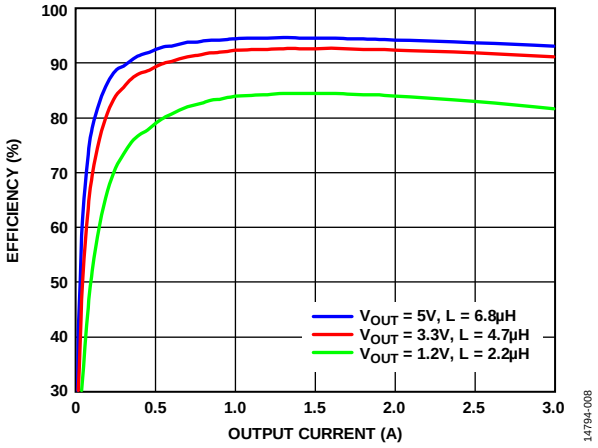

Figure 8. Efficiency at V_{IN} = 12 V, f_{SW} = 600 kHz

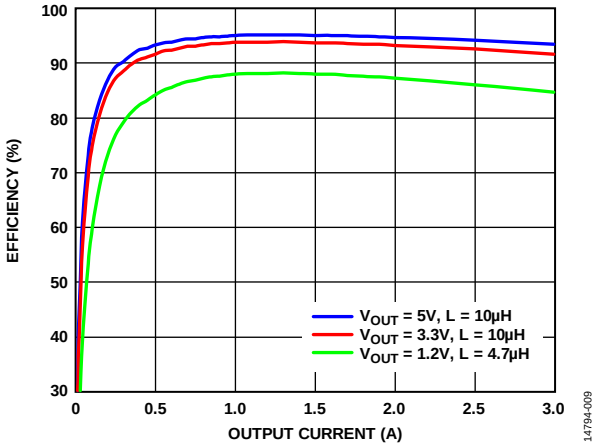

Figure 9. Efficiency at V_{IN} = 12 V, f_{SW} = 300 kHz

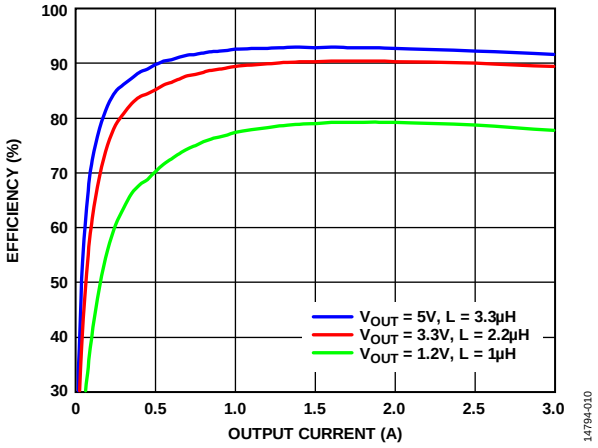

Figure 10. Efficiency at V_{IN} = 12 V, f_{SW} = 1.2 MHz

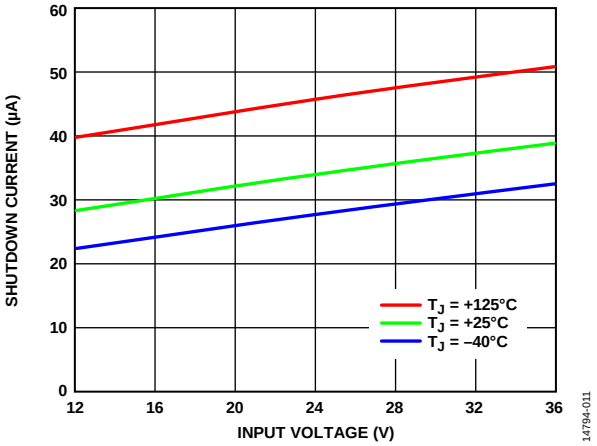

Figure 11. Shutdown Current vs. Input Voltage (V_{PVIN})

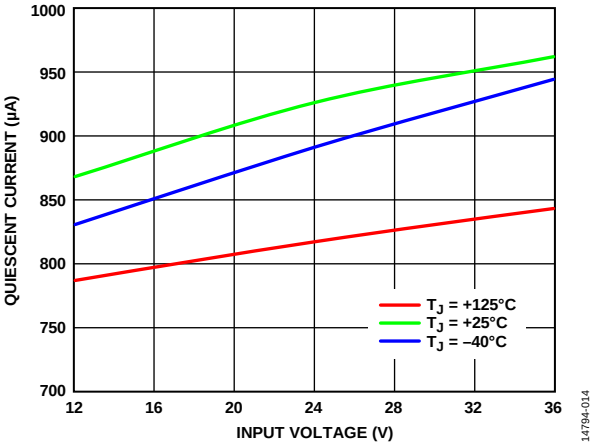

Figure 14. Quiescent Current vs. Input Voltage (V_{PVIN})

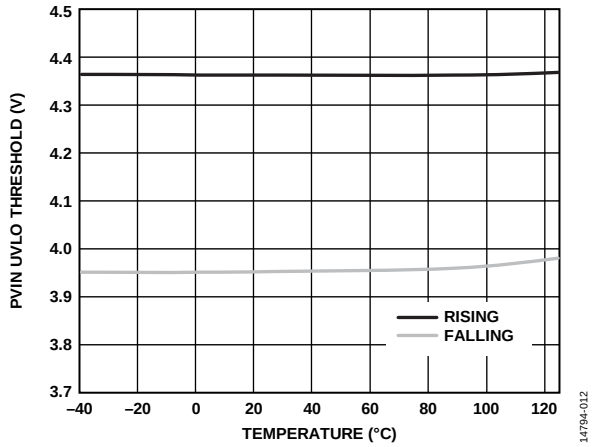

Figure 12. PVIN UVLO Threshold vs. Temperature

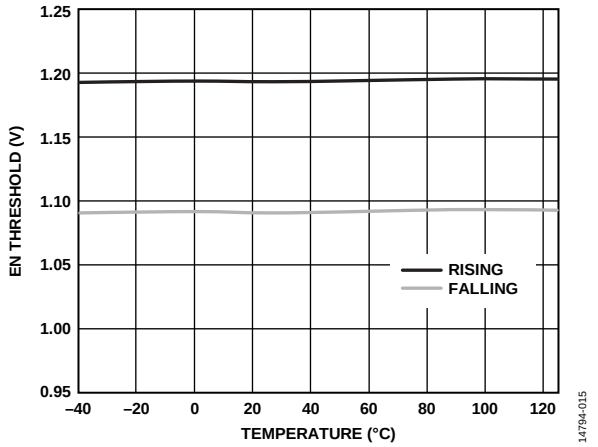

Figure 15. EN Threshold vs. Temperature

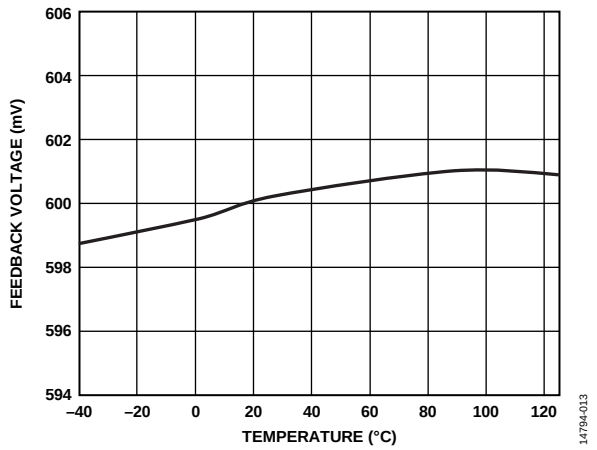

Figure 13. Feedback Voltage vs. Temperature

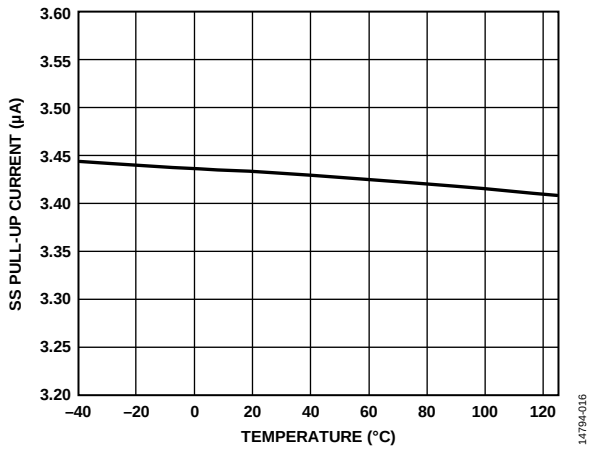

Figure 16. SS Pin Pull-Up Current vs. Temperature

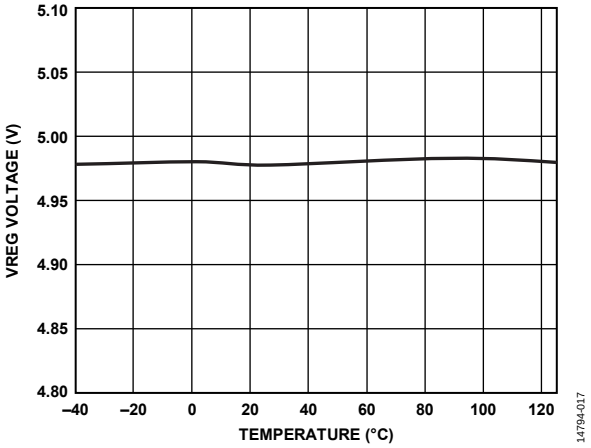

Figure 17. VREG Voltage vs. Temperature

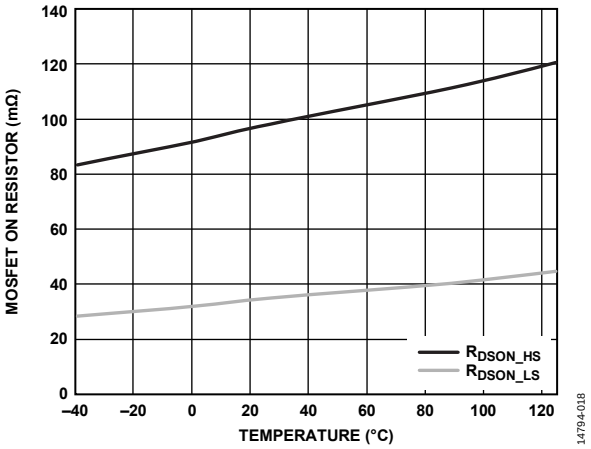

Figure 18. MOSFET On Resistor vs. Temperature

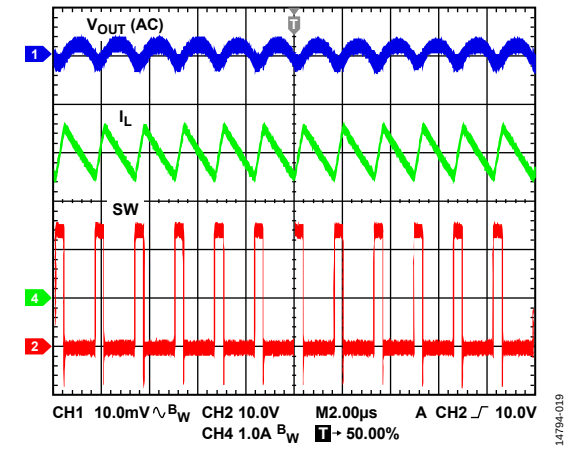

Figure 19. Working Mode Waveform

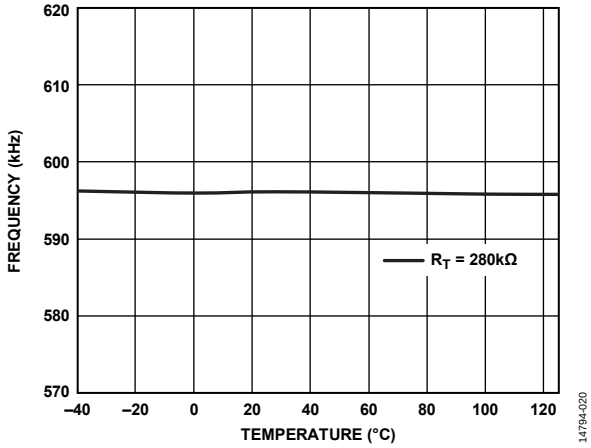

Figure 20. Frequency vs. Temperature

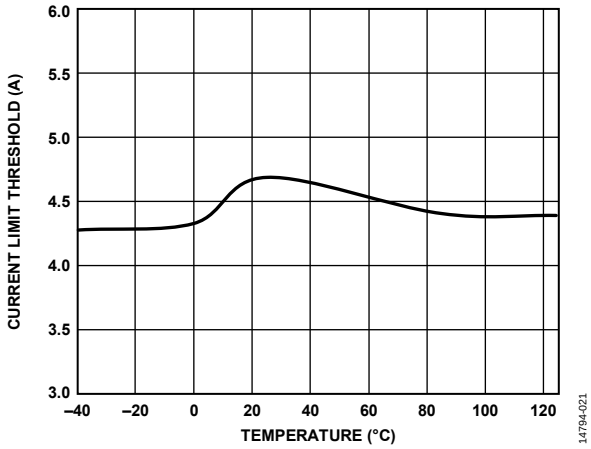

Figure 21. Current-Limit Threshold vs. Temperature

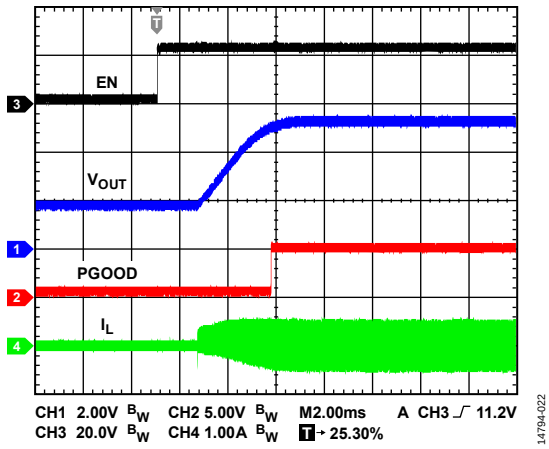

Figure 22. Voltage Precharged Output

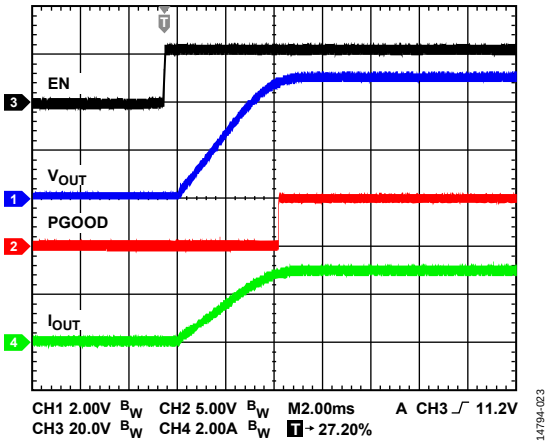

Figure 23. Soft Start with Full Load

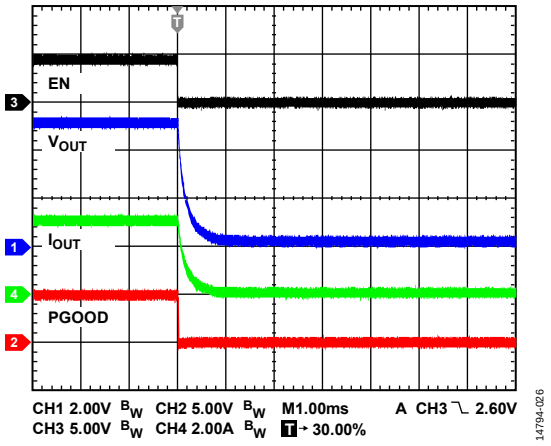

Figure 26. Shutdown with Full Load

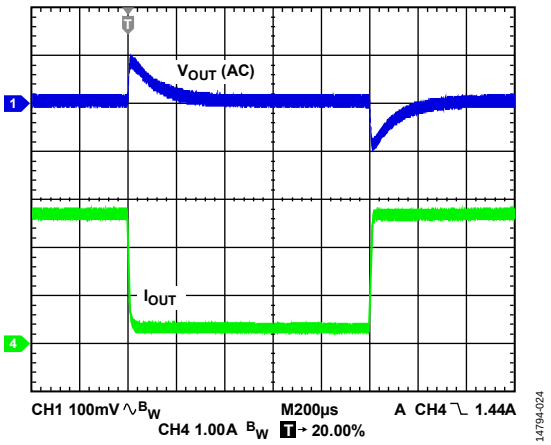

Figure 24. Load Transient Response, 0.3 A to 2.7 A

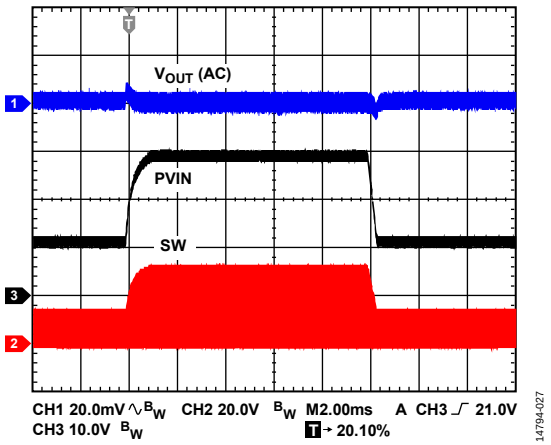

Figure 27. Line Transient Response, V_{IN} = 12 V to 30 V, I_{OUT} = 3 A

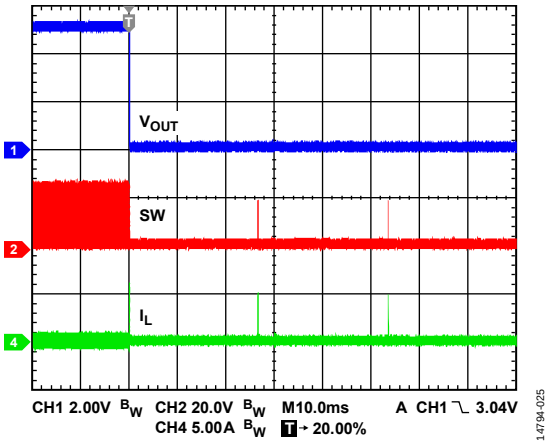

Figure 25. Output Short Entry

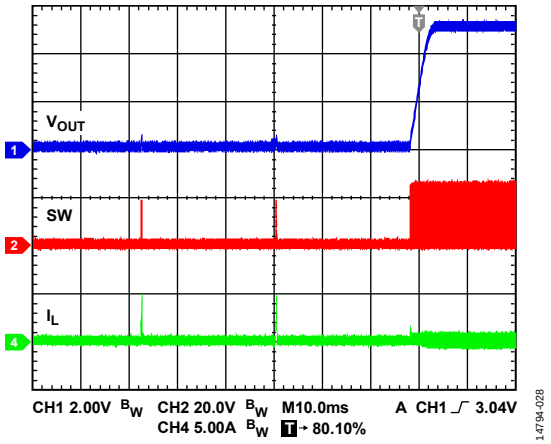

Figure 28. Output Short Recovery

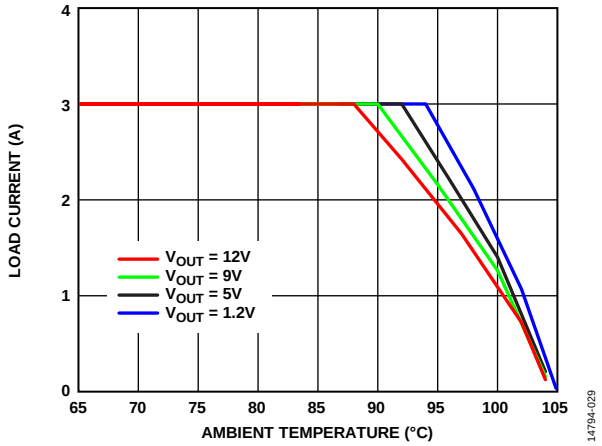

Figure 29. Load Current vs. Ambient Temperature at V_{IN} = 24 V, f_{SW} = 600 kHz, Measured on ADP2443-EVALZ

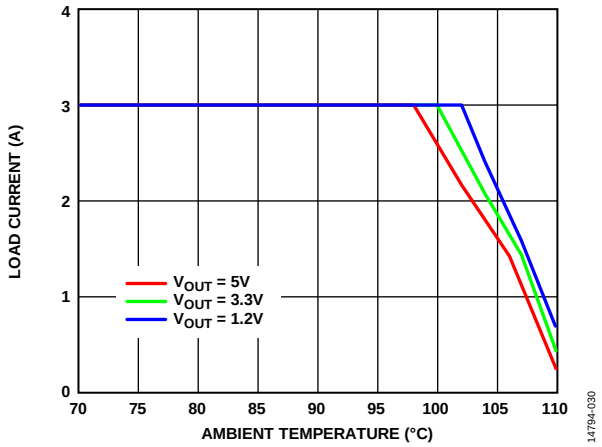

Figure 30. Load Current vs. Ambient Temperature at V_{IN} = 12 V, f_{SW} = 600 kHz, Measured on ADP2443-EVALZ

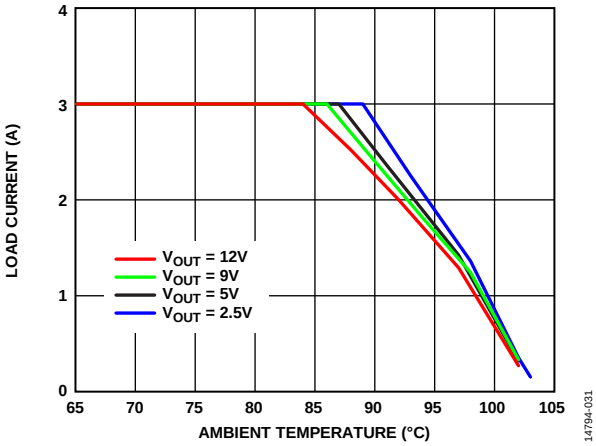

Figure 31. Load Current vs. Ambient Temperature at V_{IN} = 36 V, f_{SW} = 600 kHz, Measured on ADP2443-EVALZ

THEORY OF OPERATION

The ADP2443 is synchronous step-down, dc-to-dc regulator that uses an emulated current-mode architecture with an integrated high-side power switch and a low-side synchronous rectifier. The regulator targets high performance applications that require high efficiency and design flexibility.

The ADP2443 operates with an input voltage from 4.5 V to 36 V and regulates the output voltage down to 0.6 V. Additional features that maximize design flexibility include programmable switching frequency, programmable soft start, external compensation, precision enable, and a power-good output.

CONTROL SCHEME

The ADP2443 uses a fixed frequency, current mode PWM control architecture to achieve high efficiency and low noise operation.

The ADP2443 operates at a fixed frequency set by an external resistor from RT/SYNC to GND. It uses the low side NFET current for the PWM control as shown in Figure 32. The valley current information is captured at the end of the off period and combines with the slope ramp to form the emulated current ramp voltage. The slope ramp voltage is controlled by the resistor between RAMP and PVIN. At the start of each oscillator cycle, the high-side NFET turns on and the inductor current increases until the emulated current ramp voltage crosses the COMP voltage, which turns off the high-side NFET and turns on the low-side NFET, which in turn places a negative voltage across the inductor, causing a reduction in the inductor current. The low-side NFET stays on for the remainder of the cycle.

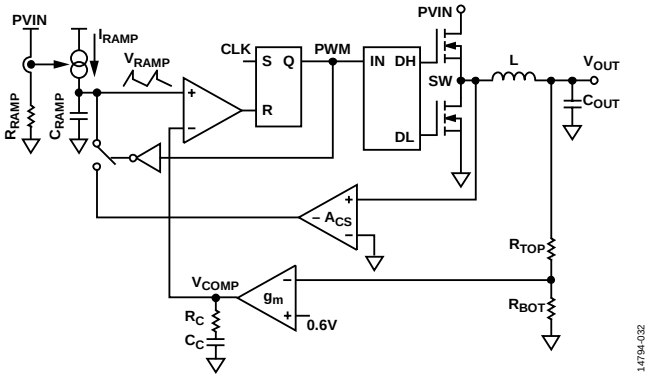

Figure 32. PWM Control Scheme

PRECISION ENABLE/SHUTDOWN

The EN input pin has a precision analog threshold of 1.2 V (typical) with 100 mV of hysteresis. When the enable voltage exceeds 1.2 V, the regulator turns on; when it falls below 1.1 V (typical), the regulator turns off. To force the regulator to start automatically when input power is applied, connect EN to PVIN.

The precision EN pin has an internal pull-down current source (0.13 µA) that provides a default turn-off when the EN pin is open.

When the EN pin voltage exceeds 1.2 V (typical), the ADP2443 is enabled and the internal pull-up current increases to 4 µA, which allows users to program the PVIN UVLO and hysteresis.

INTERNAL REGULATOR (VREG)

The on-board 5 V regulator provides a stable supply for the internal circuits. It is recommended that a 1 µF ceramic capacitor be placed between the VREG pin and GND. The internal regulator includes a current-limit circuit to protect the output if the maximum external load current is exceeded.

BOOTSTRAP CIRCUITRY

The ADP2443 includes a regulator to provide the gate drive voltage for the high-side N-MOSFET. It uses differential sensing to generate a 5 V bootstrap voltage between the BST and SW pins.

It is recommended that a 0.1 µF, X7R or X5R ceramic capacitor be placed between the BST pin and the SW pin.

OSCILLATOR

The switching frequency of ADP2443 is controlled by the RT/SYNC pin. A resistor from RT/SYNC to GND programs the switching frequency according to the following equation:

$$f_{SW}\ (\text{kHz}) = \frac{168{,}000}{R_T\ (\text{k}\Omega)}$$

A 280 kΩ resistor sets the frequency to 600 kHz, and a 560 kΩ resistor sets the frequency to 300 kHz. Figure 33 shows the typical relationship between f_{SW} and R_T.

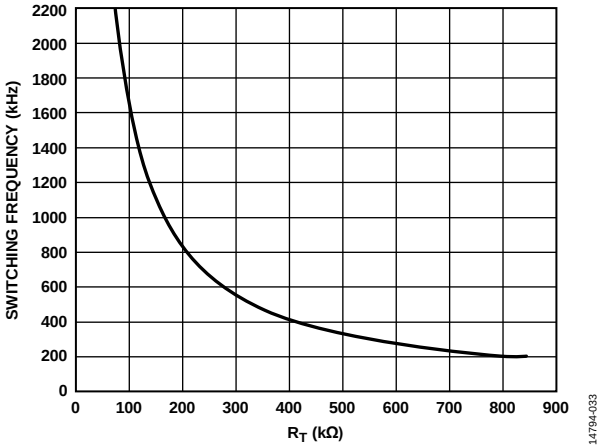

Figure 33. Switching Frequency vs. R_T

SYNCHRONIZATION

To synchronize the ADP2443, connect an external clock to the RT/SYNC pin. The frequency of the external clock can be in the range of 200 kHz to 1.8 MHz. During synchronization, the regulator operates in continuous conduction mode (CCM) and the rising edge of the switching waveform runs 180° out of phase to the rising edge of the external clock.

When the ADP2443 is operating in synchronization mode, a resistor must be connected from the RT/SYNC pin to GND to program the internal oscillator to run at 80% to 120% of the external synchronization clock.

SOFT START

The ADP2443 uses the SS pin to program the soft start time. Place a capacitor between SS and GND; an internal current charges this capacitor to establish the soft start ramp. Calculate the soft start time (t_{SS}) using the following equation:

$$t_{SS} = \frac{0.6\ \text{V} \times C_{SS}}{I_{SS}}$$

where:
C_{SS} is the soft start capacitance.
I_{SS} is the typical soft start pull-up current (3.4 µA).

If the output voltage is precharged before power up, the ADP2443 prevents the low-side MOSFET from turning on until the soft start voltage exceeds the voltage on the FB pin.

POWER GOOD

The power-good pin (PGOOD) is an active high, open-drain output that requires an external resistor to pull it up to a voltage. A logic high on the PGOOD pin indicates that the voltage on the FB pin (and therefore the output voltage) is within regulation.

The power-good circuitry monitors the output voltage on the FB pin and compares it to the rising and falling thresholds that are specified in Table 1. If the rising output voltage exceeds the target value, the PGOOD pin is held low. The PGOOD pin continues to be held low until the falling output voltage returns to the target value.

If the output voltage falls below the target output voltage, the PGOOD pin is held low. The PGOOD pin continues to be held low until the rising output voltage returns to the target value.

The power-good rising and falling thresholds are shown in Figure 34. There is always a 16-cycle waiting period (deglitch) before the PGOOD pin is pulled from low to high or from high to low.

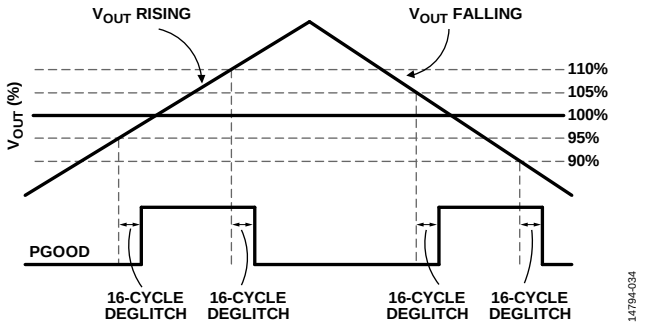

Figure 34. PGOOD Rising and Falling Thresholds

PEAK CURRENT-LIMIT AND SHORT-CIRCUIT PROTECTION

The ADP2443 uses the emulated current ramp voltage for cycle-by-cycle current limit protection to prevent current runaway. When the emulated current ramp voltage reaches the valley current limit threshold plus the ramp voltage, the high-side MOSFET turns off and the low-side MOSFET turns on until the next cycle.

The overcurrent counter increments during this process; otherwise the overcurrent counter decreases. If the overcurrent counter reaches 10 or the FB voltage drops below 0.2 V after the soft start, the device enters hiccup mode. During hiccup mode, the high-side NFET and low-side NFET are both turned off. The device remains in this mode for seven soft start cycles and then attempts to restart with soft start. If the current-limit fault is cleared, the device resumes normal operation; otherwise, it reenters hiccup mode.

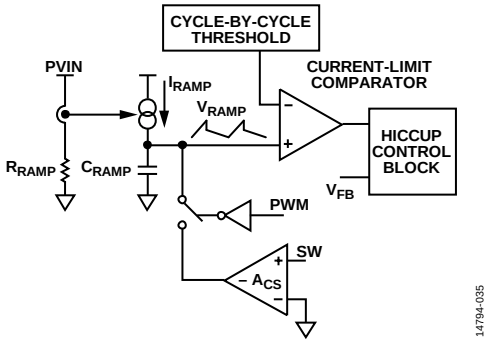

Figure 35. Current-Limit Circuit

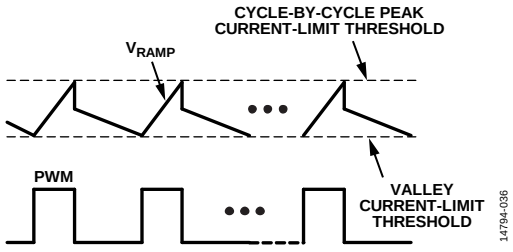

Figure 36. Cycle-By-Cycle Current-Limit Waveform

OVERVOLTAGE PROTECTION (OVP)

The ADP2443 includes an OVP feature to protect the regulator against an output short to a higher voltage supply or when a strong load disconnect transient occurs. If the feedback voltage increases to 0.7 V, the internal high-side MOSFET and low-side MOSFET are turned off until the voltage at the FB pin decreases to 0.63 V. At that time, the ADP2443 resumes normal operation.

UNDERVOLTAGE LOCKOUT (UVLO)

UVLO circuitry is integrated in the ADP2443 to prevent the occurrence of power-on glitches. If the V_{PVIN} voltage drops below 3.9 V typical, the device shuts down and both the power switch and synchronous rectifier turn off. When the V_{PVIN} voltage rises again above 4.3 V typical, the soft start period is initiated and the device is enabled.

THERMAL SHUTDOWN

If the ADP2443 junction temperature rises above 150°C, the internal thermal shutdown circuit turns off the regulator for self protection. Extreme junction temperatures can be the result of high current operation, poor PCB layout thermal design, and/or high ambient temperature. A 25°C hysteresis is included in the thermal shutdown circuit so that, if an overtemperature event occurs, the ADP2443 does not return to normal operation until the on-chip temperature drops below 125°C. Upon recovery, a soft start is initiated before normal operation begins.

APPLICATIONS INFORMATION

INPUT CAPACITOR SELECTION

The input capacitor reduces the input voltage ripple caused by the switch current on PVIN. Place the input capacitor as close as possible to the PVIN pin. A ceramic capacitor in the 10 µF to 47 µF range is recommended. The loop that is composed of this input capacitor, the high-side N-MOSFET, and the low-side N-MOSFET must be kept as small as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. The rms current rating of the input capacitor must be larger than the value calculated from the following equation:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

OUTPUT VOLTAGE SETTING

The output voltage of the ADP2443 is set by an external resistor divider. The resistor values are calculated using

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$$

To limit output voltage accuracy degradation due to FB bias current (0.1 µA maximum) to less than 0.5% (maximum), ensure that R_{BOT} < 30 kΩ.

Table 5 lists the recommended resistor divider values for various output voltages.

Table 5. Resistor Divider Values for Various Output Voltages

V_{OUT} (V)	R_{TOP} ± 1% (kΩ)	R_{BOT} ± 1% (kΩ)
1.0	10	15
1.2	10	10
1.5	15	10
1.8	20	10
2.5	47.5	15
3.3	10	2.21
5.0	22	3
8.0	44.2	3.57
10.0	39.2	2.49
12.0	52.3	2.74

VOLTAGE CONVERSION LIMITATIONS

The minimum output voltage for a given input voltage and switching frequency is constrained by the minimum on time. The minimum on time of the ADP2443 is typically 50 ns. Calculate the minimum output voltage at a given input voltage and frequency using the following equation:

$$V_{OUT\_MIN} = V_{IN} \times t_{MIN\_ON} \times f_{SW} - (R_{DSON\_HS} - R_{DSON\_LS}) \times I_{OUT\_MIN} \times t_{MIN\_ON} \times f_{SW} - (R_{DSON\_LS} + R_L) \times I_{OUT\_MIN} \quad (1)$$

where:
V_{OUT_MIN} is the minimum output voltage.
t_{MIN_ON} is the minimum on time.
f_{SW} is the switching frequency.
R_{DSON_HS} is the high-side MOSFET on resistance.
R_{DSON_LS} is the low-side MOSFET on resistance.
I_{OUT_MIN} is the minimum output current.
R_L is the series resistance of output inductor.

The maximum output voltage for a given input voltage and switching frequency is constrained by the minimum off time and the maximum duty cycle. The minimum off time is typically 200 ns.

Calculate the maximum output voltage, limited by the minimum off time at a given input voltage and frequency, using the following equation:

$$V_{OUT\_MAX} = V_{IN} \times (1 - t_{MIN\_OFF} \times f_{SW}) - (R_{DSON\_HS} - R_{DSON\_LS}) \times I_{OUT\_MAX} \times (1 - t_{MIN\_OFF} \times f_{SW}) - (R_{DSON\_LS} + R_L) \times I_{OUT\_MAX} \quad (2)$$

where:
V_{OUT_MAX} is the maximum output voltage.
t_{MIN_OFF} is the minimum off time.
I_{OUT_MAX} is the maximum output current.

As Equation 1 and Equation 2 show, reducing the switching frequency alleviates the minimum on time and minimum off time limitations.

INDUCTOR SELECTION

The inductor value is determined by the operating frequency, input voltage, output voltage, and inductor ripple current. Using a small inductor results in a faster transient response but degrades efficiency, due to a larger inductor ripple current; whereas using a large inductor value results in s smaller ripple current and better efficiency, but also results in a slower transient response.

As a guideline, the inductor ripple current, ΔI_L, is typically set to one-third of the maximum load current. Calculate the inductor value using the following equation:

$$L = \frac{(V_{IN} - V_{OUT}) \times D}{\Delta I_L \times f_{SW}}$$

where:
V_{IN} is the input voltage.
V_{OUT} is the output voltage.
D is the duty cycle.
ΔI_L is the inductor current ripple.
f_{SW} is the switching frequency.

$$D = \frac{V_{OUT}}{V_{IN}}$$

Calculate the peak inductor current using

$$I_{PEAK} = I_{OUT} + \frac{\Delta I_L}{2}$$

The saturation current (I_{SAT}) of the inductor must be larger than the peak inductor current. For ferrite core inductors with a quick saturation characteristic, the saturation current rating of the inductor must be greater than the current limit threshold of the switch, which prevents the inductor from reaching saturation.

Calculate the rms current of the inductor from the following equation:

$$I_{RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L^2}{12}}$$

Shielded ferrite core materials are recommended for low core loss and low EMI. Table 6 lists recommended inductors.

Table 6. Recommended Inductors

Vendor	Part Number	Value (µH)	I_{SAT} (A)	I_{RMS} (A)	DC Resistance (DCR) (mΩ)
Toko	FDVE0630-R75M	0.75	10.9	10.7	6.2
	FDVE0630-1R0M	1.0	9.5	9.5	8.5
	FDVE1040-1R5M	1.5	13.7	14.6	4.6
	FDVE1040-2R2M	2.2	11.4	11.6	6.8
	FDVE1040-3R3M	3.3	9.8	9.0	10.1
	FDVE1040-4R7M	4.7	8.2	8.0	13.8
	FDVE1040-5R6M	5.6	7.9	7.3	18.0
	FDVE1040-6R8M	6.8	7.1	7.1	20.2
	FDVE1040-100M	10	6.1	5.2	34.1
CoilCraft	XAL5030-601ME	0.6	19.8	17.7	4.52
	XAL5030-801ME	0.8	18.5	13	5.65
	XAL6030-102ME	1.0	23	18	6.18
	XAL6030-122ME	1.2	22	16	7.5
	XAL6030-182ME	1.8	18.2	14	10.5
	XAL6030-222ME	2.2	15.9	10	14.0
	XAL6030-332ME	3.3	12.2	8	20.8
	XAL6060-472ME	4.7	10.5	11	16.4
	XAL6060-562ME	5.6	9.9	10	17.8
	XAL6060-682ME	6.8	9.2	9	20.8
	XAL6060-822ME	8.2	8.4	8	26.4
	XAL6060-103ME	10	7.6	7	29.8
	XAL6060-153ME	15	5.8	6	43.8
	XAL6060-223ME	22	5.6	5	60.6
Würth Elektronik	744 333 0068	0.68	38	20	1.35
	744 333 0082	0.82	36	20	1.35
	744 333 0100	1.0	27.5	20	1.35
	744 333 0150	1.5	27	18	2.5
	744 333 0220	2.2	22	16.5	3.7
	744 333 0330	3.3	15.5	14	5.4
	744 333 0470	4.7	15	13	8.2
	744 333 0680	6.8	11	11.5	13.2
	744 333 0820	8.2	8	11.5	13.2
	744 333 100 0	10	8	9	20.7
	744 373 490 068	0.68	26	12	4.5
	744 373 490 082	0.82	25	11.3	4.9
	744 373 490 10	1.0	19.5	10	6.5
	744 373 490 15	1.5	14.5	8	9
	744 373 490 22	2.2	14	7.5	12
	744 373 490 33	3.3	12	6	20.9
	744 373 490 47	4.7	11	5	30.8
	744 373 490 68	6.8	9.5	3.5	51.5
	744 373 490 82	8.2	9	3.3	63
	744 373 491 00	10	8	3.2	69
	744 373 492 20	22	6.5	2.1	170

OUTPUT CAPACITOR SELECTION

The output capacitor selection affects the output ripple voltage load step transient and the loop stability of the regulator.

For example, during a load step transient where the load is suddenly increased, the output capacitor supplies the load until the control loop can ramp up the inductor current. The delay caused by the control loop causes the output to undershoot. Calculate the output capacitance that is required to satisfy the voltage droop requirement using the following equation:

$$C_{OUT\_UV} = \frac{K_{UV} \times \Delta I_{STEP}^{2} \times L}{2 \times (V_{IN} - V_{OUT}) \times \Delta V_{OUT\_UV}}$$

where:
K_{UV} is a factor, with a typical setting of K_{UV} = 2.
ΔI_{STEP} is the load step.
ΔV_{OUT_UV} is the allowable undershoot on the output voltage.

Another example occurs when a load is suddenly removed from the output, and the energy stored in the inductor rushes into the output capacitor, causing the output to overshoot.

Calculate the output capacitance that is required to meet the overshoot requirement using the following equation:

$$C_{OUT\_OV} = \frac{K_{OV} \times \Delta I_{STEP}^{2} \times L}{(V_{OUT} + \Delta V_{OUT\_OV})^{2} - V_{OUT}^{2}}$$

where:
K_{OV} is a factor, with a typical setting of K_{OV} = 2.
ΔV_{OUT_OV} is the allowable overshoot on the output voltage.

The output ripple is determined by the effective series resistance (ESR) and the value of the capacitance. Use the following equation to select a capacitor that can meet the output ripple requirements:

$$C_{OUT\_RIPPLE} = \frac{\Delta I_{L}}{8 \times f_{SW} \times \Delta V_{OUT\_RIPPLE}}$$

where ΔV_{OUT_RIPPLE} is the allowable output ripple voltage.

$$R_{ESR} = \frac{\Delta V_{OUT\_RIPPLE}}{\Delta I_{L}}$$

where R_{ESR} is the equivalent series resistance of the output capacitor in ohms (Ω).

Select the largest output capacitance given by C_{OUT_UV}, C_{OUT_OV}, and C_{OUT_RIPPLE} to meet both load transient and output ripple performance.

The selected output capacitor voltage rating must be greater than the output voltage. The rms current rating of the output capacitor must be greater than the value that is calculated by using the following equation:

$$I_{COUT\_RMS} = \frac{\Delta I_{L}}{\sqrt{12}}$$

PROGRAMMING INPUT VOLTAGE UVLO

The ADP2443 has a precision enable input to program the UVLO threshold of the input voltage (see Figure 37).

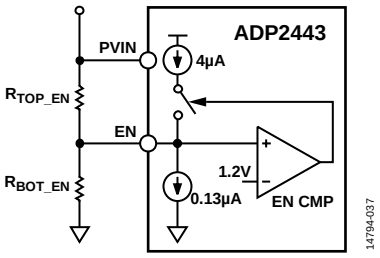

Figure 37. Programming the Input Voltage UVLO

Use the following equation to calculate R_{TOP_EN} and R_{BOT_EN}:

$$R_{TOP\_EN} = \frac{1.1\ \text{V} \times V_{IN\_RISING} - 1.2\ \text{V} \times V_{IN\_FALLING}}{1.1\ \text{V} \times 0.13\ \mu\text{A} + 1.2\ \text{V} \times 3.87\ \mu\text{A}}$$

where:
V_{IN_RISING} is the V_{IN} rising threshold.
$V_{IN\_FALLING}$ is the V_{IN} falling threshold.

$$R_{BOT\_EN} = \frac{1.2\ \text{V} \times R_{TOP\_EN}}{V_{IN\_RISING} - R_{TOP\_EN} \times 0.13\ \mu\text{A} - 1.2\ \text{V}}$$

SLOPE COMPENSATION SETTING

The slope compensation is necessary in a current mode control architecture to prevent subharmonic oscillation and to maintain a stable output. The ADP2443 uses the emulated current mode and the slope compensation is implemented by connecting a resistor (R_{RAMP}) between the RAMP pin and PVIN pin.

Theoretically, an extra slope of $V_{OUT}/(2 \times L)$ is enough to stabilize the system. To guarantee that any noise is decimated in one cycle and the system is stable from subharmonic oscillation, the ADP2443 uses an extra slope of V_{OUT}/L.

Calculate the ramp resistor value, R_{RAMP}, using the following equation:

$$R_{RAMP} = \frac{L \times 10^{12}}{3.9}$$

where L is the inductor value.

COMPENSATION DESIGN

The ADP2443 uses an emulated current mode control architecture that combines the fast line transient response of traditional peak current mode with the capability to convert a high input voltage to a very low output voltage. Furthermore, the small signal characteristics of the emulated current mode are almost identical to those of traditional peak current mode. Therefore, the compensation network design method used in traditional peak current mode can also be applied to the emulated current mode control.

The power stage can be simplified as a voltage controlled current source supplying current to the output capacitor and load resistor. It is composed of one domain pole and a zero.

The control to output transfer function is based on the following equations:

$$G_{VD}(s) = \frac{V_{OUT}(s)}{V_{COMP}(s)} = A_{VI} \times R \times \frac{\left(1 + \frac{s}{2\pi \times f_Z}\right)}{\left(1 + \frac{s}{2\pi \times f_P}\right)}$$

where:
A_{VI} = 10 A/V.
R is the load resistance.

$$f_Z = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}}$$

where:
R_{ESR} is the ESR of the output capacitor.
C_{OUT} is the output capacitance.

$$f_P = \frac{1}{2\pi \times (R + R_{ESR}) \times C_{OUT}}$$

The ADP2443 uses a transconductance amplifier for the error amplifier and to compensate the system. Figure 38 shows the simplified, peak current mode control, small signal circuit.

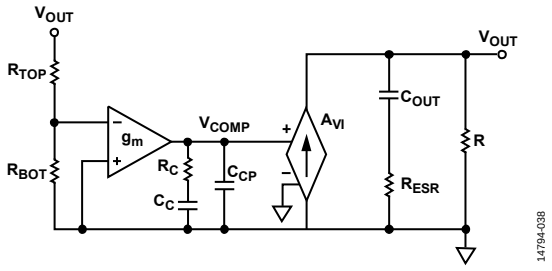

Figure 38. Simplified Peak Current Mode Control, Small Signal Circuit

The compensation components, R_C and C_C, contribute a zero, and the optional C_{CP} and R_C contribute an optional pole.

The closed-loop transfer equation is as follows:

$$T_V(s) = \frac{R_{BOT}}{R_{BOT} + R_{TOP}} \times \frac{-g_m}{C_C + C_{CP}} \times \frac{1 + R_C \times C_C \times s}{s \times \left(1 + \frac{R_C \times C_C \times C_{CP}}{C_C + C_{CP}} \times s\right)} \times G_{VD}(s)$$

The following design guideline shows how to select the R_C, C_C, and C_{CP} compensation components for ceramic output capacitor applications:

1. Determine the cross frequency, f_C. Generally, f_C is between $f_{SW}/12$ and $f_{SW}/6$.
2. Calculate R_C using the following equation:

$$R_C = \frac{2 \times \pi \times V_{OUT} \times C_{OUT} \times f_C}{0.6\ \text{V} \times g_m \times A_{VI}}$$

3. Place the compensation zero at the domain pole, f_P; then determine C_C using the following equation:

$$C_C = \frac{(R + R_{ESR}) \times C_{OUT}}{R_C}$$

4. C_{CP} is optional. It can be used to cancel the zero caused by the ESR of the output capacitor.

$$C_{CP} = \frac{R_{ESR} \times C_{OUT}}{R_C}$$

ADIsimPOWER DESIGN TOOL

The ADP2443 is supported by the ADIsimPower™ design tool set. ADIsimPower is a collection of tools that produce complete power designs that are optimized for a specific design goal. The tools enable the user to generate a full schematic and bill of materials and calculate performance in minutes. ADIsimPower can optimize designs for cost, area, efficiency, and component count, while taking into consideration the operating conditions and limitations of the IC and all real external components. For more information about the ADIsimPower design tools, refer to www.analog.com/ADIsimPower. The tool set is available from this website, and users can request an unpopulated board.

DESIGN EXAMPLE

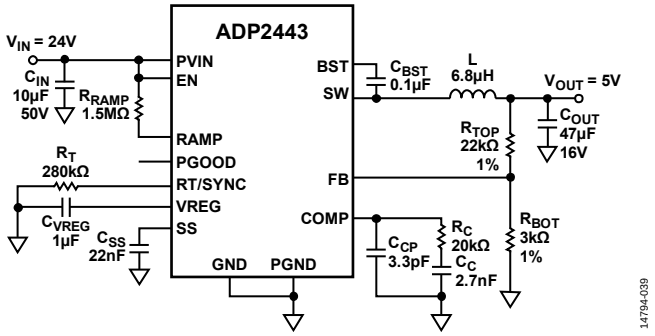

Figure 39. Schematic for Design Example

This section describes the procedures for selecting the external components based on the example specifications that are listed in Table 7. See Figure 39 for the schematic of this design example.

Table 7. Step-Down DC-to-DC Regulator Requirements

Parameter	Symbol	Specification
Input Voltage	V_{IN}	V_{IN} = 24.0 V ± 10%
Output Voltage	V_{OUT}	V_{OUT} = 5 V
Output Current	I_{OUT}	I_{OUT} = 3 A
Output Voltage Ripple	ΔV_{OUT_RIPPLE}	ΔV_{OUT_RIPPLE} = 50 mV
Load Transient	I_{LOAD}	±5%, 0.5 A to 2.5 A, 2 A/µs
Switching Frequency	f_{SW}	f_{SW} = 600 kHz

OUTPUT VOLTAGE SETTING

Choose a 22 kΩ resistor as the top feedback resistor (R_{TOP}), and calculate the bottom feedback resistor (R_{BOT}) by using the following equation:

$$R_{BOT} = R_{TOP} \times \left(\frac{0.6}{V_{OUT} - 0.6} \right)$$

To set the output voltage to 5 V, the resistors values are as follows: R_{TOP} = 22 kΩ and R_{BOT} = 3 kΩ.

FREQUENCY SETTING

To set the switching frequency to 600 kHz, connect a 280 kΩ resistor from the RT/SYNC pin to GND.

INDUCTOR SELECTION

The peak-to-peak inductor ripple current, ΔI_L, is set to 30% of the maximum output current. Use the following equation to estimate the inductor value:

$$L = \frac{(V_{IN} - V_{OUT}) \times D}{\Delta I_L \times f_{SW}}$$

where:
V_{IN} = 24 V.
V_{OUT} = 5 V.
D = 0.208.
ΔI_L = 0.9 A.
f_{SW} = 600 kHz.

This calculation results in L = 7.33 µH. Choose the standard inductor value of 6.8 µH.

The peak-to-peak inductor ripple current can be calculated by using the following equation:

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \times D}{L \times f_{SW}}$$

This calculation results in ΔI_L = 0.97 A.

Use the following equation to calculate the peak inductor current:

$$I_{PEAK} = I_{OUT} + \frac{\Delta I_L}{2}$$

This calculation results in I_{PEAK} = 3.49 A.

Use the following equation to calculate the rms current flowing through the inductor:

$$I_{RMS} = \sqrt{{I_{OUT}}^2 + \frac{{\Delta I_L}^2}{12}}$$

This calculation results in I_{RMS} = 3.013 A.

Based on the calculated current value, select an inductor with a minimum rms current rating of 3.013 A and a minimum saturation current rating of 3.49 A.

However, to protect the inductor from reaching its saturation point under the current-limit condition, the inductor must be rated for at least a 5.1 A saturation current for reliable operation.

Based on the requirements described previously, select a 6.8 µH inductor, such as the FDVE1040-6R8M from Toko, which has a 20.2 mΩ DCR and an 7.1 A saturation current.

OUTPUT CAPACITOR SELECTION

The output capacitor is required to meet both the output voltage ripple and load transient response requirements.

To meet the output voltage ripple requirement, use the following equation to calculate the ESR and capacitance value of the output capacitor:

$$C_{OUT\_RIPPLE} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{OUT\_RIPPLE}}$$

$$R_{ESR} = \frac{\Delta V_{OUT\_RIPPLE}}{\Delta I_L}$$

This calculation results in C_{OUT_RIPPLE} = 4.04 µF, and R_{ESR} = 51.5 mΩ.

To meet the ±5% overshoot and undershoot transient requirements, use the following equations to calculate the capacitance:

$$C_{OUT\_OV} = \frac{K_{OV} \times \Delta I_{STEP}{}^2 \times L}{(V_{OUT} + \Delta V_{OUT\_OV})^2 - V_{OUT}{}^2}$$

where:
$K_{OV} = K_{UV} = 2$ are the coefficients for estimation purposes.
ΔI_{STEP} = 2 A is the load transient step.
ΔV_{OUT_OV} = 5% V_{OUT} is the overshoot voltage.

$$C_{OUT\_UV} = \frac{K_{UV} \times \Delta I_{STEP}{}^2 \times L}{2 \times (V_{IN} - V_{OUT}) \times \Delta V_{OUT\_UV}}$$

where ΔV_{OUT_UV} = 5% V_{OUT} is the undershoot voltage.

This calculation results in C_{OUT_OV} = 21.2 µF, and C_{OUT_UV} = 5.7 µF.

According to the calculation, the output capacitance must be greater than 21.2 µF, and the ESR of the output capacitor must be smaller than 51.5 mΩ. It is recommended that one 47 µF/X5R/16 V ceramic capacitor be used, such as the GRM32ER61C476KE15K from Murata, with an ESR of 2 mΩ.

SLOPE COMPENSATION SETTING

The ramp resistor, R_{RAMP}, determines the slope compensation. Use the following equation to calculate the R_{RAMP} value:

$$R_{RAMP} = \frac{L \times 10^{12}}{3.9} = \frac{6.8\ \mu H \times 10^{12}}{3.9} = 1.74\ M\Omega$$

Choose a standard component value, as follows: R_{RAMP} = 1.5 MΩ.

COMPENSATION COMPONENTS

For better load transient and stability performance, set the cross frequency, f_C, to f_{SW}/10. In this case, f_{SW} is running at 600 kHz; therefore, the f_C is set to 60 kHz.

The 47 µF ceramic output capacitor has a derated value of 32 µF.

$$R_C = \frac{2 \times \pi \times 5\ V \times 32\ \mu F \times 60\ kHz}{0.6\ V \times 515\ \mu s \times 10\ A/V} = 19.5\ k\Omega$$

$$C_C = \frac{1.667\ \Omega + 0.002\ \Omega \times 32\ \mu F}{19.5\ k\Omega} = 2739\ pF$$

$$C_{CP} = \frac{0.002\ \Omega \times 32\ \mu F}{19.5\ k\Omega} = 3.3\ pF$$

Choose standard components, as follows: R_C = 20 kΩ, C_C = 2700 pF, and C_{CP} = 3.3 pF.

Figure 40 shows the Bode plot at a 3 A load current. The cross frequency is 59 kHz, and the phase margin is 66°.

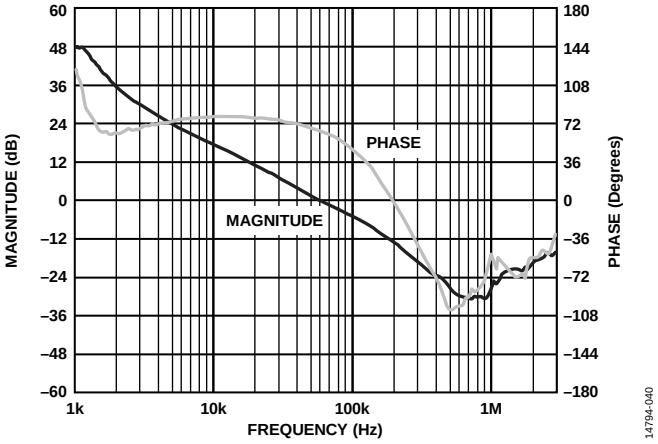

Figure 40. Bode Plot at 3 A

SOFT START TIME PROGRAM

The soft start feature allows the output voltage to ramp up in a controlled manner, eliminating output voltage overshoot during soft start and limiting the inrush current. Set the soft start time to 4 ms.

$$C_{SS} = \frac{t_{SS\_EXT} \times I_{SS}}{0.6\ V} = \frac{4\ ms \times 3.4\ \mu A}{0.6\ V} = 22.7\ nF$$

Choose a standard component value, as follows: C_{SS} = 22 nF.

INPUT CAPACITOR SELECTION

A minimum 10 µF ceramic capacitor must be placed near the PVIN pin. In this application, it is recommended that one 10 µF, X5R, 50 V ceramic capacitor be used.

RECOMMENDED EXTERNAL COMPONENTS

Table 8. Recommended External Components for Typical Applications with a 3 A Output Current

f_{SW} (kHz)	V_{IN} (V)	V_{OUT} (V)	L (µH)	C_{OUT} (µF)[1]	R_{TOP} (kΩ)	R_{BOT} (kΩ)	R_{RAMP} (kΩ)	R_C (kΩ)	C_C (pF)	C_{CP} (pF)
300	12	1	3.3	470 + 100	10	15	845	33.2	5600	120
		1.2	3.3	330 + 100	10	10	845	29.4	5600	100
		1.5	4.7	330	15	10	1000	30.9	5600	100
		1.8	4.7	220	20	10	1000	24.9	5600	82
		2.5	6.8	3 × 100	47.5	15	1500	28	5600	12
		3.3	8.2	2 × 100	10	2.21	2700	24.9	5600	10
		5	10	2 × 47	22	3	2700	18.7	5600	6.8
	24	1	3.3	470 + 100	10	15	845	33.2	5600	120
		1.2	4.7	470 + 100	10	10	1000	40.2	5600	100
		1.5	4.7	330	15	10	1000	30.9	5600	100
		1.8	6.8	330	20	10	1500	37.4	5600	82
		2.5	8.2	220	47.5	15	2700	34.8	5600	68
		3.3	10	3 × 100	10	2.21	2700	37.4	5600	10
		5	15	2 × 100	22	3	3300	28	5600	6.8
		8	22	2 × 47	44.2	3.57	5600	22.1	5600	3.9
		12	22	47	52.3	2.74	5600	10.5	5600	2.7
600	12	1	1.5	220 + 47	10	15	383	31.6	2700	56
		1.2	2.2	220 + 47	10	10	562	37.4	2700	47
		1.5	2.2	3 × 100	15	10	562	34	2700	10
		1.8	3.3	3 × 100	20	10	845	41.2	2700	8.2
		2.5	3.3	100 + 47	47.5	15	845	28	2700	6.8
		3.3	4.7	2 × 47	10	2.21	1000	24.9	2700	4.7
		5	4.7	47	22	3	1000	18.7	2700	3.3
	24	1.2	2.2	220 + 47	10	10	562	37.4	2700	47
		1.5	2.2	3 × 100	15	10	562	34	2700	10
		1.8	3.3	3 × 100	20	10	845	41.2	2700	8.2
		2.5	4.7	2 × 100	47.5	15	1000	37.4	2700	6.8
		3.3	4.7	2 × 47	10	2.21	1000	24.9	2700	4.7
		5	6.8	100	22	3	1500	28	2700	3.3
		8	10	47	44.2	3.57	2700	22.1	2700	1.8
		12	10	47	52.3	2.74	2700	21	2700	1.2
1200	12	1.2	1	2 × 100	10	10	255	36.5	1200	6.8
		1.5	1	2 × 47	15	10	255	22.6	1200	5.6
		1.8	1.5	100 + 47	20	10	383	41.2	1200	4.7
		2.5	1.5	100	47.5	15	383	37.4	1200	3.3
		3.3	2.2	47	10	2.21	562	24.9	1200	2.2
		5	2.2	47	22	3	562	37.4	1200	1.5
	24	2.5	2.2	100	47.5	15	562	37.4	1200	3.3
		3.3	2.2	47	10	2.21	562	24.9	1200	2.2
		5	3.3	47	22	3	845	37.4	1200	1.5
		8	4.7	47	44.2	3.57	1000	44.2	1200	1
		12	4.7	47	52.3	2.74	1000	42.2	1200	0.5

[1] 680 µF: 4 V, KEMET T520Y687M004ATE010; 470 µF: 6.3 V, KEMET T520X477M006ATE010; 330 µF: 6.3 V, KEMET T520D337M006ATE009; 220 µF: 6.3 V, KEMET T520D227M006ATE009; 100 µF: 6.3 V, X5R, Murata GRM32ER60J107ME20; 47 µF: 16 V, X5R, Murata GRM32ER61C476KE15K.

PRINTED CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Good PCB layout is essential for obtaining the best performance from the ADP2443. Poor PCB layout can degrade the output regulation, as well as the electromagnetic interface (EMI) and electromagnetic compatibility (EMC) performance. Figure 42 shows an example of a good PCB layout for the ADP2443. For optimum layout, refer to the following guidelines:

- Use separate analog ground planes and power ground planes. Connect the ground reference of sensitive analog circuitry, such as output voltage divider components, compensation components, frequency setting components, and soft start capacitor, to analog ground (GND). In addition, connect the ground reference of the power components, such as input and output capacitors, to power ground (PGND). Connect both ground planes to the exposed GND pad of the ADP2443.
- Place the input capacitor, inductor, and output capacitor as close as possible to the IC, and use short traces.
- Ensure that the high current loop traces are as short and as wide as possible. Make the high current path from the input capacitor through the inductor, the output capacitor, and the power ground plane back to the input capacitor as short as possible. To accomplish this, ensure that the input and output capacitors share a common power ground plane.
  In addition, ensure that the high current path from the power ground plane through the inductor and output capacitor back to the power ground plane is as short as possible by tying the PGND pins of the ADP2443 to the PGND plane as close as possible to the input and output capacitors.
- Connect the exposed GND pad of the ADP2443 to a large, external copper ground plane to maximize its power dissipation capability and minimize junction temperature. In addition, connect the exposed SW pad to the SW pins of the ADP2443, using short, wide traces; or connect the exposed SW pad to a large copper plane of the switching node for high current flow.
- Place the feedback resistor divider as close as possible to the FB pin to prevent noise pickup. Minimize the length of the trace that connects the top of the feedback resistor divider to the output while keeping the trace away from the high current traces and the switching node to avoid noise pickup. To reduce noise pickup further, place an analog ground plane on either side of the FB trace and ensure that the trace is as short as possible to reduce the parasitic capacitance pickup.

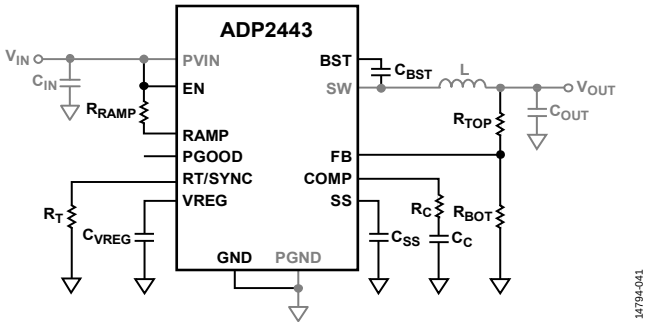

Figure 41. High Current Path in the PCB Circuit

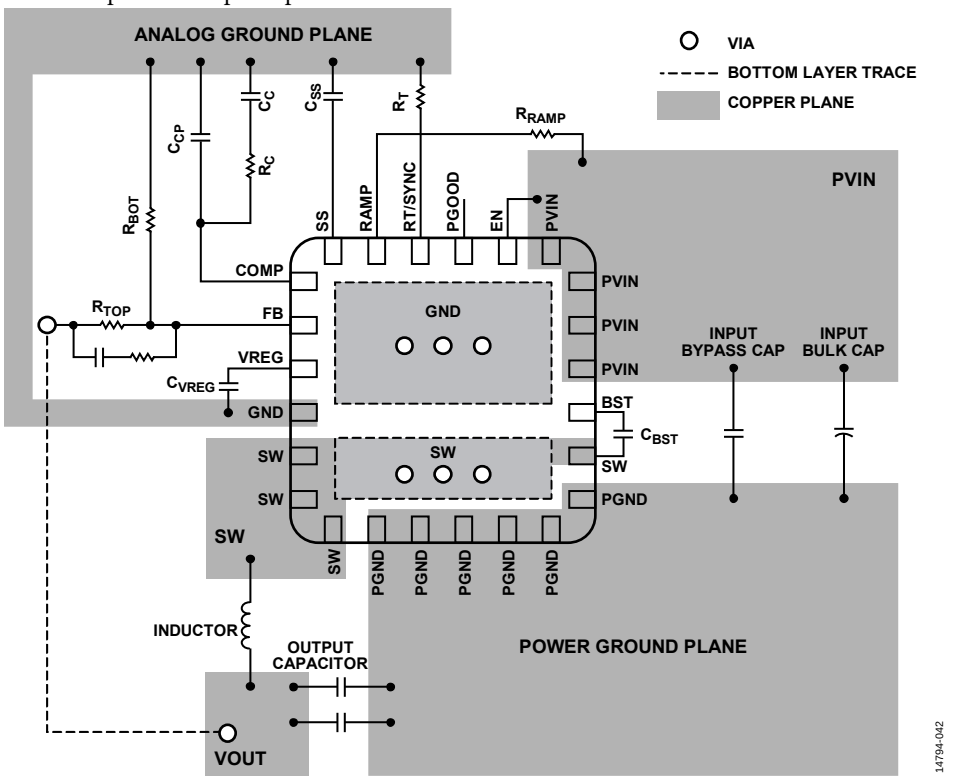

Figure 42. Recommended PCB Layout

TYPICAL APPLICATIONS CIRCUITS

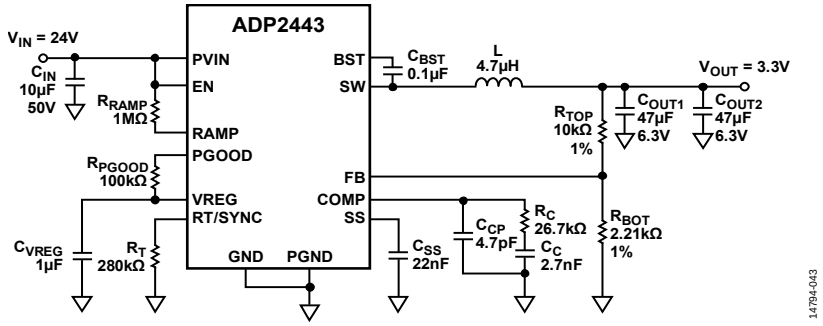

Figure 43. Typical Application Circuit, V_{IN} = 24 V, V_{OUT} = 3.3 V, I_{OUT} = 3A, f_{SW} = 600 kHz

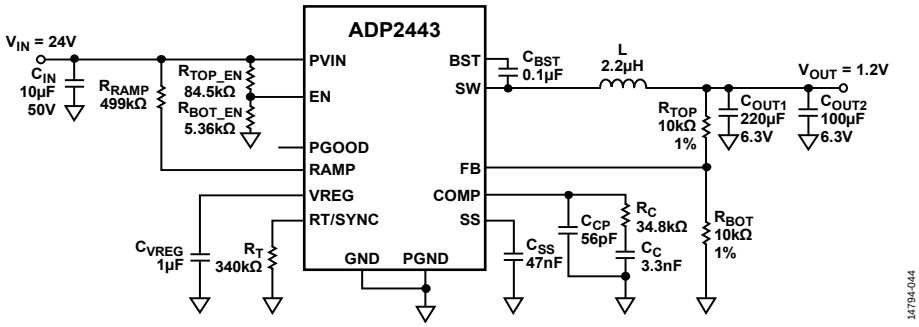

Figure 44. Programming Input Voltage UVLO Rising Threshold at 20 V, Falling Threshold at 18 V, V_{IN} = 24 V, V_{OUT} = 1.2 V, I_{OUT} = 3 A, f_{SW} = 500 kHz

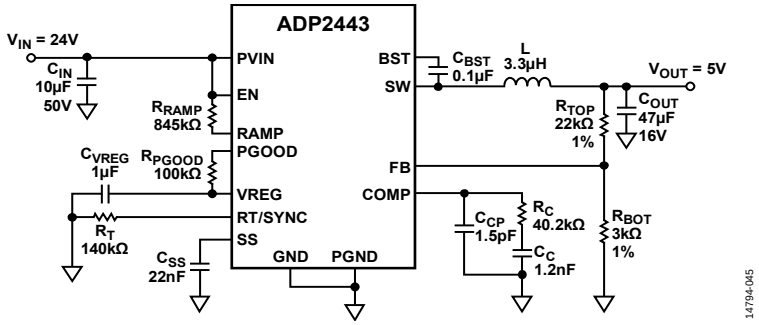

Figure 45. Typical Application Circuit, V_{IN} = 24 V, V_{OUT} = 5 V, I_{OUT} = 3 A, f_{SW} = 1.2 MHz

OUTLINE DIMENSIONS

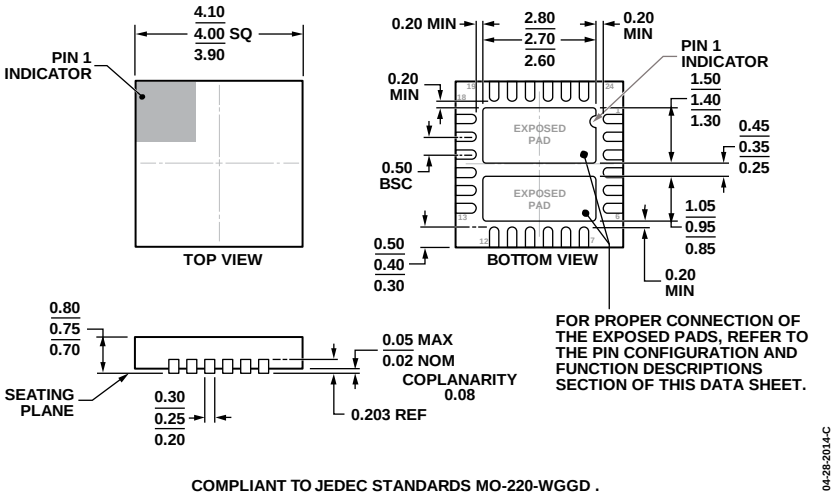

Figure 46. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-24-12)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Output Voltage	Package Description	Package Option
ADP2443ACPZN-R7	−40°C to +125°C	Adjustable	24-Lead LFCSP	CP-24-12
ADP2443-EVALZ			Evaluation Board	

[1] Z = RoHS Compliant Part.

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