SE98A

DDR memory module temp sensor, 1.7 V to 3.6 V

Rev. 04 — 25 November 2009 **Product data sheet**

1. General description

The NXP Semiconductors SE98A measures temperature from –40 °C and +125 °C with JEDEC Grade B ±1 °C accuracy between +75 °C and +95 °C communicating via the I^2C-bus/SMBus. It is typically mounted on a Dual In-Line Memory Module (DIMM) measuring the DRAM temperature in accordance with the new JEDEC (JC-42.4) *Mobile Platform Memory Module Thermal Sensor Component* specification.

The SE98A thermal sensor operates over the V_{DD} range of 1.7 V to 3.6 V. The SE98A does not include the 2 k SPD and is designed for custom DIMM where larger SPD is required.

The Temp Sensor (TS) consists of an Analog-to-Digital Converter (ADC) that monitors and updates its own temperature readings 8 times per second, converts the reading to a digital data, and latches them into the data temperature registers. User-programmable registers, such as Shutdown or Low-power modes and the specification of temperature event and critical output boundaries, provide flexibility for DIMM temperature-sensing applications.

When the temperature changes beyond the specified boundary limits, the SE98A outputs an $\overline{\text{EVENT}}$ signal using an open-drain output that can be pulled up between 0.9 V and 3.6 V. The user has the option of setting the $\overline{\text{EVENT}}$ output signal polarity as either an active LOW or active HIGH comparator output for thermostat operation, or as a temperature event interrupt output for microprocessor-based systems. The $\overline{\text{EVENT}}$ output can even be configured as a critical temperature output.

The SE98A supports the industry-standard 2-wire I^2C-bus/SMBus serial interface. The SMBus TIMEOUT function is supported to prevent system lock-ups. Manufacturer and Device ID registers provide the ability to confirm the identify of the device. Three address pins allow up to eight devices to be controlled on a single bus.

The SE98A is an improved SE98 and is comparable to the thermal sensor in the SE97 but with voltage range of 1.7 V to 3.6 V.

2. Features

- JEDEC (JC-42.4) TS3000B1 DIMM ± 0.5 °C (typ.) between 75 °C and 95 °C temperature sensor
- Optimized for voltage range: 1.7 V to 3.6 V
- Shutdown current: 0.1 μA (typ.) and 5.0 μA (max.)
- 2-wire interface: I^2C-bus/SMBus compatible, 0 Hz to 400 kHz
- SMBus ALERT and TIMEOUT (programmable)
- 11-bit ADC Temperature-to-Digital converter with 0.125 °C resolution

founded by Philips

- Operating current: 250 µA (typ.) and 400 µA (max.)
- Programmable hysteresis threshold: 0 °C, 1.5 °C, 3 °C, 6 °C
- Over/under/critical temperature $\overline{\text{EVENT}}$ output
- B grade accuracy:
  - ±0.5 °C/±1 °C (typ./max.) → +75 °C to +95 °C
  - ±1 °C/±2 °C (typ./max.) → +40 °C to +125 °C
  - ±2 °C/±3 °C (typ./max.) → –40 °C to +125 °C
- ESD protection exceeds 2000 V HBM per JESD22-A114, 250 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Available packages: TSSOP8, HWSON8 (PSON8 VCED-3) and HXSON8

3. Applications

- DDR2 and DDR3 memory modules
- Laptops, personal computers and servers
- Enterprise networking
- Hard disk drives and other PC peripherals

4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
SE98APW	S98A	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 4.4 mm	SOT530-1
SE98ATP[1]	98A	HWSON8	plastic thermal enhanced very very thin small outline package; no leads; 8 terminals; body 2 × 3 × 0.8 mm	SOT1069-2
SE98ATL	8AL	HXSON8	plastic thermal enhanced extremely thin small outline package; no leads; 8 terminals; body 2 × 3 × 0.5 mm	SOT1052-1

[1] Industry standard 2 mm × 3 mm × 0.8 mm package to JEDEC VCED-3 PSON8 in 8 mm × 4 mm pitch tape 4 k quantity reels.

5. Block diagram

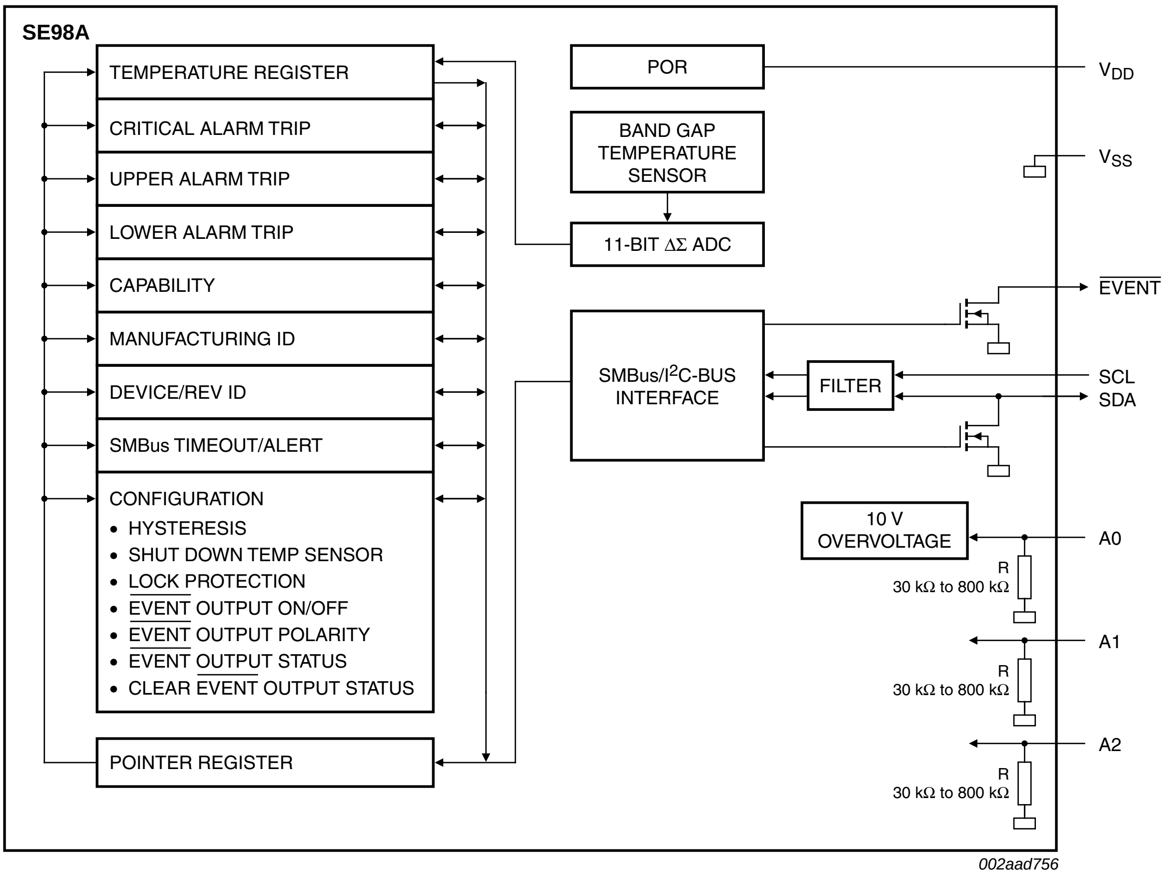


Fig 1. Block diagram of SE98A

6. Pinning information

6.1 Pinning

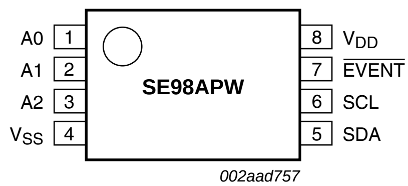


Fig 2. Pin configuration for TSSOP8

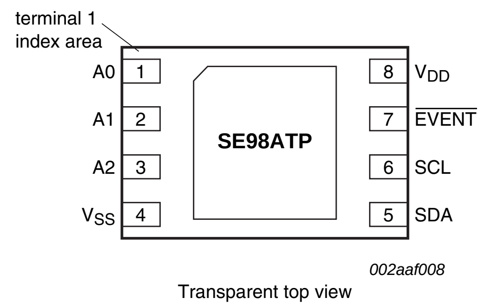


Fig 3. Pin configuration for HWSON8

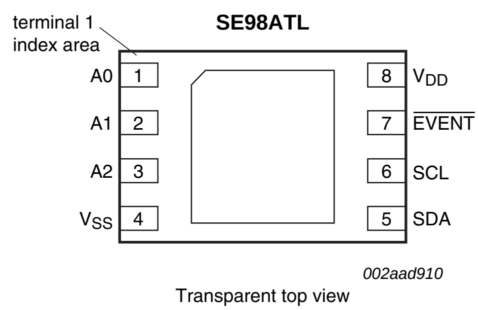


Fig 4. Pin configuration for HXSON8

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type	Description
A0[1]	1	I	I^2C-bus/SMBus slave address bit 0 with internal pull-down
A1	2	I	I^2C-bus/SMBus slave address bit 1 with internal pull-down
A2	3	I	I^2C-bus/SMBus slave address bit 2 with internal pull-down
V_{SS}	4	ground	device ground
SDA	5	I/O	SMBus/I^2C-bus serial data input/output (open-drain). Must have external pull-up resistor.
SCL	6	I	SMBus/I^2C-bus serial clock input/output (open-drain). Must have external pull-up resistor.
$\overline{\text{EVENT}}$	7	O	Thermal alarm output for high/low and critical temperature limit (open-drain). Must have external pull-up resistor.
V_{DD}	8	power	device power supply (1.7 V to 3.6 V)

[1] This input is overvoltage tolerant to support software write protection when applied to SPD.

7. Functional description

7.1 Serial bus interface

The SE98A uses the 2-wire serial bus (I^2C-bus/SMBus) to communicate with a host controller. The serial bus consists of a clock (SCL) and data (SDA) signals. The device can operate on either the I^2C-bus Standard/Fast mode or SMBus. The I^2C-bus Standard-mode is defined to have bus speeds from 0 Hz to 100 kHz, I^2C-bus Fast-mode from 0 Hz to 400 kHz, and the SMBus is from 10 kHz to 100 kHz. The host or bus master generates the SCL signal, and the SE98A uses the SCL signal to receive or send data on the SDA line. Data transfer is serial, bidirectional, and is one bit at a time with the Most Significant Bit (MSB) transferred first, and a complete I^2C-bus data is 1 byte. Since SCL and SDA are open-drain, pull-up resistors must be installed on these pins.

7.2 Slave address

The SE98A uses a 4-bit fixed and 3-bit programmable (A0, A1 and A2) 7-bit slave address that allows a total of eight devices to coexist on the same bus. The input of each pin is sampled at the start of each I^2C-bus/SMBus access. The A0, A1 and A2 pins are pulled LOW internally. The A0 pin is also overvoltage tolerant, supporting 10 V software write protection when applied to the SPD that shares common address lines.

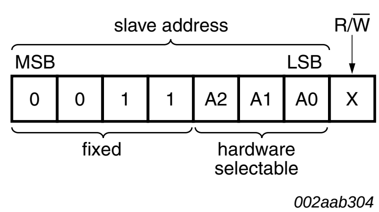


Fig 5. Slave address

7.3 EVENT output condition

The EVENT output indicates conditions such as the temperature crossing a predefined boundary. The EVENT modes are very configurable and selected using the configuration register (CONFIG). The interrupt mode or comparator mode is selected using CONFIG[0], using either TCRIT/UPPER/LOWER or TCRIT only temperature bands (CONFIG[2]) as modified by hysteresis (CONFIG[10:9]). The UPPER/LOWER (CONFIG[6]) and TCRIT (CONFIG[7]) bands can be locked. Figure 6 shows an example of the measured temperature versus time, with the corresponding behavior of the EVENT output in each of these modes.

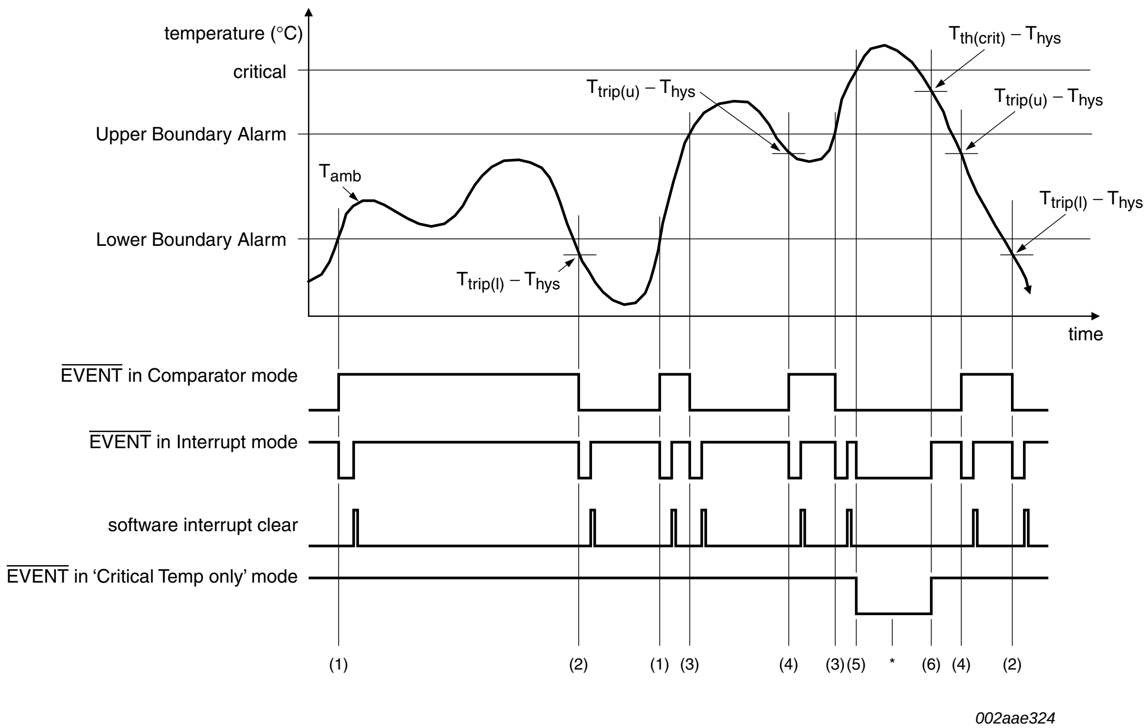
Upon device power-up, the default condition for the EVENT output is high-impedance to prevent spurious or unwanted alarms, but can be later enabled (CONFIG[3]). EVENT output polarity can be set to active HIGH or active LOW (CONFIG[1]). EVENT status can be read (CONFIG[4]) and cleared (CONFIG[5]).

- **Advisory notification:**
  - NXP device: After power-up, bit 3 (1) and bit 2 or bit 0 (leave as 0 or 1) can be set at the same time (e.g., in same byte) but once bit 3 is set (1) then changing bit 2 or bit 0 has no effect on the device operation.
  - Competitor device: Does not require that bit 3 be cleared (e.g., set back to (0)) before changing bit 2 or bit 0.
  - Work-around: In order to change bit 2 or bit 0 once bit 3 (1) is set, bit 3 (0) must be cleared in one byte and then change bit 2 or bit 0 and reset bit 3 (1) in the next byte.
  - SE98B will allow bit 2 or bit 0 to be changed even if bit 3 is set.

If the device enters Shutdown mode (CONFIG[8]) with asserted EVENT output, the output remains asserted during shutdown.

7.3.1 EVENT pin output voltage levels and resistor sizing

The EVENT open-drain output is typically pulled up to a voltage level from 0.9 V to 3.6 V with an external pull-up resistor, but there is no real lower limit on the pull-up voltage for the EVENT pin since it is simply an open-drain output. It could be pulled up to 0.1 V and would not affect the output. From the system perspective, there will be a practical limit. That limit will be the voltage necessary for the device monitoring the interrupt pin to detect a HIGH on its input. A possible practical limit for a CMOS input would be 0.4 V. Another thing to consider is the value of the pull-up resistor. When a low supply voltage is applied to the drain (through the pull-up resistor) it is important to use a higher value pull-up resistor, to allow a larger maximum signal swing on the EVENT pin.



Refer to Table 3 for figure note information.

Fig 6. $\overline{\text{EVENT}}$ output condition

Table 3. $\overline{\text{EVENT}}$ output condition

Figure note	$\overline{\text{EVENT}}$ output boundary conditions	$\overline{\text{EVENT}}$ output			Temperature Register Status bits		
		Comparator mode	Interrupt mode	Critical Temp only mode	Bit 15 Above Critical Trip	Bit 14 Above Alarm Window	Bit 13 Below Alarm Window
(1)	$T_{amb} \geq T_{trip(l)}$	H	L	H	0	0	0
(2)	$T_{amb} < T_{trip(l)} - T_{hys}$	L	L	H	0	0	1
(3)	$T_{amb} > T_{trip(u)}$	L	L	H	0	1	0
(4)	$T_{amb} \leq T_{trip(u)} - T_{hys}$	H	L	H	0	0	0
(5)	$T_{amb} \geq T_{th(crit)}$	L	L	L	1	1	0
(6)	$T_{amb} < T_{th(crit)} - T_{hys}$	L	H	H	0	1	0

When $T_{amb} \geq T_{th(crit)}$ and $T_{amb} < T_{th(crit)} - T_{hys}$ the $\overline{\text{EVENT}}$ output is in Comparator mode and bit 0 of CONFIG ($\overline{\text{EVENT}}$ output mode) is ignored.

7.3.2 EVENT thresholds

7.3.2.1 Alarm window

The device provides a comparison window with an UPPER trip point and a LOWER trip point, programmed through the Upper Boundary Alarm Trip register (02h), and Lower Boundary Alarm Trip register (03h). The Upper Boundary Alarm Trip register holds the upper temperature trip point, while the Lower Boundary Alarm Trip register holds the lower temperature trip point as modified by hysteresis as programmed in the Configuration register. When enabled, the EVENT output triggers whenever entering or exiting (crossing above or below) the alarm window.

- **Advisory notification:**
  - NXP device: The EVENT output can be cleared through the Clear EVENT bit (CEVNT) or SMBus ALERT.
  - Competitor device: The EVENT output can be cleared only through the Clear EVENT bit (CEVNT).
  - Work-around: Only clear EVENT output using the Clear EVENT bit (CEVNT).
  - There will be no change to the NXP device.

The Upper Boundary Alarm Trip should always be set above the Lower Boundary Alarm Trip.

- **Advisory notification:**
  - NXP device: Requires one conversion cycle (125 ms) after setting the alarm window before comparing the alarm limit with temperature register to ensure that there is correct data in the temperature register before comparing with the Alarm Window and operating EVENT output.
  - Competitor devices: Compares the alarm limit with temperature register at any time, so they get the EVENT output immediately when new UPPER or LOWER Alarm Windows and the EVENT output are set at the same time.
  - Work-around: Wait at least 125 ms before enabling EVENT output (EOCTL = 1).
  - SE98B will compare alarm window and temperature register immediately after setting.

7.3.2.2 Critical trip

The $T_{th(crit)}$ temperature setting is programmed in the Critical Alarm Trip register (04h) as modified by hysteresis as programmed in the Configuration register. When the temperature reaches the critical temperature value in this register (and EVENT is enabled), the EVENT output asserts and cannot be de-asserted until the temperature drops below the critical temperature threshold. The EVENT cannot be cleared through the Clear EVENT bit (CEVNT) or SMBus ALERT.

The Critical Alarm Trip should always be set above the Upper Boundary Alarm Trip.

- **Advisory notification:**
  - NXP device: Requires one conversion cycle (125 ms) after setting the Alarm Window before comparing the alarm limit with temperature register to ensure that there is correct data in the temperature register before comparing with the Alarm Window and operating EVENT output.
  - Competitor devices: Compares the Alarm Window with temperature register at any time, so they get the EVENT output immediately when new $T_{th(crit)}$ and EVENT output are set at the same time.
  - Work-around: Wait at least 125 ms before enabling EVENT output (EOCTL = 1). Intel will change Nehalem BIOS so that $T_{th(crit)}$ is set for more than 125 ms before EVENT output is enabled and Event value is checked.

    1. Set $T_{th(crit)}$.
    2. Doing something else (make sure that exceeds 125 ms).
    3. Enable the EVENT output (EOCTL = 1).
    4. Wait 20 μs.
    5. Read Event value.
  - SE98B will compare Alarm Window and temperature register immediately after setting.

7.3.3 Event operation modes

7.3.3.1 Comparator mode

In comparator mode, the EVENT output behaves like a window-comparator output that asserts when the temperature is outside the window (e.g., above the value programmed in the Upper Boundary Alarm Trip register or below the value programmed in the Lower Boundary Alarm Trip register or above the Critical Alarm Trip resister if $T_{th(crit)}$ only is selected). Reads/writes on the registers do not affect the EVENT output in comparator mode. The EVENT signal remains asserted until the temperature goes inside the alarm window or the window thresholds are reprogrammed so that the current temperature is within the alarm window.

The comparator mode is useful for thermostat-type applications, such as turning on a cooling fan or triggering a system shutdown when the temperature exceeds a safe operating range.

7.3.3.2 Interrupt mode

In interrupt mode, EVENT asserts whenever the temperature crosses an alarm window threshold. After such an event occurs, writing a 1 to the Clear EVENT bit in the configuration register de-asserts the EVENT output until the next trigger condition occurs.

In interrupt mode, $\overline{\text{EVENT}}$ asserts when the temperature crosses the alarm upper boundary. If the $\overline{\text{EVENT}}$ output is cleared and the temperature continues to increase until it crosses the critical temperature threshold, $\overline{\text{EVENT}}$ asserts again. Because the temperature is greater than the critical temperature threshold, a Clear $\overline{\text{EVENT}}$ command does not clear the $\overline{\text{EVENT}}$ output. Once the temperature drops below the critical temperature, $\overline{\text{EVENT}}$ de-asserts immediately.

- **Advisory notification:**
  - NXP device: If the $\overline{\text{EVENT}}$ output is not cleared before the temperature goes above the critical temperature threshold $\overline{\text{EVENT}}$ de-asserts immediately when temperature drops below the critical temperature.
  - Competitor devices: If the $\overline{\text{EVENT}}$ output is not cleared before or when the temperature is in the critical temperature threshold, $\overline{\text{EVENT}}$ will remain asserted after the temperature drops below the critical temperature until a Clear $\overline{\text{EVENT}}$ command.
  - Work-around: Always clear the $\overline{\text{EVENT}}$ output before temperature exceeds the critical temperature.
  - SE98B will keep $\overline{\text{EVENT}}$ asserted after the temperature drops below the critical temperature until a Clear $\overline{\text{EVENT}}$ command de-asserts $\overline{\text{EVENT}}$.

7.4 Conversion rate

The conversion time is the amount of time required for the ADC to complete a temperature measurement for the local temperature sensor. The conversion rate is the inverse of the conversion period which describes the number of cycles the temperature measurement completes in one second—the faster the conversion rate, the faster the temperature reading is updated. The SE98A’s conversion rate is at least 8 Hz or 125 ms.

7.4.1 What temperature is read when conversion is in progress

The SE98A has been designed to ensure a valid temperature is always available. When a read to the temperature register is initiated through the SMBus, the device checks to see if the temperature conversion process (Analog-to-Digital conversion) is complete and a new temperature is available:

- If the temperature conversion process is complete, then the new temperature value is sent out on the SMBus.
- If the temperature conversion process in **not** complete, then the previous temperature value is sent out on the SMBus.

It is possible that while the SMBus Master is reading the temperature register, a new temperature conversion completes. However, this will not affect the data (MSB or LSB) that is being shifted out. On the next read of the temperature register the new temperature value will be shifted out.

7.5 Power-up default condition

After power-on, the SE98A is initialized to the following default condition:

- Starts monitoring local sensor
- $\overline{\text{EVENT}}$ register is cleared—$\overline{\text{EVENT}}$ output is pulled HIGH by external pull-ups
- $\overline{\text{EVENT}}$ hysteresis is defaulted to 0 °C
- Command pointer is defaulted to '00h'
- Critical Temp, Alarm Temperature Upper and Lower Boundary Trip register are defaulted to 0 °C
- Capability register is defaulted to '0037h' for the B-grade and VHV capability
- Operational mode: comparator
- SMBus register is defaulted to '00h'

7.6 Device initialization

SE98A temperature sensors have programmable registers, which, upon power-up, default to zero. The open-drain $\overline{\text{EVENT}}$ output is default to being disabled, comparator mode and active LOW. The alarm trigger registers default to being unprotected. The configuration registers, upper and lower alarm boundary registers and critical temperature window are defaulted to zero and need to be programmed to the desired values. SMBus TIMEOUT feature defaults to being enabled and can be programmed to disable. These registers are required to be initialized before the device can properly function. Except for the SPD, which does not have any programmable registers, and does not need to be initialized.

Table 4 shows the default values and the example value to be programmed to these registers.

Table 4. Registers to be initialized

Register	Default value	Example value	Description
01h	0000h	0209h	Configuration register • hysteresis = 1.5 °C • $\overline{\text{EVENT}}$ output = Interrupt mode • $\overline{\text{EVENT}}$ output is enabled
02h	0000h	0550h	Upper Boundary Alarm Trip register = 85 °C
03h	0000h	1F40h	Lower Boundary Alarm Trip register = –20 °C
04h	0000h	05F0h	Critical Alarm Trip register = 95 °C
22h	0000h	0000h	SMBus register = no change

7.7 SMBus Time-out

The SE98A supports the SMBus time-out feature. If the host holds SCL LOW between 25 ms and 35 ms, the SE98A would reset its internal state machine to the bus idle state to prevent the system bus hang-up. This feature is turned on by default. The SMBus time-out is disabled by writing a logic 1 to bit 7 of register 22h.

Remark: When SMBus time-out is enabled, the I^2C-bus minimum bus speed is limited by the SMBus time-out timer, and goes down to only 10 kHz.

The SE98A has no SCL driver, so it cannot hold the SCL line LOW.

Remark: SMBus time-out works over the entire supply range of 1.7 V to 3.6 V unless shutdown bit (SHMD) is set and turns off the oscillator.

7.8 SMBus ALERT

The SE98A supports SMBus ALERT when it is programmed for the Interrupt mode and when the EVENT polarity bit is set to logic 0. The EVENT pin can be ANDed with other EVENT or ALERT signals from other slave devices to signal their intention to communicate with the host controller. When the host detects EVENT or ALERT signal LOW, it issues an Alert Response Address (ARA) to which a slave device would respond with its address. When there are multiple slave devices generating an ALERT the SE98A performs bus arbitration. If it wins the bus, it responds to the ARA and then clears the EVENT pin.

Remark: Either in comparator mode or when the SE98A crosses the critical temperature, the host must also read the EVENT status bit and provide remedy to the situation by bringing the temperature to within the alarm window or below the critical temperature if that bit is set. Otherwise, the EVENT pin will not get de-asserted.

Remark: In the SE98A, the ARA is set to default ON. However, in the SE98B the ARA will be set to default OFF since ARA is not anticipated to be used in DDR3 DIMM applications.

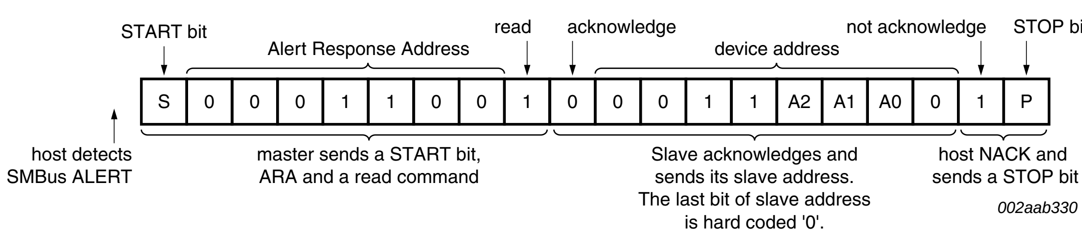


Fig 7. How SE98A responds to SMBus ALERT

7.9 SMBus/I²C-bus interface

The data registers in this device are selected by the Pointer register. At power-up, the Pointer register is set to '00', the location for the Capability register. The Pointer register latches the last location it was set to. Each data register falls into one of three types of user accessibility:

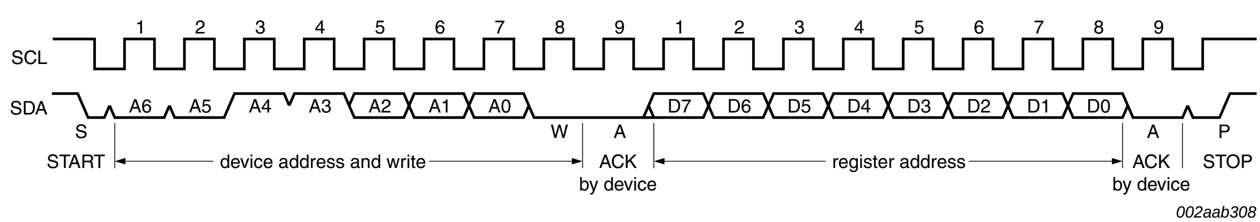
- Read only
- Write only
- Write/Read same address.

A 'write' to this device will always include the address byte and the pointer byte. A write to any register other than the Pointer register requires two data bytes.

Reading this device can take place either of two ways:

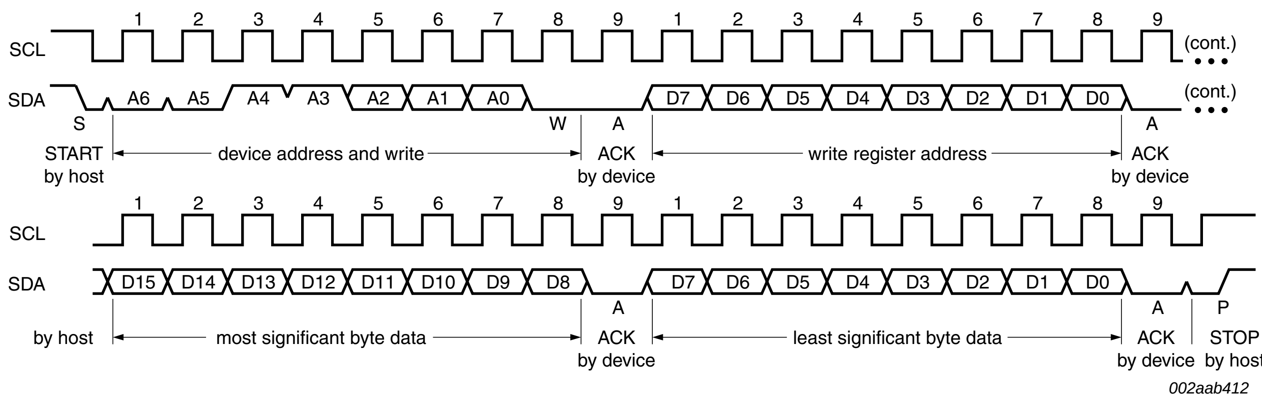
- If the location latched in the Pointer register is correct (most of the time it is expected that the Pointer register will point to one of the Temperature register (as it will be the data most frequently read), then the read can simply consist of an address byte, followed by retrieving the two data bytes.
- If the Pointer register needs to be set, then an address byte, pointer byte, repeat START, and another address byte will accomplish a read.

The data byte has the most significant bit first. At the end of a read, this device can accept either Acknowledge (ACK) or No Acknowledge (NACK) from the Master (No Acknowledge is typically used as a signal for the slave that the Master has read its last byte). It takes this device 125 ms to measure the temperature. Refer to the timing diagrams in Figure 8, Figure 9, Figure 10 and Figure 11 on how to program the device.



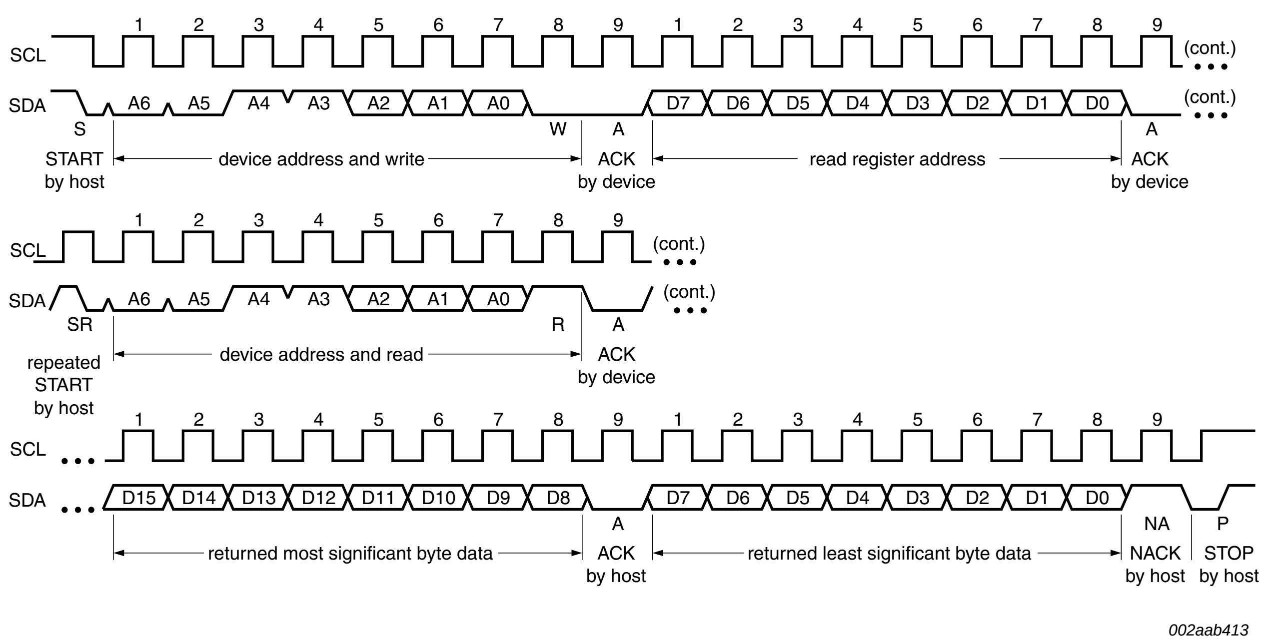
A = ACK = Acknowledge bit. W = Write bit = 0. R = Read bit = 1.

Fig 8. SMBus/I²C-bus write to the Pointer register



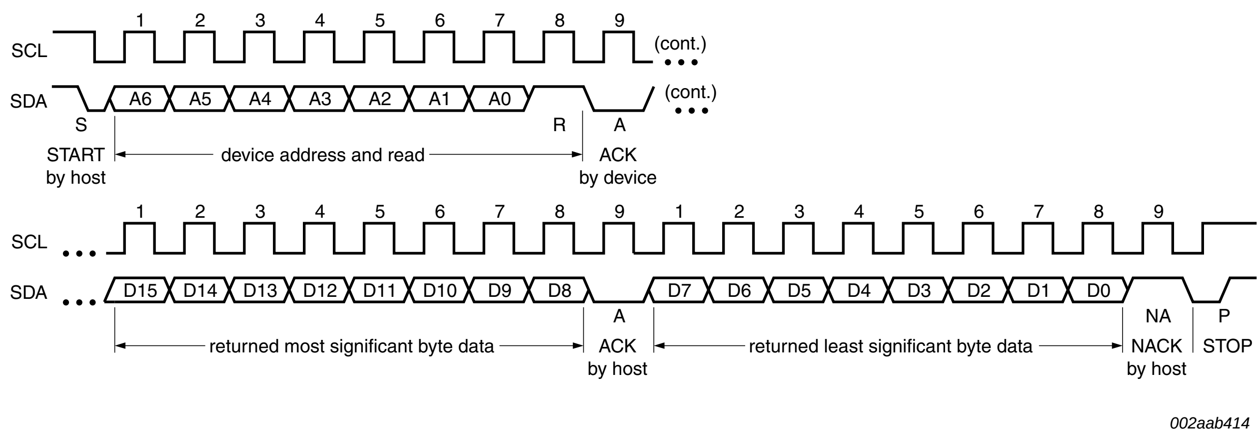
A = ACK = Acknowledge bit. W = Write bit = 0. R = Read bit = 1.

Fig 9. SMBus/I^{2}C-bus write to the Pointer register followed by a write data word



A = ACK = Acknowledge bit. NA = Not Acknowledge bit. W = Write bit = 0. R = Read bit = 1.

Fig 10. SMBus/I^{2}C-bus write to Pointer register followed by a repeat START and an immediate data word read



A = ACK = Acknowledge bit. NA = Not Acknowledge bit. W = Write bit = 0. R = Read bit = 1.

Fig 11. SMBus/I²C-bus word read from register with a pre-set pointer

7.10 Hot plugging

The SE98A can be used in hot plugging applications. Internal circuitry prevents damaging current backflow through the device when it is powered down, but with the I²C-bus, EVENT or address pins still connected. The open-drain SDA and EVENT pins (SCL and address pins are input only) effectively places the outputs in a high-impedance state during power-up and power-down, which prevents driver conflict and bus contention. The 50 ns noise filter will filter out any insertion glitches from the state machine, which is very robust and not prone to false operation.

The device needs a proper power-up sequence to reset itself, not only for the device I²C-bus and I/O initial states, but also to load specific pre-defined data or calibration data into its operational registers. The power-up sequence should occur correctly with a fast ramp rate and the I²C-bus active. The SE98A might not respond immediately after power-up, but it should not damage the part if the power-up sequence is abnormal. If the SCL line is held LOW, the part will not exit the power-on reset mode since the part is held in reset until SCL is released.

8. Register descriptions

8.1 Register overview

This section describes all the registers used in the SE98A. The registers are used for latching the temperature reading, storing the low and high temperature limits, configuring, the hysteresis threshold and the ADC, as well as reporting status. The device uses the Pointer register to access these registers. Read registers, as the name implies, are used for read only, and the write registers are for write only. Any attempt to read from a write-only register will result in reading zeroes. Writing to a read-only register will have no effect on the read even though the write command is acknowledged. The Pointer register is an 8-bit register. All other registers are 16-bit.

Table 5. Register summary

Address	POR state	Register name
n/a	n/a	Pointer register
00h	0037h	Capability register (B grade = 0037h)
01h	0000h	Configuration register
02h	0000h	Upper Boundary Alarm Trip register
03h	0000h	Lower Boundary Alarm Trip register
04h	0000h	Critical Alarm Trip register
05h	n/a	Temperature register
06h	1131h	Manufacturer ID register
07h	A102h	Device ID/Revision register
08h to 21h	0000h	reserved registers
22h	0000h	SMBus register
23h to FFh	0000h	reserved registers

A write to reserved registers my cause unexpected results which may result in requiring a reset by removing and re-applying its power.

8.2 Capability register (00h, 16-bit read-only)

Table 6. Capability register (address 00h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	RFU[9:2]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	RFU[1:0]		VHV	TRES[1:0]		WRNG	HACC	BCAP
Reset	0	0	1	1	0	1	1	1
Access	R	R	R	R	R	R	R	R

Table 7. Capability register (address 00h) bit description

Bit	Symbol	Description
15:6	RFU	Reserved for future use. Must be zero.
5	VHV	High voltage standoff for pin A0. 1 — This part can support a voltage up to 10 V on the A0 pin to support JC42.4 ballot 1435.00.
4:3	TRES	Temperature resolution. 10 — 0.125 °C LSB (11-bit)
2	WRNG	Wider range. 1 — can read temperatures below 0 °C and set sign bit accordingly
1	HACC	Higher accuracy (set during manufacture). 1 — B grade accuracy
0	BCAP	Basic capability. 1 — has Alarm and Critical Trips interrupt capability.

8.3 Configuration register (01h, 16-bit read/write)

Table 8. Configuration register (address 01h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	RFU					HEN[1:0]		SHMD
Default	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	CTLB	AWLB	CEVNT	ESTAT	EOCTL	CVO	EP	EMD
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 9. Configuration register (address 01h) bit description

Bit	Symbol	Description
15:11	RFU	reserved for future use; must be ‘0’.
10:9	HEN	Hysteresis Enable 00 — Disable hysteresis (default) 01 — Enable hysteresis at 1.5 °C 10 — Enable hysteresis at 3 °C 11 — Enable hysteresis at 6 °C When enabled, hysteresis is applied to temperature movement around trigger points. For example, consider the behavior of the ‘Above Alarm Window’ bit (bit 14 of the Temperature register) when the hysteresis is set to 3 °C. As the temperature rises, bit 14 will be set to 1 (temperature is above the alarm window) when the Temperature register contains a value that is greater than the value in the Alarm Temperature Upper Boundary register. If the temperature decreases, bit 14 will remain set until the measured temperature is less than or equal to the value in the Alarm Temperature Upper Boundary register minus 3 °C. (Refer to Figure 6 and Table 10). Similarly, the ‘Below Alarm Window’ bit (bit 13 of the Temperature register) will be set to 0 (temperature is equal to or above the Alarm Window Lower Boundary Trip register) when the value in the Temperature register is equal to or greater than the value in the Alarm Temperature Lower Boundary register. As the temperature decreases, bit 13 will be set to 1 when the value in the Temperature register is equal to or less than the value in the Alarm Temperature Lower Boundary register minus 3 °C. Note that hysteresis is also applied to EVENT pin functionality. When either of the Critical Trip or Alarm Window lock bits is set, these bits cannot be altered until unlocked.
8	SHMD	Shutdown Mode. 0 — Enabled Temperature Sensor (default) 1 — Disabled Temperature Sensor When shut down, the thermal sensor diode and Analog-to-Digital Converter (ADC) are disabled to save power, no events will be generated. When either of the Critical Trip or Alarm Window lock bits is set, this bit cannot be set until unlocked. However, it can be cleared at any time.

Table 9. Configuration register (address 01h) bit description *…continued*

Bit	Symbol	Description
7	CTLB	Critical Trip Lock bit. 0 — Critical Alarm Trip register is not locked and can be altered (default). 1 — Critical Alarm Trip register settings cannot be altered. This bit is initially cleared. When set, this bit will return a 1, and remains locked until cleared by internal Power-on reset. This bit can be written with a single write and do not require double writes.
6	AWLB	Alarm Window Lock bit. 0 — Upper and Lower Alarm Trip registers are not locked and can be altered (default). 1 — Upper and Lower Alarm Trip registers setting cannot be altered. This bit is initially cleared. When set, this bit will return a 1 and remains locked until cleared by internal power-on reset. This bit can be written with a single write and does not require double writes.
5	CEVNT	Clear $\overline{\text{EVENT}}$ (write only). 0 — No effect (default). 1 — Clears active $\overline{\text{EVENT}}$ in Interrupt mode. Writing to this register has no effect in Comparator mode. When read, this register always returns zero.
4	ESTAT	$\overline{\text{EVENT}}$ Status (read only). 0 — $\overline{\text{EVENT}}$ output condition is not being asserted by this device (default). 1 — $\overline{\text{EVENT}}$ output pin is being asserted by this device due to Alarm Window or Critical Trip condition. The actual event causing the $\overline{\text{EVENT}}$ can be determined from the Read Temperature register. Interrupt Events can be cleared by writing to the ‘Clear $\overline{\text{EVENT}}$’ bit (CEVNT). Writing to this bit will have no effect.
3	EOCTL	$\overline{\text{EVENT}}$ Output Control. 0 — $\overline{\text{EVENT}}$ output disabled (default). 1 — $\overline{\text{EVENT}}$ output enabled. When either of the Critical Trip or Alarm Window lock bits is set, this bit cannot be altered until unlocked.
2	CVO	Critical Event Only. 0 — $\overline{\text{EVENT}}$ output on Alarm or Critical temperature event (default) 1 — $\overline{\text{EVENT}}$ only if temperature is above the value in the critical temperature register When the Critical Trip or Alarm Window lock bit is set, this bit cannot be altered until unlocked. • **Advisory note:** – JEDEC specification requires only the Alarm Window lock bit to be set. – Work-around: Clear both Critical Trip and Alarm Window lock bits. – Future 1.7 V to 3.6 V SE98B will require only the Alarm Window lock bit to be set.

Table 9. Configuration register (address 01h) bit description *...continued*

Bit	Symbol	Description
1	EP	$\overline{\text{EVENT}}$ Polarity. 0 — active LOW (default). 1 — active HIGH. When either of the Critical Trip or Alarm Window lock bits is set, this bit cannot be altered until unlocked.
0	EMD	$\overline{\text{EVENT}}$ Mode. 0 — comparator output mode (default) 1 — interrupt mode When either of the Critical Trip or Alarm Window lock bits is set, this bit cannot be altered until unlocked.

Table 10. Hysteresis enable

Action	Below Alarm Window bit (bit 13)		Above Alarm Window bit (bit 14)		Above Critical Trip bit (bit 15)	
	Temperature slope	Threshold temperature	Temperature slope	Threshold temperature	Temperature slope	Threshold temperature
sets	falling	$T_{trip(l)} - T_{hys}$	rising	$T_{trip(u)}$	rising	$T_{th(crit)}$
clears	rising	$T_{trip(l)}$	falling	$T_{trip(u)} - T_{hys}$	falling	$T_{th(crit)} - T_{hys}$

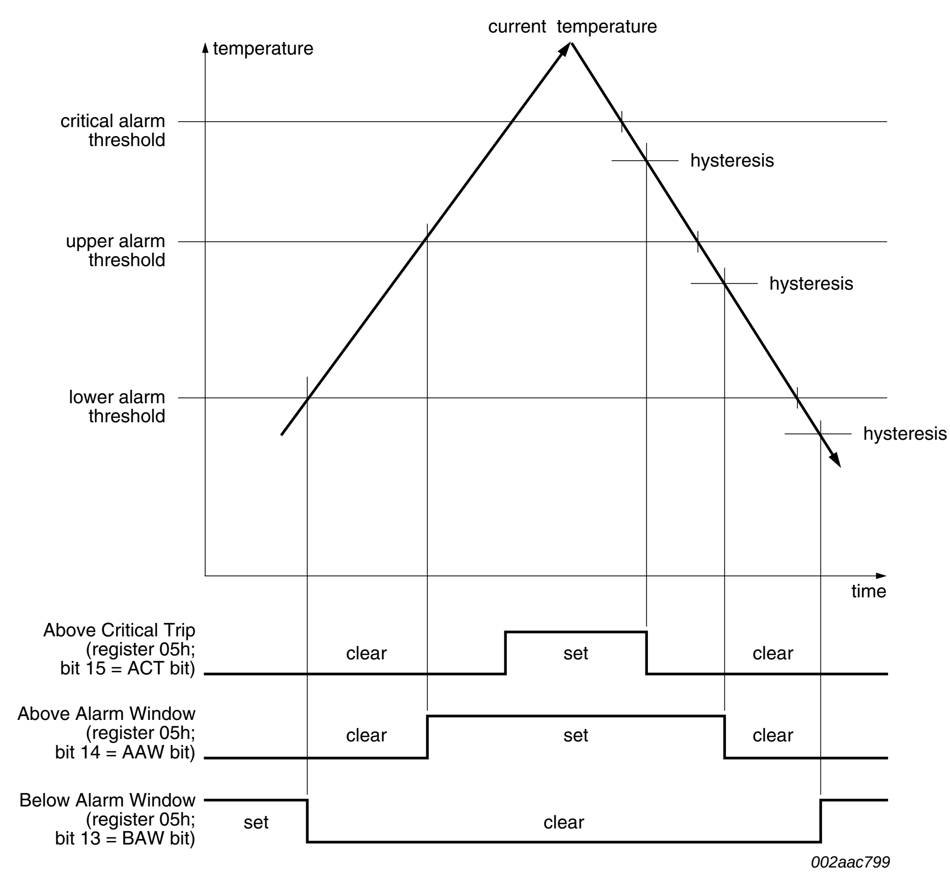


Fig 12. Hysteresis: how it works

8.4 Temperature format

The 16-bit value used in the following Trip Point Set and Temperature Read-Back registers is 2's complement with the Least Significant Bit (LSB) equal to 0.0625 °C. For example:

- A value of 019Ch will represent 25.75 °C
- A value of 07C0h will represent 124 °C
- A value of 1E64h will represent –25.75 °C.

The resolution is 0.125 °C. The unused LSB (bit 0) is set to '0'. Bit 11 will have a resolution of 128 °C.

The upper 3 bits of the temperature register indicate Trip Status based on the current temperature, and are not affected by the status of the EVENT output.

Table 11 lists the examples of the content of the temperature data register for positive and negative temperature for two scenarios of status bits: status bits = 000b and status bits = 111b.

Table 11. Degree Celsius and Temperature Data register

Temperature	Content of Temperature Data register			
	Status bits = 000b		Status bits = 111b	
	Binary	Hex	Binary	Hex
+125 °C	000 0 01111101 000 0	07D0h	111 0 01111101 000 0	E7D0h
+25 °C	000 0 00011001 000 0	0190h	111 0 00011001 000 0	E190h
+1 °C	000 0 00000001 000 0	0010h	111 0 00000001 000 0	E010h
+0.25 °C	000 0 00000000 010 0	0004h	111 0 00000000 010 0	E004h
+0.125 °C	000 0 00000000 001 0	0002h	111 0 00000000 001 0	E002h
0 °C	000 0 00000000 000 0	0000h	111 0 00000000 000 0	E000h
–0.125 °C	000 1 11111111 111 0	1FFEh	111 1 11111111 111 0	FFFEh
–0.25 °C	000 1 11111111 110 0	1FFCh	111 1 11111111 110 0	FFFCh
–1 °C	000 1 11111111 000 0	1FF0h	111 1 11111111 000 0	FFF0h
–20 °C	000 1 11110100 000 0	1F40h	111 1 11110100 000 0	FF40h
–25 °C	000 1 11100111 000 0	1E70h	111 1 11100111 000 0	FE70h
–55 °C	000 1 11001001 000 0	1C90h	111 1 11001001 000 0	FC90h

8.5 Temperature Trip Point registers

8.5.1 Upper Boundary Alarm Trip register (16-bit read/write)

The value is the upper threshold temperature value for Alarm mode. The data format is 2's complement with bit 2 = 0.25 °C. 'RFU' bits will always report zero. Interrupts will respond to the presently programmed boundary values. If boundary values are being altered in-system, it is advised to turn off interrupts until a known state can be obtained to avoid superfluous interrupt activity.

Table 12. Upper Boundary Alarm Trip register bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	RFU			SIGN	UBT[9:6]			
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	UBT[5:0]						RFU	
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Table 13. Upper Boundary Alarm Trip register bit description

Bit	Symbol	Description
15:13	RFU	reserved; always 0
12	SIGN	Sign (MSB)
11:2	UBT	Upper Boundary Alarm Trip Temperature (LSB = 0.25 °C)
1:0	RFU	reserved; always 0

8.5.2 Lower Boundary Alarm Trip register (16-bit read/write)

The value is the lower threshold temperature value for Alarm mode. The data format is 2's complement with bit 2 = 0.25 °C. RFU bits will always report zero. Interrupts will respond to the presently programmed boundary values. If boundary values are being altered in-system, it is advised to turn off interrupts until a known state can be obtained to avoid superfluous interrupt activity.

Table 14. Lower Boundary Alarm Trip register bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	RFU			SIGN	LBT[9:6]			
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	LBT[5:0]						RFU	
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Table 15. Lower Boundary Alarm Trip register bit description

Bit	Symbol	Description
15:13	RFU	reserved; always 0
12	SIGN	Sign (MSB)
11:2	LBT	Lower Boundary Alarm Trip Temperature (LSB = 0.25 °C)
1:0	RFU	reserved; always 0

8.5.3 Critical Alarm Trip register (16-bit read/write)

The value is the critical temperature. The data format is 2's complement with bit 2 = 0.25 °C. RFU bits will always report zero.

Table 16. Lower Boundary Alarm Trip register bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	RFU			SIGN	CT[9:6]			
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	CT[5:0]						RFU	
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Table 17. Critical Alarm Trip register bit description

Bit	Symbol	Description
15:13	RFU	reserved; always 0
12	SIGN	Sign (MSB)
11:2	CT	Critical Alarm Trip Temperature (LSB = 0.25 °C)
1:0	RFU	reserved; always 0

8.6 Temperature register (16-bit read-only)

Table 18. Temperature register bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	ACT	AAW	BAW	SIGN	TEMP[10:7]			
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	TEMP[6:0]							RFU
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 19. Temperature register bit description

Bit	Symbol	Description
15	ACT	Above Critical Trip. Increasing T_{amb}: 0 — $T_{amb} < T_{th(crit)}$ 1 — $T_{amb} \geq T_{th(crit)}$ Decreasing T_{amb}: 0 — $T_{amb} < T_{th(crit)} - T_{hys}$ 1 — $T_{amb} \geq T_{th(crit)} - T_{hys}$
14	AAW	Above Alarm Window. Increasing T_{amb}: 0 — $T_{amb} \leq T_{trip(u)}$ 1 — $T_{amb} > T_{trip(u)}$ Decreasing T_{amb}: 0 — $T_{amb} \leq T_{trip(u)} - T_{hys}$ 1 — $T_{amb} > T_{trip(u)} - T_{hys}$
13	BAW	Below Alarm Window. Increasing T_{amb}: 0 — $T_{amb} \geq T_{trip(l)}$ 1 — $T_{amb} < T_{trip(l)}$ Decreasing T_{amb}: 0 — $T_{amb} \geq T_{trip(l)} - T_{hys}$ 1 — $T_{amb} < T_{trip(l)} - T_{hys}$
12	SIGN	Sign bit. 0 — positive temperature value 1 — negative temperature value
11:1	TEMP	Temperature Value (2’s complement). (LSB = 0.125 °C)
0	RFU	reserved; always 0

8.7 Manufacturer’s ID register (16-bit read-only)

The manufacture’s ID matches that assigned to NXP Semiconductors PCI-SIG (1131h), and is intended for use to identify the manufacturer of the device.

Table 20. Manufacturer’s ID register bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	Manufacturer ID							
Reset	0	0	0	1	0	0	0	1
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	(continued)							
Reset	0	0	1	1	0	0	0	1
Access	R	R	R	R	R	R	R	R

8.8 Device ID register

The device ID and device revision are A1h and 02h, respectively.

Table 21. Device ID register bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	Device ID							
Reset	1	0	1	0	0	0	0	1
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	Device revision							
Reset	0	0	0	0	0	0	1	0
Access	R	R	R	R	R	R	R	R

8.9 SMBus register

Table 22. SMBus Time-out register bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	RFU							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	STMOUT	RFU						SALRT
Reset	0	0	0	0	0	0	0	0
Access	R/W	R	R	R	R	R	R	R/W

Table 23. SMBus Time-out register bit description

Bit	Symbol	Description
15:8	RFU	reserved; always 0
7	STMOUT	SMBus time-out. 0 — SMBus time-out is enabled (default) 1 — disable SMBus time-out When either of the Critical Trip or Alarm Window lock bits is set, this bit cannot be altered until unlocked.
6:1	RFU	reserved; always 0
0	SALRT	SMBus ALERT. 0 — SMBus ALERT is enabled (default) 1 — disable SMBus ALERT When either of the Critical Trip or Alarm Window lock bits is set, this bit cannot be altered until unlocked.

9. Application design-in information

In a typical application, the SE98A behaves as a slave device and interfaces to the master (or host) via the SCL and SDA lines. The host monitors the EVENT output pin, which is asserted when the temperature reading exceeds the programmed values in the alarm registers. The A0, A1 and A2 pins are directly connected to the shared SPD's A0, A1 and A2 pins, otherwise they must be pulled HIGH or LOW. The SDA and SCL serial interface pins are open-drain and require pull-up resistors, and are able to sink a maximum current of 3 mA with a voltage drop less than 0.4 V. Typical pull-up values for SCL and SDA are 10 kΩ, but the resistor values can be changed in order to meet the rise time requirement if the capacitance load is too large due to routing, connectors, or multiple components sharing the same bus.

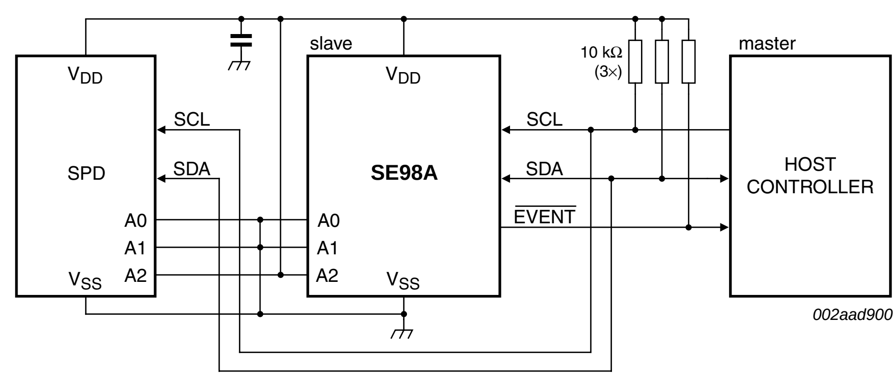


Fig 13. Typical application

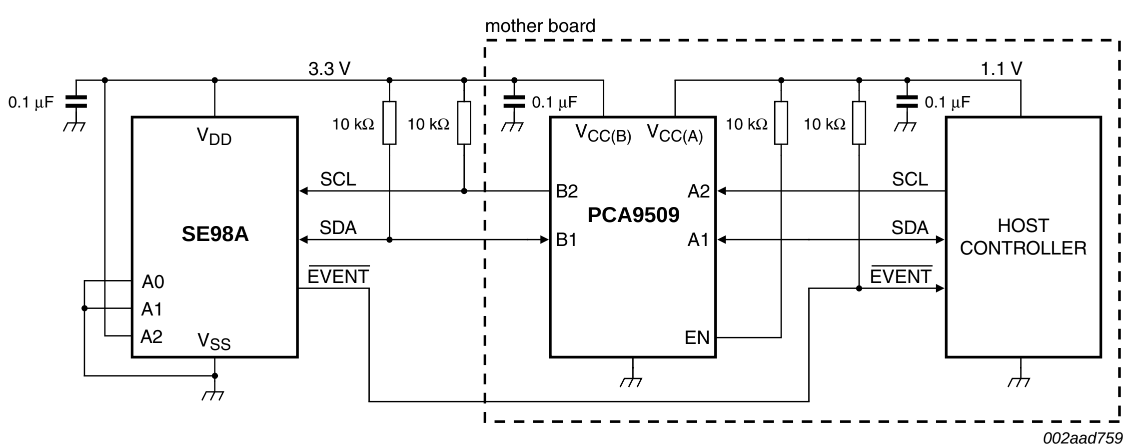


Fig 14. SE98A interfacing with 1.1 V host controller

9.1 SE98A in memory module application

Figure 15 shows the SE98A being placed in the memory module application with the SPD. The SE98A is centered in the memory module to provide the function to monitor the temperature of the DRAM. In the event of overheat, the SE98A triggers the $\overline{\text{EVENT}}$ output and the memory controller can throttle the memory bus to slow the DRAM, or the CPU can increase the refresh rate for the DRAM. The memory controller can also read the SE98A and watch the DRAM thermal behavior.

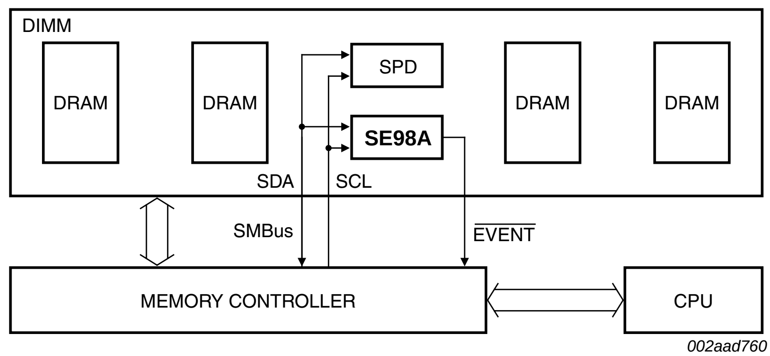


Fig 15. System application

9.2 Layout consideration

The SE98A does not require any additional components other than the host controller to measure temperature. A 0.1 μF bypass capacitor between the V_{DD} and V_{SS} pins is located as close as possible to the power and ground pins for noise protection.

9.3 Thermal considerations

In general, self-heating is the result of power consumption and not a concern, especially with the SE98A, which consumes very low power. In the event the SDA and $\overline{\text{EVENT}}$ pins are heavily loaded with small pull-up resistor values, self-heating affects temperature accuracy by approximately 0.5 °C.

Equation 1 is the formula to calculate the effect of self-heating:

$$\Delta T = R_{th(j\text{-}a)} \times [(V_{DD} \times I_{DD(AV)}) + (V_{OL(SDA)} \times I_{OL(sink)(SDA)}) + (V_{OL(EVENT)} \times I_{OL(sink)EVENT})] \quad (1)$$

where:

$\Delta T = T_j - T_{amb}$

T_j = junction temperature

T_{amb} = ambient temperature

$R_{th(j\text{-}a)}$ = package thermal resistance

V_{DD} = supply voltage

$I_{DD(AV)}$ = average supply current

$V_{OL(SDA)}$ = LOW-level output voltage on pin SDA

$V_{OL(EVENT)}$ = LOW-level output voltage on pin $\overline{\text{EVENT}}$

$I_{OL(sink)(SDA)}$ = SDA output current LOW

$I_{OL(sink)EVENT}$ = $\overline{EVENT}$ output current LOW

10. Limiting values

Table 24. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.3	+4.2	V
V_n	voltage on any other pin	SDA, SCL, $\overline{EVENT}$ pins	–0.3	+4.2	V
V_{A0}	voltage on pin A0	overvoltage input; A0 pin	–0.3	+12.5	V
I_{sink}	sink current	at SDA, SCL, $\overline{EVENT}$ pins	–1	+50.0	mA
$T_{j(max)}$	maximum junction temperature		-	150	°C
T_{stg}	storage temperature		–65	+165	°C

11. Characteristics

Table 25. Characteristics

V_{DD} = 1.7 V to 3.6 V; T_{amb} = –40 °C to +125 °C; unless otherwise specified.

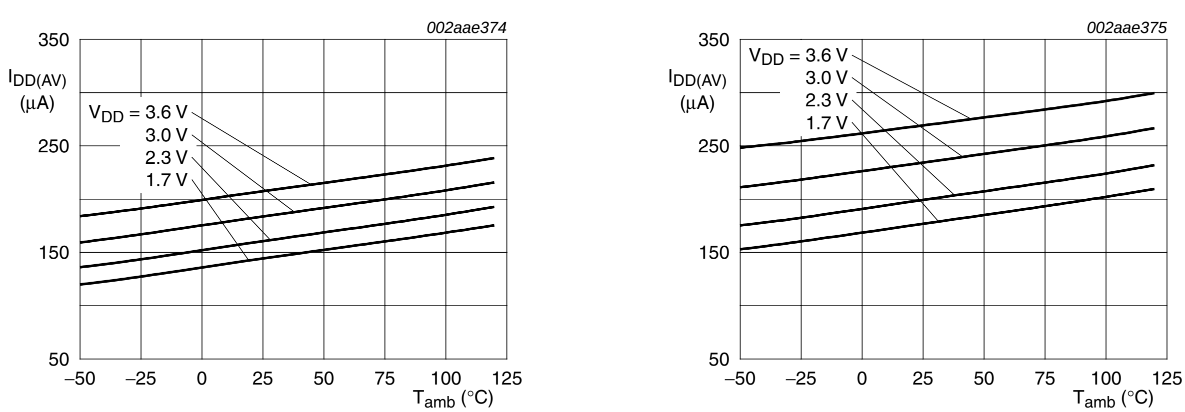
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{acc}	temperature accuracy	B grade temperature accuracy; V_{DD} = 1.7 V to 3.6 V				
		T_{amb} = 75 °C to 95 °C	–1.0	< ±0.5	+1.0	°C
		T_{amb} = 40 °C to 125 °C	–2.0	< ±1	+2.0	°C
		T_{amb} = –40 °C to +125 °C	–3.0	< ±2	+3.0	°C
T_{res}	temperature resolution		-	0.125	-	°C
$I_{DD(AV)}$	average supply current		-	250	400	µA
$I_{DD(stb)}$	standby supply current	SMBus inactive	-	0.1	5	µA
T_{conv}	conversion period		-	100	120	ms
$E_{f(conv)}$	conversion rate error	percentage error in programmed data	–30	-	+30	%
I_{LIL}	LOW-level input leakage current	pins A0, A1, A2; $V_I = V_{SS}$	–1.0	-	+1.0	µA
I_{pd}	pull-down current	internal; pins A0, A1, A2; $V_I = 0.3V_{DD}$ to V_{DD}	0.05	-	4.0	µA
Z_{IL}	LOW-level input impedance	pins A0, A1, A2; $V_I < 0.3V_{DD}$	30	-	-	kΩ
Z_{IH}	HIGH-level input impedance	pins A0, A1, A2; $V_I \geq 0.3V_{DD}$	800	-	-	kΩ
V_{DD}	supply voltage		1.7	1.8 or 2.5 or 3.3	3.6	V

Table 26. SMBus DC characteristics

V_{DD} = 1.7 V to 3.6 V; T_{amb} = −20 °C to +120 °C; unless otherwise specified. These specifications are guaranteed by design.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	SCL, SDA; V_{DD} = 1.7 V to 3.6 V		0.7V_{DD}	-	V_{DD} + 1	V
V_{IL}	LOW-level input voltage	SCL, SDA; V_{DD} = 1.7 V to 3.6 V		-	-	0.3V_{DD}	V
$V_{I(ov)}$	overvoltage input voltage	pin A0; $V_{I(ov)} - V_{DD}$ > 4.8 V	[1]	7.0	-	10	V
$V_{th(POR)H}$	HIGH-level power-on reset threshold voltage			-	-	1.7	V
$V_{th(rec)POR}$	power-on reset recovery threshold voltage	for device reset		-	-	0.5	V
$I_{OL(sink)EVENT}$	LOW-level output sink current on pin $\overline{EVENT}$	V_{OL} = 0.4 V		6	-	-	mA
$I_{OL(sink)(SDA)}$	LOW-level output sink current on pin SDA	V_{OL} = 0.5 V		3	-	-	mA
I_{LOH}	HIGH-level output leakage current	$V_{OH} = V_{DD}$		-	-	1.0	μA
I_{LIH}	HIGH-level input leakage current	pins SCL, SDA; $V_I = V_{DD}$ or V_{SS}		−1.0	-	+1.0	μA
I_{LIL}	LOW-level input leakage current	pins SCL, SDA; $V_I = V_{DD}$ or V_{SS}		−1.0	-	+1.0	μA
C_i	input capacitance	SCL, SDA pins		-	5	10	pF

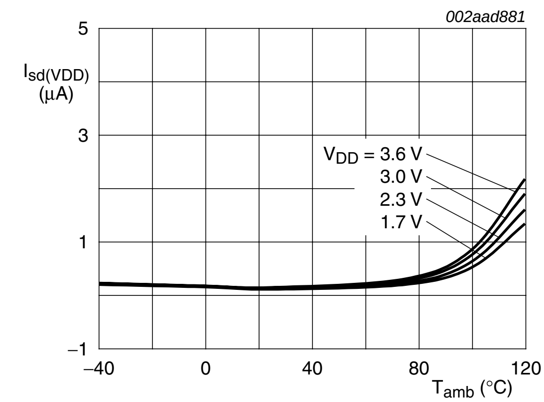
[1] High-voltage input voltage applied to pin A0 during RWP and CRWP operations of the equivalent SPD-included parts. The JEDEC specification is 7 V (min.) and 10 V (max.). When V_{DD} is 3.6 V, then $V_{I(ov)}$ > 4.8 V + V_{DD} or > 4.8 V + 3.6 V then the minimum voltage is 8.4 V.



a. I²C-bus inactive

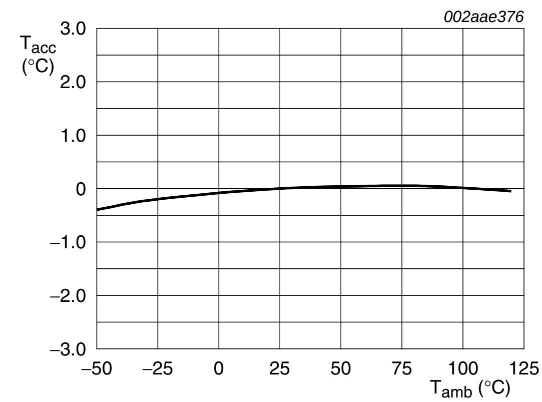
b. I²C-bus active

Fig 16. Average supply current



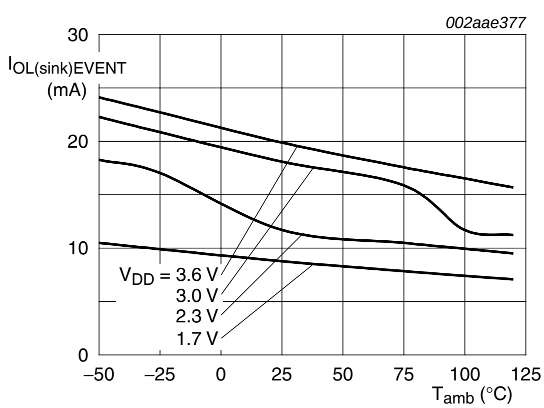
I^2C-bus and temp sensor inactive.

Fig 17. Shutdown supply current



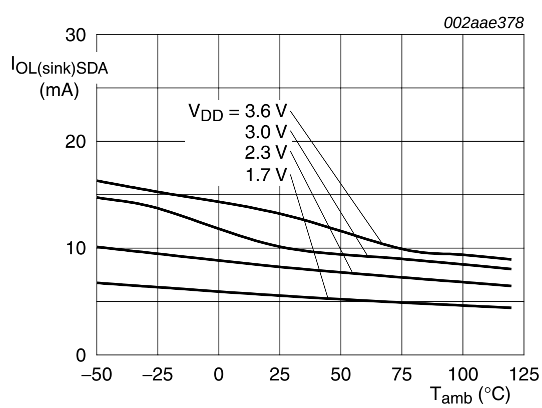
V_{DD} = 1.7 V to 3.6 V.

Fig 18. Typical temperature accuracy



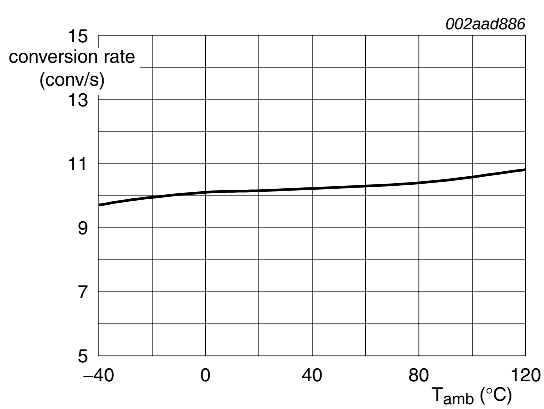
V_{OL} = 0.4 V.

Fig 19. EVENT output current



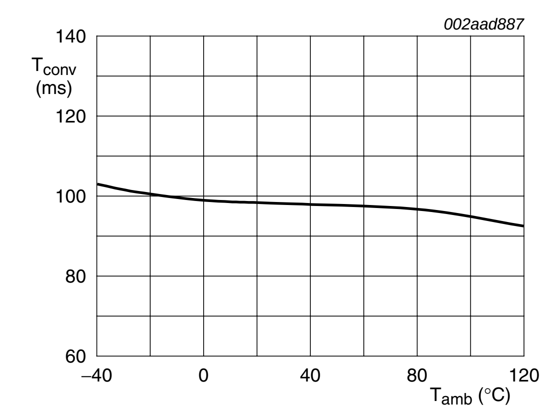
V_{OL} = 0.5 V.

Fig 20. SDA output current



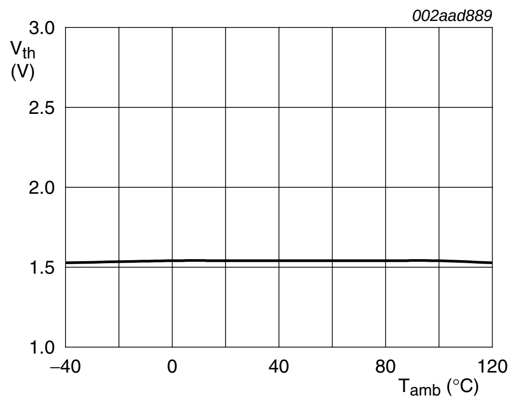
V_{DD} = 3.0 V to 3.6 V.

Fig 21. Conversion rate



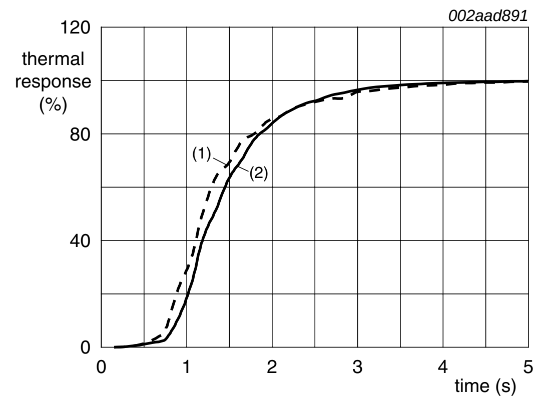
V_{DD} = 3.0 V to 3.6 V.

Fig 22. Conversion period



For temp sensor conversion.

Fig 23. Average power-on threshold voltage

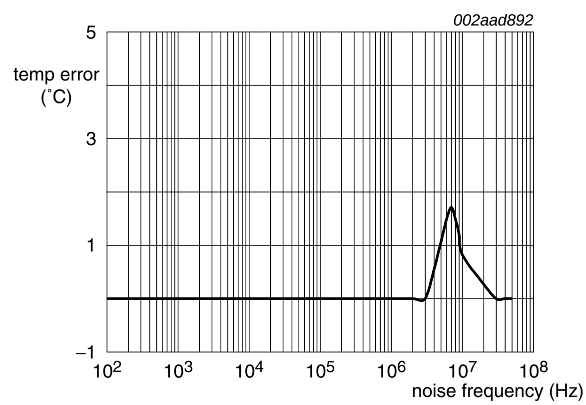


From 25 °C (air) to 120 °C (oil bath).

(1) TSSOP8

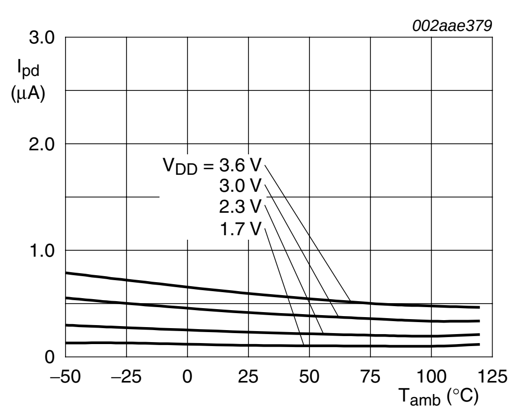
(2) HWSON8

Fig 24. Package thermal response

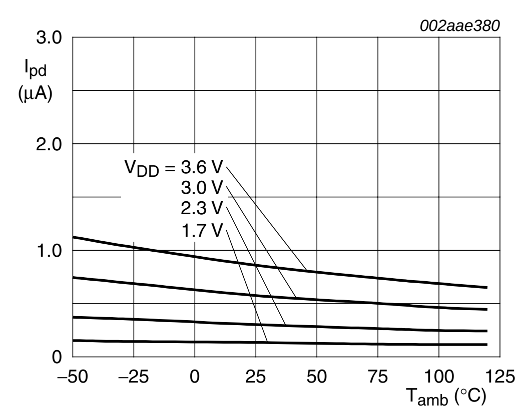


V_{DD} = 3.3 V + 150 mV (p-p); 0.1 μF AC coupling capacitor; no decoupling capacitor; T_{amb} = 25 °C.

Fig 25. Temperature error versus power supply noise frequency



a. $V_I = 0.3V_{DD}$; pins A0, A1, A2



b. $V_I = 0.7V_{DD}$; pins A0, A1, A2

Fig 26. Typical pull-down current

Table 27. SMBus AC characteristics

V_{DD} = 1.7 V to 3.6 V; T_{amb} = −40 °C to +125 °C; unless otherwise specified. These specifications are guaranteed by design. The AC specifications fully meet or exceed SMBus 2.0 specifications, but allow the bus to interface with the I^2C-bus from DC to 400 kHz.

Symbol	Parameter	Conditions		Standard mode		Fast mode		Unit
				Min	Max	Min	Max	
f_{SCL}	SCL clock frequency			10[1]	100	10[1]	400	kHz
t_{HIGH}	HIGH period of the SCL clock	70 % to 70 %		4000	-	600	-	ns
t_{LOW}	LOW period of the SCL clock	30 % to 30 %		4700	-	1300	-	ns
$t_{to(SMBus)}$	SMBus time-out time	LOW period to reset SMBus		25	35	25	35	ms
t_r	rise time of both SDA and SCL signals			-	1000	20	300	ns
t_f	fall time of both SDA and SCL signals			-	300	-	300	ns
$t_{SU;DAT}$	data set-up time			250	-	100	-	ns
$t_{h(i)(D)}$	data input hold time		[2][3]	0	-	0	-	ns
$t_{HD;DAT}$	data hold time		[4]	200	3450	200	900	ns
$t_{SU;STA}$	set-up time for a repeated START condition		[5]	4700	-	600	-	ns
$t_{HD;STA}$	hold time (repeated) START condition	30 % of SDA to 70 % of SCL	[6]	4000	-	600	-	ns
$t_{SU;STO}$	set-up time for STOP condition			4000	-	600	-	ns
t_{BUF}	bus free time between a STOP and START condition		[2]	4700	-	1300	-	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter			-	50	-	50	ns
$t_{VD;DAT}$	data valid time	from clock		200	-	200	-	ns
$t_{f(o)}$	output fall time			-	-	-	250	ns
t_{POR}	power-on reset pulse time	power supply falling		0.5	-	0.5	-	µs

[1] Minimum clock frequency is 0 kHz if SMBus Time-out is disabled.

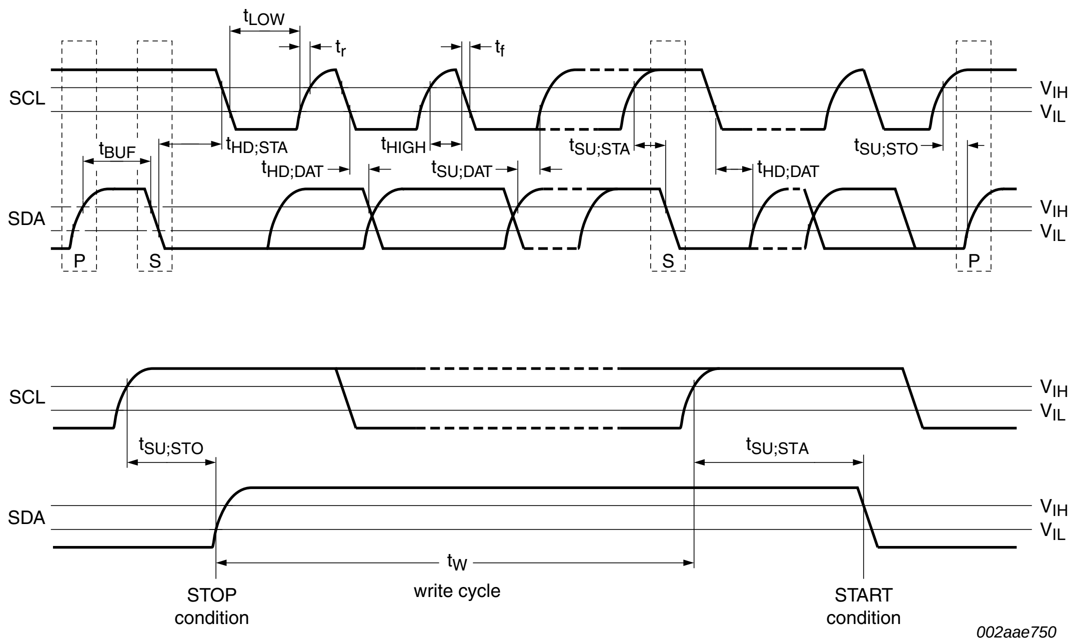
[2] Delay from SDA STOP to SDA START.

[3] A device must internally provide a hold time of at least 200 ns for SDA signal (referenced to the $V_{IH(min)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[4] Delay from SCL HIGH-to-LOW transition to SDA edges.

[5] Delay from SCL LOW-to-HIGH transition to restart SDA.

[6] Delay from SDA START to first SCL HIGH-to-LOW transition.



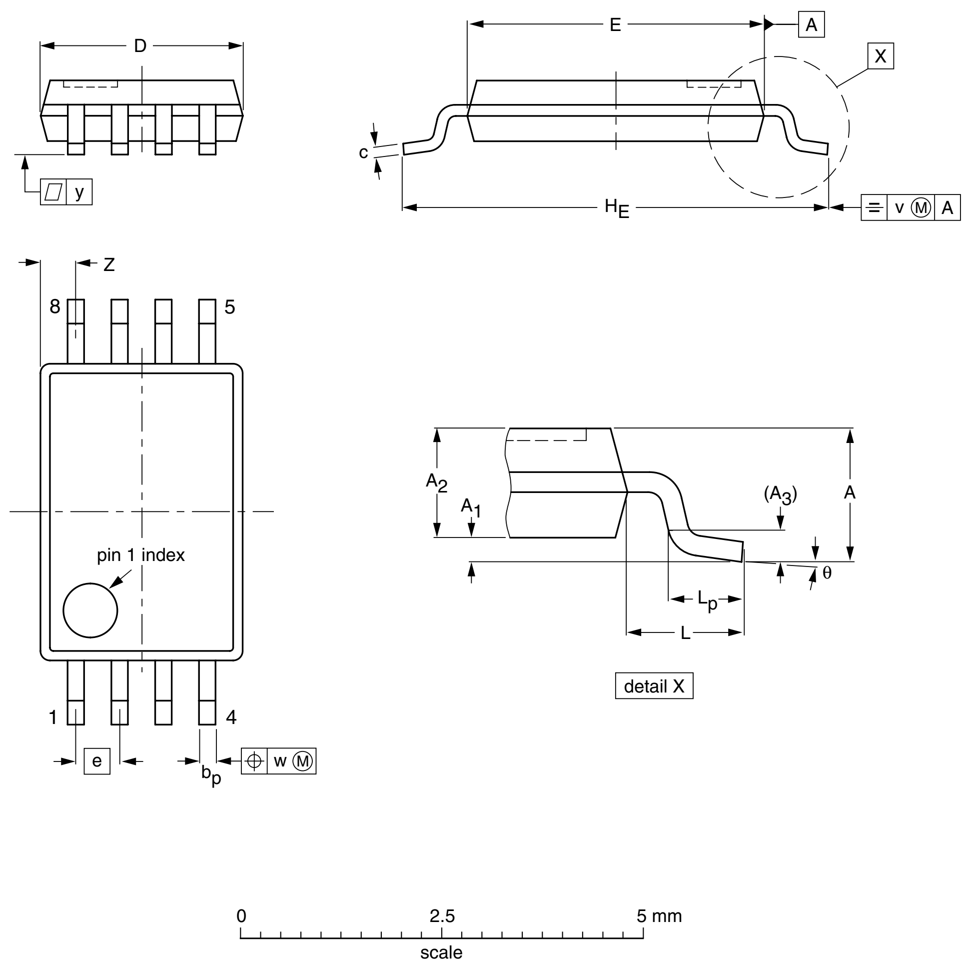
S = START condition

P = STOP condition

Fig 27. AC waveforms

12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 4.4 mm **SOT530-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.85	0.25	0.30 0.19	0.20 0.13	3.1 2.9	4.5 4.3	0.65	6.5 6.3	0.94	0.7 0.5	0.1	0.1	0.1	0.70 0.35	8° 0°

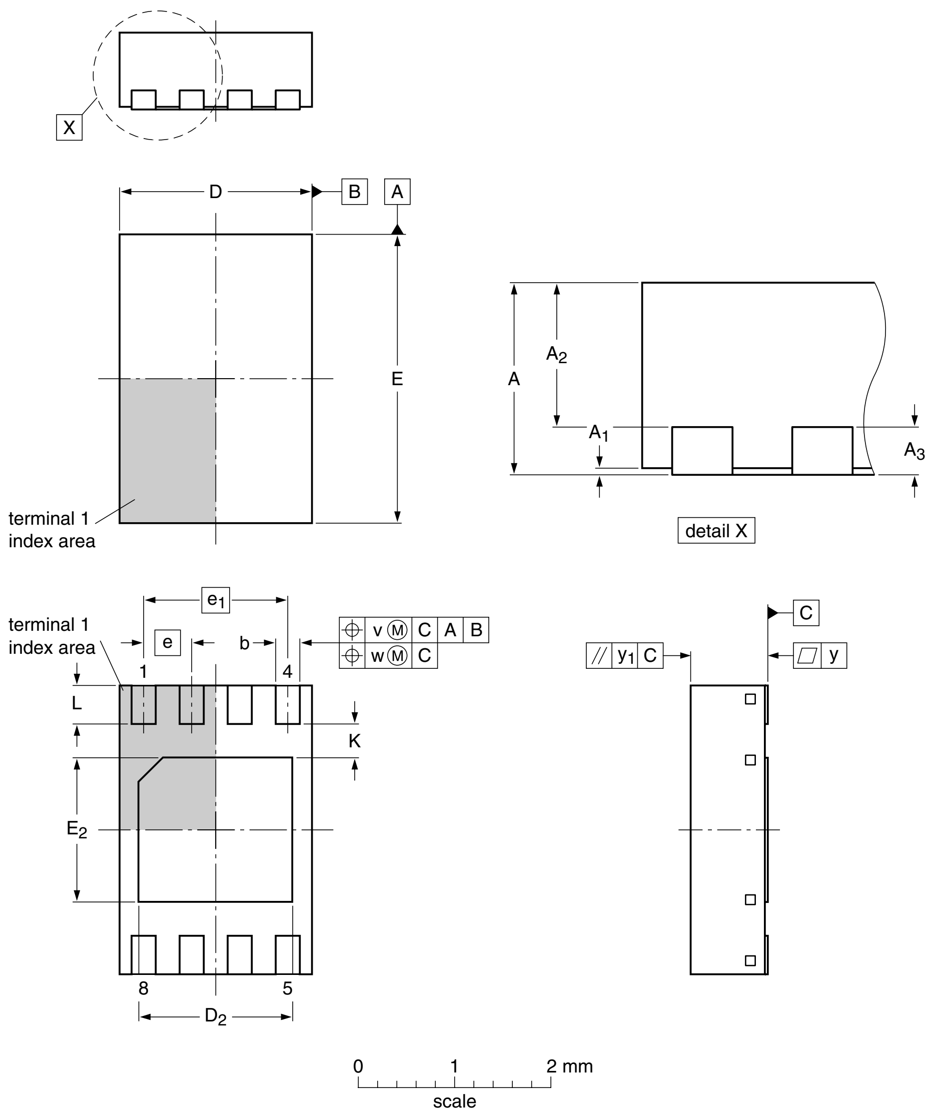
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT530-1		MO-153				~~00-02-24~~ 03-02-18

Fig 28. Package outline SOT530-1 (TSSOP8)

HWSON8: plastic thermal enhanced very very thin small outline package; no leads; 8 terminals; body 2 x 3 x 0.8 mm **SOT1069-2**



Dimensions

Unit		A(1)	A_1	A_2	A_3	b	D(1)	D_2	E(1)	E_2	e	e_1	K	L	v	w	y	y_1
	max	0.80	0.05	0.65		0.30	2.1	1.6	3.1	1.6			0.40	0.45				
mm	nom	0.75	0.02	0.55	0.2	0.25	2.0	1.5	3.0	1.5	0.5	1.5	0.35	0.40	0.1	0.05	0.05	0.05
	min	0.70	0.00	0.45		0.18	1.9	1.4	2.9	1.4			0.30	0.35				

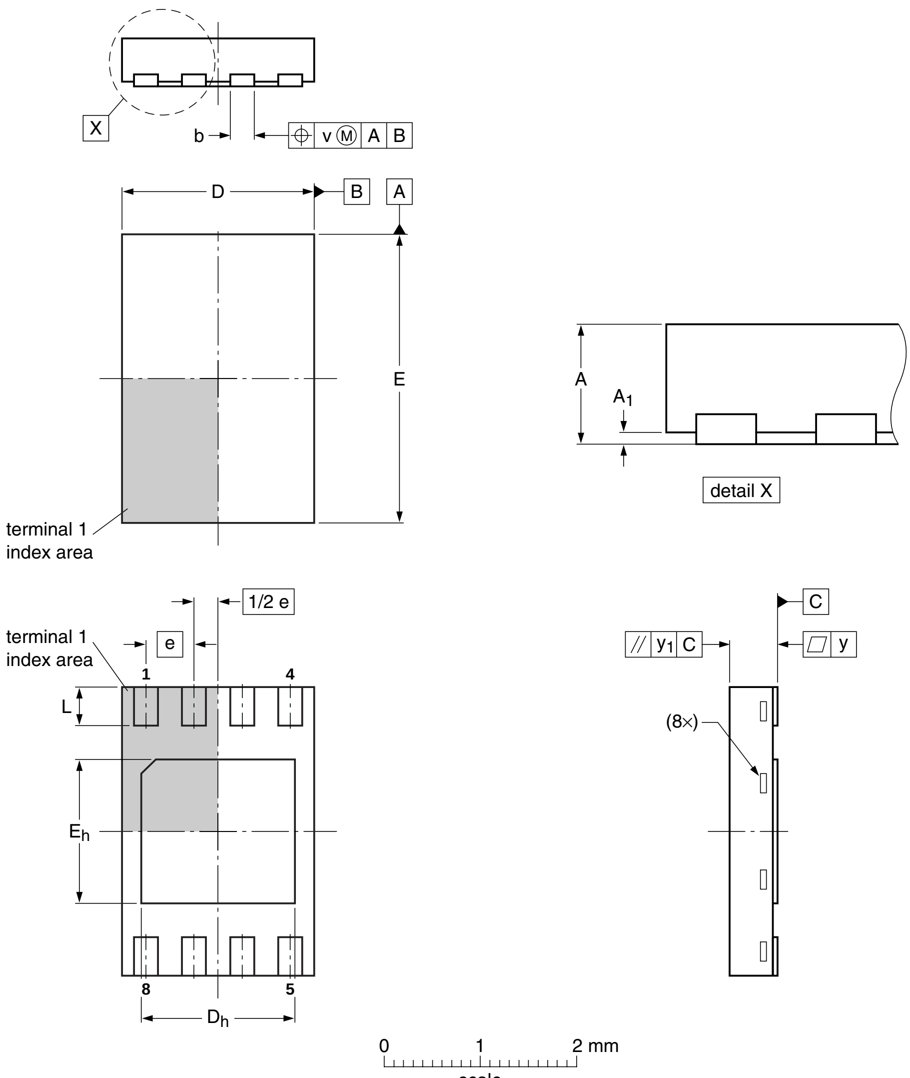
Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1069-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1069-2	- - -	MO-229	- - -			~~09-10-22~~ 09-11-18

Fig 29. Package outline SOT1069-2 (HWSON8)

HXSON8: plastic thermal enhanced extremely thin small outline package; no leads; 8 terminals; body 2 x 3 x 0.5 mm **SOT1052-1**



DIMENSIONS (mm are the original dimensions)

UNIT		$A^{(1)}$	A_1	b	D	D_1	E	E_1	e	L	v	y	y_1
mm	max	0.5	0.04	0.3	2.1	1.6	3.1	1.6		0.45			
	nom				2.0		3.0		0.5		0.1	0.05	0.05
	min			0.2	1.9	1.4	2.9	1.4		0.35			

Note

1. Dimension A is including plating thickness. The package footprint is compatible with JEDEC MO229

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT1052-1		MO-229				~~08-01-11~~ 08-03-11

Fig 30. Package outline SOT1052-1 (HXSON8)

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 31) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 28 and 29

Table 28. SnPb eutectic process (from J-STD-020C)

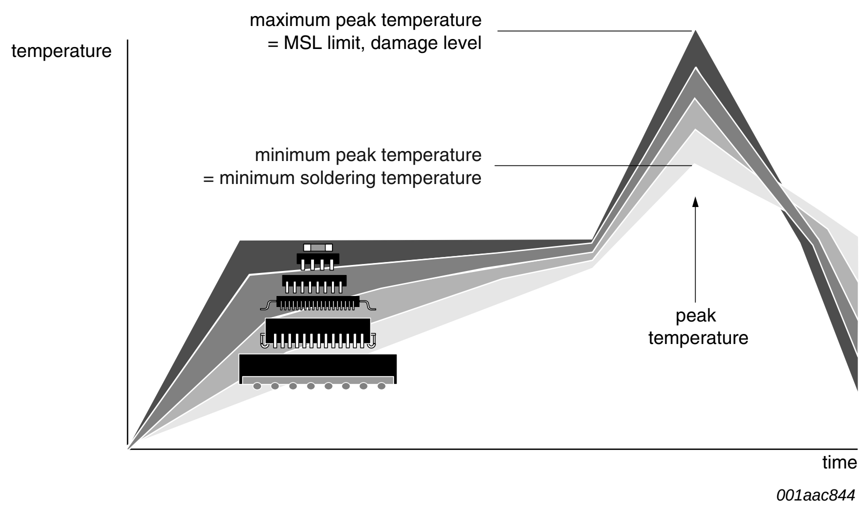
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 29. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 31.



MSL: Moisture Sensitivity Level

Fig 31. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

14. Abbreviations

Table 30. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
ARA	Alert Response Address
BIOS	Basic Input/Output System
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
CRWP	Clear Reversible Write Protection
DDR	Double Data Rate
DDR2	Double Data Rate 2
DDR3	Double Data Rate 3
DIMM	Dual In-line Memory Module
DRAM	Dynamic Random Access Memory
ESD	ElectroStatic Discharge
HBM	Human Body Model
I^2C-bus	Inter IC bus
I/O	Input/Output
LSB	Least Significant Bit
MM	Machine Model
MSB	Most Significant Bit

Table 30. Abbreviations *…continued*

Acronym	Description
RDIMM	Registered Dual In-line Memory Module
SO-DIMM	Small Outline Dual In-line Memory Module
PC	Personal Computer
POR	Power-On Reset
RWP	Reversible Write Protection
SMBus	System Management Bus
SPD	Serial Presence Detect

15. Revision history

Table 31. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SE98A_4	20091125	Product data sheet	-	SE98A_3
Modifications:	• Table 1 “Ordering information”: for Type number SE98ATP, the Version is changed from “SOT1069-1” to “SOT1069-2” • Figure 29: package outline drawing changed from “SOT1069-1” to “SOT1069-2”			
SE98A_3	20090817	Product data sheet	-	SE98A_2
SE98A_2	20090806	Product data sheet	-	SE98A_1
SE98A_1	20090305	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Contents

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