

## 2.4GHz Band SP3T Switch + LNA GaAs MMIC

### ■ GENERAL DESCRIPTION

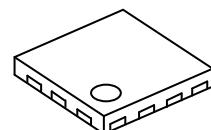
The NJG1730MD7 is a 2.4GHz band SP3T Switch + low noise amplifier GaAs MMIC designed for wireless LAN and Bluetooth front-end applications.

The NJG1730MD7 features low insertion loss of Transmit/Bluetooth path and high gain and low noise figure of RX LNA mode.

The NJG1730MD7 has ESD protection devices to achieve excellent ESD performances.

A small and ultra-thin package of EQFN14-D7 is adopted.

### ■ PACKAGE OUTLINE



NJG1730MD7

### ■ APPLICATIONS

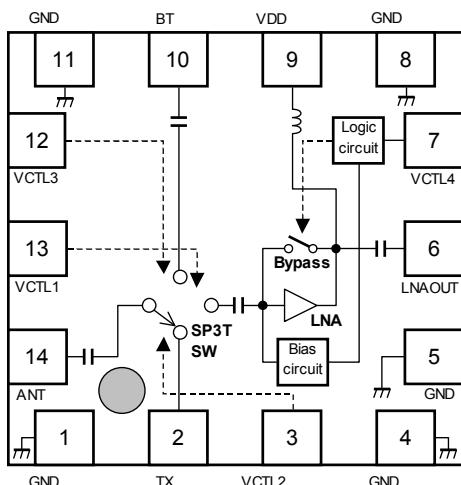
2.4GHz Band WLAN and Bluetooth front-end application

### ■ FEATURES

- Operating voltage  $V_{DD}=3.6V$  typ.
- Operating frequency freq=2400 to 2500MHz
- [ RX LNA mode ]
  - Operating current 10mA typ. @ $V_{DD}=3.6V$ ,  $V_{CTL1}=V_{CTL4}=3.3V$ ,  $V_{CTL2}=V_{CTL3}=0V$
  - Small signal gain 15.0dB typ.
  - Noise figure 1.6dB typ.
  - Input power 1dB compression -4dBm typ.
- [ RX Bypass mode ]
  - Operating current 4μA typ. @ $V_{DD}=3.6V$ ,  $V_{CTL1}=3.3V$ ,  $V_{CTL2}=V_{CTL3}=V_{CTL4}=0V$
  - Input power 1dB compression +9dBm typ.
- [ TX mode ]
  - Insertion loss 0.5dB typ.
  - Input power 0.1dB compression +30dBm typ.
- [ BT mode ]
  - Insertion loss 0.6dB typ.
  - Input power 0.1dB compression +26dBm typ.
- Package EQFN14-D7 (Package size: 1.6mm x 1.6mm x 0.397mm typ.)
- RoHS compliant and Halogen Free, MSL1

### ■ PIN CONFIGURATION

(Top view)



#### Pin Connection

1. GND	8. GND
2. TX	9. VDD
3. VCTL2	10. BT
4. GND	11. GND
5. GND	12. VCTL3
6. LNAOUT	13. VCTL1
7. VCTL4	14. ANT
Exposed Pad: GND	

Note: Specifications and description listed in this datasheet are subject to change without notice.

## ■ ABSOLUTE MAXIMUM RATINGS

Ta=+25°C

PARAMETERS	SYMBOL	CONDITIONS	RATINGS	UNITS
Supply voltage	V <sub>DD</sub>		5.5	V
Control voltage	V <sub>CTL</sub>		5.5	V
Input power 1	P <sub>IN1</sub>	ANT terminal, V <sub>DD</sub> =3.6V, V <sub>CTL1</sub> =3.3V V <sub>CTL2</sub> =V <sub>CTL3</sub> =0V, V <sub>CTL4</sub> =3.3/0V	+15	dBm
Input power 2	P <sub>IN2</sub>	TX terminal, V <sub>DD</sub> =3.6V, V <sub>CTL2</sub> =3.3V V <sub>CTL1</sub> =V <sub>CTL3</sub> =V <sub>CTL4</sub> =0V	+25	dBm
Input power 3	P <sub>IN3</sub>	BT terminal, V <sub>DD</sub> =3.6V, V <sub>CTL3</sub> =3.3V V <sub>CTL1</sub> =V <sub>CTL2</sub> =V <sub>CTL4</sub> =0V	+25	dBm
Power dissipation	P <sub>D</sub>	Four-layer FR4 PCB with through-hole (76.2x114.3mm), T <sub>j</sub> =150°C	1300	mW
Operation temperature	T <sub>opr</sub>		-40 to +85	°C
Storage temperature	T <sub>stg</sub>		-55 to +150	°C

## ■ ELECTRICAL CHARACTERISTICS 1 (DC Characteristics)

V<sub>DD</sub>=3.6V, V<sub>CTL(H)</sub>=3.3V, V<sub>CTL(L)</sub>=0V, Ta=+25°C, Z<sub>S</sub>=Z<sub>L</sub>=50Ω

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply voltage	V <sub>DD</sub>		3.0	3.6	5.0	V
Control voltage 1(High)	V <sub>CTL1(H)</sub>		2.8	3.3	5.0	V
Control voltage 2(High)	V <sub>CTL2(H)</sub>		2.8	3.3	5.0	V
Control voltage 3(High)	V <sub>CTL3(H)</sub>		2.8	3.3	5.0	V
Control voltage 4(High)	V <sub>CTL4(H)</sub>		2.8	3.3	5.0	V
Control voltage 1(Low)	V <sub>CTL1(L)</sub>		0.0	-	0.4	V
Control voltage 2(Low)	V <sub>CTL2(L)</sub>		0.0	-	0.4	V
Control voltage 3(Low)	V <sub>CTL3(L)</sub>		0.0	-	0.4	V
Control voltage 4(Low)	V <sub>CTL4(L)</sub>		0.0	-	0.4	V
LNA operating current 1 (RX LNA mode)	I <sub>DD1</sub>	RF OFF, V <sub>CTL1</sub> =V <sub>CTL4</sub> =3.3V, V <sub>CTL2</sub> =V <sub>CTL3</sub> =0V	-	10	14	mA
LNA operating current 2 (RX Bypass mode)	I <sub>DD2</sub>	RF OFF, V <sub>CTL1</sub> =3.3V, V <sub>CTL2</sub> =V <sub>CTL3</sub> =V <sub>CTL4</sub> =0V	-	4	15	μA
LNA operating current 3 (Sleep mode)	I <sub>DD3</sub>	RF OFF, V <sub>CTL1</sub> =V <sub>CTL2</sub> =V <sub>CTL3</sub> =V <sub>CTL4</sub> =0.4V	-	4	15	μA
LNA operating current 4 (VCTL OPEN)	I <sub>DD4</sub>	RF OFF, V <sub>CTL1</sub> =V <sub>CTL2</sub> =V <sub>CTL3</sub> =V <sub>CTL4</sub> =open	-	4	15	μA
Control current 1	I <sub>CTL1</sub>	RF OFF, V <sub>CTL1</sub> =3.3V, V <sub>CTL2</sub> =V <sub>CTL3</sub> =V <sub>CTL4</sub> =0V	-	5	20	μA
Control current 2	I <sub>CTL2</sub>	RF OFF, V <sub>CTL2</sub> =3.3V, V <sub>CTL1</sub> =V <sub>CTL3</sub> =V <sub>CTL4</sub> =0V	-	5	20	μA
Control current 3	I <sub>CTL3</sub>	RF OFF, V <sub>CTL3</sub> =3.3V, V <sub>CTL1</sub> =V <sub>CTL2</sub> =V <sub>CTL4</sub> =0V	-	5	20	μA
Control current 4	I <sub>CTL4</sub>	RF OFF, V <sub>CTL4</sub> =3.3V, V <sub>CTL1</sub> =V <sub>CTL2</sub> =V <sub>CTL3</sub> =0V	-	5	20	μA

## ■ ELECTRICAL CHARACTERISTICS 2 (RF Characteristics: RX LNA mode, LNA+SP3T SW)

$V_{DD}=3.6V$ ,  $V_{CTL1}=V_{CTL4}=3.3V$ ,  $V_{CTL2}=V_{CTL3}=0V$ , freq=2400 to 2500MHz,  
 $Ta=+25^{\circ}C$ ,  $Zs=Zl=50\Omega$ , with application circuit

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small signal gain 1	Gain1	Exclude PCB and connector losses*1	13.0	15.0	17.0	dB
Gain flatness 1	Gflat1	f=2400 to 2420MHz, f=2440 to 2460MHz, f=2480 to 2500MHz	-	-	0.25	dB
Isolation 1	ISL1		-	28	-	dB
Noise figure 1	NF1	Exclude PCB and connector losses*2	-	1.6	1.9	dB
Input power at 1dB compression 1	$P_{-1dB(IN)}1$		-	-4	-	dBm
Input 3rd order Intercept point 1	IIP3_1	f1=freq, f2=freq+100kHz, $P_{IN}=-22dBm$	-	+7	-	dBm
ANT port return loss 1	RLi1		-	12	-	dB
LNAOUT port return loss 1	RLo1		-	10	-	dB
LNA switching time	Tsw1_1		-	100	400	ns
Other switching time	Tsw2_1		-	200	500	ns

\*1) 0.36dB (2400MHz), 0.36dB (2450MHz), 0.37dB (2500MHz)

\*2) 0.18dB (2400MHz), 0.18dB (2450MHz), 0.18dB (2500MHz)

## ■ ELECTRICAL CHARACTERISTICS 3 (RF Characteristics: RX Bypass mode, Bypass SW+SP3T SW)

$V_{DD}=3.6V$ ,  $V_{CTL1}=3.3V$ ,  $V_{CTL2}=V_{CTL3}=V_{CTL4}=0V$ , freq=2400 to 2500MHz,  
 $Ta=+25^{\circ}C$ ,  $Zs=Zl=50\Omega$ , with application circuit

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion loss 2	LOSS2	Exclude PCB and connector losses*3	4.0	6.0	8.0	dB
Input power at 1dB compression 2	$P_{-1dB(IN)}2$		-	+9	-	dBm
Input 3rd order Intercept point 2	IIP3_2	f1=freq, f2=freq+100kHz, $P_{IN}=-14dBm$	-	+13	-	dBm
ANT port return loss 2	RLi2		-	7	-	dB
LNAOUT port return loss 2	RLo2		-	7	-	dB

\*3) 0.36dB (2400MHz), 0.36dB (2450MHz), 0.37dB (2500MHz)

## ■ ELECTRICAL CHARACTERISTICS 4 (RF Characteristics: TX mode)

$V_{DD}=3.6V$ ,  $V_{CTL2}=3.3V$ ,  $V_{CTL1}=V_{CTL3}=V_{CTL4}=0V$ , freq=2400 to 2500MHz,  
 $Ta=+25^{\circ}C$ ,  $Zs=Zl=50\Omega$ , with application circuit

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion loss 3	LOSS3	$P_{IN}=+23dBm$ , Exclude PCB and connector losses*4	-	0.5	0.7	dB
Input power at 0.1dB compression 3	$P_{-0.1dB(IN)3}$		-	+30	-	dBm
ANT port return loss 3	RLi3		-	22	-	dB
TX port return loss 3	RLo3		-	22	-	dB

\*4) 0.34dB (2400MHz), 0.35dB (2450MHz), 0.36dB (2500MHz)

## ■ ELECTRICAL CHARACTERISTICS 5 (RF Characteristics: BT mode)

$V_{DD}=3.6V$ ,  $V_{CTL3}=3.3V$ ,  $V_{CTL1}=V_{CTL2}=V_{CTL4}=0V$ , freq=2400 to 2500MHz,  
 $Ta=+25^{\circ}C$ ,  $Zs=Zl=50\Omega$ , with application circuit

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion loss 4	LOSS4	$P_{IN}=+20dBm$ , Exclude PCB and connector losses*5	-	0.6	0.8	dB
Input power at 0.1dB compression 4	$P_{-0.1dB(IN)4}$		-	+26	-	dBm
ANT port return loss 4	RLi4		-	22	-	dB
BT port return loss 4	RLo4		-	22	-	dB

\*5) 0.70dB (2400MHz), 0.72dB (2450MHz), 0.73dB (2500MHz)

## ■ ELECTRICAL CHARACTERISTICS 6 (RF Characteristics)

$V_{DD}=3.6V$ ,  $V_{CTL1}=3.3V$ ,  $V_{CTL2}=V_{CTL3}=0V$ ,  $V_{CTL4}=3.3/0V$ , freq=2400 to 2500MHz,  
 $Ta=+25^{\circ}C$ ,  $Zs=Zl=50\Omega$ , with application circuit

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Gain dynamic range	GDR	Gain1+LOSS2	18.0	21.0	24.0	dB

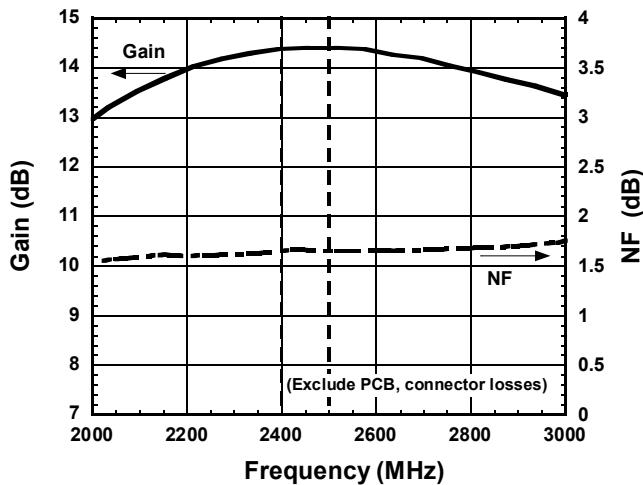
## ■ TERMINAL INFORMATION

Pin No.	SYMBOL	DESCRIPTION
1	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
2	TX	RF transmitting signal input terminal. DC blocking capacitor is required for this port.
3	VCTL2	Control signal input terminal. This terminal is set to High-Level (+2.8 to +5.0V) or Low-Level (0 to +0.4V).
4	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
5	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
6	LNAOUT	RF receiving signal output terminal. No DC blocking capacitor is required for this port because of internal output matching circuit including DC blocking capacitor.
7	VCTL4	Control signal input terminal. This terminal is set to High-Level (+2.8 to +5.0V) or Low-Level (0 to +0.4V).
8	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
9	VDD	Positive voltage supply terminal. The positive voltage (+3.0 to +5.0V) has to be supplied. Please connect a bypass capacitor with GND terminal for excellent RF performance.
10	BT	Bluetooth terminal. No DC blocking capacitor is required for this port because of internal capacitor.
11	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
12	VCTL3	Control signal input terminal. This terminal is set to High-Level (+2.8 to +5.0V) or Low-Level (0 to +0.4V).
13	VCTL1	Control signal input terminal. This terminal is set to High-Level (+2.8 to +5.0V) or Low-Level (0 to +0.4V).
14	ANT	RF transmitting/receiving terminal. No DC blocking capacitor is required for this port because of internal capacitor.
Exposed Pad	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance, and through holes for GND should be placed near by the pin connection

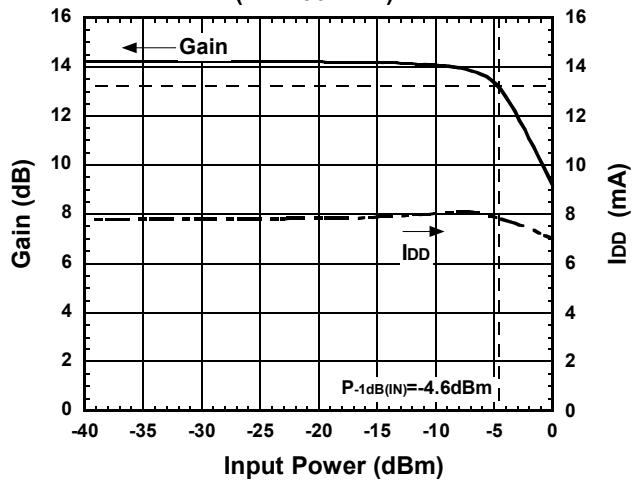
## ■ ELECTRICAL CHARACTERISTICS (RX LNA mode)

$V_{DD}=3.6V$ ,  $V_{CTL1}=V_{CTL4}=3.3V$ ,  $V_{CTL2}=V_{CTL3}=0V$ ,  $T_a=25^{\circ}C$ ,  $Z_s=Z_l=50\Omega$

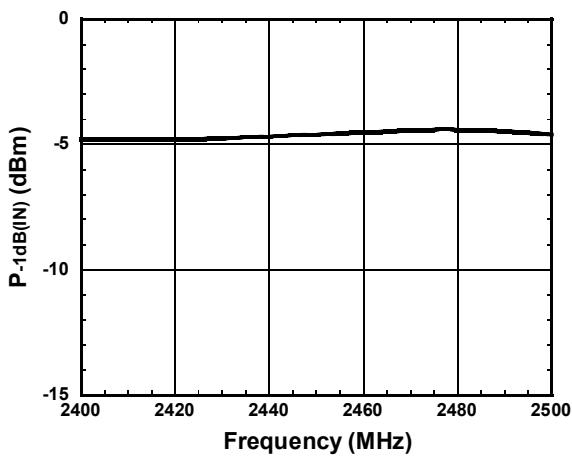
**Gain, NF vs. Frequency**



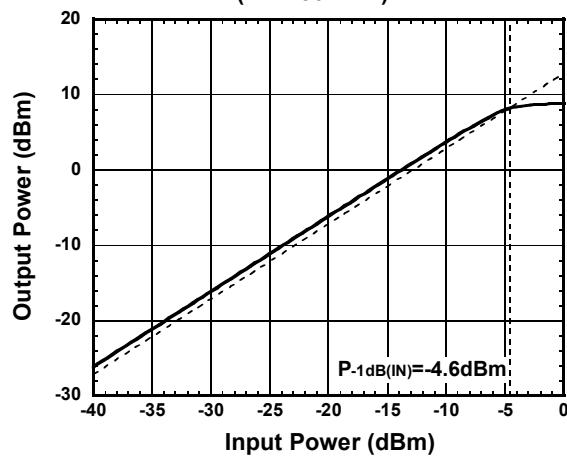
**Gain, I<sub>DD</sub> vs. P<sub>IN</sub>**  
(f=2450MHz)



**P-1dB(IN) vs. Frequency**

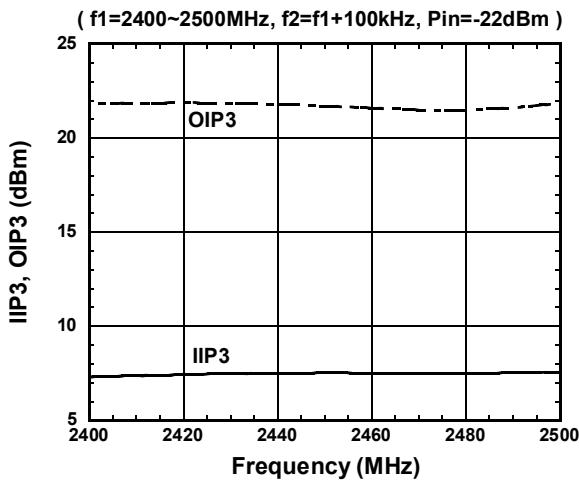


**P<sub>OUT</sub> vs. P<sub>IN</sub>**  
(f=2450MHz)



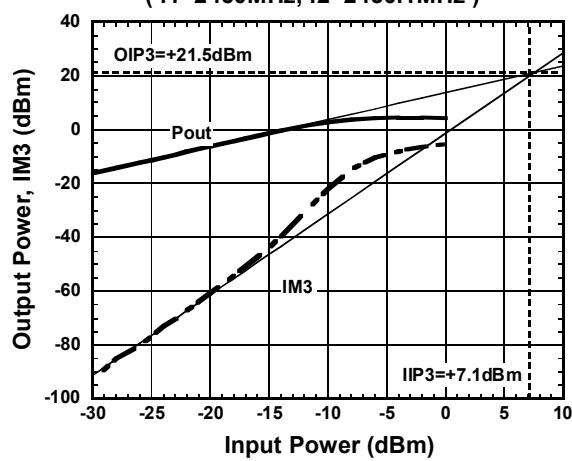
**IIP3, OIP3 vs. Frequency**

(f1=2400~2500MHz, f2=f1+100kHz, Pin=-22dBm)



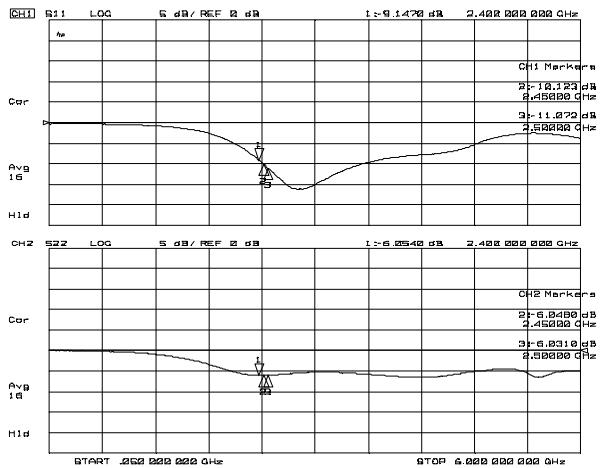
**P<sub>OUT</sub>, IM3 vs. P<sub>IN</sub>**

(f1=2450MHz, f2=2450.1MHz)

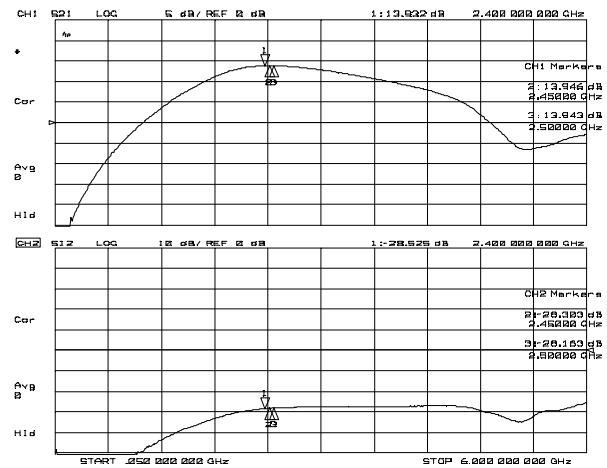


## ■ ELECTRICAL CHARACTERISTICS (RX LNA mode)

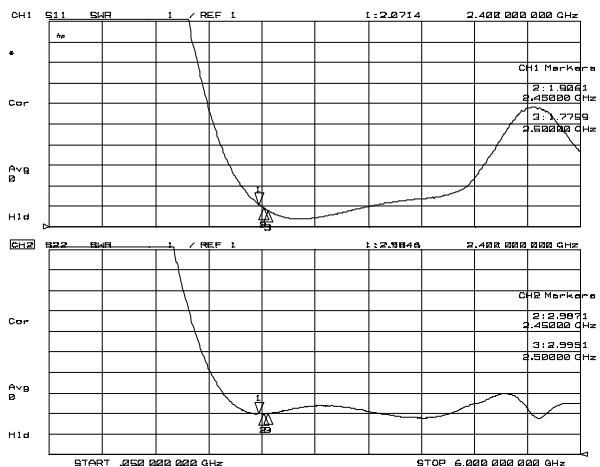
$V_{DD}=3.6V$ ,  $V_{CTL1}=V_{CTL4}=3.3V$ ,  $V_{CTL2}=V_{CTL3}=0V$ ,  $T_a=25^\circ C$ ,  $Z_s=Z_l=50\Omega$



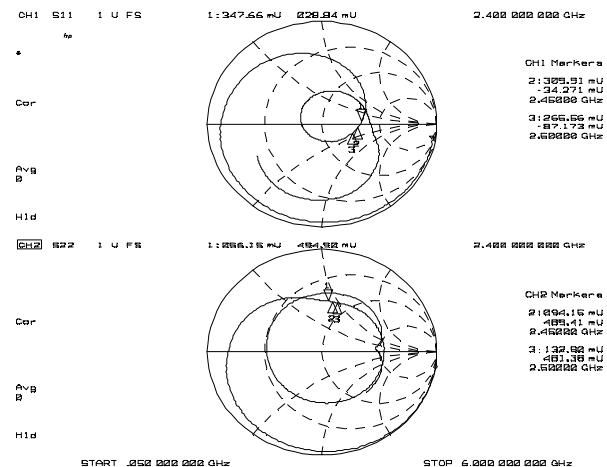
S11, S22 (f=50MHz to 6GHz)



S21, S12 (f=50MHz to 6GHz)



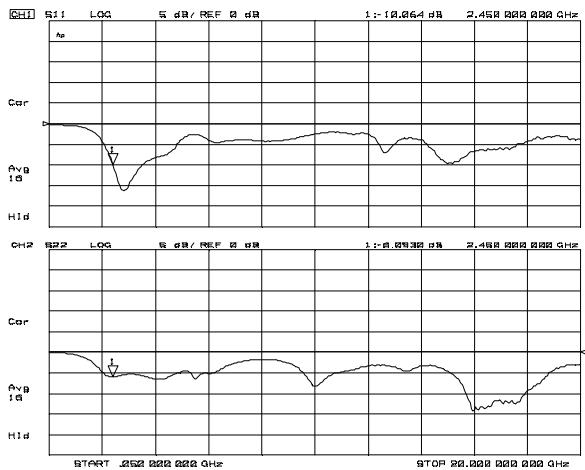
VSWRi, VSWRo (f=50MHz to 6GHz)



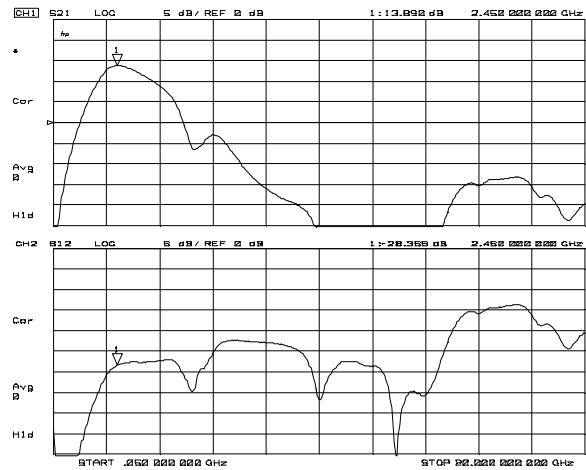
Zin, Zout (f=50MHz to 6GHz)

## ■ ELECTRICAL CHARACTERISTICS (RX LNA mode)

$V_{DD}=3.6V$ ,  $V_{CTL1}=V_{CTL4}=3.3V$ ,  $V_{CTL2}=V_{CTL3}=0V$ ,  $T_a=25^{\circ}C$ ,  $Z_s=Z_l=50\Omega$



S11, S22 (f=50MHz to 20GHz)

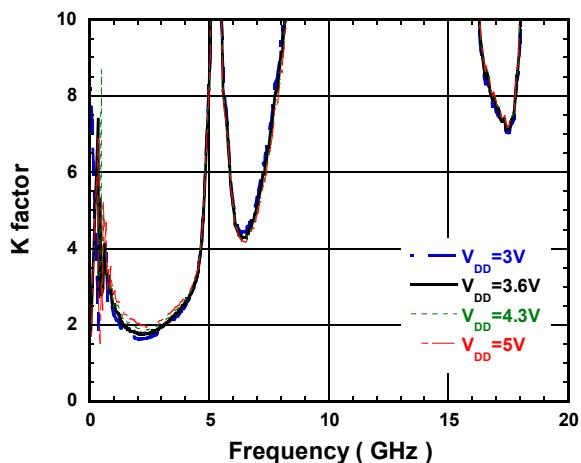


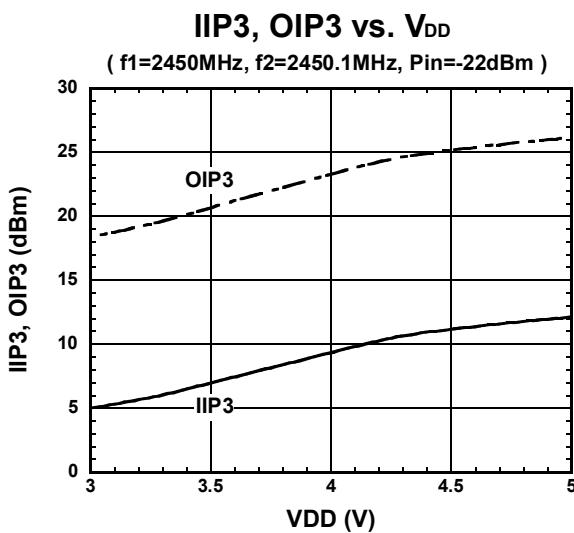
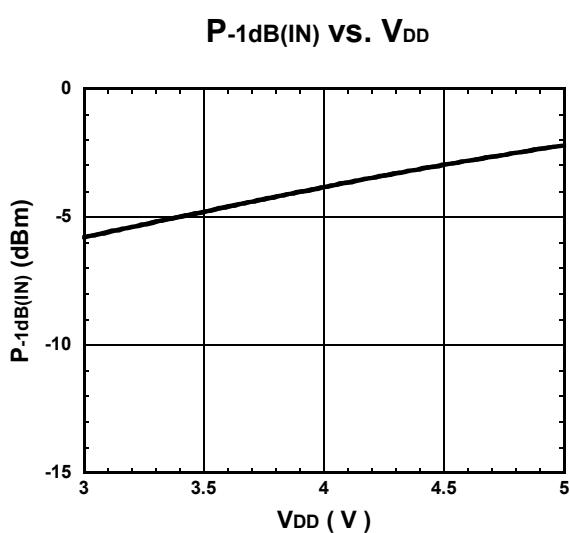
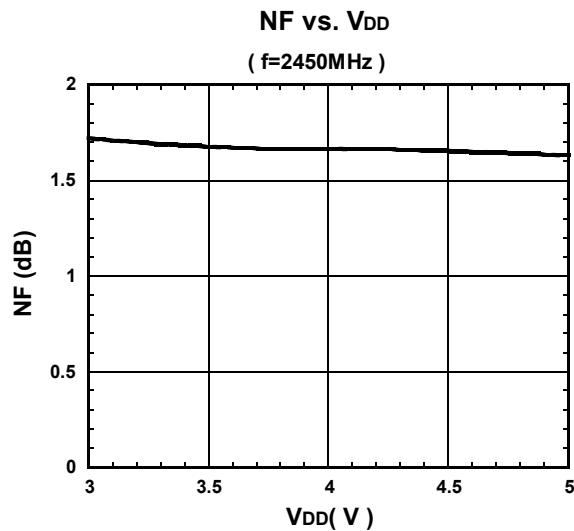
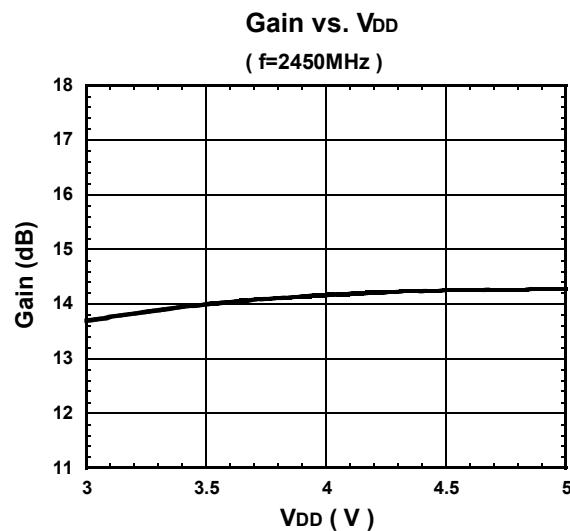
S21, S12 (f=50MHz to 20GHz)

## ■ ELECTRICAL CHARACTERISTICS (RX LNA mode)

$V_{CTL1}=V_{CTL4}=3.3V$ ,  $V_{CTL2}=V_{CTL3}=0V$ ,  $T_a=25^{\circ}C$ ,  $Z_s=Z_l=50\Omega$

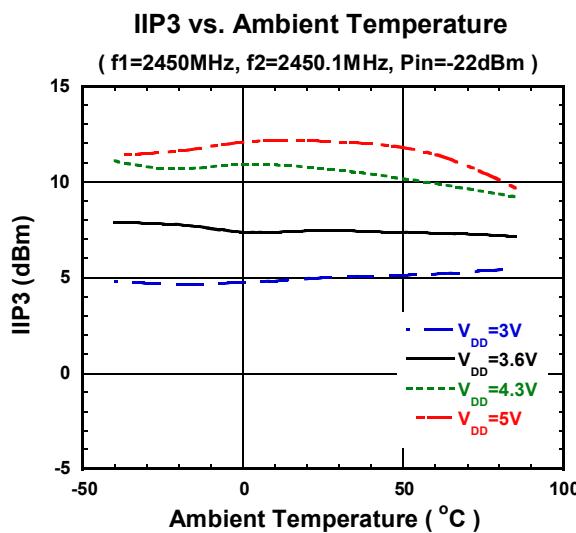
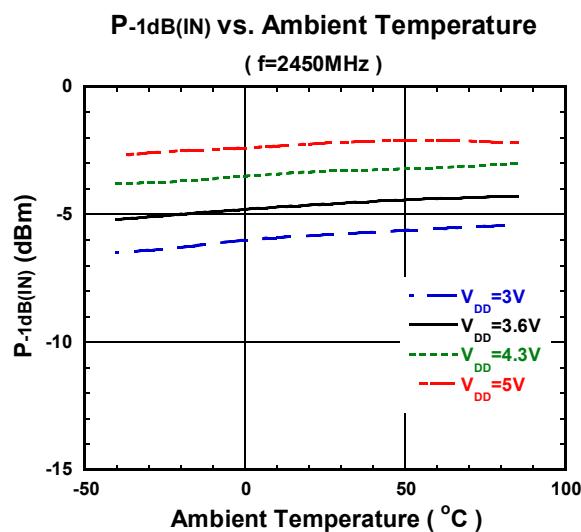
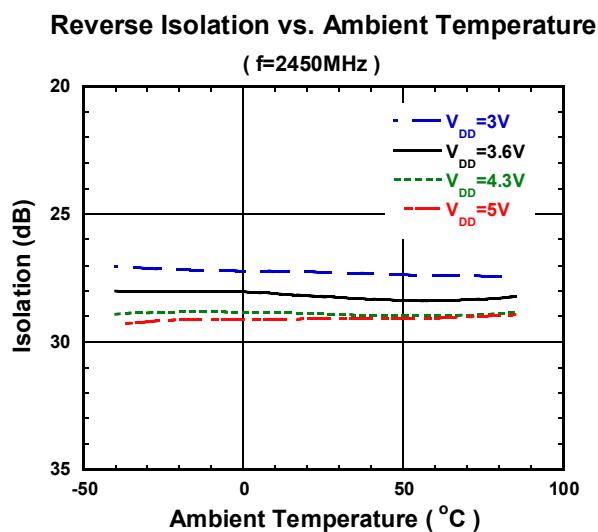
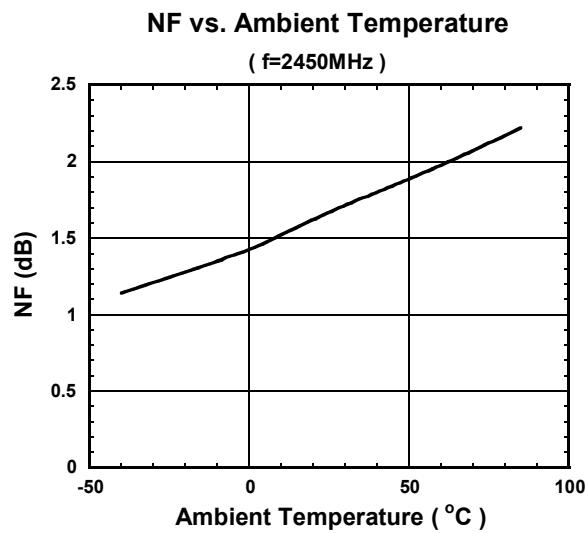
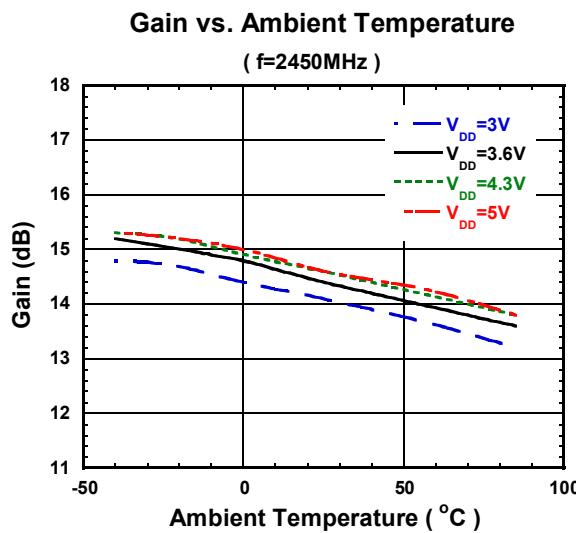
### K factor vs. Frequency



**■ ELECTRICAL CHARACTERISTICS (RX LNA mode)** $V_{CTL1}=V_{CTL4}=3.3V$ ,  $V_{CTL2}=V_{CTL3}=0V$ ,  $T_a=25^{\circ}C$ ,  $Z_s=Z_l=50\Omega$ 

## ■ ELECTRICAL CHARACTERISTICS (RX LNA mode)

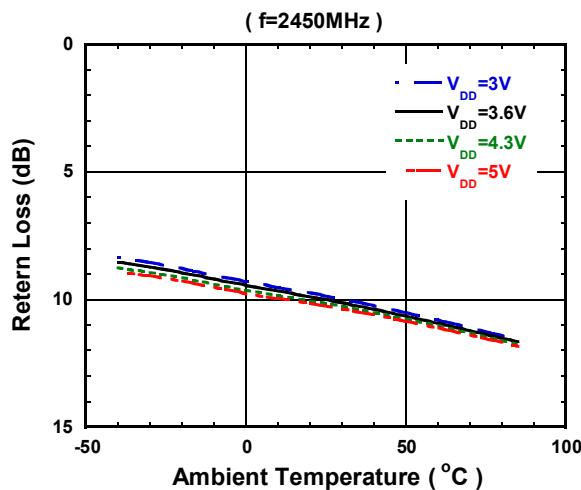
$V_{CTL1}=V_{CTL4}=3.3V$ ,  $V_{CTL2}=V_{CTL3}=0V$ ,  $Z_S=Z_L=50\Omega$



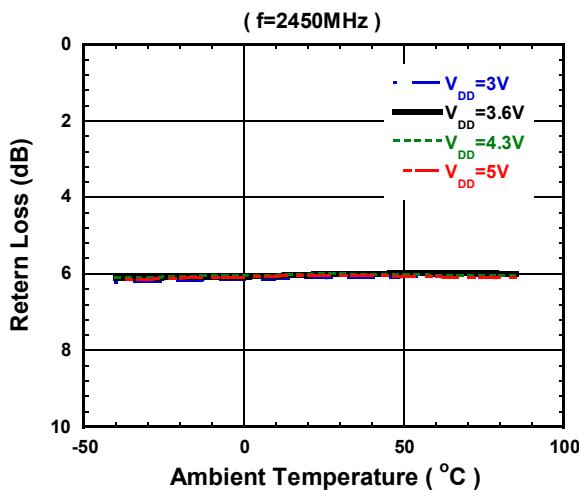
## ■ ELECTRICAL CHARACTERISTICS (RX LNA mode)

$V_{CTL1}=V_{CTL4}=3.3V$ ,  $V_{CTL2}=V_{CTL3}=0V$ ,  $Z_s=Z_l=50\Omega$

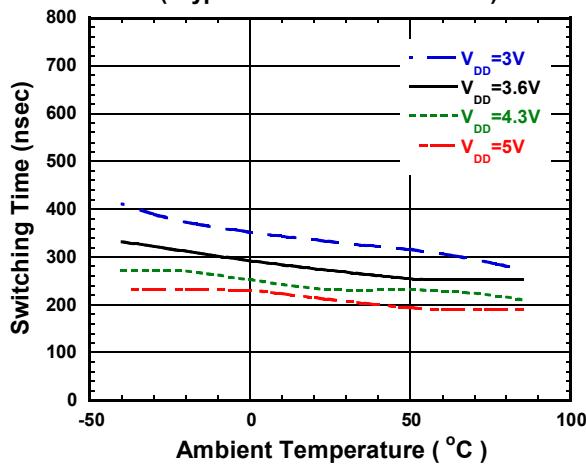
### ANT Port Return Loss vs. Ambient Temperature



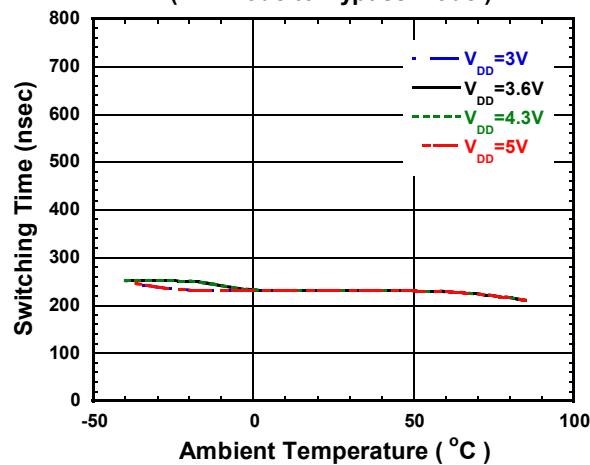
### LNAOUT Port Return Loss vs. Ambient Temperature



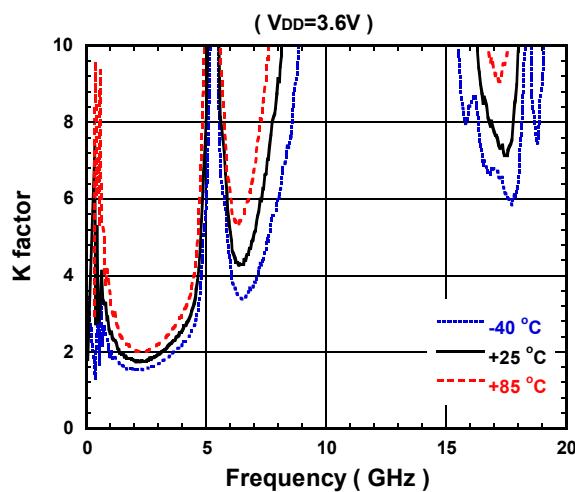
### Switching Time vs. Ambient Temperature (Bypass Mode to LNA Mode)



### Switching Time vs. Ambient Temperature (TX mode to Bypass Mode)



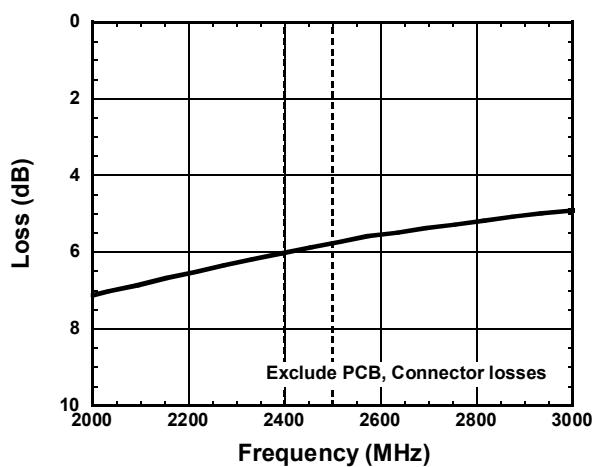
### K factor vs. Frequency



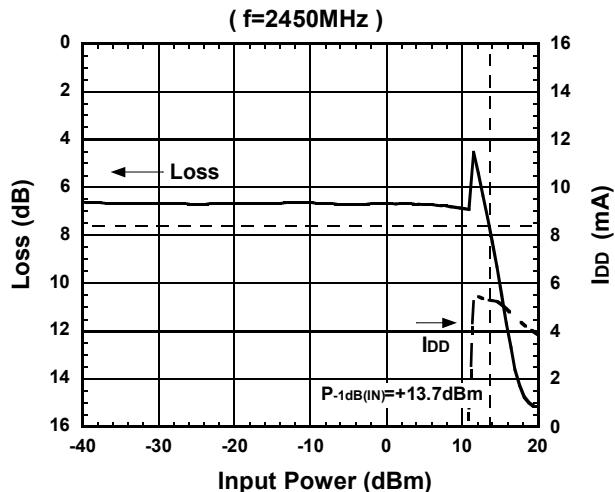
## ■ ELECTRICAL CHARACTERISTICS (RX Bypass mode)

$V_{DD}=3.6V$ ,  $V_{CTL1}=3.3V$ ,  $V_{CTL2}=V_{CTL3}=V_{CTL4}=0V$ ,  $T_a=25^{\circ}C$ ,  $Z_s=Z_l=50\Omega$

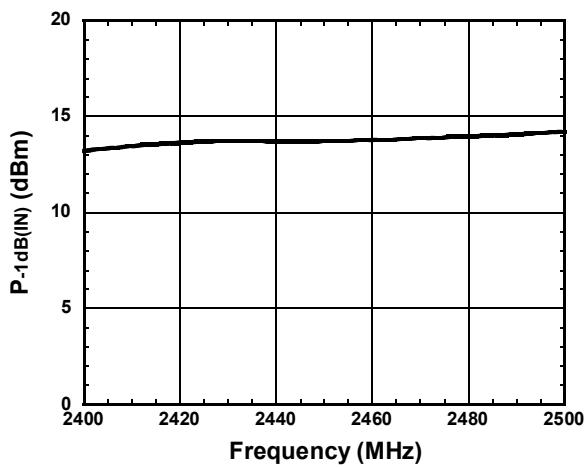
### Loss vs. Frequency



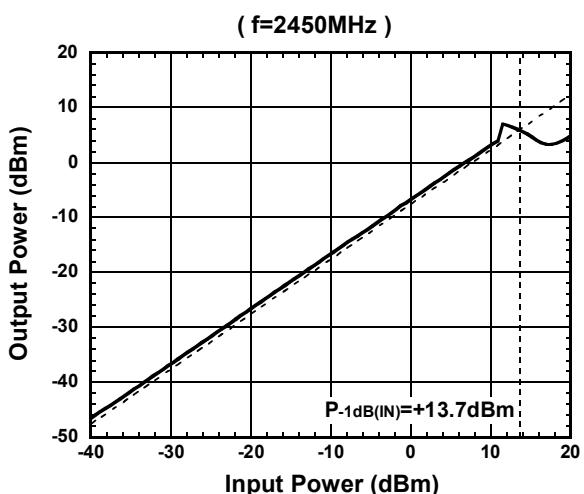
### Loss, IDD vs. PIN



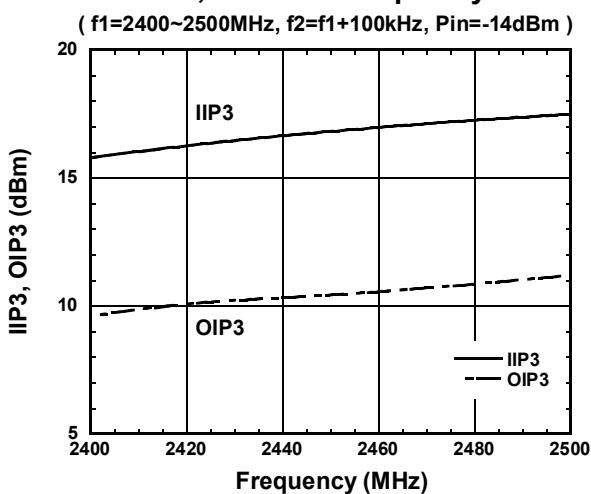
### $P_{-1dB(IN)}$ vs. Frequency



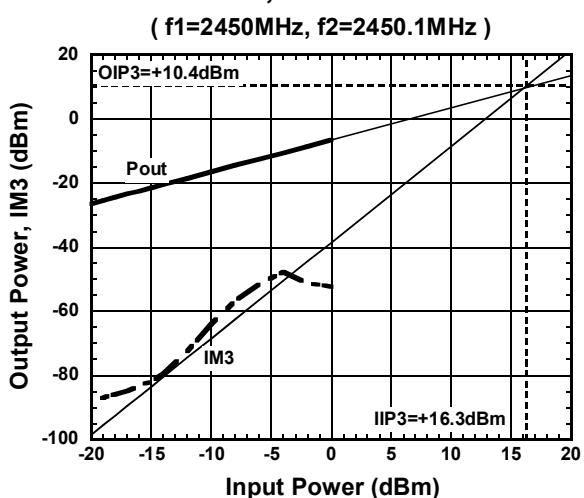
### $P_{OUT}$ vs. PIN



### IIP3, OIP3 vs. Frequency

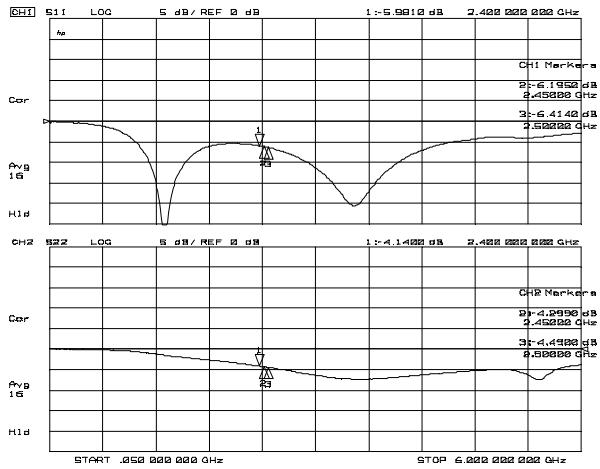


### $P_{OUT}$ , IM3 vs. PIN

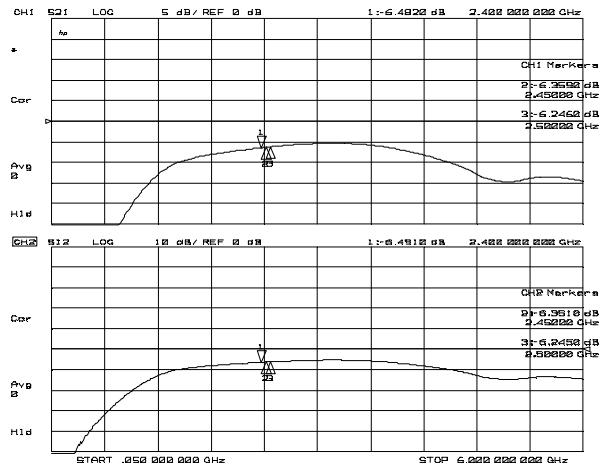


## ■ ELECTRICAL CHARACTERISTICS (RX Bypass mode)

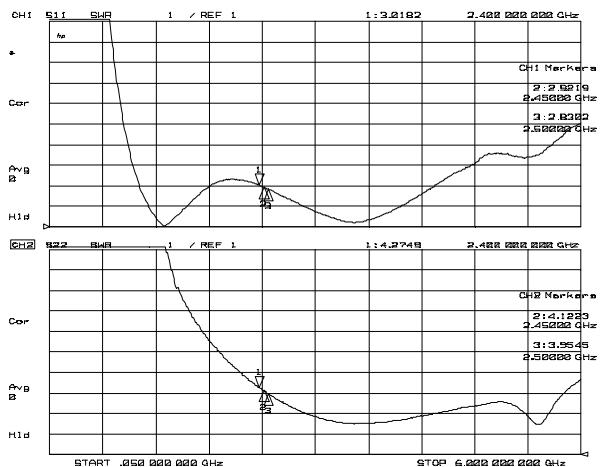
$V_{DD}=3.6V$ ,  $V_{CTL1}=3.3V$ ,  $V_{CTL2}=V_{CTL3}=V_{CTL4}=0V$ ,  $T_a=25^\circ C$ ,  $Z_s=Z_l=50\Omega$



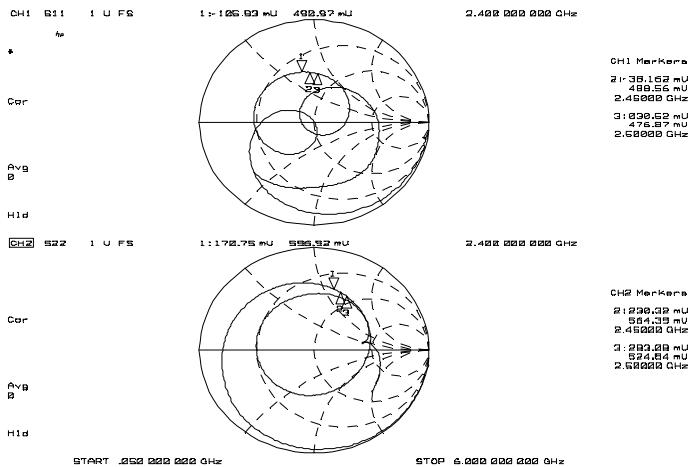
S11, S22 ( $f=50MHz$  to  $6GHz$ )



S21, S12 ( $f=50MHz$  to  $6GHz$ )



VSWRi, VSWRo ( $f=50MHz$  to  $6GHz$ )

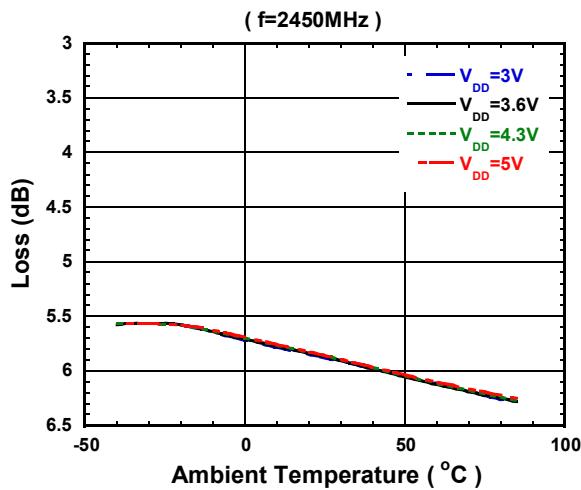


Zin, Zout ( $f=50MHz$  to  $6GHz$ )

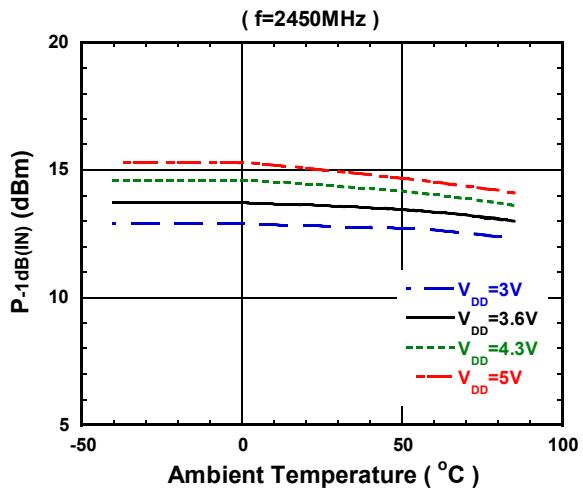
■ ELECTRICAL CHARACTERISTICS (RX Bypass mode)

$V_{CTL1}=3.3V$ ,  $V_{CTL2}=V_{CTL3}=V_{CTL4}=0V$ ,  $Z_S=Z_L=50\Omega$

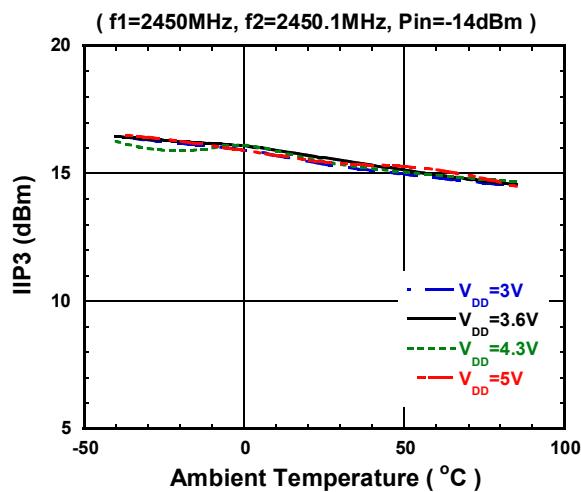
**Loss vs. Ambient Temperature**



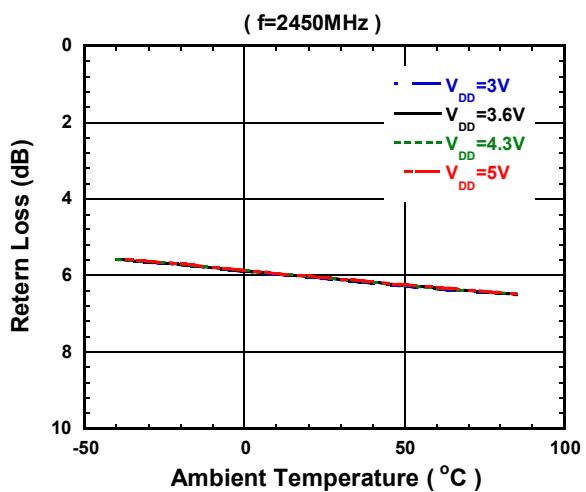
**P-1dB(IN) vs. Ambient Temperature**



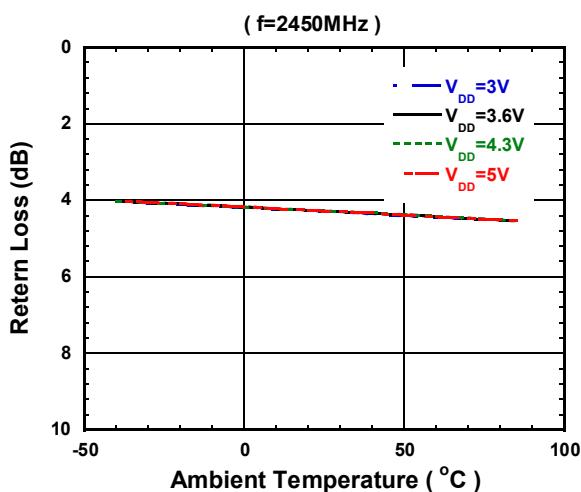
**IIP3 vs. Ambient Temperature**



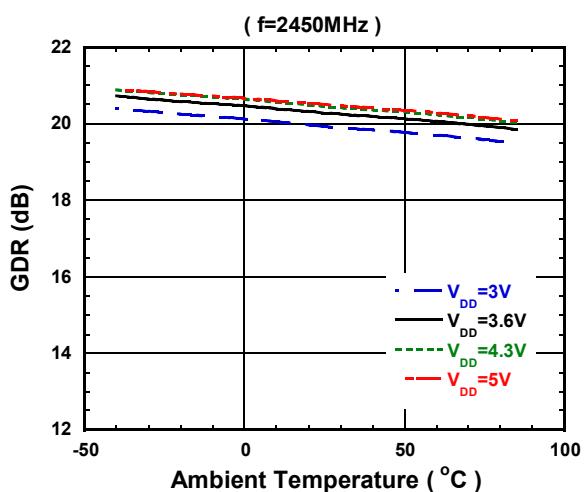
**ANT Port Return Loss vs. Ambient Temperature**



**LNAOUT Port Return Loss vs. Ambient Temperature**



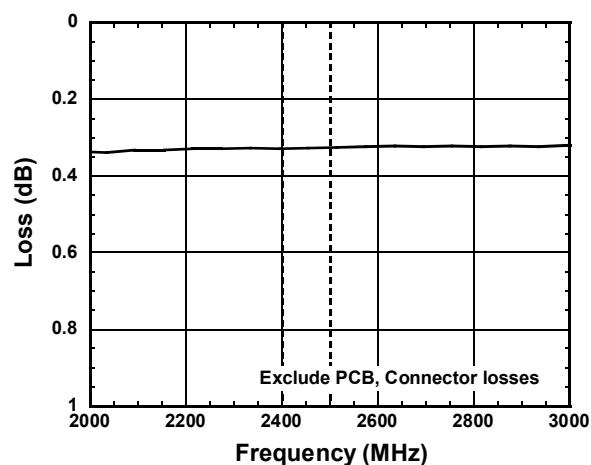
**GDR vs. Ambient Temperature**



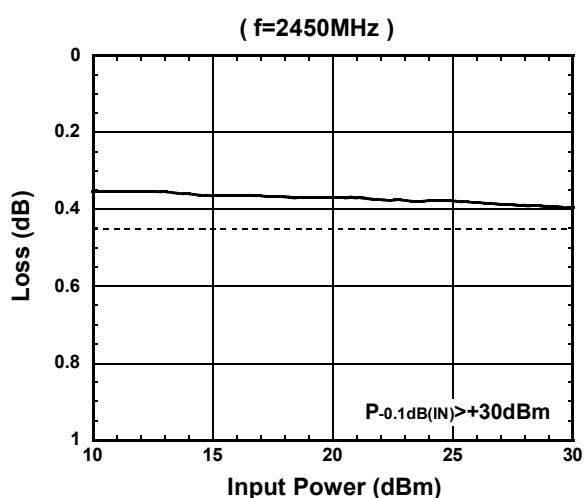
## ■ ELECTRICAL CHARACTERISTICS (TX mode)

$V_{DD}=3.6V$ ,  $V_{CTL2}=3.3V$ ,  $V_{CTL1}=V_{CTL3}=V_{CTL4}=0V$ ,  $T_a=25^{\circ}C$ ,  $Z_s=Z_l=50\Omega$

**Loss vs. Frequency**

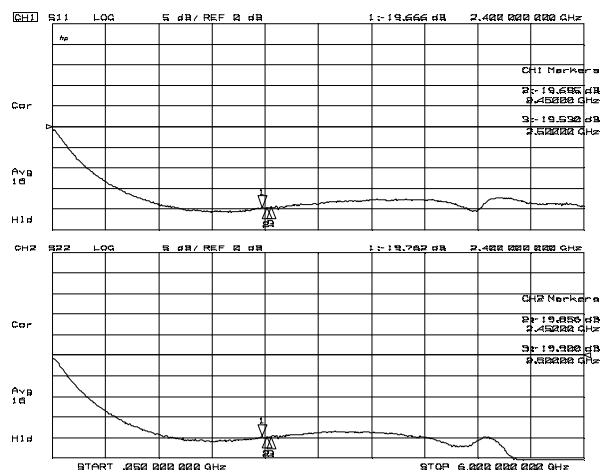


**Loss vs. PIN**

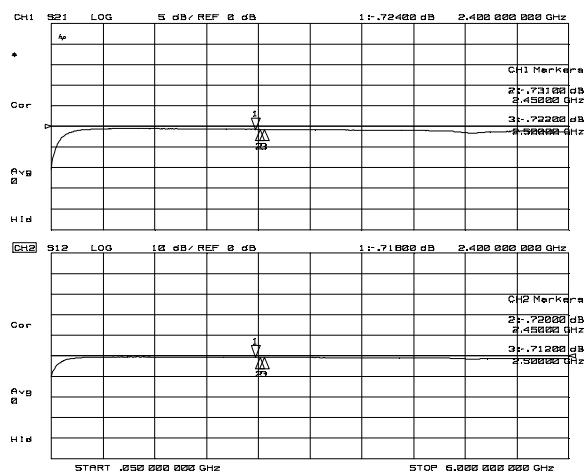


## ■ ELECTRICAL CHARACTERISTICS (TX mode)

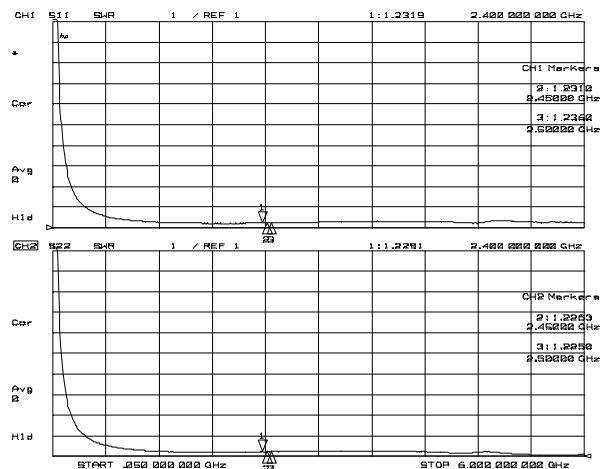
$V_{DD}=3.6V$ ,  $V_{CTL2}=3.3V$ ,  $V_{CTL1}=V_{CTL3}=V_{CTL4}=0V$ ,  $T_a=25^\circ C$ ,  $Z_s=Z_l=50\Omega$



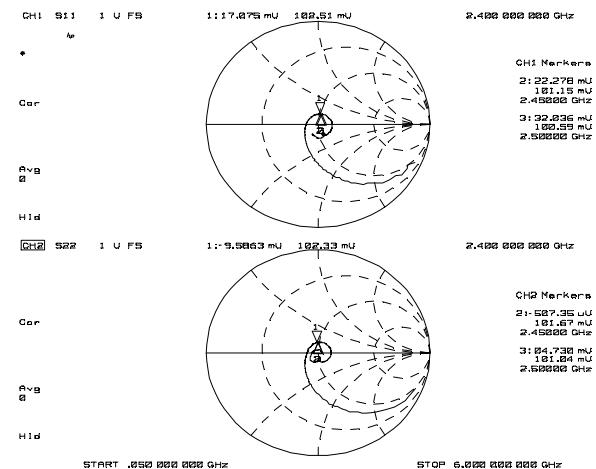
S11, S22 ( $f=50\text{MHz}$  to  $6\text{GHz}$ )



S21, S12 ( $f=50\text{MHz}$  to  $6\text{GHz}$ )



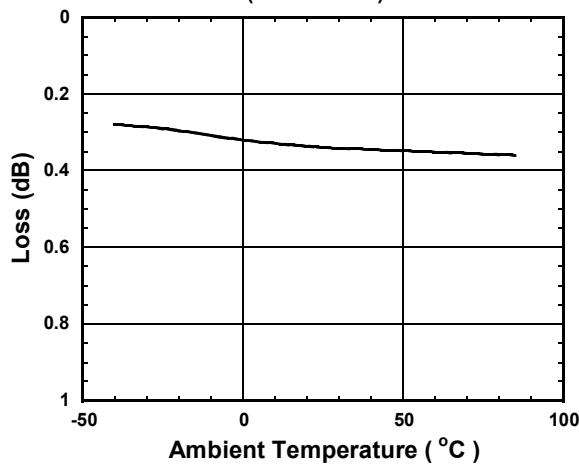
VSWRi, VSWRo ( $f=50\text{MHz}$  to  $6\text{GHz}$ )



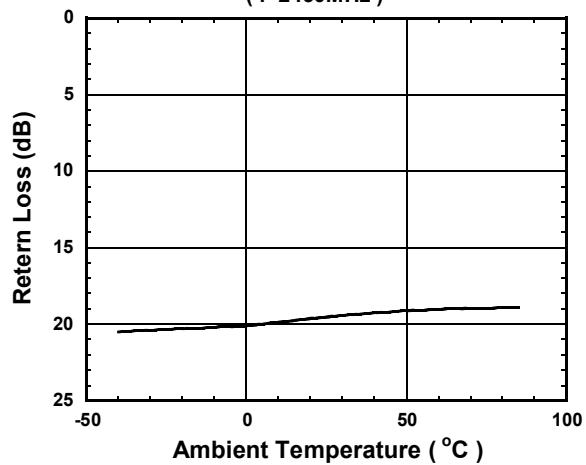
Zin, Zout ( $f=50\text{MHz}$  to  $6\text{GHz}$ )

**■ ELECTRICAL CHARACTERISTICS (TX mode)** $V_{DD}=3.6V$ ,  $V_{CTL2}=3.3V$ ,  $V_{CTL1}=V_{CTL3}=V_{CTL4}=0V$ ,  $Z_s=Z_l=50\Omega$ **Loss vs. Ambient Temperature**

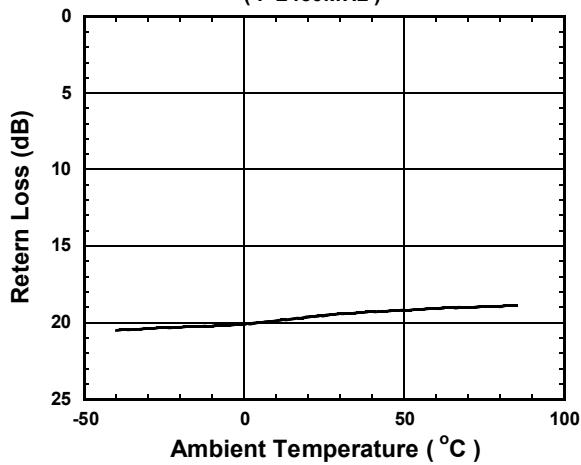
( f=2450MHz )

**ANT Port Return Loss vs. Ambient Temperature**

( f=2450MHz )

**TX Port Return Loss vs. Ambient Temperature**

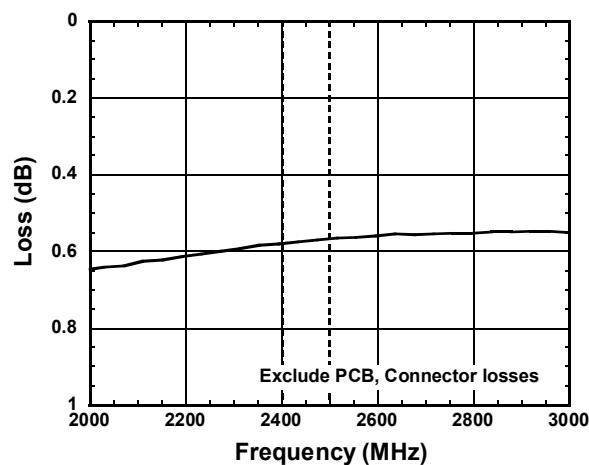
( f=2450MHz )



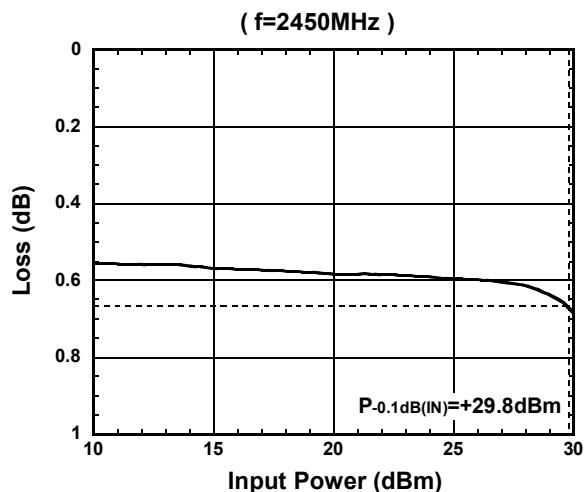
## ■ ELECTRICAL CHARACTERISTICS (BT mode)

$V_{DD}=3.6V$ ,  $V_{CTL3}=3.3V$ ,  $V_{CTL1}=V_{CTL2}=V_{CTL4}=0V$ ,  $T_a=25^{\circ}C$ ,  $Z_s=Z_l=50\Omega$

**Loss vs. Frequency**

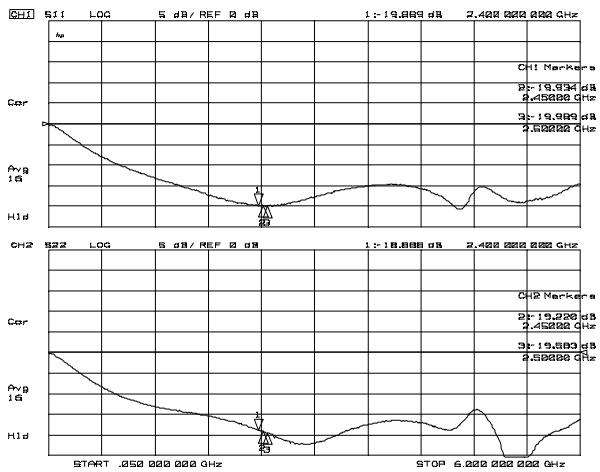


**Loss vs. PIN**

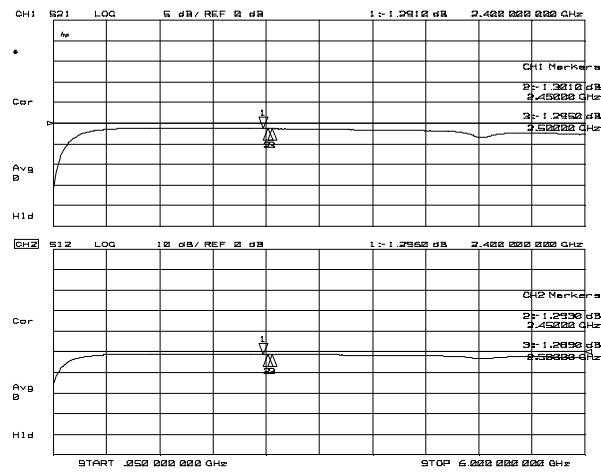


## ■ ELECTRICAL CHARACTERISTICS (BT mode)

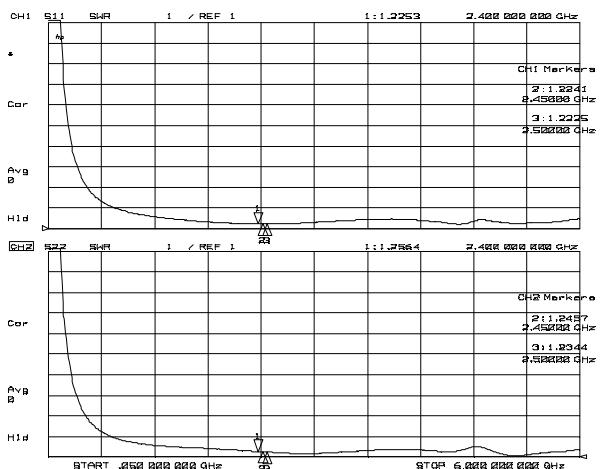
$V_{DD}=3.6V$ ,  $V_{CTL3}=3.3V$ ,  $V_{CTL1}=V_{CTL2}=V_{CTL4}=0V$ ,  $T_a=25^\circ C$ ,  $Z_s=Z_l=50\Omega$



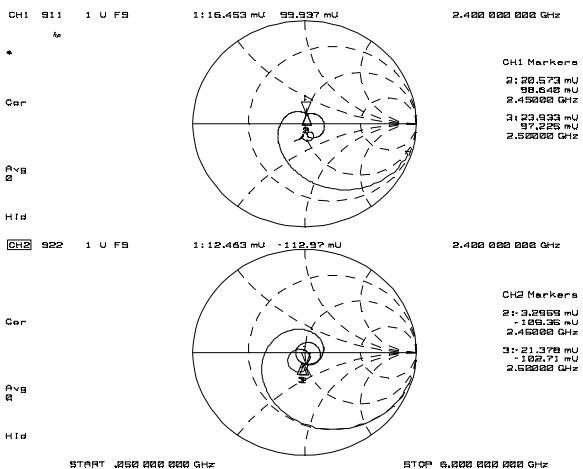
S11, S22 (f=50MHz to 6GHz)



S21, S12 (f=50MHz to 6GHz)



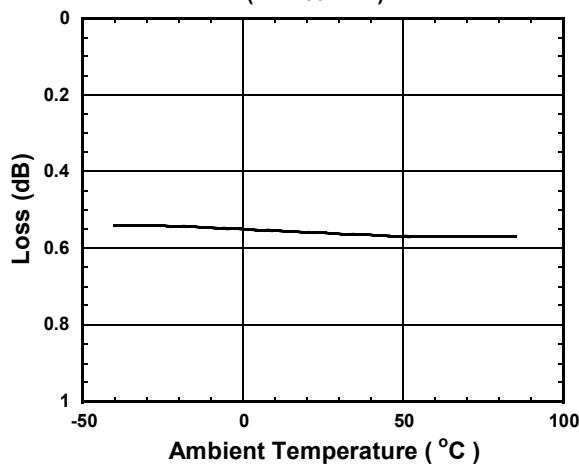
VSWRi, VSWRo (f=50MHz to 6GHz)



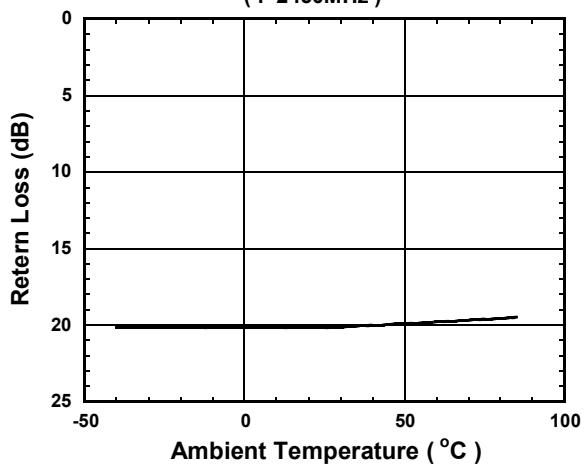
Zin, Zout (f=50MHz to 6GHz)

**■ ELECTRICAL CHARACTERISTICS (BT mode)** $V_{DD}=3.6V$ ,  $V_{CTL3}=3.3V$ ,  $V_{CTL1}=V_{CTL2}=V_{CTL4}=0V$ ,  $Z_s=Z_l=50\Omega$ **Loss vs. Ambient Temperature**

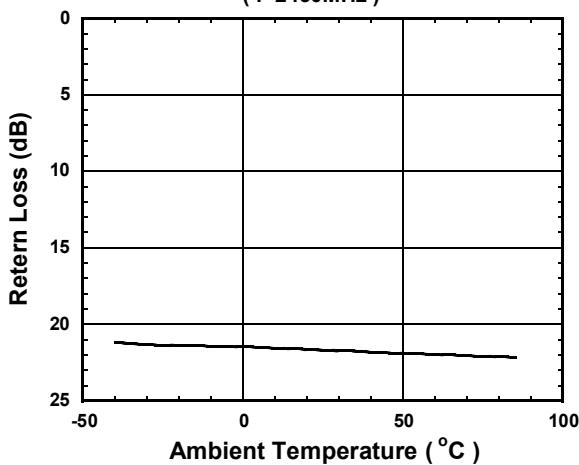
( f=2450MHz )

**ANT Port Return Loss vs. Ambient Temperature**

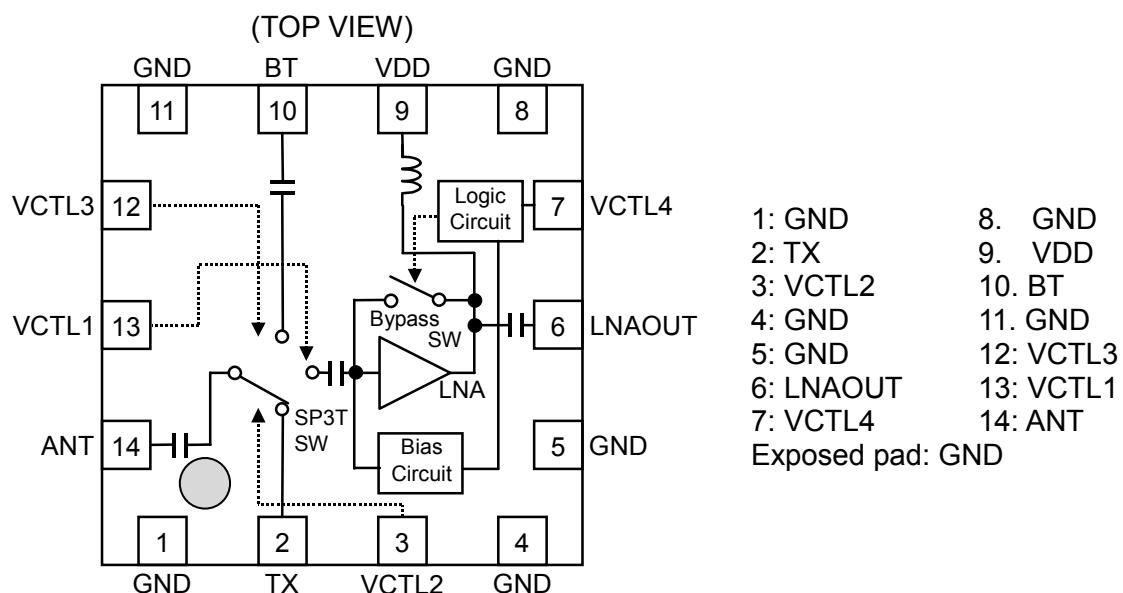
( f=2450MHz )

**BT Port Return Loss vs. Ambient Temperature**

( f=2450MHz )



## ■ PIN CONFIGURATION

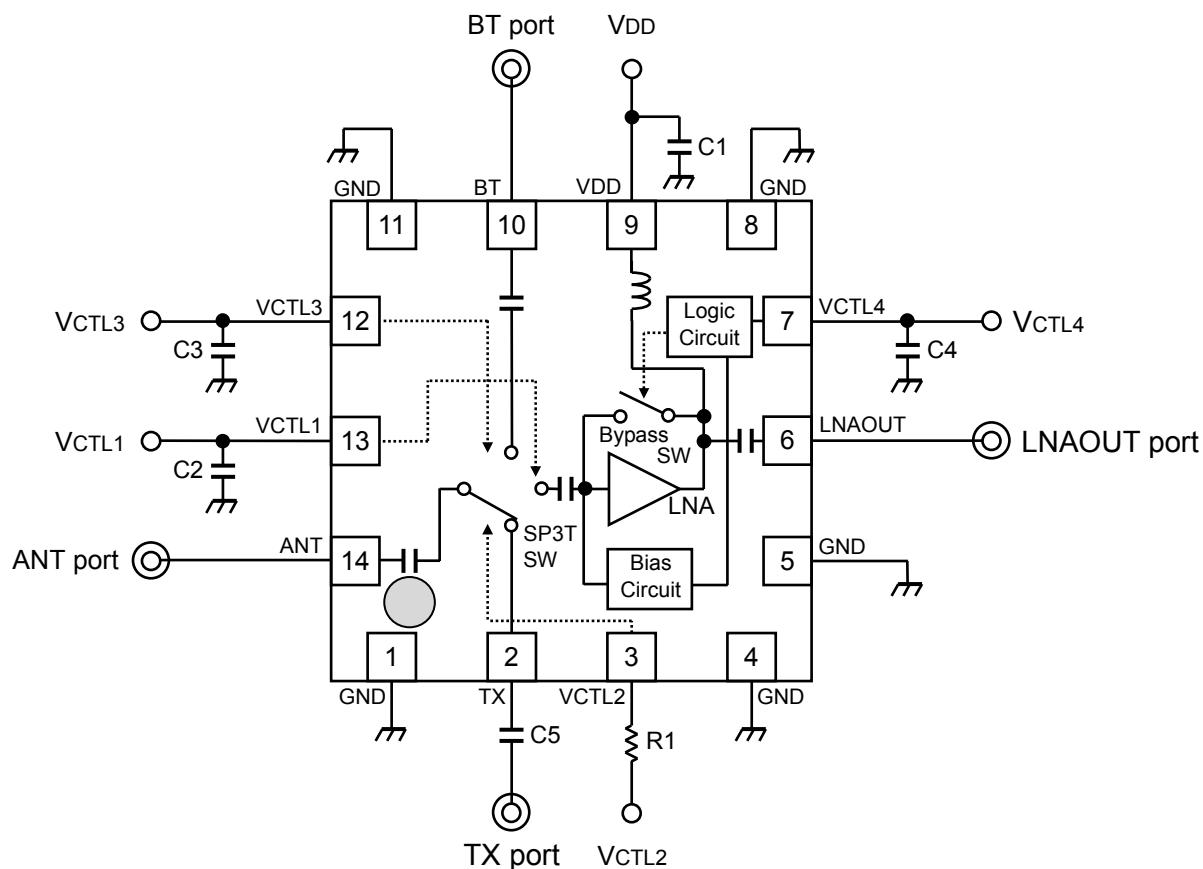


## ■ TRUTH TABLE

"H" =  $V_{CTL}(H)$ , "L" =  $V_{CTL}(L)$

mode	VCTL1 (SW RX)	VCTL2 (SW TX)	VCTL3 (SW BT)	VCTL4 (LNA)	STATE					
					IDD	LNA	Bypass	RX SW	TX SW	BT SW
RX LNA	H	L	L	H	$I_{DD1}$	ON	OFF	ON	OFF	OFF
RX Bypass	H	L	L	L	$I_{DD2}$	OFF	ON	ON	OFF	OFF
TX	L	H	L	L	$I_{DD2}$	OFF	ON	OFF	ON	OFF
BT	L	L	H	L	$I_{DD2}$	OFF	ON	OFF	OFF	ON
Sleep	L	L	L	L	$I_{DD3}$	OFF	OFF	OFF	OFF	OFF

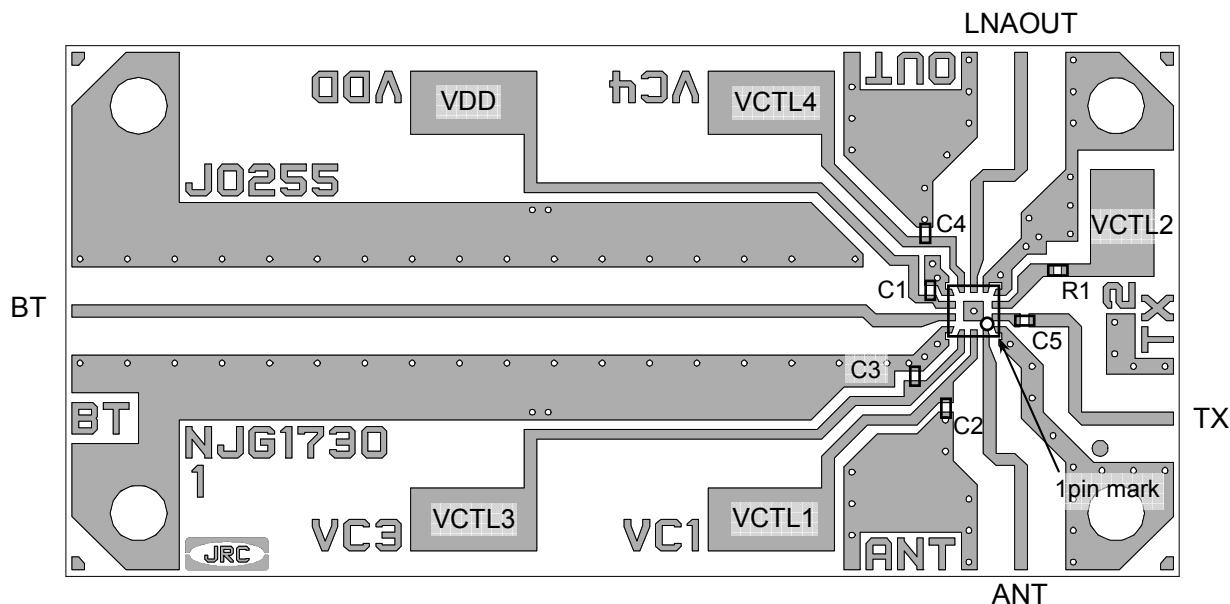
## ■ APPLICATION CIRCUIT



## ■ PARTS LIST

ID No.	Value	Notes
C1	1000pF	
C2 to C4	10pF	MURATA (GRM03 series)
C5	56pF	
R1	10kΩ	KOA (RK73B series)

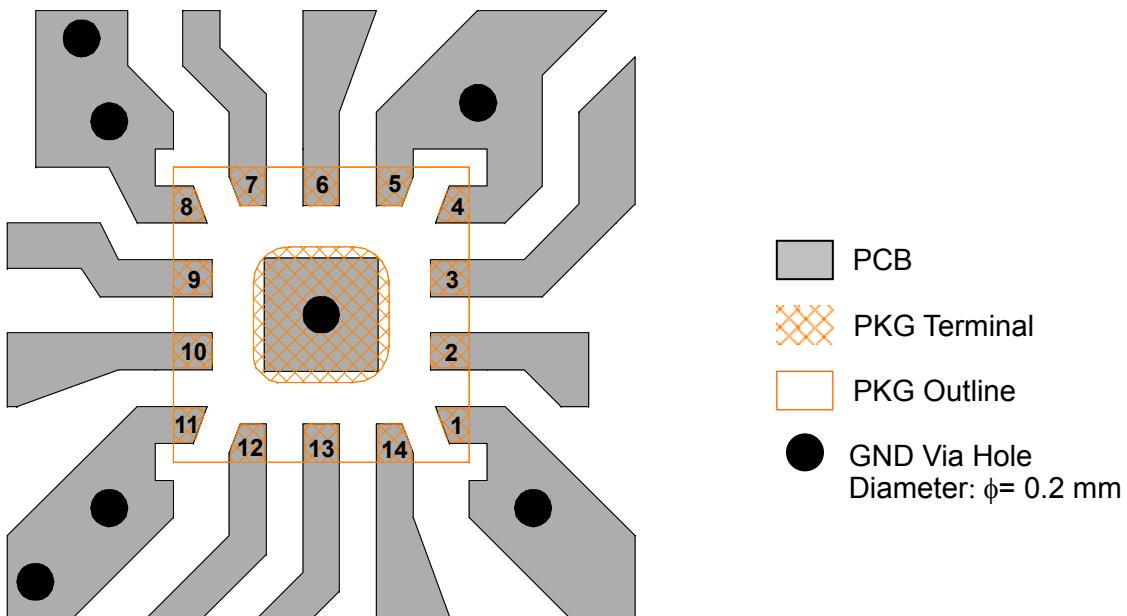
## ■ APPLIED CIRCUIT BOARD EXAMPLE



### PCB Information

Substrate: FR-4  
 Thickness: 0.2mm  
 Microstrip line width: 0.4mm ( $Z_0=50\Omega$ )  
 PCB size: 35.2mm x 16.8mm

### <PCB LAYOUT GUIDELINE>



### PRECAUTIONS

- [1] All external parts should be placed as close as possible to the IC.
- [2] For avoiding the degradation of RF performance, the bypass capacitor (C1) should be placed as close as possible to VDD terminal.
- [3] For good RF performance, the ground terminals must be placed possibly close to ground plane of substrate, and through holes for GND should be placed near by the pin connection.

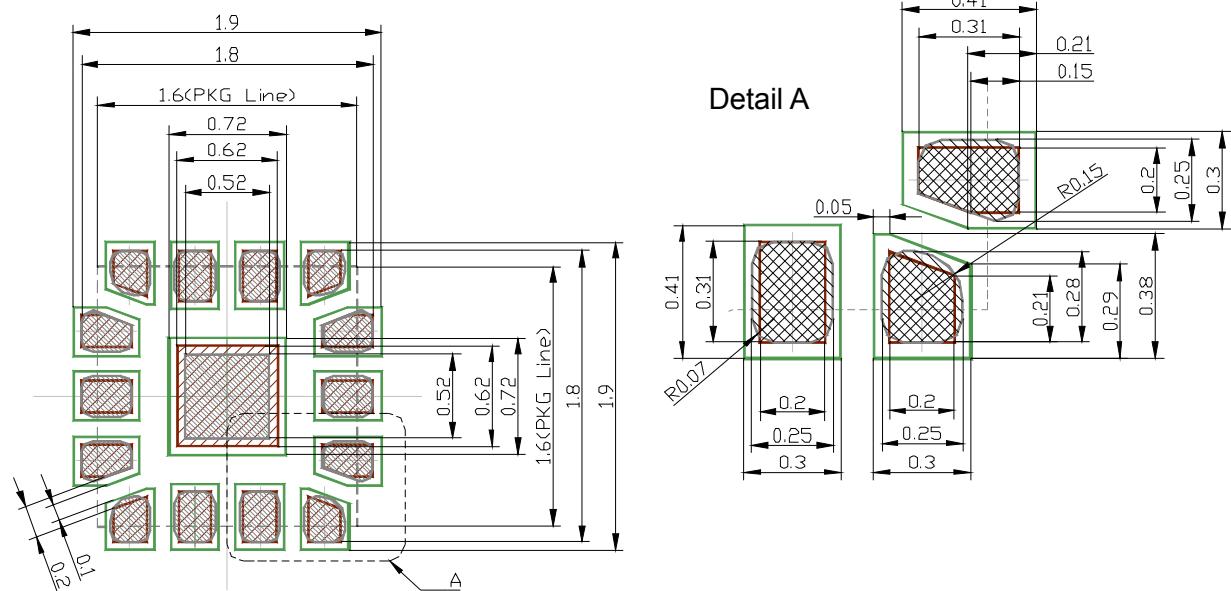
## ■ RECOMMENDED FOOTPRINT PATTERN (EQFN14-D7 Package Reference)

: Land

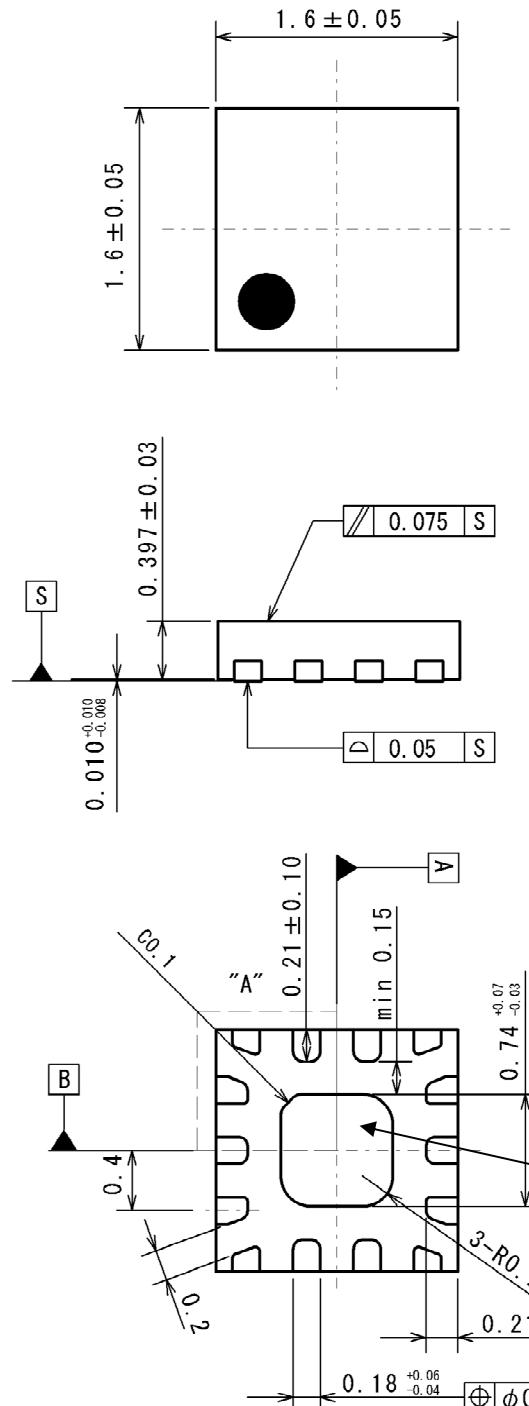
: Mask (Open area) \*Metal mask thickness: 100μm

: Resist (Open area)

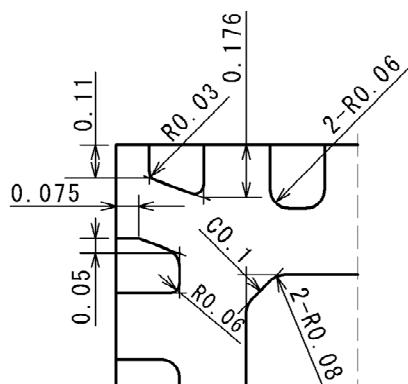
Package: 1.6mm x 1.6mm  
Pin pitch: 0.4mm



## ■ PACKAGE OUTLINE (EQFN14-D7)



Mold material: Epoxy resin  
 Substrate material: Cu  
 Terminal treatment: Sn-Bi Plating  
 Units: mm  
 Weight: 3.4mg

Details of "A" part ( $\times 2$ )

Exposed PAD:  
 Ground connection is required.

**Cautions on using this product**

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.

**[CAUTION]**

The specifications on this databook are only given for information , without any guarantee as regards either mistakes or omissions.

The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.

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