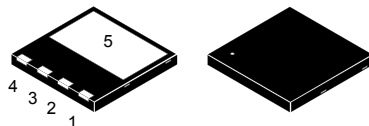
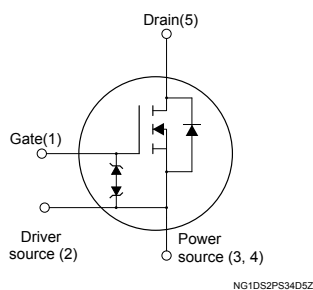


## N-channel 600 V, 70 mΩ typ., 31 A MDmesh™ M6 Power MOSFET in a PowerFLAT™ 8x8 HV package



PowerFLAT™ 8x8 HV



### Product status link

[STL47N60M6](#)

### Product summary

|            |                   |
|------------|-------------------|
| Order code | STL47N60M6        |
| Marking    | 47N60M6           |
| Package    | PowerFLAT™ 8x8 HV |
| Packing    | Tape and reel     |

## Features

| Order code | V <sub>DS</sub> | R <sub>DS(on)</sub> max. | I <sub>D</sub> |
|------------|-----------------|--------------------------|----------------|
| STL47N60M6 | 600 V           | 82 mΩ                    | 31 A           |

- Reduced switching losses
- Lower R<sub>DS(on)</sub> x area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected
- Excellent switching performance thanks to the extra driving source pin

## Applications

- Switching applications

## Description

The new MDmesh™ M6 technology incorporates the most recent advancements to the well-known and consolidated MDmesh family of SJ MOSFETs. STMicroelectronics builds on the previous generation of MDmesh devices through its new M6 technology, which combines excellent R<sub>DS(on)</sub> per area improvement with one of the most effective switching behaviors available, as well as a user-friendly experience for maximum end-application efficiency.

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol         | Parameter                                                         | Value      | Unit               |
|----------------|-------------------------------------------------------------------|------------|--------------------|
| $V_{GS}$       | Gate-source voltage                                               | $\pm 25$   | V                  |
| $I_D$          | Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$  | 31         | A                  |
| $I_D$          | Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$ | 20         | A                  |
| $I_{DM}^{(1)}$ | Drain current (pulsed)                                            | 124        | A                  |
| $P_{TOT}$      | Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$     | 190        | W                  |
| $dv/dt^{(2)}$  | Peak diode recovery voltage slope                                 | 15         | V/ns               |
| $dv/dt^{(3)}$  | MOSFET $dv/dt$ ruggedness                                         | 100        | V/ns               |
| $T_{stg}$      | Storage temperature range                                         | -55 to 150 | $^{\circ}\text{C}$ |
| $T_j$          | Operating junction temperature range                              |            |                    |

1. Pulse width is limited by safe operating area.
2.  $I_{SD} \leq 31\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DS(peak)} < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$
3.  $V_{DS} \leq 480\text{ V}$

**Table 2. Thermal data**

| Symbol              | Parameter                        | Value | Unit                        |
|---------------------|----------------------------------|-------|-----------------------------|
| $R_{thj-case}$      | Thermal resistance junction-case | 0.66  | $^{\circ}\text{C}/\text{W}$ |
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-pcb  | 50    | $^{\circ}\text{C}/\text{W}$ |

1. When mounted on 1 inch<sup>2</sup> FR-4, 2 Oz copper board

**Table 3. Avalanche characteristics**

| Symbol   | Parameter                                                                                                                 | Value | Unit |
|----------|---------------------------------------------------------------------------------------------------------------------------|-------|------|
| $I_{AR}$ | Avalanche current, repetitive or not repetitive<br>(pulse width limited by $T_{jmax}$ )                                   | 5.3   | A    |
| $E_{AS}$ | Single pulse avalanche energy<br>(starting $T_j = 25\text{ }^{\circ}\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ ) | 800   | mJ   |

## 2 Electrical characteristics

( $T_C = 25\text{ }^{\circ}\text{C}$  unless otherwise specified)

**Table 4. On/off states**

| Symbol        | Parameter                         | Test conditions                                                                             | Min. | Typ. | Max.    | Unit             |
|---------------|-----------------------------------|---------------------------------------------------------------------------------------------|------|------|---------|------------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage    | $V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$                                                 | 600  |      |         | V                |
| $I_{DSS}$     | Zero gate voltage drain current   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$                                             |      |      | 1       | $\mu\text{A}$    |
|               |                                   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$ , $T_C = 125\text{ }^{\circ}\text{C}^{(1)}$ |      |      | 100     | $\mu\text{A}$    |
| $I_{GSS}$     | Gate-body leakage current         | $V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$                                          |      |      | $\pm 5$ | $\mu\text{A}$    |
| $V_{GS(th)}$  | Gate threshold voltage            | $V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$                                          | 3.25 | 4    | 4.75    | V                |
| $R_{DS(on)}$  | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$ , $I_D = 15.5\text{ A}$                                              |      | 70   | 82      | $\text{m}\Omega$ |

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

| Symbol                     | Parameter                     | Test conditions                                                                                                                              | Min. | Typ. | Max. | Unit     |
|----------------------------|-------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|----------|
| $C_{iss}$                  | Input capacitance             | $V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$                                                                         | -    | 2340 | -    | pF       |
| $C_{oss}$                  | Output capacitance            |                                                                                                                                              | -    | 149  | -    | pF       |
| $C_{rss}$                  | Reverse transfer capacitance  |                                                                                                                                              | -    | 3.7  | -    | pF       |
| $C_{oss\text{ eq.}}^{(1)}$ | Equivalent output capacitance | $V_{DS} = 0\text{ to }480\text{ V}$ , $V_{GS} = 0\text{ V}$                                                                                  | -    | 390  | -    | pF       |
| $R_G$                      | Intrinsic gate resistance     | $f = 1\text{ MHz}$ , $I_D = 0\text{ A}$                                                                                                      | -    | 1.4  | -    | $\Omega$ |
| $Q_g$                      | Total gate charge             | $V_{DD} = 480\text{ V}$ , $I_D = 36\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$<br>(see Figure 14. Test circuit for gate charge behavior) | -    | 52.2 | -    | nC       |
| $Q_{gs}$                   | Gate-source charge            |                                                                                                                                              | -    | 16.5 | -    | nC       |
| $Q_{gd}$                   | Gate-drain charge             |                                                                                                                                              | -    | 23   | -    | nC       |

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 6. Switching times**

| Symbol       | Parameter           | Test conditions                                                                                                                                                                                                  | Min. | Typ. | Max. | Unit |
|--------------|---------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $t_{d(on)}$  | Turn-on delay time  | $V_{DD} = 300\text{ V}$ , $I_D = 18\text{ A}$ ,<br>$R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$<br>(see Figure 13. Switching times test circuit for resistive load and Figure 18. Switching time waveform) | -    | 21.5 | -    | ns   |
| $t_r$        | Rise time           |                                                                                                                                                                                                                  | -    | 18.7 | -    | ns   |
| $t_{d(off)}$ | Turn-off delay time |                                                                                                                                                                                                                  | -    | 54.6 | -    | ns   |
| $t_f$        | Fall time           |                                                                                                                                                                                                                  | -    | 8.1  | -    | ns   |

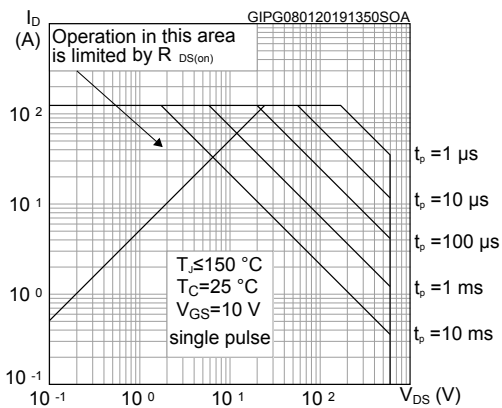
**Table 7. Source-drain diode**

| Symbol              | Parameter                     | Test conditions                                                                                                                                                                                                 | Min. | Typ. | Max. | Unit          |
|---------------------|-------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $I_{SD}^{(1)}$      | Source-drain current          |                                                                                                                                                                                                                 | -    |      | 31   | A             |
| $I_{SDM}^{(2) (1)}$ | Source-drain current (pulsed) |                                                                                                                                                                                                                 | -    |      | 124  | A             |
| $V_{SD}^{(3)}$      | Forward on voltage            | $V_{GS} = 0\text{ V}$ , $I_{SD} = 31\text{ A}$                                                                                                                                                                  | -    |      | 1.6  | V             |
| $t_{rr}$            | Reverse recovery time         | $I_{SD} = 36\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$<br>(see Figure 15. Test circuit for inductive load switching and diode recovery times)                                     | -    | 281  |      | ns            |
| $Q_{rr}$            | Reverse recovery charge       |                                                                                                                                                                                                                 | -    | 3.67 |      | $\mu\text{C}$ |
| $I_{RRM}$           | Reverse recovery current      |                                                                                                                                                                                                                 | -    | 26.1 |      | A             |
| $t_{rr}$            | Reverse recovery time         | $I_{SD} = 36\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ ,<br>$T_j = 150\text{ }^\circ\text{C}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times) | -    | 424  |      | ns            |
| $Q_{rr}$            | Reverse recovery charge       |                                                                                                                                                                                                                 | -    | 7.2  |      | $\mu\text{C}$ |
| $I_{RRM}$           | Reverse recovery current      |                                                                                                                                                                                                                 | -    | 34   |      | A             |

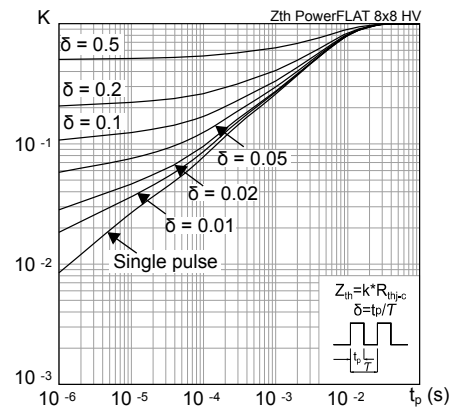
1. This value is limited by package.
2. Pulse width is limited by safe operating area.
3. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

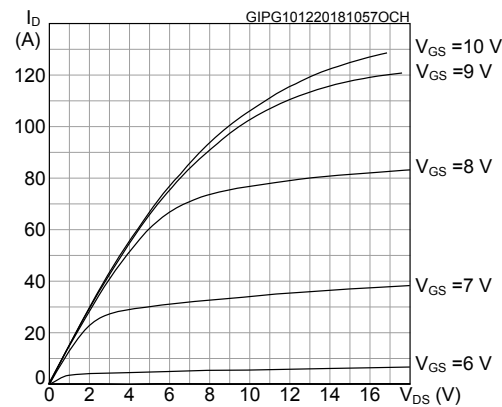
**Figure 1. Safe operating area**



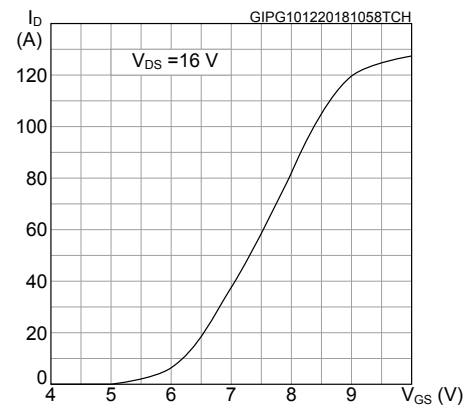
**Figure 2. Thermal impedance**



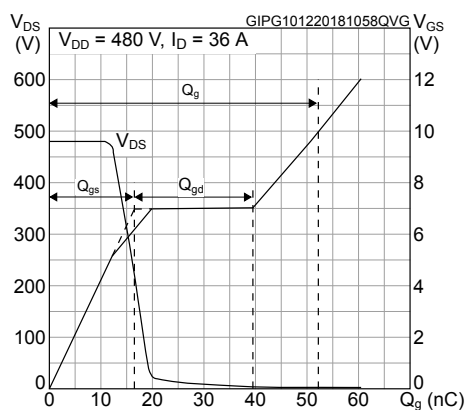
**Figure 3. Output characteristics**



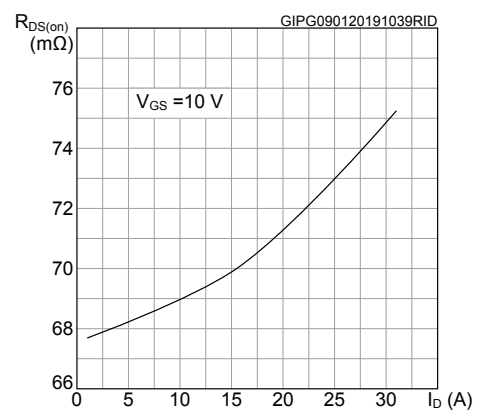
**Figure 4. Transfer characteristics**



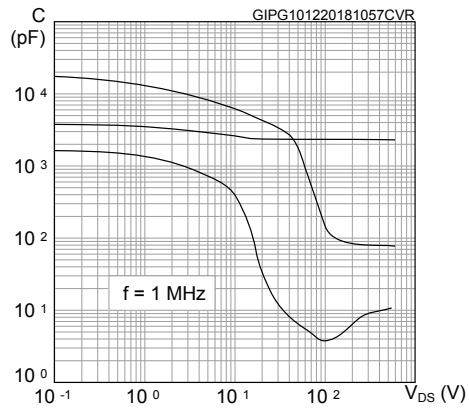
**Figure 5. Gate charge vs gate-source voltage**



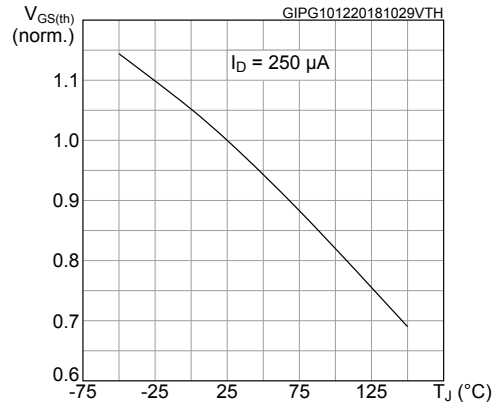
**Figure 6. Static drain-source on-resistance**



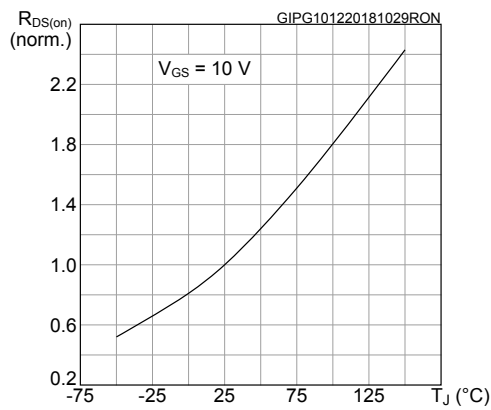
**Figure 7. Capacitance variations**



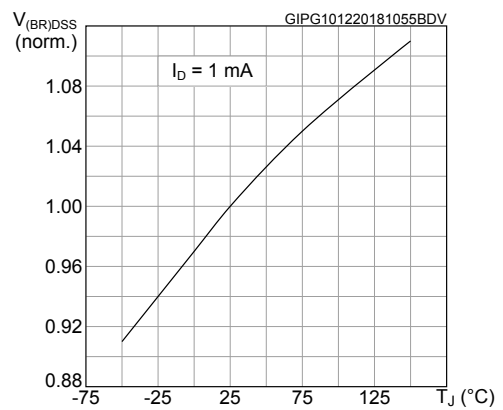
**Figure 8. Normalized gate threshold voltage vs temperature**



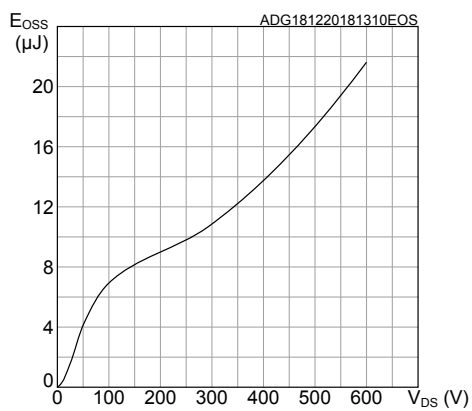
**Figure 9. Normalized on-resistance vs temperature**



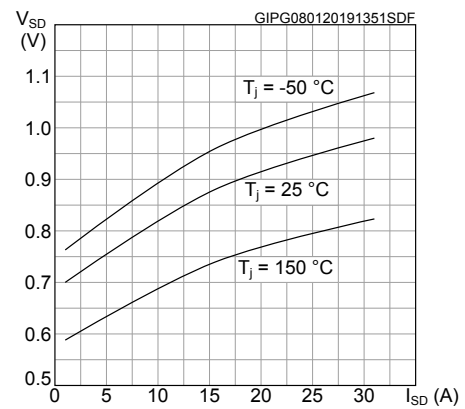
**Figure 10. Normalized  $V_{(BR)DSS}$  vs temperature**



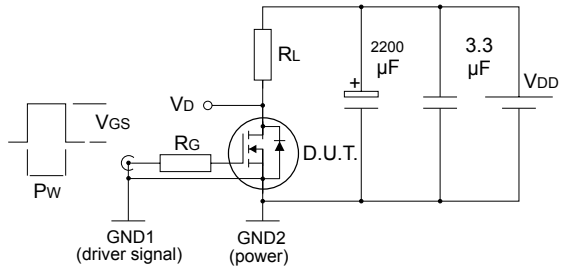
**Figure 11. Output capacitance stored energy**



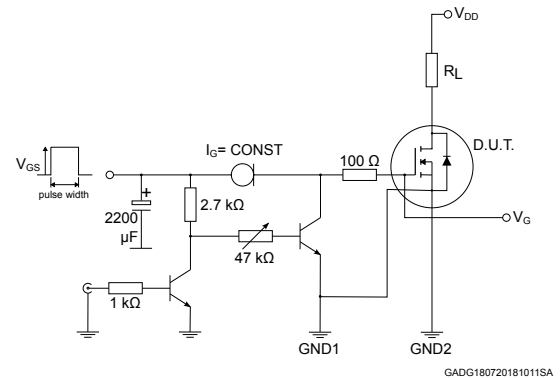
**Figure 12. Source-drain diode forward characteristics**



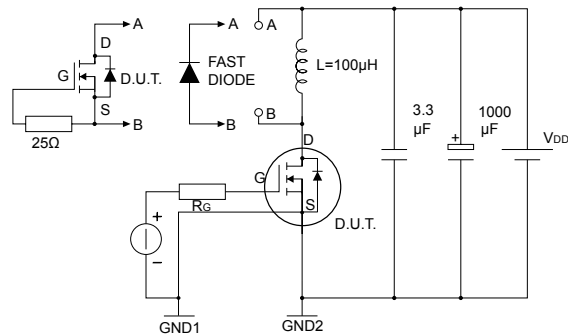
### 3 Test circuits

**Figure 13. Switching times test circuit for resistive load**


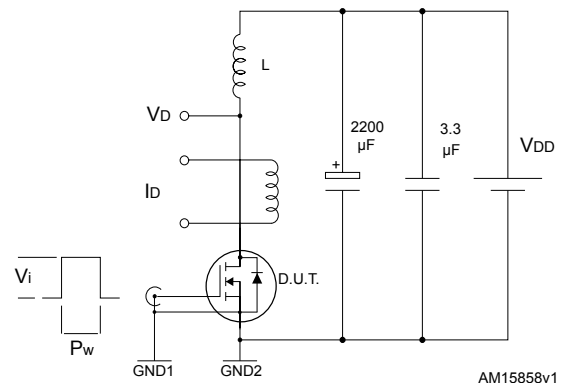
AM15855v1

**Figure 14. Test circuit for gate charge behavior**


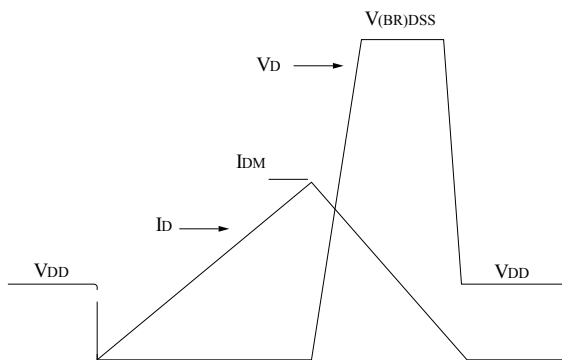
GADG180720181011SA

**Figure 15. Test circuit for inductive load switching and diode recovery times**


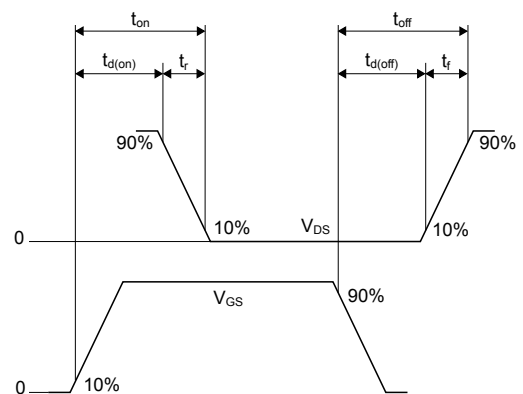
AM15857v1

**Figure 16. Unclamped inductive load test circuit**


AM15858v1

**Figure 17. Unclamped inductive waveform**


AM01472v1

**Figure 18. Switching time waveform**


AM01473v1

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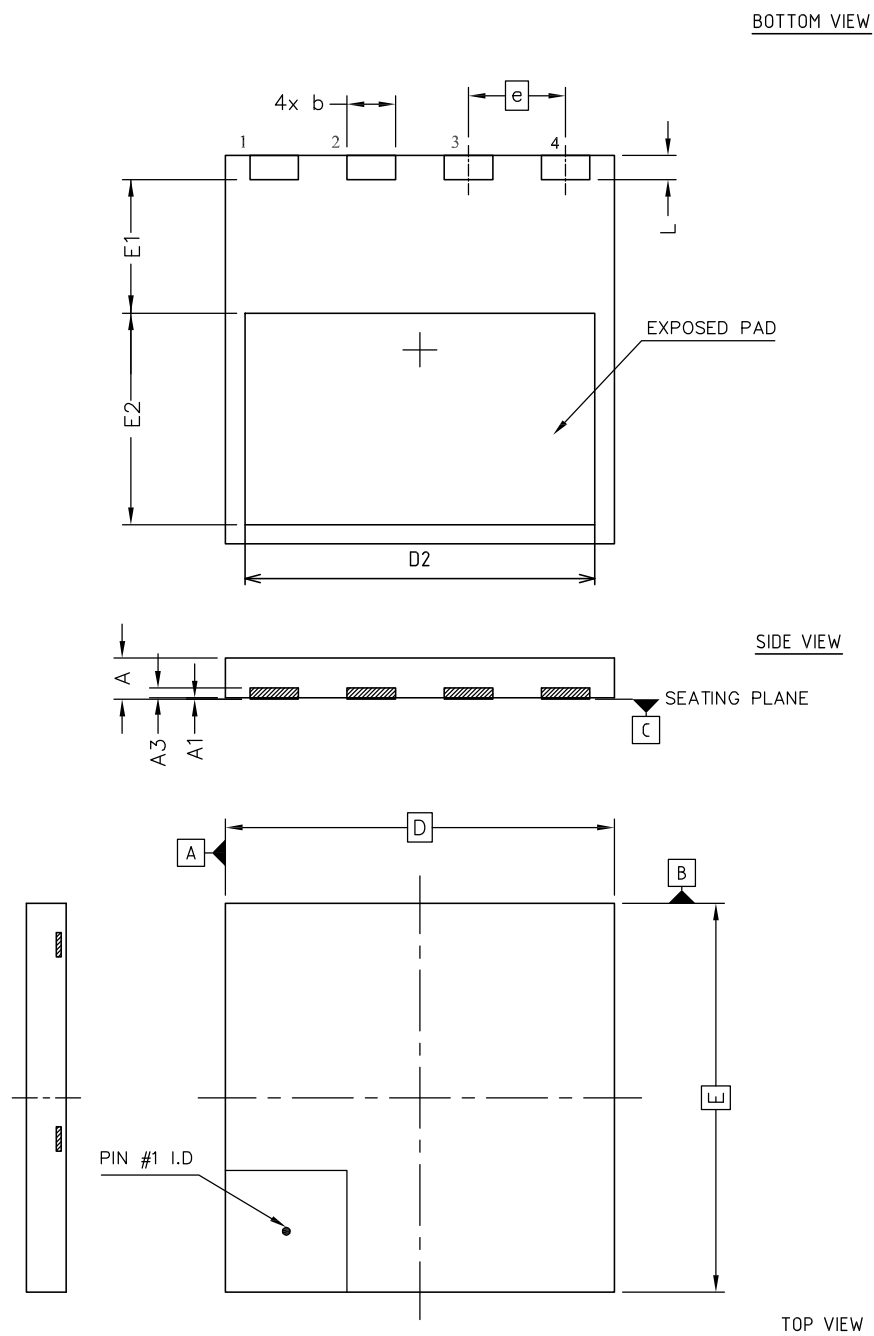
## 4 Package information

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In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK®** packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

## 4.1 PowerFLAT™ 8x8 HV package information

Figure 19. PowerFLAT™ 8x8 HV package outline

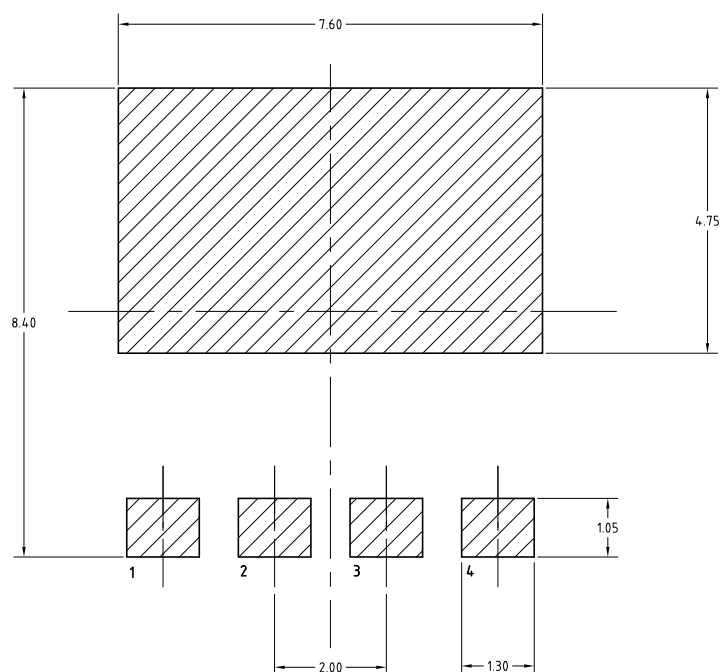


8222871\_Rev\_4

**Table 8. PowerFLAT™ 8x8 HV mechanical data**

| Ref. | Dimensions (in mm) |      |      |
|------|--------------------|------|------|
|      | Min.               | Typ. | Max. |
| A    | 0.75               | 0.85 | 0.95 |
| A1   | 0.00               |      | 0.05 |
| A3   | 0.10               | 0.20 | 0.30 |
| b    | 0.90               | 1.00 | 1.10 |
| D    | 7.90               | 8.00 | 8.10 |
| E    | 7.90               | 8.00 | 8.10 |
| D2   | 7.10               | 7.20 | 7.30 |
| E1   | 2.65               | 2.75 | 2.85 |
| E2   | 4.25               | 4.35 | 4.45 |
| e    | 2.00 BSC           |      |      |
| L    | 0.40               | 0.50 | 0.60 |

**Figure 20. PowerFLAT™ 8x8 HV footprint**

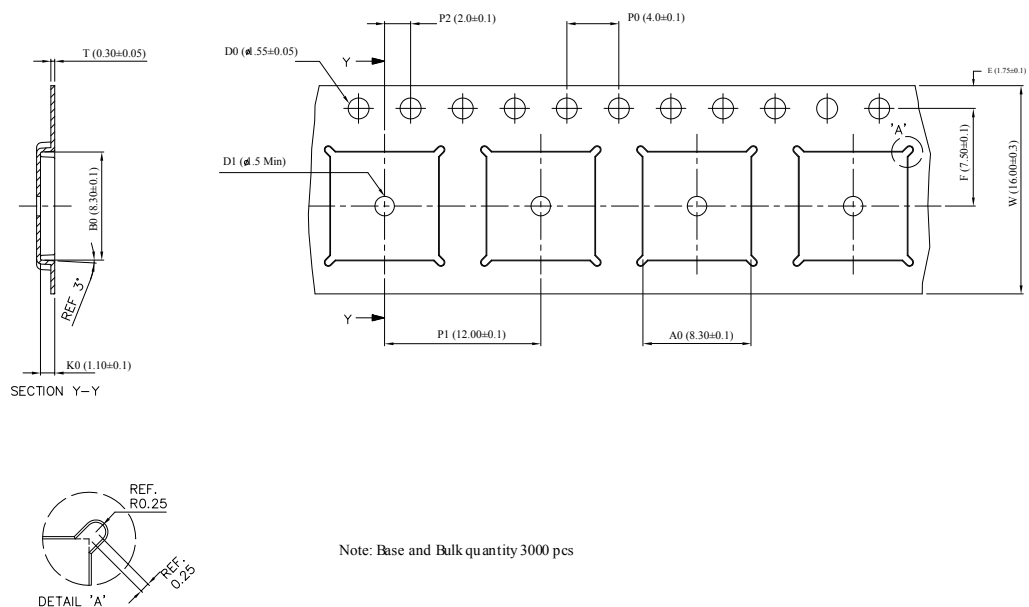


8222871\_REV\_4\_footprint

**Note:** All dimensions are in millimeters.

## 4.2 PowerFLAT™ 8x8 HV packing information

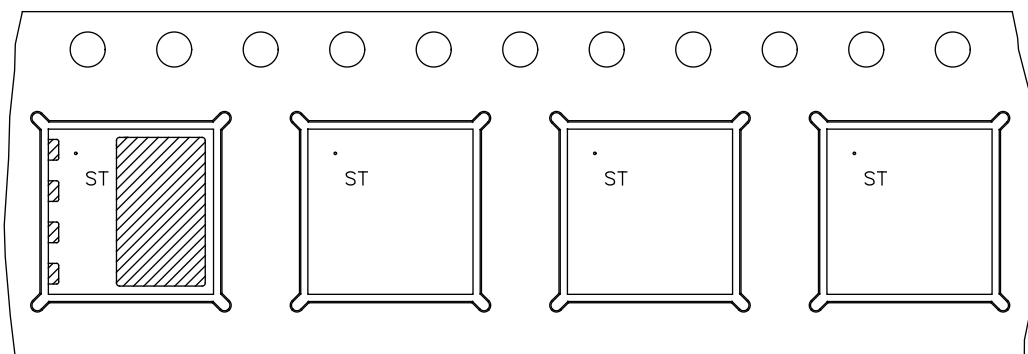
**Figure 21. PowerFLAT™ 8x8 HV tape**



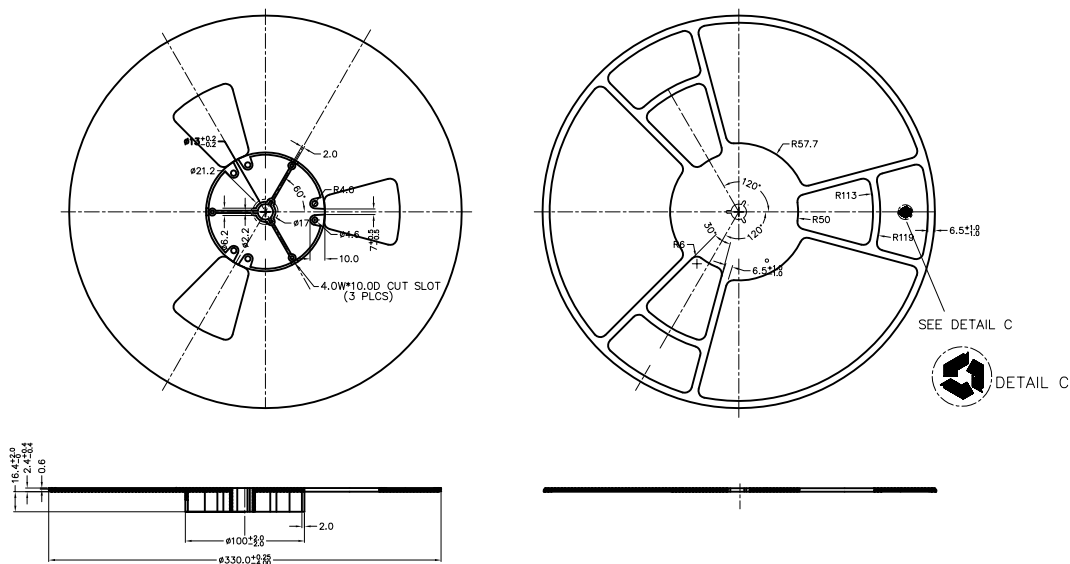
8229819\_Tape\_revA

**Note:** All dimensions are in millimeters.

**Figure 22. PowerFLAT™ 8x8 HV package orientation in carrier tape**



**Figure 23. PowerFLAT™ 8x8 HV reel**



8229819\_Reel\_revA

**Note:** All dimensions are in millimeters.

## Revision history

**Table 9. Document revision history**

| Date        | Revision | Changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15-Nov-2017 | 1        | First release                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 22-Jan-2019 | 2        | Modified <a href="#">Table 1. Absolute maximum ratings</a> , <a href="#">Table 2. Thermal data</a> , <a href="#">Table 3. Avalanche characteristics</a> , <a href="#">Table 4. On/off states</a> , <a href="#">Table 5. Dynamic</a> , <a href="#">Table 6. Switching times</a> and <a href="#">Table 7. Source-drain diode</a> .<br>Added <a href="#">Section 2.1 Electrical characteristics (curves)</a> .<br>Modified <a href="#">Section 3 Test circuits</a> .<br>Minor text changes. |

## Contents

|            |                                             |           |
|------------|---------------------------------------------|-----------|
| <b>1</b>   | <b>Electrical ratings .....</b>             | <b>2</b>  |
| <b>2</b>   | <b>Electrical characteristics.....</b>      | <b>3</b>  |
| <b>2.1</b> | Electrical characteristics (curves) .....   | 5         |
| <b>3</b>   | <b>Test circuits .....</b>                  | <b>7</b>  |
| <b>4</b>   | <b>Package information.....</b>             | <b>8</b>  |
| <b>4.1</b> | PowerFLAT 8x8 HV package information .....  | 8         |
| <b>4.2</b> | PowerFLAT™ 8x8 HV packing information ..... | 10        |
|            | <b>Revision history .....</b>               | <b>13</b> |

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