Balanced Modulator/Demodulator

Data Sheet

AD630

FEATURES

Recovers signal from 100 dB noise
2 MHz channel bandwidth
45 V/µs slew rate
Low crosstalk: −120 dB at 1 kHz, −100 dB at 10 kHz
Pin programmable, closed-loop gains of ±1 and ±2
0.05% closed-loop gain accuracy and match
100 µV channel offset voltage (AD630)
350 kHz full power bandwidth
Chips available

APPLICATIONS

Balanced modulation and demodulation
Synchronous detection
Phase detection
Quadrature detection
Phase sensitive detection
Lock in amplification
Square wave multiplication

GENERAL DESCRIPTION

The AD630 is a high precision balanced modulator/demodulator that combines a flexible commutating architecture with the accuracy and temperature stability afforded by laser wafer trimmed thin film resistors. A network of on-board applications resistors provides precision closed-loop gains of ±1 and ±2 with 0.05% accuracy (AD630B). These resistors may also be used to accurately configure multiplexer gains of 1, 2, 3, or 4. External feedback enables high gain or complex switched feedback topologies.

The AD630 can be thought of as a precision op amp with two independent differential input stages and a precision comparator that is used to select the active front end. The rapid response time of this comparator coupled with the high slew rate and fast settling of the linear amplifiers minimize switching distortion.

The AD630 is used in precision signal processing and instrumentation applications that require wide dynamic range. When used as a synchronous demodulator in a lock-in amplifier configuration, the AD630 can recover a small signal from 100 dB of interfering noise (see the Lock-In Amplifier Applications section). Although optimized for operation up to 1 kHz, the circuit is useful at frequencies up to several hundred kilohertz.

FUNCTIONAL BLOCK DIAGRAM

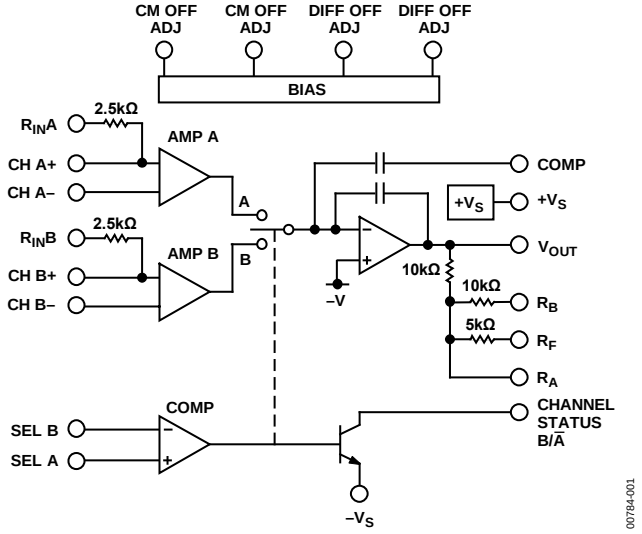

Figure 1.

Other features of the AD630 include pin programmable frequency compensation; optional input bias current compensation resistors, common-mode and differential-offset voltage adjustment, and a channel status output that indicates which of the two differential inputs is active.

PRODUCT HIGHLIGHTS

1. The application flexibility of the AD630 makes it the best choice for applications that require precisely fixed gain, switched gain, multiplexing, integrating-switching functions, and high speed precision amplification.
2. The 100 dB dynamic range of the AD630 exceeds that of any hybrid or IC balanced modulator/demodulator and is comparable to that of costly signal processing instruments.
3. The op amp format of the AD630 ensures easy implementation of high gain or complex switched feedback functions. The application resistors facilitate the implementation of most common applications with no additional parts.
4. The AD630 can be used as a 2-channel multiplexer with gains of 1, 2, 3, or 4. The channel separation of 100 dB at 10 kHz approaches the limit achievable with an empty IC package.
5. Laser trimming of the comparator and amplifying channel offsets eliminate the need for external nulling in most cases.

Rev. F **Document Feedback**

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SPECIFICATIONS

At 25°C and $\pm V_S$ = ±15 V, unless otherwise noted.

Table 1.

Parameter	AD630J/AD630A Min	AD630J/AD630A Typ	AD630J/AD630A Max	AD630K/AD630B Min	AD630K/AD630B Typ	AD630K/AD630B Max	AD630S Min	AD630S Typ	AD630S Max	Unit
GAIN										
Open-Loop Gain	90	110		100	120		90	110		dB
±1, ±2 Closed-Loop Gain Error		0.1				0.05		0.1		%
Closed-Loop Gain Match		0.1				0.05		0.1		%
Closed-Loop Gain Drift		2			2			2		ppm/°C
CHANNEL INPUTS										
V_{IN} Operational Limit[1]	$(-V_S + 4)$ to $(+V_S - 1)$			$(-V_S + 4)$ to $(+V_S - 1)$			$(-V_S + 4)$ to $(+V_S - 1)$			V
Input Offset Voltage			500			100			500	µV
T_{MIN} to T_{MAX}			800			160			1000	µV
Input Bias Current		100	300		100	300		100	300	nA
Input Offset Current		10	50		10	50		10	50	nA
Channel Separation at 10 kHz		100			100			100		dB
COMPARATOR										
V_{IN} Operational Limit[1]	$(-V_S + 3)$ to $(+V_S - 1.5)$			$(-V_S + 3)$ to $(+V_S - 1.5)$			$(-V_S + 3)$ to $(+V_S - 1.3)$			V
Switching Window			±1.5			±1.5			±1.5	mV
T_{MIN} to T_{MAX}			±2.0			±2.0			±2.5	mV
Input Bias Current		100	300		100	300		100	300	nA
Response Time (−5 mV to +5 mV Step)		200			200			200		ns
Channel Status										
I_{SINK} at $V_{OL} = -V_S + 0.4$ V[2]	1.6			1.6			1.6			mA
Pull-Up Voltage			$(-V_S + 33)$			$(-V_S + 33)$			$(-V_S + 33)$	V
DYNAMIC PERFORMANCE										
Unity Gain Bandwidth		2			2			2		MHz
Slew Rate[3]		45			45			45		V/µs
Settling Time to 0.1% (20 V Step)		3			3			3		µs
OPERATING CHARACTERISTICS										
Common-Mode Rejection	85	105		90	110		90	110		dB
Power Supply Rejection	90	110		90	110		90	110		dB
Supply Voltage Range	±5		±16.5	±5		±16.5	±5		±16.5	V
Supply Current		4	5		4	5		4	5	mA
OUTPUT VOLTAGE, AT R_L = 2 kΩ										
T_{MIN} to T_{MAX}	±10			±10			±10			V
Output Short-Circuit Current		25			25			25		mA
TEMPERATURE RANGES										
N Package	0		70	0		70				°C
D Package	−25		+85	−25		+85	−55		+125	°C

[1] If one terminal of each differential channel or comparator input is kept within these limits the other terminal may be taken to the positive supply.
[2] I_{SINK} at $V_{OL} = (-V_S + 1$ V) is typically 4 mA.
[3] Pin 12 open. Slew rate with Pin 12 and Pin 13 shorted is typically 35 V/µs.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	±18 V
Internal Power Dissipation	600 mW
Output Short-Circuit to Ground	Indefinite
Storage Temperature	
Ceramic Package	−65°C to +150°C
Plastic Package	−55°C to +125°C
Lead Temperature Range (Soldering, 10 sec)	300°C
Maximum Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 3. Thermal Resistance

Package Type	θ_{JC}	θ_{JA}	Unit
20-Lead PDIP (N-20)	24	61	°C/W
20-Lead SBDIP (D-20)	35	120	°C/W
20-Lead LCC (E-20-4)	35	120	°C/W
20-Lead SOIC_W (RW-20)	38	75	°C/W

CHIP AVAILABILITY

The AD630 is available in laser trimmed, passivated chip form. Figure 2 shows the AD630 metallization pattern, bonding pads, and dimensions. AD630 chips are available; consult factory for details.

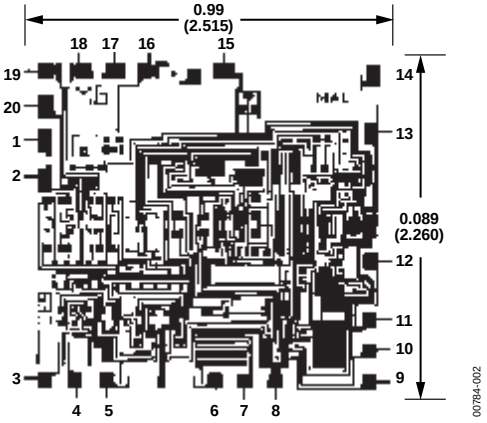


Figure 2. Chip Metallization and Pinout
Dimensions shown in inches and (millimeters)
Contact factory for latest dimensions

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

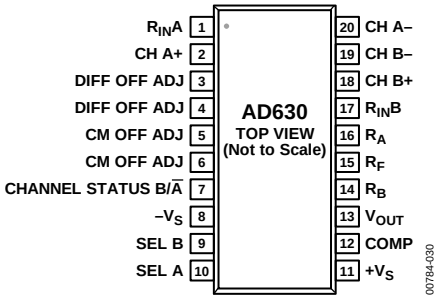


Figure 3. 20-Lead SOIC Pin Configuration

Table 4. 20-Lead SOIC Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$R_{IN}A$	2.5 kΩ Resistor to Noninverting Input of Op Amp A
2	CH A+	Noninverting Input of Op Amp A
3	DIFF OFF ADJ	Differential Offset Adjustment
4	DIFF OFF ADJ	Differential Offset Adjustment
5	CM OFF ADJ	Common-Mode Offset Adjustment
6	CM OFF ADJ	Common-Mode Offset Adjustment
7	CHANNEL STATUS B/$\overline{A}$	B or A Channel Status
8	$-V_S$	Negative Supply
9	SEL B	B Channel Comparator Input
10	SEL A	A Channel Comparator Input
11	$+V_S$	Positive Supply
12	COMP	Pin to Connect Internal Compensation Capacitor
13	V_{OUT}	Output Voltage
14	R_B	10 kΩ Gain Setting Resistor
15	R_F	10 kΩ Feedback Resistor
16	R_A	5 kΩ Feedback Resistor
17	$R_{IN}B$	2.5 kΩ Resistor to Noninverting Input of Op Amp B
18	CH B+	Noninverting Input of Op Amp B
19	CH B–	Inverting Input of Op Amp B
20	CH A–	Inverting Input of Op Amp A

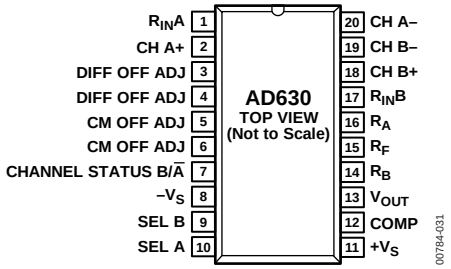


Figure 4. 20-Lead PDIP Pin Configuration

Table 5. 20-Lead PDIP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$R_{IN}A$	2.5 kΩ Resistor to Noninverting Input of Op Amp A
2	CH A+	Noninverting Input of Op Amp A
3	DIFF OFF ADJ	Differential Offset Adjustment
4	DIFF OFF ADJ	Differential Offset Adjustment
5	CM OFF ADJ	Common-Mode Offset Adjustment
6	CM OFF ADJ	Common-Mode Offset Adjustment
7	CHANNEL STATUS B/$\overline{A}$	B or A Channel Status
8	$-V_S$	Negative Supply
9	SEL B	B Channel Comparator Input
10	SEL A	A Channel Comparator Input
11	$+V_S$	Positive Supply
12	COMP	Pin to Connect Internal Compensation Capacitor
13	V_{OUT}	Output Voltage
14	R_B	10 kΩ Gain Setting Resistor
15	R_F	10 kΩ Feedback Resistor
16	R_A	5 kΩ Feedback Resistor
17	$R_{IN}B$	2.5 kΩ Resistor to Noninverting Input of Op Amp B
18	CH B+	Noninverting Input of Op Amp B
19	CH B–	Inverting Input of Op Amp B
20	CH A–	Inverting Input of Op Amp A

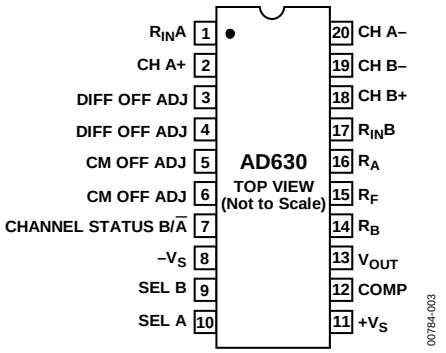


Figure 5. 20-Lead CERDIP Pin Configuration

Table 6. 20-Lead CERDIP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$R_{IN}A$	2.5 kΩ Resistor to Noninverting Input of Op Amp A
2	CH A+	Noninverting Input of Op Amp A
3	DIFF OFF ADJ	Differential Offset Adjustment
4	DIFF OFF ADJ	Differential Offset Adjustment
5	CM OFF ADJ	Common-Mode Offset Adjustment
6	CM OFF ADJ	Common-Mode Offset Adjustment
7	CHANNEL STATUS B/$\overline{A}$	B or A Channel Status
8	$-V_S$	Negative Supply
9	SEL B	B Channel Comparator Input
10	SEL A	A Channel Comparator Input
11	$+V_S$	Positive Supply
12	COMP	Pin to Connect Internal Compensation Capacitor
13	V_{OUT}	Output Voltage
14	R_B	10 kΩ Gain Setting Resistor
15	R_F	10 kΩ Feedback Resistor
16	R_A	5 kΩ Feedback Resistor
17	$R_{IN}B$	2.5 kΩ Resistor to Noninverting Input of Op Amp B
18	CH B+	Noninverting Input of Op Amp B
19	CH B–	Inverting Input of Op Amp B
20	CH A–	Inverting Input of Op Amp A

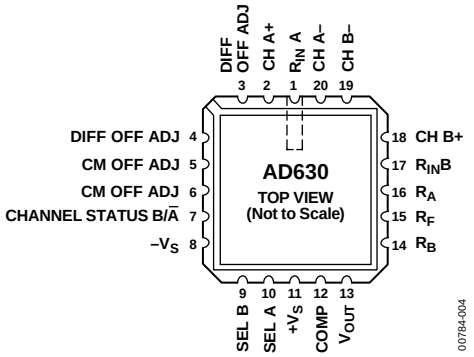


Figure 6. 20-Terminal CLCC Pin Configuration

Table 7. 20-Terminal CLCC Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$R_{IN}A$	2.5 kΩ Resistor to Noninverting Input of Op Amp A
2	CH A+	Noninverting Input of Op Amp A
3	DIFF OFF ADJ	Differential Offset Adjustment
4	DIFF OFF ADJ	Differential Offset Adjustment
5	CM OFF ADJ	Common-Mode Offset Adjustment
6	CM OFF ADJ	Common-Mode Offset Adjustment
7	CHANNEL STATUS B/$\overline{A}$	B or A Channel Status
8	$-V_S$	Negative Supply
9	SEL B	B Channel Comparator Input
10	SEL A	A Channel Comparator Input
11	$+V_S$	Positive Supply
12	COMP	Pin to Connect Internal Compensation Capacitor
13	V_{OUT}	Output Voltage
14	R_B	10 kΩ Gain Setting Resistor
15	R_F	10 kΩ Feedback Resistor
16	R_A	5 kΩ Feedback Resistor
17	$R_{IN}B$	2.5 kΩ Resistor to Noninverting Input of Op Amp B
18	CH B+	Noninverting Input of Op Amp B
19	CH B–	Inverting Input of Op Amp B
20	CH A–	Inverting Input of Op Amp A

TYPICAL PERFORMANCE CHARACTERISTICS

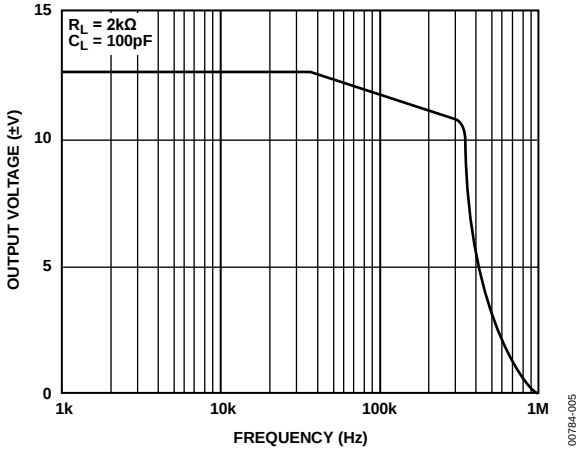


Figure 7. Output Voltage vs. Frequency (See Figure 16)

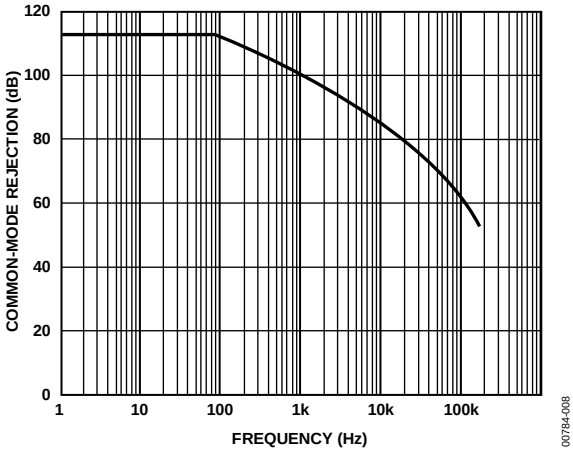


Figure 10. Common-Mode Rejection vs. Frequency

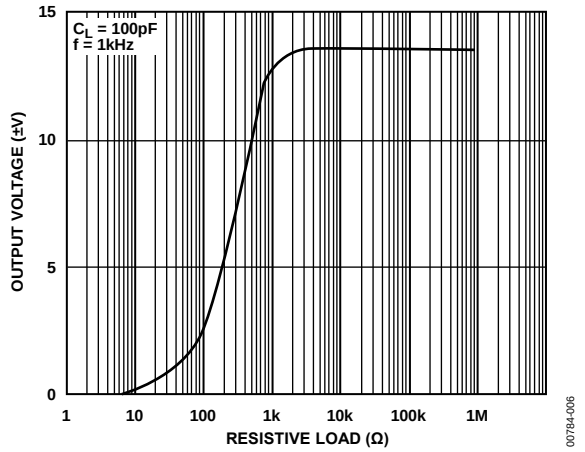


Figure 8. Output Voltage vs. Resistive Load (See Figure 16)

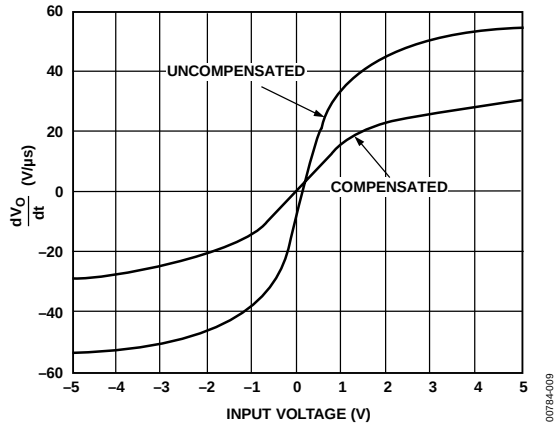


Figure 11. $\frac{dV_O}{dt}$ vs. Input Voltage

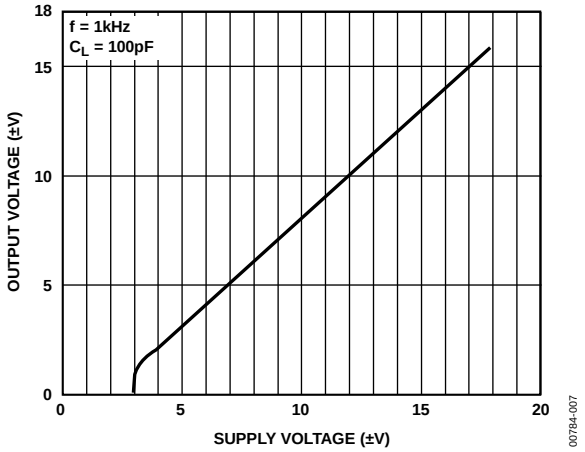


Figure 9. Output Voltage Swing vs. Supply Voltage (See Figure 16)

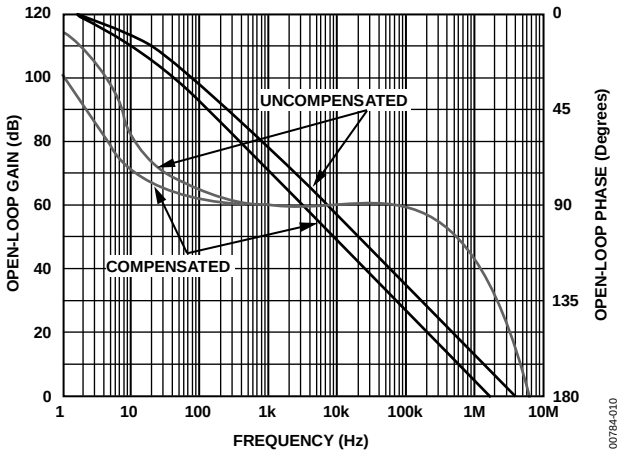


Figure 12. Gain and Phase vs. Frequency

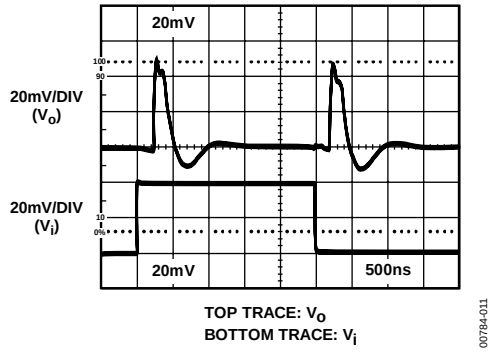


Figure 13. Channel-to-Channel Switch-Settling Characteristic (See Figure 17)

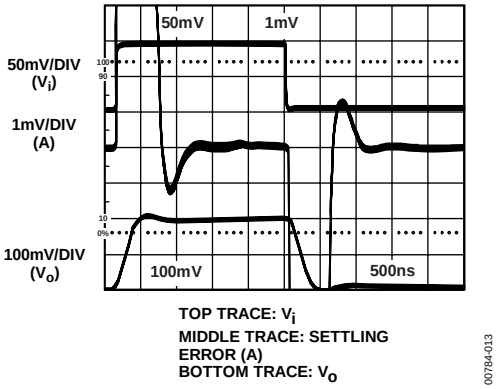


Figure 14. Small Signal Noninverting Step Response (See Figure 18)

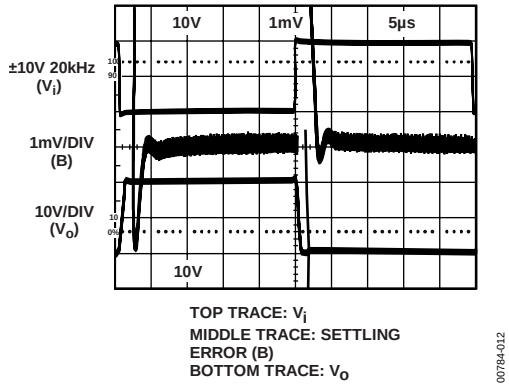


Figure 15. Large Signal Inverting Step Response (See Figure 19)

TEST CIRCUITS

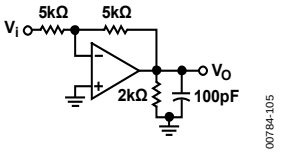


Figure 16. Test Circuit for Output Voltage vs. Frequecy, Resistive Load, and Supply Voltage (See Figure 7, Figure 8, and Figure 9)

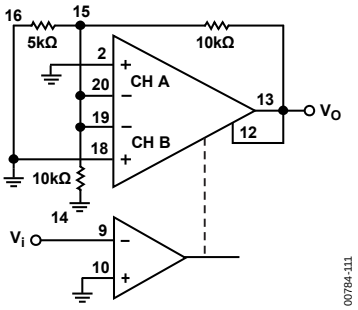


Figure 17. Test Circuit for Channel-to-Channel Switch-Settling Characteristic (See Figure 13)

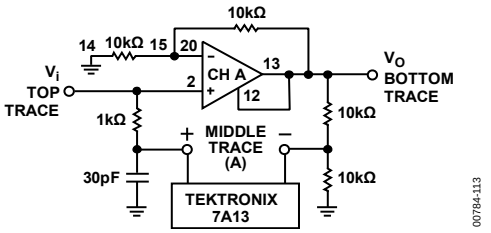


Figure 18. Test Circuit for Small Signal Noninverting Step Response (See Figure 14)

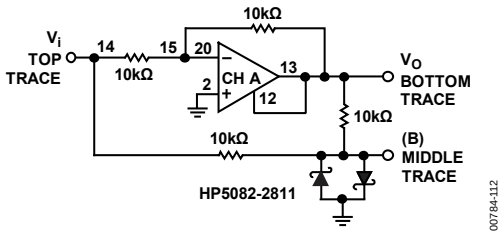


Figure 19. Test Circuit for Large Signal Noninverting Step Response (See Figure 15)

THEORY OF OPERATION

TWO WAYS TO LOOK AT THE AD630

The functional block diagram of the AD630 (see Figure 1) shows the pin connections of the internal functions. An alternative architectural diagram is shown in Figure 20. In this diagram, the individual A and B channel preamps, the switch, and the integrator output amplifier are combined in a single op amp. This amplifier has two differential input channels, only one of which is active at a time.

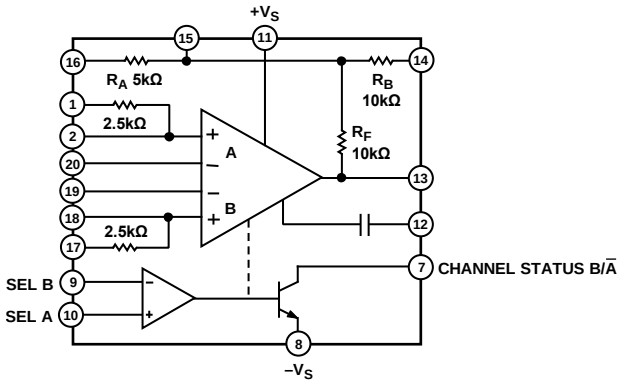


Figure 20. Architectural Block Diagram

HOW THE AD630 WORKS

The basic mode of operation of the AD630 may be easier to recognize as two fixed gain stages, which can be inserted into the signal path under the control of a sensitive voltage comparator. When the circuit is switched between inverting and noninverting gain, it provides the basic modulation/demodulation function. The AD630 is unique in that it includes laser wafer trimmed thin-film feedback resistors on the monolithic chip. The configuration shown in Figure 21 yields a gain of ±2 and can be easily changed to ±1 by shifting R_B from its ground connection to the output.

The comparator selects one of the two input stages to complete an operational feedback connection around the AD630. The deselected input is off and has a negligible effect on operation.

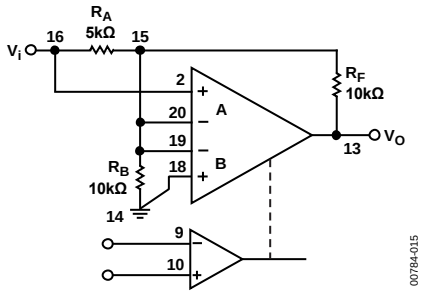


Figure 21. AD630 Symmetric Gain (±2)

When Channel B is selected, the R_A and R_F resistors are connected for inverting feedback as shown in the inverting gain configuration diagram in Figure 22. The amplifier has sufficient loop gain to minimize the loading effect of R_B at the virtual ground produced by the feedback connection. When the sign of the comparator input is reversed, Input B is deselected and Input A is selected. The new equivalent circuit is the noninverting gain configuration shown in Figure 23. In this case, R_A appears across the op amp input terminals, but because the amplifier drives this difference voltage to zero, the closed-loop gain is unaffected.

The two closed-loop gain magnitudes are equal when $R_F/R_A = 1 + R_F/R_B$, which results from making R_A equal to $R_FR_B/(R_F + R_B)$ the parallel equivalent resistance of R_F and R_B.

The 5 kΩ and the two 10 kΩ resistors on the AD630 chip can be used to make a gain of 2 as shown in Figure 22 and Figure 23. By paralleling the 10 kΩ resistors to make R_F equal to 5 kΩ and omitting R_B, the circuit can be programmed for a gain of ±1 (as shown in Figure 28). These and other configurations using the on-chip resistors present the inverting inputs with a 2.5 kΩ source impedance. The more complete AD630 diagrams show 2.5 kΩ resistors available at the noninverting inputs which can be conveniently used to minimize errors resulting from input bias currents.

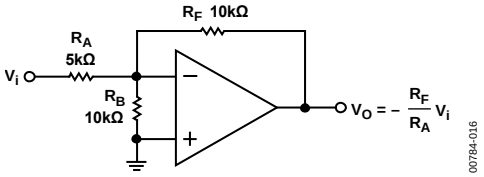


Figure 22. Inverting Gain Configuration

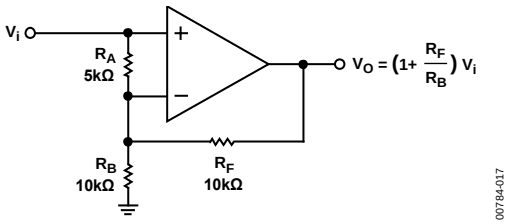


Figure 23. Noninverting Gain Configuration

CIRCUIT DESCRIPTION

The simplified schematic of the AD630 is shown in Figure 24. It has been subdivided into three major sections, the comparator, the two input stages, and the output integrator. The comparator consists of a front end made up of Q52 and Q53, a flip-flop load formed by Q3 and Q4, and two current steering switching cells Q28, Q29 and Q30, Q31. This structure is designed so that a differential input voltage greater than 1.5 mV in magnitude applied to the comparator inputs completely selects one of the switching cells. The sign of this input voltage determines which of the two switching cells is selected.

The collectors of each switching cell connect to an input transconductance stage. The selected cell conveys bias currents i_{22} and i_{23} to the input stage it controls, causing it to become active. The deselected cell blocks the bias to its input stage, which, as a consequence, remains off.

The structure of the transconductance stages is such that it presents a high impedance at its input terminals and draws no bias current when deselected. The deselected input does not interfere with the operation of the selected input ensuring maximum channel separation.

Another feature of the input structure is that it enhances the slew rate of the circuit. The current output of the active stage follows a quasihyperbolic sine relationship to the differential input voltage. This means that the greater the input voltage, the harder this stage drives the output integrator, and the faster the output signal moves. This feature helps ensure rapid, symmetric settling when switching between inverting and noninverting closed loop configurations.

The output section of the AD630 includes a current mirror load (Q24 and Q25), an integrator voltage gain stage (Q32), and a complementary output buffer (Q44 and Q74). The outputs of both transconductance stages are connected in parallel to the current mirror. Because the deselected input stage produces no output current and presents a high impedance at its outputs, there is no conflict. The current mirror translates the differential output current from the active input transconductance amplifier into single-ended form for the output integrator. The complementary output driver then buffers the integrator output to produce a low impedance output.

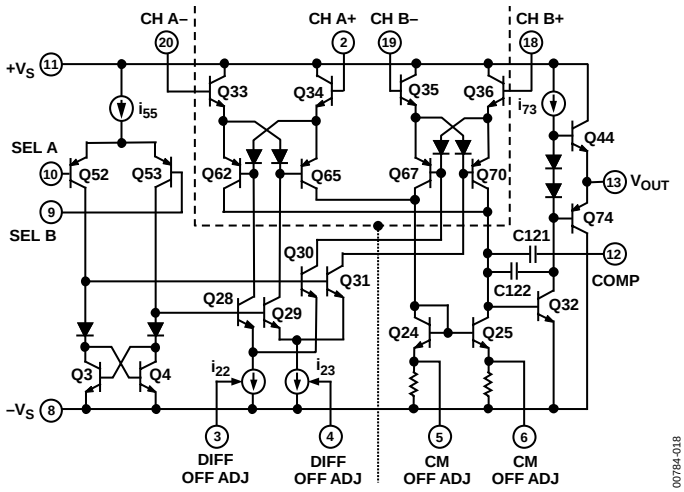


Figure 24. AD630 Simplified Schematic

OTHER GAIN CONFIGURATIONS

Many applications require switched gains other than the ±1 and ±2, which the self-contained applications resistors provide. The AD630 can be readily programmed with three external resistors over a wide range of positive and negative gain by selecting and R_B and R_F to give the noninverting gain $1 + R_F/R_B$ and subsequent R_A to give the desired inverting gain. Note that when the inverting magnitude equals the noninverting magnitude, the value of R_A is found to be $R_BR_F/(R_B + R_F)$. That is, R_A equals the parallel combination of R_B and R_F to match positive and negative gain.

The feedback synthesis of the AD630 may also include reactive impedance. The gain magnitudes match at all frequencies if the A impedance is made to equal the parallel combination of the B and F impedances. The same considerations apply to the AD630 as to conventional op amp feedback circuits. Virtually any function that can be realized with simple noninverting L network feedback can be used with the AD630. A common arrangement is shown in Figure 25. The low frequency gain of this circuit is 10. The response has a pole (−3 dB) at a frequency $f \simeq 1/(2\pi\ 100\ k\Omega \times C)$ and a zero (3 dB from the high frequency asymptote) at about 10 times this frequency. The 2 kΩ resistor in series with each capacitor mitigates the loading effect on circuitry driving this circuit, eliminates stability problems, and has a minor effect on the pole-zero locations.

As a result of the reactive feedback, the high frequency components of the switched input signal are transmitted at unity gain while the low frequency components are amplified. This arrangement is useful in demodulators and lock-in amplifiers. It increases the circuit dynamic range when the modulation or interference is substantially larger than the desired signal amplitude. The output signal contains the desired signal multiplied by the low frequency gain (which may be several hundred for large feedback ratios) with the switching signal and interference superimposed at unity gain.

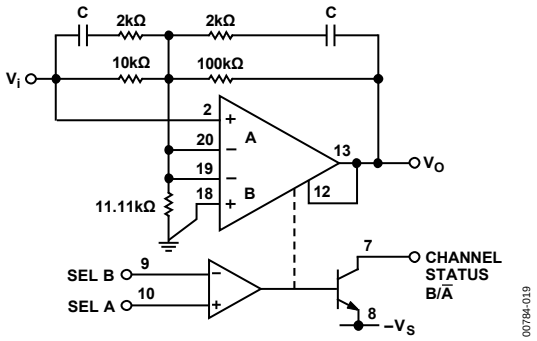


Figure 25. AD630 with External Feedback

SWITCHED INPUT IMPEDANCE

The noninverting mode of operation is a high input impedance configuration while the inverting mode is a low input impedance configuration. This means that the input impedance of the circuit undergoes an abrupt change as the gain is switched under control of the comparator. If the gain is switched when the input signal is not zero, as it is in many practical cases, a transient is delivered to the circuitry driving the AD630. In most applications, this requires the AD630 circuit to be driven by a low impedance source, which remains stiff at high frequencies. This is generally a wideband buffer amplifier.

FREQUENCY COMPENSATION

The AD630 combines the convenience of internal frequency compensation with the flexibility of external compensation by means of an optional self-contained compensation capacitor.

In gain of ±2 applications, the noise gain that must be addressed for stability purposes is actually 4. In this circumstance, the phase margin of the loop is on the order of 60° without the optional compensation. This condition provides the maximum bandwidth and slew rate for closed loop gains of |2| and above.

When the AD630 is used as a multiplexer, or in other configurations where one or both inputs are connected for unity gain feedback, the phase margin is reduced to less than 20°. This may be acceptable in applications where fast slewing is a first priority, but the transient response is not optimum. For these applications, the self-contained compensation capacitor may be added by connecting Pin 12 to Pin 13. This connection reduces the closed-loop bandwidth somewhat and improves the phase margin.

For intermediate conditions, such as a gain of ±1 where the loop attenuation is 2, determine the use of the compensation by whether bandwidth or settling response must be optimized. Also, use optional compensation when the AD630 is driving capacitive loads or whenever conservative frequency compensation is desired.

OFFSET VOLTAGE NULLING

The offset voltages of both input stages and the comparator have been pretrimmed so that external trimming is only required in the most demanding applications. The offset adjustment of the two input channels is accomplished by means of a differential and common-mode scheme. This facilitates fine adjustment of system errors in switched gain applications. With the system input tied to 0 V, and a switching or carrier waveform applied to the comparator, a low level square wave appears at the output. The differential offset adjustment potentiometers can be used to null the amplitude of this square wave (Pin 3 and Pin 4). The common-mode offset adjustment can be used to zero the residual dc output voltage (Pin 5 and Pin 6). Implement these functions using 10 kΩ trim potentiometers with wipers connected directly to Pin 8 as shown in Figure 28 and Figure 29.

CHANNEL STATUS OUTPUT

The channel status output, Pin 7, is an open collector output referenced to $-V_S$ that can be used to indicate which of the two input channels is active. The output is active (pulled low) when Channel A is selected. This output can also be used to supply positive feedback around the comparator. This produces hysteresis which serves to increase noise immunity. Figure 26 shows an example of how hysteresis may be implemented. Note that the feedback signal is applied to the inverting (−) terminal of the comparator to achieve positive feedback. This is because the open collector channel status output inverts the output sense of the internal comparator.

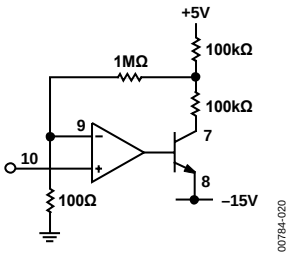


Figure 26. Comparator Hysteresis

The channel status output may be interfaced with TTL inputs as shown in Figure 27. This circuit provides appropriate level shifting from the open-collector AD630 channel status output to TTL inputs.

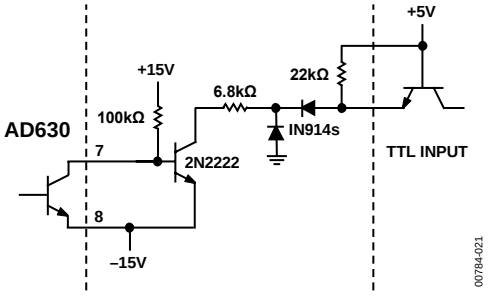


Figure 27. Channel Status—TTL Interface

APPLICATIONS INFORMATION

BALANCED MODULATOR

Perhaps the most commonly used configuration of the AD630 is the balanced modulator. The application resistors provide precise symmetric gains of ±1 and ±2. The ±1 arrangement is shown in Figure 28 and the ±2 arrangement is shown in Figure 29. These cases differ only in the connection of the 10 kΩ feedback resistor (Pin 14) and the compensation capacitor (Pin 12). Note the use of the 2.5 kΩ bias current compensation resistors in these examples. These resistors perform the identical function in the ±1 gain case. Figure 30 demonstrates the performance of the AD630 when used to modulate a 100 kHz square wave carrier with a 10 kHz sinusoid. The result is the double sideband suppressed carrier waveform.

These balanced modulator topologies accept two inputs, a signal (or modulation) input applied to the amplifying channels and a reference (or carrier) input applied to the comparator.

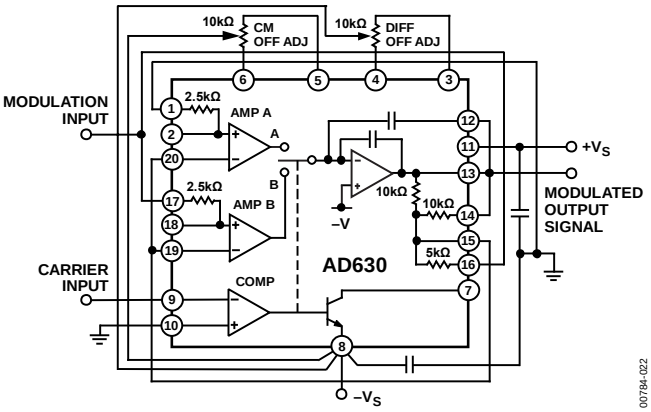


Figure 28. AD630 Configured as a Gain-of-One Balanced Modulator

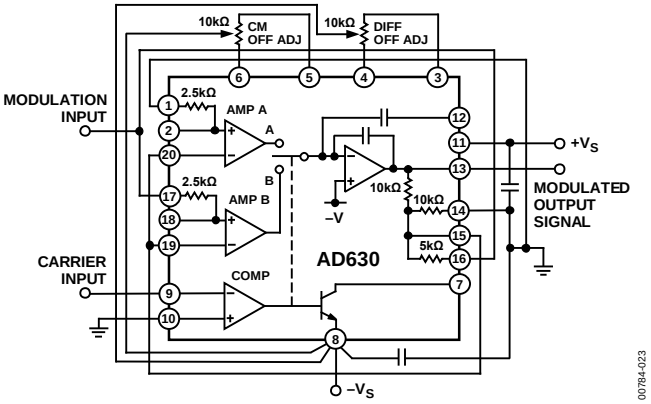


Figure 29. AD630 Configured as a Gain-of-Two Balanced Modulator

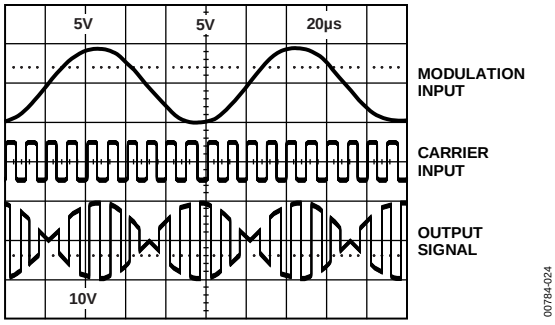


Figure 30. Gain-of-Two Balanced Modulator Sample Waveforms

BALANCED DEMODULATOR

The balanced modulator topology described in the Balanced Modulator section also acts as a balanced demodulator if a double sideband suppressed carrier waveform is applied to the signal input and the carrier signal is applied to the reference input. The output under these circumstances is the baseband modulation signal. Higher order carrier components that can be removed with a low-pass filter are also present. Other names for this function are synchronous demodulation and phase-sensitive detection.

PRECISION PHASE COMPARATOR

The balanced modulator topologies of Figure 28 and Figure 29 can also be used as precision phase comparators. In this case, an ac waveform of a particular frequency is applied to the signal input and a waveform of the same frequency is applied to the reference input. The dc level of the output (obtained by low-pass filtering) is proportional to the signal amplitude and phase difference between the input signals. If the signal amplitude is held constant, the output can be used as a direct indication of the phase. When these input signals are 90° out of phase, they are said to be in quadrature and the AD630 dc output is zero.

PRECISION RECTIFIER ABSOLUTE VALUE

If the input signal is used as its own reference in the balanced modulator topologies, the AD630 acts as a precision rectifier. The high frequency performance is superior to that which can be achieved with diode feedback and op amps. There are no diode drops that the op amp must leap over with the commutating amplifier.

LVDT SIGNAL CONDITIONER

Many transducers function by modulating an ac carrier. A linear variable differential transformer (LVDT) is a transducer of this type. The amplitude of the output signal corresponds to core displacement. Figure 31 shows an accurate synchronous demodulation system, which can be used to produce a dc voltage that corresponds to the LVDT core position. The inherent precision and temperature stability of the AD630 reduce demodulator drift to a second-order effect.

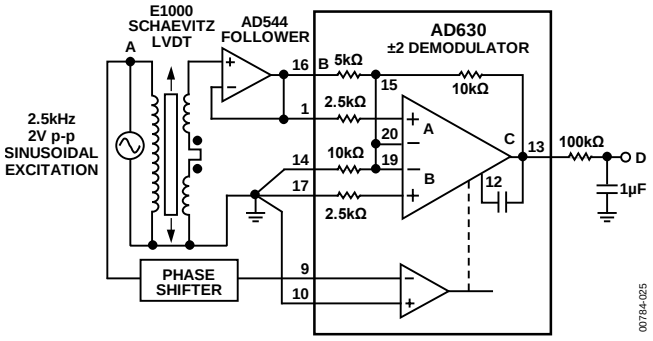


Figure 31. LVDT Signal Conditioner

AC BRIDGE

Bridge circuits that use dc excitation are often plagued by errors caused by thermocouple effects, 1/f noise, dc drifts in the electronics, and line noise pick-up. One way to get around these problems is to excite the bridge with an ac waveform, amplify the bridge output with an ac amplifier, and synchronously demodulate the resulting signal. The ac phase and amplitude information from the bridge is recovered as a dc signal at the output of the synchronous demodulator. The low frequency system noise, dc drifts, and demodulator noise all get mixed to the carrier frequency and can be removed by means of a low-pass filter. Dynamic response of the bridge must be traded off against the amount of attenuation required to adequately suppress these residual carrier components in the selection of the filter.

Figure 33 is an example of an ac bridge system with the AD630 used as a synchronous demodulator. The bridge is excited by a 1 V 400 Hz excitation. Trace A in Figure 32 is the amplified bridge signal. Trace B is the output of the synchronous demodulator and Trace C is the filtered dc system output.

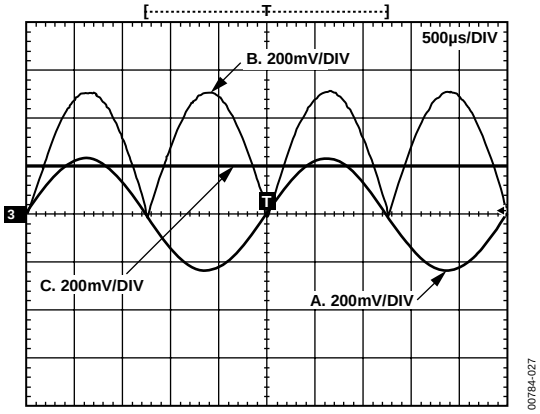


Figure 32. AC Bridge Waveforms (1 V Excitation)

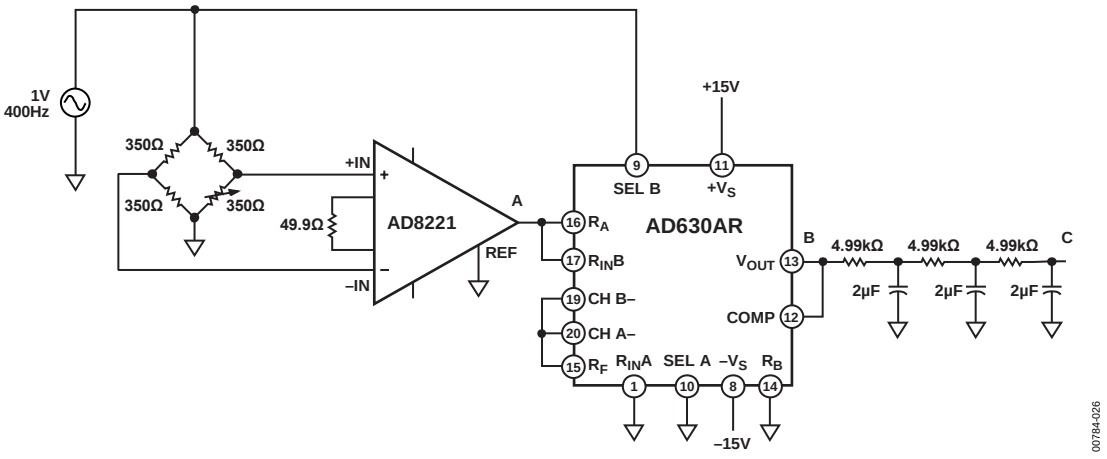


Figure 33. AC Bridge System

LOCK-IN AMPLIFIER APPLICATIONS

Lock-in amplification is a technique used to separate a small, narrow-band signal from interfering noise. The lock-in amplifier acts as a detector and narrow-band filter combined. Very small signals can be detected in the presence of large amounts of uncorrelated noise when the frequency and phase of the desired signal are known.

The lock-in amplifier is basically a synchronous demodulator followed by a low-pass filter. An important measure of performance in a lock-in amplifier is the dynamic range of its demodulator. The schematic diagram of a demonstration circuit which exhibits the dynamic range of an AD630 as it might be used in a lock-in amplifier is shown in Figure 35. Figure 34 is an oscilloscope photo demonstrating the large dynamic range of the AD630. The photo shows the recovery of a signal modulated at 400 Hz from a noise signal approximately 100,000 times larger.

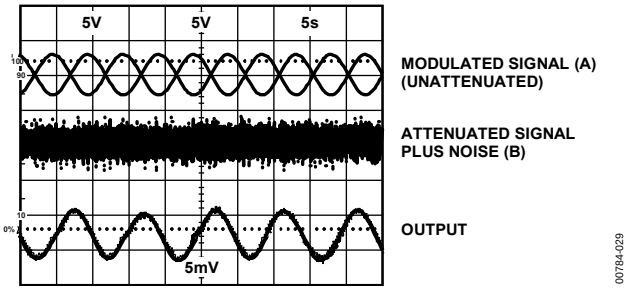


Figure 34. Lock-In Amplifier Waveforms

The test signal is produced by modulating a 400 Hz carrier with a 0.1 Hz sine wave. The signals produced, for example, by chopped radiation (that is, IR, optical) detectors may have similar low frequency components. A sinusoidal modulation is used for clarity of illustration. This signal is produced by a circuit similar to Figure 28 and is shown in the upper trace of Figure 34. It is attenuated 100,000 times normalized to the output, B, of the summing amplifier. A noise signal that might represent, for example, background and detector noise in the chopped radiation case, is added to the modulated signal by the summing amplifier. This signal is simply band limited, clipped white noise. Figure 34 shows the sum of attenuated signal plus noise in the center trace. This combined signal is demodulated synchronously using phase information derived from the modulator, and the result is low-pass filtered using a 2-pole simple filter which also provides a gain of 100 to the output. This recovered signal is the lower trace of Figure 34.

The combined modulated signal and interfering noise used for this illustration is similar to the signals often requiring a lock-in amplifier for detection. The precision input performance of the AD630 provides more than 100 dB of signal range and its dynamic response permits it to be used with carrier frequencies more than two orders of magnitude higher than in this example. A more sophisticated low-pass output filter aids in rejecting wider bandwidth interference.

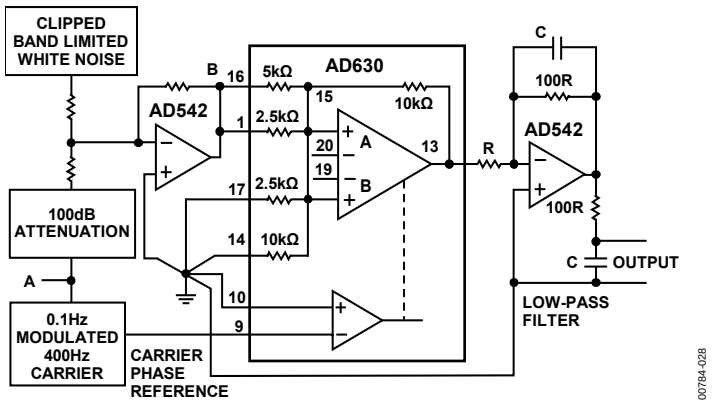
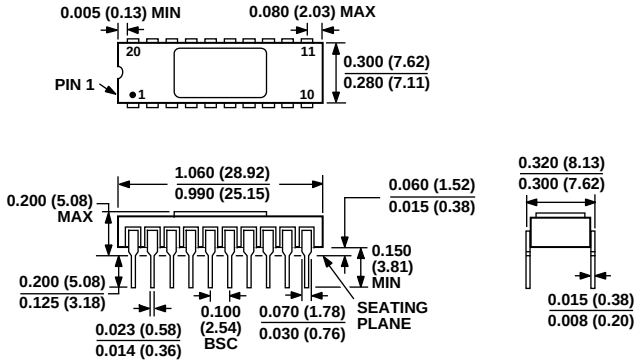


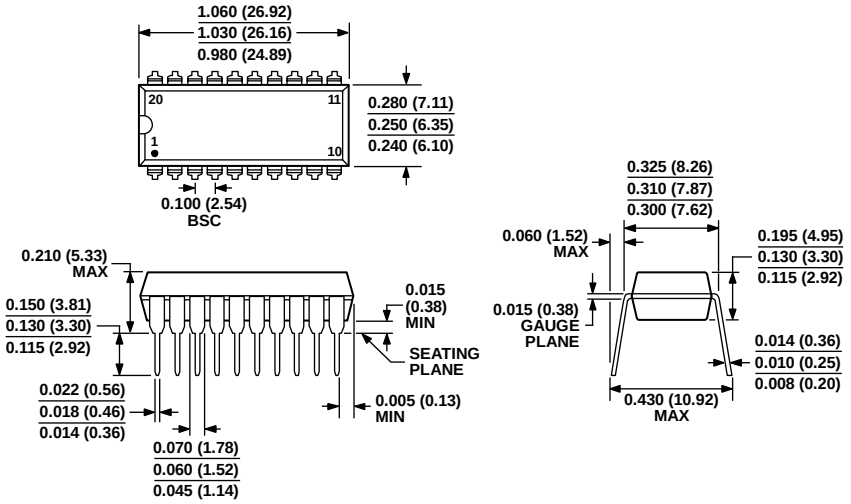
Figure 35. Lock-In Amplifier

OUTLINE DIMENSIONS



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 36. 20-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]
(D-20)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-001

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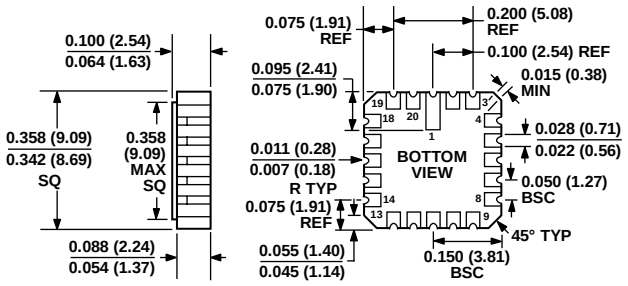
070706-A

Figure 37. 20-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-20)
Dimensions shown in inches and (millimeters)



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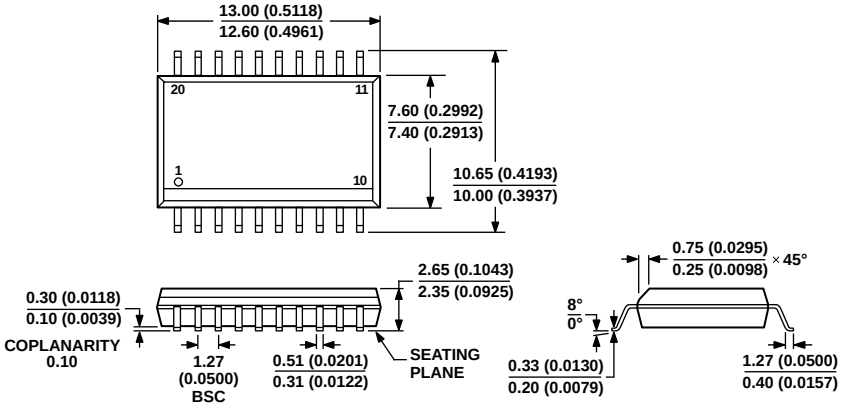
022106-A

Figure 38. 20-Terminal Ceramic Leadless Chip Carrier [LCC]
(E-20-1)
Dimensions shown in inches and (millimeters)



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06-07-2006-A

Figure 39. 20-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-20)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD630JNZ	0°C to 70°C	20-Lead Plastic Dual In-Line Package [PDIP]	N-20
AD630KNZ	0°C to 70°C	20-Lead Plastic Dual In-Line Package [PDIP]	N-20
AD630ARZ	−25°C to +85°C	20-Lead Standard Small Outline Package [SOIC_W]	RW-20
AD630ARZ-RL	−25°C to +85°C	20-Lead Standard Small Outline Package [SOIC_W], 13" Tape and Reel	RW-20
AD630ADZ	−25°C to +85°C	20-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-20
AD630BDZ	−25C to +85°C	20-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-20
AD630SD	−55°C to +125°C	20-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-20
AD630SD/883B	−55°C to +125°C	20-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-20
5962-8980701RA	−55°C to +125°C	20-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-20
AD630SE/883B	−55°C to +125°C	20-Terminal Ceramic Leadless Chip Carrier [LCC]	E-20-1
5962-89807012A	−55°C to +125°C	20-Terminal Ceramic Leadless Chip Carrier [LCC]	E-20-1
AD630SCHIPS	−55°C to +125°C	Chip	

[1] Z = RoHS Compliant Part.