ZL9006M

Digital DC/DC PMBus 6A Power Module

FN7959
Rev 2.00
March 16, 2016

The ZL9006M is a 6A adjustable output, step-down synchronous PMBus-compliant digital power supply. Included in the module is a high-performance digital PWM controller, power MOSFETs, an inductor, and all the passive components required for a highly integrated DC/DC power solution. This power module has built-in auto compensation algorithms, which eliminates the need for manual compensation design work. The ZL9006M operates over a wide input voltage range and supports an output voltage range of 0.6V to 3.6V, which can be set by external resistors or via PMBus. Only bulk input and output capacitors are needed to finish the design. The output voltage can be precisely regulated to as low as 0.6V with ±1% output voltage regulation over line, load and temperature variations.

The ZL9006M functions as a switch mode power supply with added benefits of auto compensation, programmable power management features, parametric monitoring, and status reporting capabilities.

The ZL9006M is packaged in a thermally enhanced, compact (17.2mmx11.45mm) and low profile (2.5mm) overmolded High-Density Array (HDA) package module suitable for automated assembly by standard surface mount equipment. The ZL9006M is RoHS compliant.

Figure 1 represents a typical implementation of the ZL9006M. For PMBus operation, it is recommended to tie the Enable pin (EN) to SGND.

Features

- Complete digital switch mode power supply
- Auto compensating PID filter
- ±1% output voltage accuracy
- External synchronization
- Overcurrent/undercurrent protection
- Output voltage tracking
- Phase interleaving
- Programmable sequencing (delay and ramp time)
- *Snapshot™* parametric capture
- PMBus compliant

Applications

- Server, telecom, and datacom
- Industrial and medical equipment
- General purpose point of load

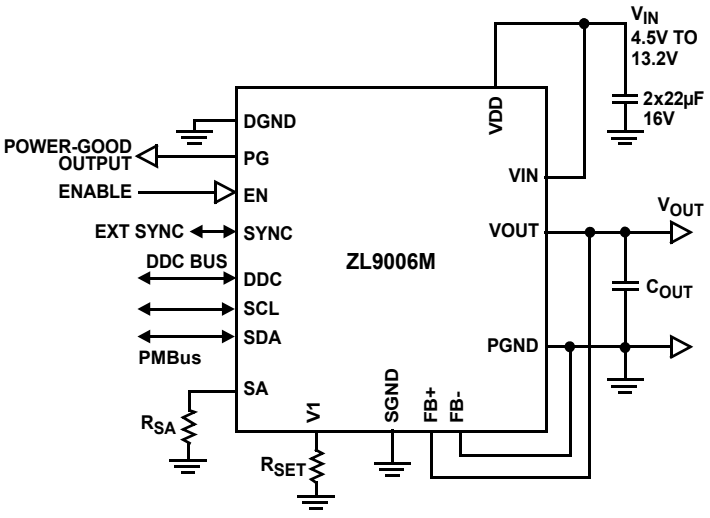
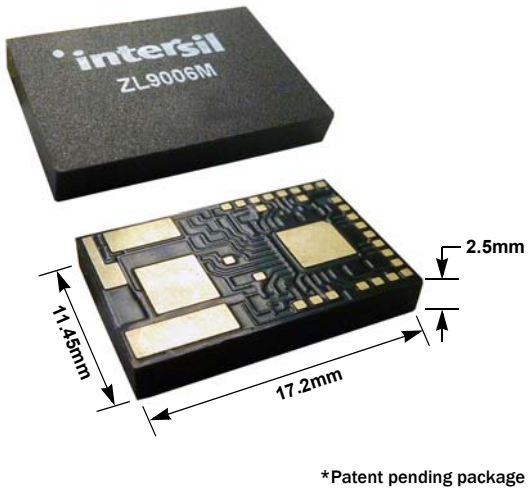


FIGURE 1. TYPICAL APPLICATION CIRCUIT



*Patent pending package

FIGURE 2. SMALL FOOTPRINT PACKAGE WITH LOW PROFILE AT 2.5mm

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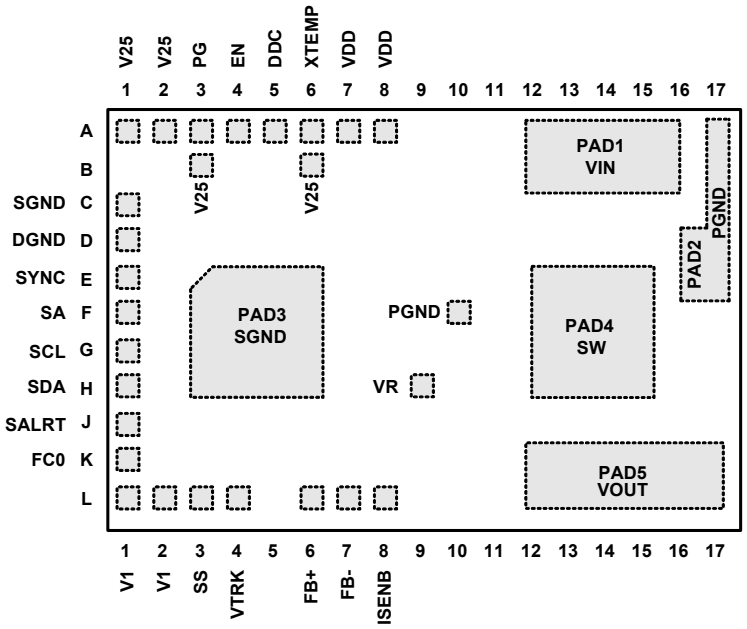
Pin Configuration

ZL9006M
(32 LD HDA)
TOP VIEW



Pin Descriptions

PIN	LABEL	TYPE	DESCRIPTION
A1, A2, B3, B6	V25	PWR	**Internal 2.5V reference.** It is used to power internal circuitry.
A3	PG	O	**Power-good output**. Provide open-drain power-good signal. By default, the PG pin asserts if the output is within +15/-10% of the target voltage. These limits and the polarity of the pin may be changed via the PMBus interface.
A4	EN	I	**Enable input.** This pin is factory set as active high. Pull-up to enable the module switching and pull-down to disable switching. If the module is controlled through PMBus command, tie a 10kΩ resistor from this pin to SGND to avoid this pin floating.
A5	DDC	I/O	**Digital-DC bus** (open drain). The DDC pin on all Digital modules in one application should be connected together. This dedicated bus provides the communication channel between modules for features such as sequencing, fault spreading, and current sharing. A pull-up resistor is required for this application.
A6	XTEMP	I	**External temperature sensor input.** Connect to an external 2N3904 transistor with a diode configuration (see Figure 25 on page 24).
A7, A8	VDD	PWR	**Controller input voltage.** Tie to VIN directly.
C1	SGND	PWR	**Signal ground.** Connect to low impedance ground plane. Refer to "Layout Guide" on page 25.
D1	DGND	PWR	**Digital ground.** Common return for digital signals. Connect to low impedance ground plane. Refer to "Layout Guide" on page 25.
E1	SYNC	I/O	**Clock synchronization.** Used for synchronization to external frequency reference and for setting switching frequency. Refer to Table 7 on page 17.
F1	SA	I	**Serial address select pin.** Used to assign unique PMBus address to each module and phase spreading.
F10	PGND	PWR	**Power ground.** Connect to low impedance ground plane.
G1	SCL	I/O	**Serial clock**. PMBus interface pin.
H1	SDA	I/O	**Serial data**. PMBus interface pin.
H9	VR	PWR	**Internal 5V reference.** Used to power internal drivers. The current limit for the VR pin is 10mA. Please consider this when using the VR pin for driving external circuitry.
J1	SALRT	O	**Serial alert**. PMBus interface pin.

Pin Descriptions (Continued)

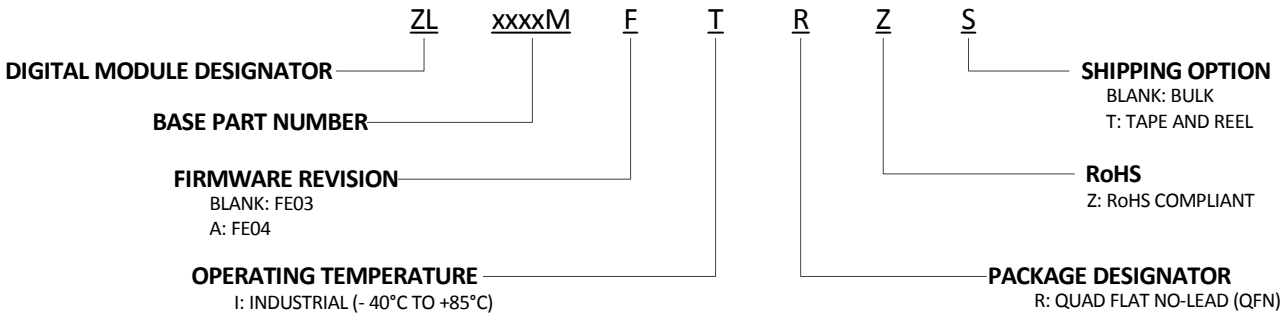
PIN	LABEL	TYPE	DESCRIPTION
K1	FCO	I	**Mode Setting.** Used to set the single-phase/current sharing mode, auto compensation, and SYNC configuration (see Table 9 on page 19).
L1, L2	V1	I	**Output voltage selection pin.** Used to program the output voltage through pin-strap setting or connecting a resistor from the V1 pin to SGND (see Table 4 on page 15). The set voltage on this pin is the maximum allowed output voltage in PMBus programming.
L3	SS	I	**Soft-start pin.** Set SS pin by pin-strapping or connecting a resistor to SGND using the appropriate resistor. The pin can program the delay from when EN is asserted until the output voltage starts to ramp, the output voltage ramp time during turn on/off, and input undervoltage lockout (UVLO) level (see Table on page 17). This pin can also set tracking ratio and upper track limit (see Table 10 on page 21).
L4	VTRK	I	**Tracking sense input.** Used to track an external voltage source.
L6	FB+	I	**Output voltage positive feedback.** Positive inputs of differential remote sense for the regulator. Connect to the output rail or the regulation point of load/processor. This pin is noise sensitive. Please refer to "Layout Guide" on page 25.
L7	FB-	I	**Output voltage negative feedback.** Negative input of the differential remote sense for the regulator. Connect to the negative rail or ground of the load/processor.
L8	ISENB	TEST	**Test pin.** For factory test use. Solder down the pin for mechanical strength, but do not connect the pin.
PAD1	VIN	PWR	**Power inputs.** Input voltage range: 4.5V to 13.2V. Tie directly to the input rail. When the input is between 4.5V to 5.5V, VIN should be tied directly to VCC.
PAD2	PGND	PWR	**Power ground.** Power ground pins for both input and output returns.
PAD3	SGND	PWR	**Signal ground.** Connect to low impedance ground plane (see Figure 26 on page 25).
PAD4	SW	PWR	**Switch node.** Use for monitoring switching frequency. SW pad should be floating or used for snubber connections. To achieve better thermal performance, the SW planes can also be used for heat removal with thermal vias connected to large inner layers (see Figure 26 on page 25).
PAD5	VOUT	PWR	**Power Output.** Apply output load between these pins and PGND pins. Output voltage range: 0.6V to 3.6V.

Ordering Information

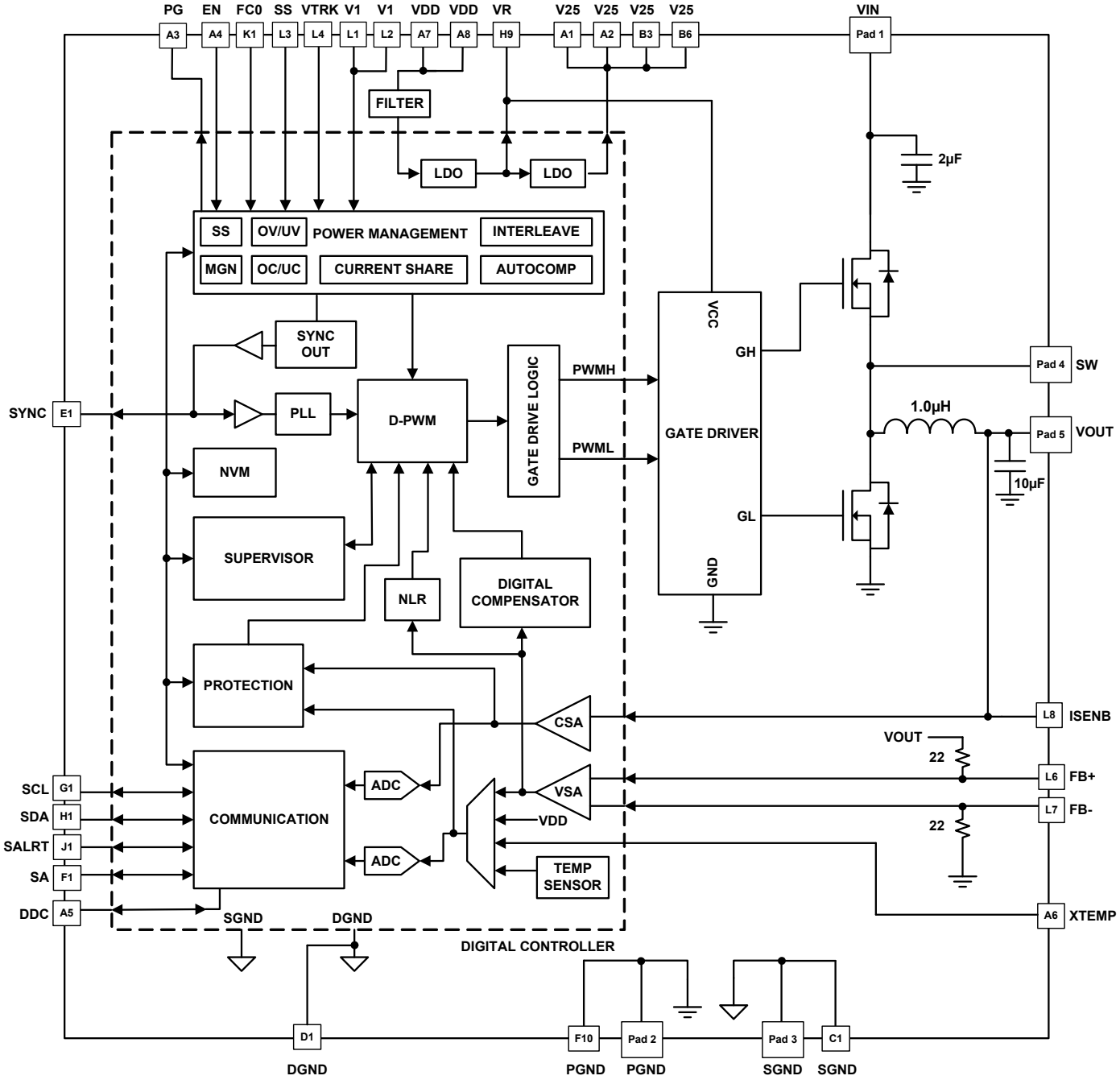
PART NUMBER (Notes 1, 2, 3)	PART MARKING	FIRMWARE REVISION (Note 4)	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ZL9006MIRZ	ZL9006M	FE03	-40 to +85	32 Ld 17.2x11.45 HDA	Y32.17.2x11.45
ZL9006MAIRZ	ZL9006M	FE04	-40 to +85	32 Ld 17.2x11.45 HDA	Y32.17.2x11.45

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil plastic packaged products are RoHS compliant by EU exemption 7C-I and employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish which is compatible with both SnPb and Pb-free soldering operations. Intersil RoHS compliant products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ZL9006M. For more information on MSL please see Tech Brief TB363.
4. See "Firmware Revision History" on page 64; only the latest firmware revision is recommended for new designs.



Pinout Internal Circuit



Absolute Maximum Ratings (Note 5)

DC Supply Voltage for VDD Pin . . . . . -0.3V to 17V
Input Voltage for VIN Pin . . . . . -0.3V to 17V
MOSFET Drive Reference for VR Pin . . . . . -0.3V to 6.5V
2.5V Logic Reference for V25 Pin. . . . . -0.3V to 3V
Logic I/O Voltage for PG, EN, DDC, SYNC,
PG, SCL, SDA, SALRT, FCO, V1, SS Pins . . . . . -0.3V to 6V
Analog Input Voltages XTEMP, VTRK,
FB+, FB-, ISENB Pins . . . . . -0.3V to 6V
Switch Node for SW Pin
Continuous . . . . . (PGND - 0.3V) to 30V
Transient (<100ns). . . . . (PGND - 5V) to 30V
Ground Voltage Differential (DGND - SGND, PGND - SGND)
for DGND, SGND and PGND Pins . . . . . -0.3V to +0.3V
ESD Rating
Human Body Model (Tested per JESD22-A114F). 2000V
Machine Model (Tested per JESD22-A115C) 200V
Charged Device Model (Tested per JESD22-C110D) 1000V
Latch-up (Tested per JESD78C; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
32 Ld HDA Package (Notes 8, 9)	17	1

Storage Temperature . . . . . -55°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Input Supply Voltage Range, V_{IN} . . . . . 4.5V to 13.2V
Input Supply for Controller, V_{DD} (Note 6). . . . . 4.5V to 13.2V
Driver Supply Voltage, VR . . . . . 4.5V to 5.5V
Output Voltage Range, V_{OUT} (Note 7) . . . . . 0.54V to 3.6V
Output Current Range, $I_{OUT(DC)}$ (Note 20). . . . . 0A to 6A
Operating Junction Temperature Range, T_J. . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. Voltage measured with respect to SGND.
6. V_{IN} supplies the power FETs. V_{DD} supplies the controller. V_{IN} can be tied to V_{DD}. For $V_{DD} \leq 5.5V$, V_{DD} should be tied to VR.
7. Includes ±10% margin limits.
8. θ_{JA} is simulated in free air with device mounted on a four-layer FR-4 test board (76.2 x 114.3 x 1.6mm) with 80% coverage, 2oz Cu on top and bottom layers, plus two, buried, one-ounce Cu layers with coverage across the entire test board area. Multiple vias were used, with via diameter = 0.3mm on 1.2mm pitch.
9. For θ_{JC}, the "case" temperature is measured at the center of the package underside.

Electrical Specifications

$V_{IN} = V_{DD} = 12V$, $T_A = -40°C$ to $+85°C$, unless otherwise noted. Typical values are at $T_A = +25°C$. **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

PARAMETER	TEST CONDITIONS	MIN (Note 10)	TYP (Note 11)	MAX (Note 10)	UNITS
INPUT AND SUPPLY CHARACTERISTICS					
Input Bias Supply Current, I_{DD}	$V_{IN} = VDD = 13.2V$, $f_{SW} = 400kHz$, No load	–	35	**45**	mA
Input Bias Shutdown Current, I_{DDS}	EN = 0V, No PMBus activity	–	15.5	**20**	mA
Input Supply Current, I_{VIN}	$V_{IN} = 12V$, $I_{OUT} = 6A$, $V_{OUT} = 1.2V$, $f_{SW} = 400kHz$	–	0.74	–	A
VR Reference Output Voltage (Note 12)	$V_{DD} > 6V$	**4.5**	5.2	**5.7**	V
V25 Reference Output Voltage (Note 12)	$V_R > 3V$	**2.25**	2.5	**2.75**	V
OUTPUT CHARACTERISTICS					
Output Voltage Adjustment Range (Note 12)	$V_{IN} > V_{OUT}$. Does not include margin limits	**0.6**	–	**3.3**	V
Output Voltage Set-point Resolution	Set using resistors. (See Table 1 on page 13)	–	50 - 200	–	mV
	Set using PMBus with temperature compensation applied	–	±0.025	–	% FS
Output Voltage Accuracy (Notes 12, 13)	Includes line, load, temperature	**-1**	–	**1**	%
VSEN Input Bias Current (Note 12)	VSEN = 5.5V	–	110	**200**	µA
Output Load Current (Note 20)	$V_{IN} = 12V$, $V_{OUT} = 1.2V$	–	6	–	A
Peak-to-peak Output Ripple Voltage, ΔV_{OUT} (Note 13)	$I_{OUT} = 6A$, $V_{OUT} = 1.2V$, $C_{OUT} = 1000µF$	–	20	–	mV
Soft-start Delay Duration Range (Notes 12, 14)	Set using SS pin or resistor	**5**	–	**20**	ms
	Set using PMBus	**0.005**	–	**500**	s

Electrical Specifications $V_{IN} = V_{DD}$ = 12V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 10)	TYP (Note 11)	MAX (Note 10)	UNITS
Soft-start Delay Duration Accuracy (Notes 12, 14)	Turn-on delay (Note 16)	-	-0.25/+4	-	ms
	Turn-off delay (Note 16)	-	-0.25/+4	-	ms
Soft-start Ramp Duration Range (Notes 12, 14)	Set using SS pin or resistor	**2**	–	**20**	ms
	Set using PMBus	**0**	–	**200**	ms
Soft-start Ramp Duration Accuracy (Note 12)		–	100	–	µs
DYNAMIC CHARACTERISTICS					
Voltage Change for Positive Load Step	I_{OUT} = 1.2A to 6A, slew rate = 1.6A/µs, V_{OUT} = 1.2V (see Figure 19 on page 12)	–	4	–	%
Voltage Change for Negative Load Step	I_{OUT} = 6A to 1.2A, slew rate = 1.6A/µs, V_{OUT} = 1.2V (see Figure 19 on page 12)	–	4	–	%
OSCILLATOR AND SWITCHING CHARACTERISTICS (Note 12)					
Switching Frequency Range		**300**	–	**1000**	kHz
Switching Frequency Set-point Accuracy	Predefined settings (See Table 1 on page 13)	**-5**	–	**5**	%
Maximum PWM Duty Cycle	Factory setting (Note 19)	-	–	**95**	%
Minimum SYNC Pulse Width		**150**	–	–	ns
Input Clock Frequency Drift Tolerance	External clock source	**-13**	–	**13**	%
LOGIC INPUT/OUTPUT CHARACTERISTICS (Note 12)					
PMBus Speed		–	100	–	kHz
Logic Input Bias Current	EN, PG, SCL, SDA pins	**-10**	–	**10**	µA
Logic Input Low, V_{IL}		–	–	**0.8**	V
Logic Input High, V_{IH}		**2.0**	–	–	V
Logic Output Low, V_{OL}	$I_{OL} \leq$ 4mA (Note 18)	–	–	**0.4**	V
Logic Output High, V_{OH}	$I_{OH} \geq$ -2mA (Note 18)	**2.25**	–	–	V
TRACKING (Note 12)					
VTRK Input Bias Current	VTRK = 5.5V	–	110	**200**	µA
VTRK Tracking Ramp Accuracy	100% Tracking, V_{OUT} -VTRK, no prebias	**-100**	–	**+ 100**	mV
VTRK Regulation Accuracy	100% Tracking, V_{OUT} -VTRK	**-1**	–	**1**	%
FAULT PROTECTION CHARACTERISTICS (Note 12)					
UVLO Threshold Range	Configurable via PMBus	**2.85**	–	**16**	V
UVLO Set-point Accuracy		**-150**	–	**150**	mV
UVLO Hysteresis	Factory setting	–	3	–	%
	Configurable via PMBus	**0**	–	**100**	%
UVLO Delay		–	–	**2.5**	µs
Power-good V_{OUT} Threshold	Factory setting	–	90	–	% V_{OUT}
Power-good V_{OUT} Hysteresis	Factory setting	–	5	–	%
Power-good Delay (Note 17)	Configurable via PMBus	**0**	–	**500**	s
VSEN Undervoltage Threshold	Factory setting	–	85	–	% V_{OUT}
	Configurable via PMBus	**0**	–	**110**	% V_{OUT}

Electrical Specifications $V_{IN} = V_{DD} = 12V$, $T_A = -40°C$ to $+85°C$, unless otherwise noted. Typical values are at $T_A = +25°C$. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 10)	TYP (Note 11)	MAX (Note 10)	UNITS
VSEN Overvoltage Threshold	Factory setting	–	115	–	% V_{OUT}
	Configurable via PMBus	**0**	–	**115**	% V_{OUT}
VSEN Undervoltage Hysteresis		–	5	–	% V_{OUT}
VSEN Undervoltage/Overvoltage Fault Response Time	Factory setting	–	16	–	µs
	Configurable via PMBus	**5**	–	**60**	µs
Thermal Protection Threshold (Controller Junction Temperature)	Factory setting	–	125	–	°C
	Configurable via PMBus	**-40**	–	**125**	°C
Thermal Protection Hysteresis		–	15	–	°C

NOTES:

10. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
11. Parameters with TYP limits are not production tested unless otherwise specified.
12. Parameters are 100% tested for internal controller prior to module assembly.
13. V_{OUT} measured at the termination of the FB+ and FB- sense points.
14. The device requires a delay period following an enable signal and prior to ramping its output.
15. Precise ramp timing mode is only valid when using the EN pin to enable the device rather than PMBus enable.
16. The devices may require up to a 4ms delay following the assertion of the enable signal (normal mode) or following the de-assertion of the enable signal.
17. Factory setting for power-good delay is set to the same value as the soft-start ramp time.
18. Nominal capacitance of logic pins is 5pF.
19. Maximum duty cycle is limited by the equation MAX_DUTY(%) = $[1 - (150 \times 10^{-9} \times f_{SW})] \times 100$ and not to exceed 95%.
20. The load current is related to the thermal derating curves. The maximum allowed current is derated while the output voltage goes higher than 2.5V.

Typical Performance Curves

Operating conditions: T_A = +25°C, No air flow, C_{OUT} = 3 x 100µF + 1 x 330µF. Typical values are used unless otherwise noted.

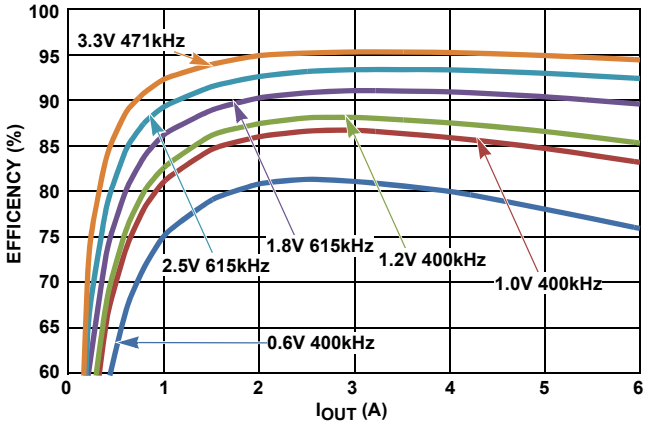


FIGURE 3. ZL9006M EFFICIENCY, V_{IN} = 5V

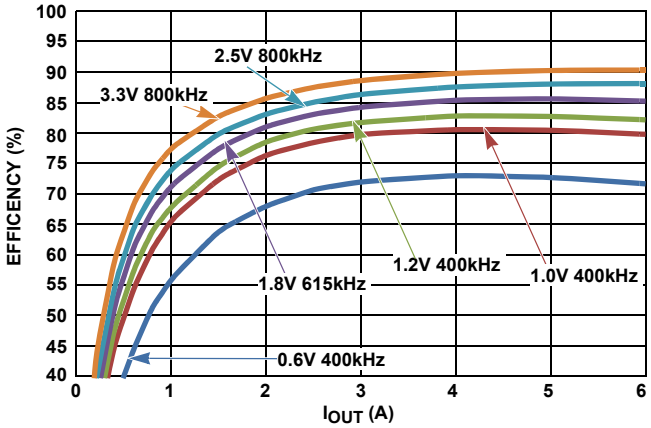


FIGURE 4. ZL9006M EFFICIENCY, V_{IN} = 12V

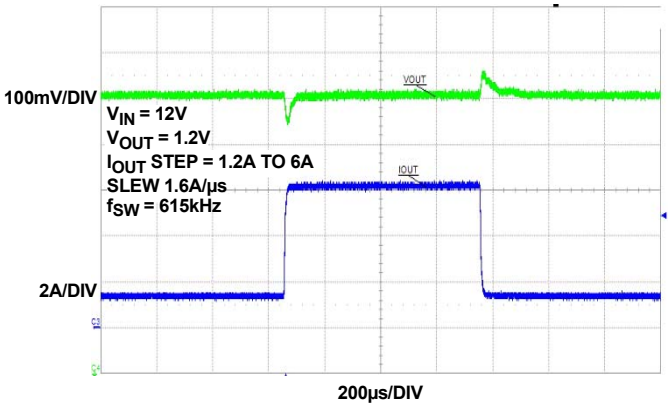


FIGURE 5. V_{OUT} = 1.2V TRANSIENT RESPONSE

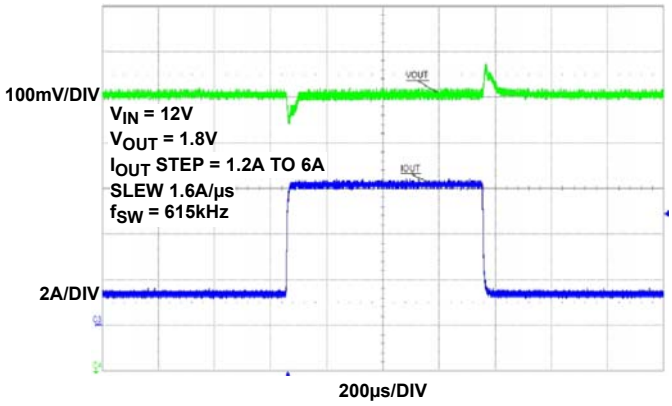


FIGURE 6. V_{OUT} = 1.8V TRANSIENT RESPONSE

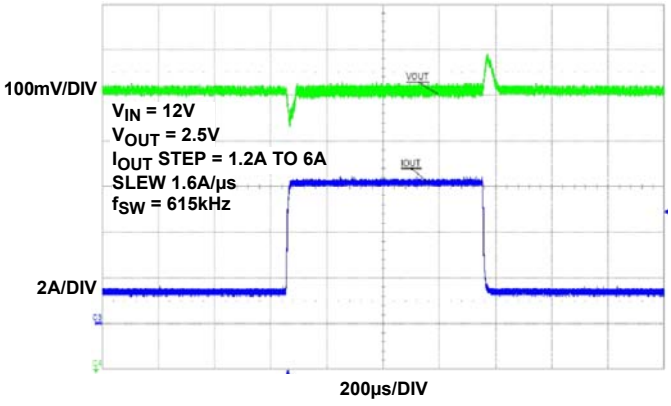


FIGURE 7. V_{OUT} = 2.5V TRANSIENT RESPONSE

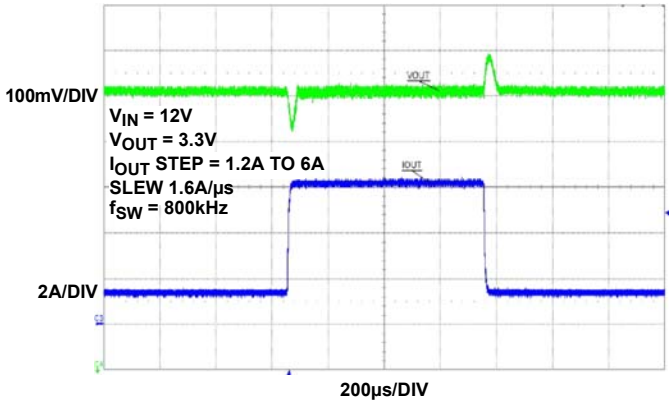


FIGURE 8. V_{OUT} = 3.3V TRANSIENT RESPONSE

Typical Performance Curves

Operating conditions: T_A = +25°C, No air flow, C_{OUT} = 3 x 100µF + 1 x 330µF. Typical values are used unless otherwise noted. **(Continued)**

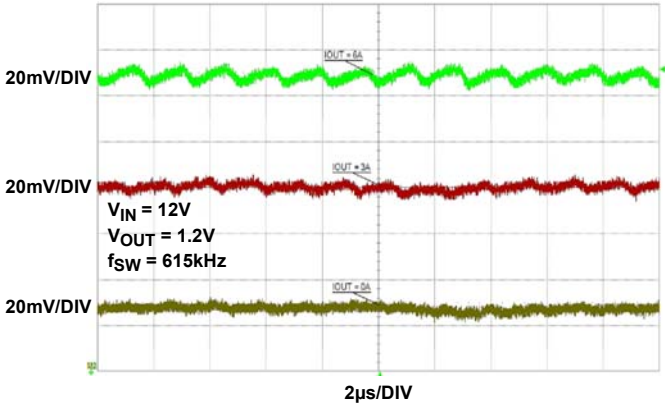


FIGURE 9. V_{OUT} = 1.2V OUTPUT VOLTAGE RIPPLE

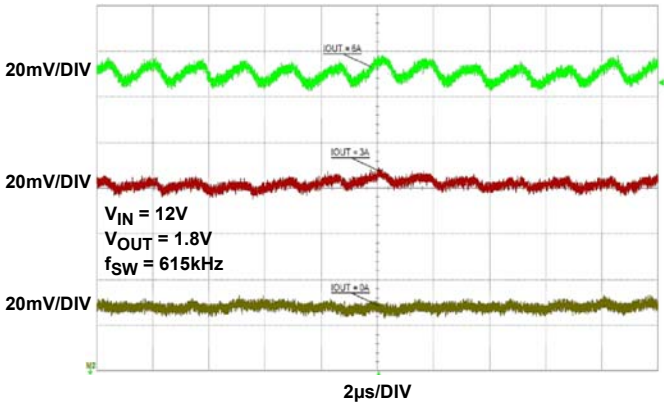


FIGURE 10. V_{OUT} = 1.8V OUTPUT VOLTAGE RIPPLE

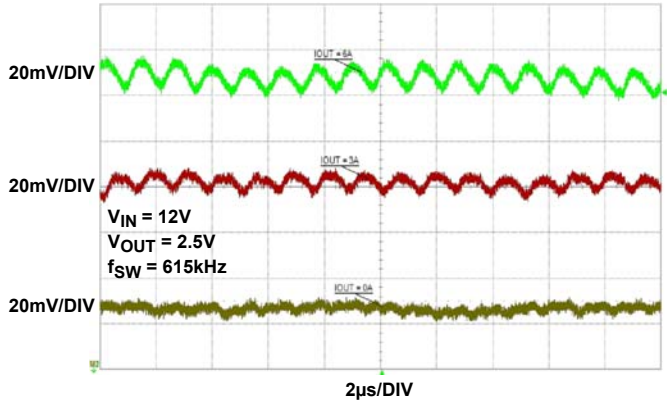


FIGURE 11. V_{OUT} = 2.5V OUTPUT VOLTAGE RIPPLE

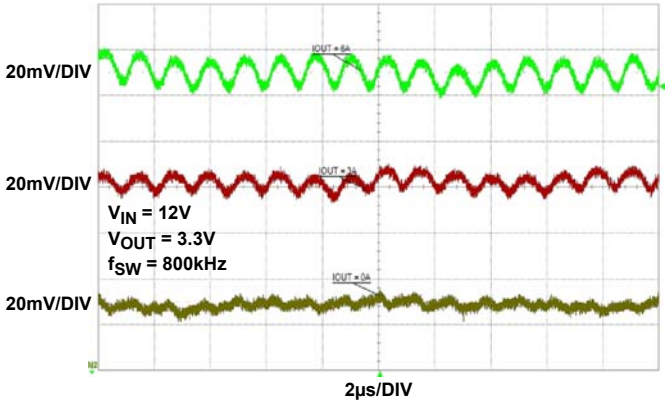


FIGURE 12. V_{OUT} = 3.3V OUTPUT VOLTAGE RIPPLE

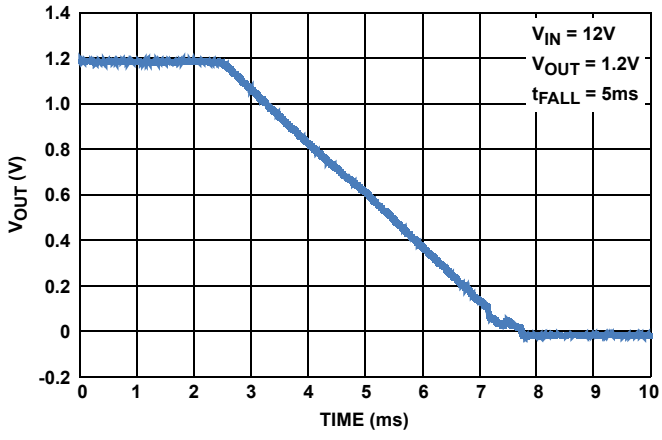


FIGURE 13. SOFT-STOP RAMP-DOWN

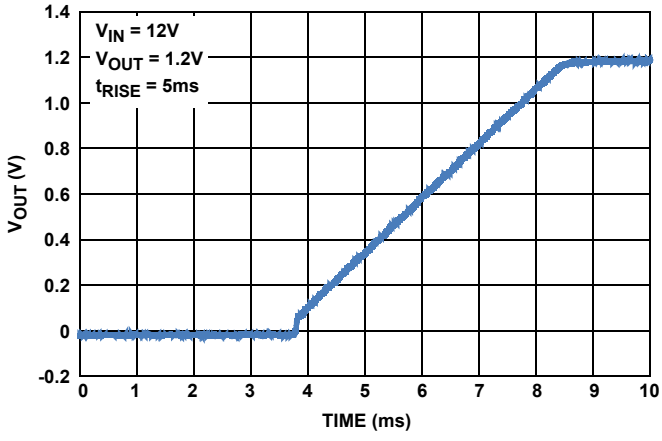


FIGURE 14. SOFT-START RAMP-UP

Derating and Power Loss Curves

Operating conditions: T_A = +25°C, No air flow. f_{SW} corresponds to those used in Efficiency curves. C_{OUT} = 3 x 100µF + 1 x 330µF. Typical values are used unless otherwise noted.

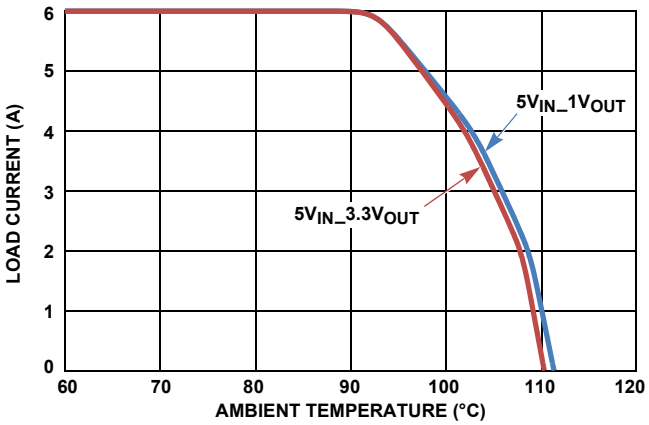


FIGURE 15. DERATING CURVE, $5V_{IN}$ FOR VARIOUS OUTPUT VOLTAGES, NO AIR FLOW

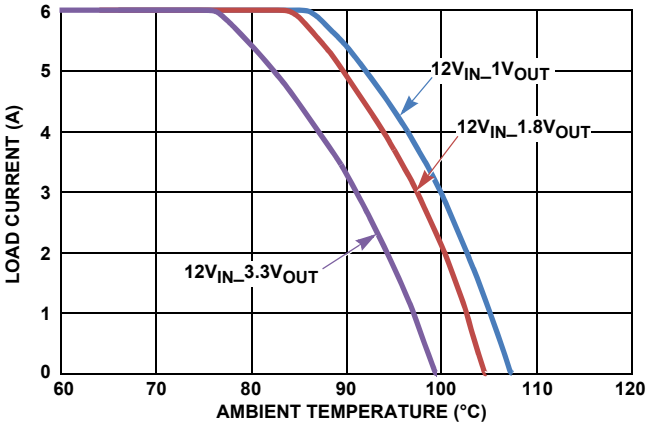


FIGURE 16. DERATING CURVE, $12V_{IN}$ FOR VARIOUS OUTPUT VOLTAGES, NO AIR FLOW

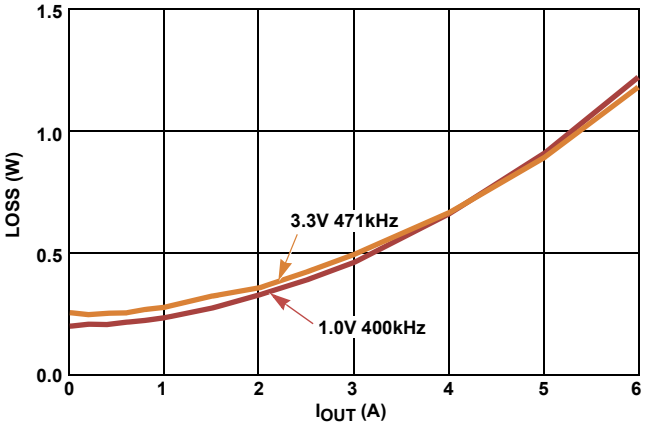


FIGURE 17. POWER LOSS CURVE, $5V_{IN}$ FOR VARIOUS OUTPUT VOLTAGES

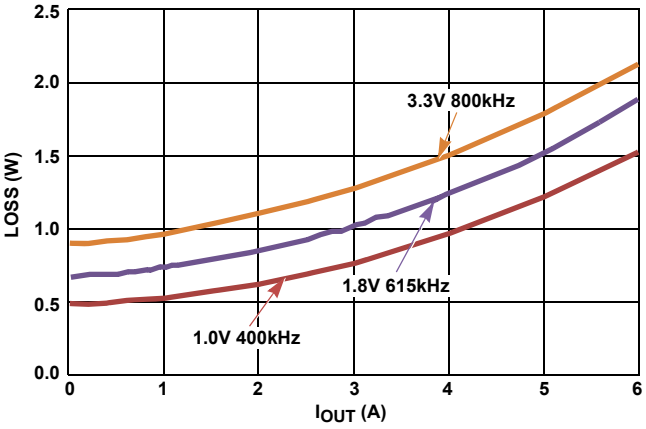


FIGURE 18. POWER LOSS CURVE, $12V_{IN}$ FOR VARIOUS OUTPUT VOLTAGES

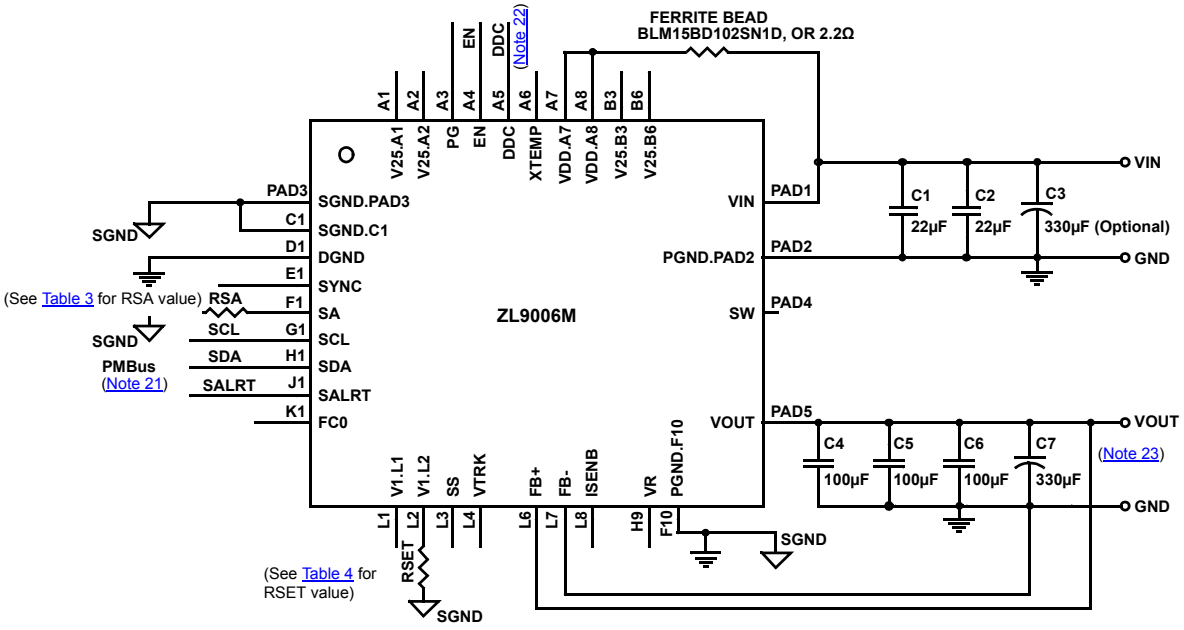


FIGURE 19. TEST CIRCUIT FOR ALL PERFORMANCE AND DERATING CURVES

NOTES:

21. The PMBus requires pull-up resistors. Please refer to the PMBus specifications for more details.
22. The DDC bus requires a pull-up resistor. The resistance will vary based on the capacitive loading of the bus (and on the number of devices connected). The 10kΩ default value, assuming a maximum of 100pF per device, provides the necessary 1µs pull-up rise time. Please refer to "Digital-DC Bus" on page 23 for more details.
23. Additional capacitance may be required to meet specific transient response targets.

Application Information

Internal Bias and Input Voltage Considerations

Beside VIN supplying the main power conversion, the ZL9006M employs two internal low dropout (LDO) regulators to supply bias voltages for internal circuitry allowing it to operate from a single input supply. The internal bias regulators are as indicated in the following:

VR - The VR LDO provides a regulated 5V bias supply for the MOSFET driver circuits. It is powered from the VDD pin.

V25 - The V25 LDO provides a regulated 2.5V bias supply for the main controller circuitry. It is powered from an internal 5V node.

When the input supply (VDD) is higher than 5.5V, the VR pin should not be connected to any other pin. Due to the dropout voltage associated with the VR bias regulator, the VDD pin can be connected to the VR pin for designs operating from a supply below 5.5V. The internal bias regulators are not designed to be outputs for powering other circuitry, so keep current into the VDD pin below 80mA.

Typically, VDD is connected directly to VIN. In the case that VDD is powered separately from VIN, the recommended power sequence is to keep EN low, power VDD, and then VIN. When the voltage is applied to VIN, VDD should also be applied to avoid unintentional turn-on of the internal high-side MOSFET. If the VDD voltage is different from VIN, Prebias start-up and auto compensation may not work correctly as the VDD voltage is used to measure input voltage as part of the Prebias and auto compensation calculation.

Preprogramming Configuration

The Intersil digital power module allows preprogramming before the main power rail is supplied to the VIN pins of the module. If the system bias (i.e., 3.3V bias) is available, the power module can be programmed to load the configuration file or change the settings without main power being on. See Figure 20 for an example with 3.3V bias voltage and 12V input voltage for the main power rail. To preprogram the module without applying power to the VIN pin, the bias voltage 3.3V is applied to pin VR through a Schottky diode such that 3.0 ≤ VR and < VDD when VIN is applied. The body diode of the PMOS will be reverse biased, preventing back feeding to the VIN rail. When the main power rail 12V VIN is ON, the PMOS is ON to supply the power to the module. In this case, only a small voltage is dropped on the PMOS, so the controller can still detect the input voltage accurately. If there are more Intersil digital modules on the board, only one PMOS (as shown in Figure 20) is required to drive the VIN voltages of all modules.

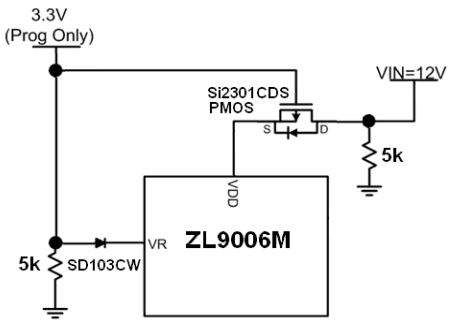


FIGURE 20. PREPROGRAMMING CONFIGURATION

Design Trade-Offs with Switching Frequency

For design of the buck power stage, there is a trade-off when choosing switching frequency to achieve higher power supply efficiency, output ripple, and transient response. For output voltages below 2.0V, a lower switching frequency results in higher efficiency. A lower output ripple and faster transient response is achieved with higher switching frequencies, and thereby can reduce the required amount of output capacitance. Also, given an input to output voltage relation, there is a limitation on the allowable switching frequency due to normal part operation. See "Switching Frequency and PLL" on page 18 for more considerations.

To start the design with a goal of high efficiency, select a frequency based on Table 1. To achieve good transient response, a minimum switching frequency of 615kHz is recommended.

TABLE 1. OPTIMAL SWITCHING FREQUENCY FOR EFFICIENCY

V_O to VIN	3.3V (kHz)	5V (kHz)	12V (kHz)
0.6 - 1.5	300	400	400
1.5 - 2.5	300	615	615
2.5 - 3.6	300	400	800

Completing a Power Supply Design

To achieve a power supply design with digital capabilities using the ZL9006M, only input and output capacitors and two resistors are needed. The two resistors are installed on the SA and V1 pins for setting the PMBus address and output voltage, respectively.

Selection of the Input Capacitor

The input filter capacitor should be based on how much ripple the supply can tolerate on the DC input line. The larger the capacitor, the less ripple expected, but consideration should be taken for the higher surge current during power-up. The ZL9006M provides the soft-start function that controls and limits the current surge. The value of the input capacitor can be calculated by Equation 1:

$$C_{IN(MIN)} = I_O \bullet \frac{D \bullet (1-D)}{V_{P\text{-}P(MAX)} \bullet f_{SW}} \quad \text{(EQ. 1)}$$

Where:

$C_{IN(MIN)}$ is the minimum input capacitance (µF) required
I_O is the output current (A)
D is the duty cycle (V_O/V_{IN})
$V_{P\text{-}P(MAX)}$ is the maximum peak-to-peak voltage (V)
f_{SW} is the switching frequency (Hz)

In addition to the bulk capacitance, some low Equivalent Series Resistance (ESR) ceramic capacitance should be placed as close as possible to decouple between the drain terminal of the high side MOSFET (VIN PAD1) and the source terminal of the low side MOSFET (PGND PAD2). This is used to reduce voltage ringing created by the switching current across parasitic circuit elements. This ripple's (I_{CINrms}) impact should be considered, and can be determined from Equation 2:

$$I_{CINrms} = I_{OUT} \times \sqrt{D \times (1-D)} \quad \text{(EQ. 2)}$$

Without capacitive filtering near the power supply circuit, this current would flow through the supply bus and return planes, coupling noise into other system circuitry. The input capacitors should be rated at 1.2x the ripple current calculated in Equation 2 to avoid overheating of the capacitors due to the high ripple current, which can cause premature failure.

Selection of the Output Capacitors

The ZL9006M is designed for low output voltage ripple. The output voltage ripple and transient requirements can be met with bulk output capacitors (C_{OUT}) with low ESR; the recommended minimum ESR is <6MΩ. C_{OUT} can be a low ESR tantalum capacitor, a low ESR polymer capacitor or a ceramic capacitor.

The typical output capacitance range is from 200µF to 1200µF, and decoupling ceramic output capacitors are used per phase. The optimized output capacitance is 700µF with an ESR of 5mΩ. The maximum recommended product of output capacitance and equivalent ESR value is given by [C_{OUT} x ESR] < 3600 (µF x mΩ).

With a step load faster than 0.2A/µs, the recommended amount of output capacitor is 100µF per ampere of step load. Additional output filtering may be needed if further reduction of output ripple or dynamic transient spikes are required.

Functional Description

Multi-mode Pins

In order to simplify circuit design, the ZL9006M family incorporates patented multi-mode pins that allow the user to easily configure many aspects of the device without programming. Most power management features can be configured using these pins. The multi-mode pins can respond to two types of configurations summarized in Table 2: pin strapping and resistor programming. These pins are sampled when power is applied or by issuing a PMBus RESTORE_FACTORY_ALL command (see "PMBus Commands Description" on page 32).

With pin strapping, parameters can be set by strapping the pins in one of three possible states: LOW, OPEN, or HIGH. These pins can be connected to SGND for logic LOW as this pin provides a voltage lower than 0.8V. For logic OPEN, they have no connection. These pins can be connected to the V25 pin for logic HIGH settings as this pin provides a regulated voltage higher than 2V when power is applied to the VDD pin.

Resistor programming allows a greater range of adjustability when connecting a finite value resistor (in a specified range) between the multi-mode pin and SGND. Standard 1% resistor values are used, and only every fourth standard resistor value is used so the device can reliably recognize the value of resistance

connected to the pin while eliminating the error associated with the resistor accuracy. Up to 31 unique selections are available using a single resistor.

TABLE 2. MULTI-MODE PIN CONFIGURATION

PIN TIED TO	VALUE
LOW (Logic LOW)	<0.8V_{DC}
OPEN (N/C)	No connection
HIGH (Logic HIGH)	>2.0V_{DC}
Resistor to SGND	Set by resistor value

There are five multi-mode pins in ZL9006M: FCO, SA, SYNC, SS and V1. The multi-mode pin configuration can set ZL9006M power management features and mode of operation to both single-phase and current sharing without any programming. SA and V1 are the only two pins that must be set for a general single-phase operation, which use the default settings associated with the other three pins, or overriding other parameters via the PMBus.

SA sets the PMBus address, phase spreading, and Reference/Member assignment in current sharing mode. The effective phase spreading depends on the mode of operation. The Reference/Member is preassigned in current sharing mode, and up to 8 two-phase with 5 three-phase current-shared group is possible.

FCO is used to distinguish between the two modes of operation, and is used in combination with SA in current sharing mode. FCO pin strapping and resistor programming in the range of 10kΩ to 42.2kΩ set the operation to single-phase mode, while the range of 46.4kΩ to 178kΩ is for current sharing mode. FCO also sets the Auto Comp and Sync configuration.

SYNC sets the switching frequency, and is only effective in single-phase mode, as SYNC pins are connected together in current-sharing mode.

SS sets the ramp timing, UVLO, and tracking. V1 sets the output voltage. SS and V1 are the same purpose in single-phase and current-share modes.

PMBus Communications

The ZL9006M provides an PMBus digital interface that enables the user to configure all aspects of the module operation as well as monitor the input and output parameters. The ZL9006M can be used with any PMBus host device. In addition, the module is compatible with PMBus version 2.0 and includes an SALRT line to help mitigate bandwidth limitations related to continuous fault monitoring. Pull-up resistors are required on the PMBus as specified in the PMBus 2.0 specification. The ZL9006M accepts most standard PMBus commands. When controlling the device with PMBus commands, it is recommended that the enable pin be tied to SGND.

The PMBus device address and VOUT_MAX are the only parameters that must be set by external pins. All other device parameters can be set via the PMBus. The device address is set using the SA pin. VOUT_MAX is determined as 10% greater than the voltage set by the V1 pin.

ZL9006M supports 100kHz and 400kHz PMBus clock speed with communication interval of 20ms between STORE and RESTORE commands and ~2ms for other general commands.

PMBus Module Address Selection

Each module must have its own unique serial address to distinguish between other devices on the bus. The module address is set by connecting a resistor between the SA pin and SGND. Table 3 lists the available module addresses.

TABLE 3. PMBus ADDRESS VALUES

R_{SA} (kΩ)	PMBus ADDRESS
LOW	0x23
OPEN	0x24
HIGH	0x25
10	0x50
11	0x51
12.1	0x52
13.3	0x53
14.7	0x54
16.2	0x55
17.8	0x56
19.6	0x57
21.5	0x58
23.7	0x59
26.1	0x5A
28.7	0x5B
31.6	0x5C
34.8	0x5D
38.3	0x5E
42.2	0x5F
46.4	0x60
51.1	0x61
56.2	0x62
61.9	0x63
68.1	0x64
75	0x65
82.5	0x66
90.9	0x67
100	0x68
110	0x69
121	0x6A
133	0x6B
147	0x6C
162	0x6D
178	0x6E

Phase Spreading for a Single-Phase Mode of Operation

When multiple point-of-load converters share a common DC input supply, it is desirable to adjust the clock phase offset of each device such that not all devices start to switch simultaneously. Setting each converter to start its switching cycle at a different point in time can dramatically reduce input capacitance requirements and efficiency losses. Since the peak current drawn from the input supply is effectively spread out over a period of time, the peak current drawn at any given moment is reduced, and the power losses proportional to the I_{RMS}^2 are reduced dramatically.

To enable spreading, all converters must be synchronized to the same switching clock. The FCO pin is used to set the configuration of the SYNC pin for each device as described in "Switching Frequency and PLL" on page 18.

Selecting the phase offset for the device in a standalone mode of operation is accomplished by selecting a device address according to the following equation:

Phase offset = device address x 45°

For example:

- A device address of 0x50 or 0x60 would configure no phase offset
- A device address of 0x51 or 0x61 would configure 45° of phase offset
- A device address of 0x52 or 0x62 would configure 90° of phase offset

The phase offset of each device may also be set to any value between 0° and 360° in 22.5° increments via the PMBus interface. Refer to "PMBus Commands Description" on page 32 for further details.

Output Voltage Selection

The output voltage may be set to a voltage between 0.6V and 3.6V provided that the input voltage is higher than the desired output voltage by an amount sufficient to prevent the device from exceeding its maximum duty cycle specification.

The V1 pins are used to set the output voltage using a single resistor, R_{SET} between the V1 pins and SGND. Table 4 lists the available output voltage settings with a single resistor.

TABLE 4. SINGLE RESISTOR V_{OUT} SETTING

R_{SET} (kΩ)	V_{OUT}
LOW	1.20
OPEN	1.50
HIGH	3.30
10	0.60
11	0.65
12.1	0.70
13.3	0.75
14.7	0.80

TABLE 4. SINGLE RESISTOR V_{OUT} SETTING (Continued)

R_{SET} (kΩ)	V_{OUT}
16.2	0.85
17.8	0.90
19.6	0.95
21.5	1.00
23.7	1.05
26.1	1.10
28.7	1.15
31.6	1.20
34.8	1.25
38.3	1.30
42.2	1.40
46.4	1.50
51.1	1.60
56.2	1.70
61.9	1.80
68.1	1.90
75	2.00
82.5	2.10
90.9	2.20
100	2.30
110	2.50
121	2.80
133	3.00
147	3.30
162	3.60

The output voltage may also be set to any value between 0.6V and 3.6V using a PMBus command over the PMBus interface. See "PMBus Commands Description" on page 32 for details.

The R_{SET} resistors program places an upper limit in output voltage setting through PMBUS programming to 10% above the value set by the resistors.

Start-Up Procedure

The ZL9006M follows a specific internal start-up procedure after power is applied to the VDD pin. Table 5 describes the start-up sequence.

If the device is to be synchronized to an external clock source, the clock frequency must be stable prior to asserting the EN pin. The device requires approximately 5ms to 6ms to check for specific values stored in its internal memory. If the user has stored values in memory, those values will be loaded. The device will then check the status of all multi-mode pins and load the values associated with the pin settings.

Once this process is completed, the device is ready to accept commands via the PMBus interface and the device is ready to be enabled. Once enabled, the device requires a minimum delay period following an enable signal and prior to ramping its output, as described in "Soft-Start Delay and Ramp Times" on page 17. If a soft-start delay period less than the minimum has been configured (using PMBus commands), the device will default to the minimum delay period. If a delay period greater than the minimum is configured, the device will wait for the configured delay period prior to starting to ramp its output.

After the delay period has expired, the output will begin to ramp towards its target voltage according to the preconfigured soft-start ramp time that has been set using the SS pin. It should be noted that if the EN pin is tied to VDD, the device will still require approximately 5ms to 6ms before the output can begin its ramp-up as described in Table 5.

TABLE 5. ZL9006M START-UP SEQUENCE

STEP #	STEP NAME	DESCRIPTION	TIME DURATION
1	Power Applied	Input voltage is applied to the ZL9006M's VDD pin	Depends on input supply ramp time
2	Internal Memory Check	The device will check for values stored in its internal memory. This step is also performed after a Restore command.	Approximately 5ms to 6ms (device will ignore an enable signal or PMBus traffic during this period)
3	Multi-mode Pin Check	The device loads values configured by the multi-mode pins.	
4	Device Ready	The device is ready to accept an enable signal.	-
5	Preramp Delay	The device requires a minimum delay period following an enable signal and prior to ramping its output, as described in "Soft-Start Delay and Ramp Times" on page 17.	-

Soft-Start Delay and Ramp Times

It may be necessary to set a delay when an enable signal is received until the output voltage starts to ramp to its target value. In addition, the designer may wish to precisely set the time required for V_{OUT} to ramp to its target value after the delay period has expired. These features may be used as part of an overall in-rush current management strategy or to precisely control how fast a load IC is turned on. The ZL9006M gives the system designer several options for precisely and independently controlling both the delay and ramp time periods.

The soft-start delay period begins when the EN pin is asserted and ends when the delay time expires. The soft-start ramp timer enables a precisely controlled ramp to the nominal V_{OUT} value that begins once the delay period has expired. The ramp-up is guaranteed monotonic and its slope may be precisely set using the SS pin.

The soft-start delay and ramp times can be set to a custom value by pin-strapping or connecting a resistor from the SS pin to SGND using the appropriate resistor value from Table 6. See "Input Undervoltage Lockout" on page 20 for further explanation of UVLO setting using SS pin. The value of this resistor is measured upon start-up or restore and will not change if the resistor is varied after power has been applied to the ZL9006M.

TABLE 6. SOFT-START PIN-STRAP/RESISTOR SETTINGS

R_{SS} (kΩ)	DELAY TIME (ms)	RAMP TIME (ms)	UVLO (V)
LOW	5	2	4.5
OPEN	5	5	
HIGH	10	10	
10	5	2	3
11	5	5	
12.1	10		
13.3	20		
14.7	5	10	
16.2	10		
17.8	20		
19.6	5	2	4.5
21.5	10		
23.7	5	5	
26.1	10		
28.7	20		
31.6	5	10	
34.8	10		
38.3	20		
42.2	5	2	10.8
46.4	10		
51.1	5	5	
56.2	10		
61.9	20		
68.1	5	10	
75	10		
82.5	20		

With the SS pin OPEN, the default value for delay time and ramp time is 5ms. The soft-start delay and ramp times are set to custom values via the PMBus interface. When the delay time is set to 0ms, the device begins its ramp-up after the internal circuitry has initialized (approximately 2ms). When the soft-start ramp period is set to 0ms, the output ramps up as quickly as the output load capacitance and loop settings allow. It is generally recommended to set the soft-start ramp to a value greater than 500µs to prevent inadvertent fault conditions due to excessive in-rush current.

The ZL9006M has a minimum t_{ON_DELAY} requirement that is a function of the operating mode. Table 7 shows the different mode configurations and the minimum t_{ON_DELAY} required for each mode. Current sharing is configured with the ISHARE_CONFIG PMBus command, auto compensation is configured with the AUTO_COMP_CONFIG command, and Standby Mode is configured as Low Power with the USER_CONFIG command. See "PMBus Commands Description" on page 32 for details. Resistor programming on the SS pin with a delay time of 20ms can be used to satisfied the minimum t_{ON_DELAY} of 15ms.

TABLE 7. MINIMUM t_{ON_DELAY} vs OPERATING MODE

CURRENT SHARING	AUTOCOMP	LOW-POWER STANDBY	MIN. t_{ON_DELAY} (ms)
X	Disabled	False	5
Disabled	Enabled	False	5
Disabled	X	True	10
Enabled	Disabled	True	15
Enabled	Enabled	X	15

Power-Good

The ZL9006M provides a Power-Good (PG) signal that indicates the output voltage is within a specified tolerance of its target level and no fault condition exists. By default, the PG pin asserts if the output is within +15/-10% of the target voltage. These limits and the polarity of the pin may be changed via the PMBus interface. See "PMBus Commands Description" on page 32 for details.

A PG delay period is defined as the time when all conditions within the ZL9006M for asserting PG are met, to when the PG pin is actually asserted. This feature is commonly used instead of using an external reset controller to control external digital logic.

By default, the ZL9006M PG delay is set to 1ms, and may be changed using the PMBus as described in "PMBus Commands Description" on page 32.

By default, the ZL9006M PG delay is set equal to the soft-start ramp time setting. Therefore, if the soft-start ramp time is set to 6ms, the PG delay is set to 6ms. The PG delay may be set independently of the soft-start ramp using the PMBus as described in "PMBus Commands Description" on page 32.

If Auto Comp is enabled, the PG timing is further controlled by the PG assert parameter, as described in "Loop Compensation" on page 19.

Switching Frequency and PLL

The ZL9006M incorporates an internal phase-locked loop (PLL) to clock the internal circuitry. The PLL can be driven by an external clock source connected to the SYNC pin. When using the internal oscillator, the SYNC pin can be configured as a clock source for other Intersil digital devices. With the FCO pin, the SYNC pin can be configured as input, Auto detect, and Output. Pinstrap resistor setting to "input" mode is applicable for member devices used in current sharing mode only.

When multiple modules are used together, connecting the SYNC pins together will force all devices to synchronize with each other. One device must set its SYNC pin as an output and the remaining devices must have their SYNC pins set as Auto Detect.

SYNC AUTO DETECT

In Auto Detect mode, the module will check for a clock signal on the SYNC pin immediately after power-up. In this case, the incoming clock signal must be in the range of 300kHz to 1.0MHz and must be stable within 10µs after V25 rises above 2.25V. If the device is in Low Power Mode, it will check for a clock signal on the SYNC pin immediately after EN goes true. In this case, the incoming clock signal must be in range and stable before EN goes true. If a clock signal is present, the ZL9006M's oscillator will then synchronize with the rising edge of the external clock.

If no incoming clock signal is present, the ZL9006M will configure the switching frequency according to an external resistor, R_{SYNC}, connected between SYNC and SGND using Table 8, given that FCO used pin-strap or has a resistor R_{FCO} in the range of 10kΩ to 13.3kΩ. When FCO is OPEN, or used with resistor settings in the range, the switching frequency of the ZL9006M is set to a default of 615kHz. The module will only read the SYNC pin connection during the first start-up sequence; changes to SYNC pin connections will not affect f_{SW} until the power (VDD) is cycled off and on. Frequency modifications without restarting the VDD power can disable the SYNC auto detect function.

SYNC OUTPUT

When the SYNC pin is configured as an output via PMBus, the device will run from its internal oscillator and will drive the resulting internal oscillator signal onto the SYNC pin so other devices can be synchronized to it. The SYNC pin will not be checked for an incoming clock signal while in this mode.

When FCO is used with resistor settings in the range of 14.7kΩ to 31.6kΩ, the ZL9006M drives the SYNC pin with frequency as described in Table 9, and will ignore any resistor settings on the SYNC pin. Similarly, when FCO is used with a selected value of resistors in the range of 46.4kΩ to 178kΩ, the ZL9006M operates in current sharing mode with the SYNC pin providing clock out.

When FCO is used with resistor settings in the range of 34.8kΩ to 42.2kΩ, ZL9006M will first read the SYNC pin connection, and drives the SYNC pin with the frequency described in Table 8. In this mode, the SYNC pin should not be pin strapped to LOW or HIGH (voltage source). It is recommended to connect a buffer with high impedance, as seen by the SYNC pin of the module providing the clock out, to subsequently drive the SYNC pin of other devices.

SYNC SETTING VIA PMBUS CONSIDERATION

The switching frequency can be set to any value between 300kHz and 1.0MHz using the PMBus interface. The available frequencies below 1.0MHz are defined by f_{SW} = 8MHz/N, where the whole number N is $8 \le N \le 27$.

If a value other than f_{SW} = 8MHz/N is entered using a PMBus command, the internal circuitry will select the valid switching frequency value that is closest to the entered value. For example, if 810kHz is entered, the device will select 800kHz (N = 10).

TABLE 8. SWITCHING FREQUENCY PIN-STRAP/RESISTOR SETTINGS

SYNC PIN/ R_{SYNC} (kΩ)	f_{SW} (kHz)	SYNC PIN/ R_{SYNC} (kΩ)	f_{SW} (kHz)
LOW	400	23.7	471
OPEN	615	26.1	533
HIGH	800	28.7	571
14.7	296	31.6	615
16.2	320	34.8	727
17.8	364	38.3	800
19.6	400	46.4	889
21.5	421	51.1	1000

Loop Compensation

The ZL9006M operates as a voltage-mode synchronous buck controller with a fixed frequency PWM scheme. The module is internally compensated via the PMBus interface. The auto compensation feature measures the characteristics of the power train and calculates the proper tap coefficients, and can be configured according to an external resistor, R_{FCO}, connected between FCO and SGND in Table 9.

If the device is configured to store auto comp values, the calculated compensation values will be saved in the Auto Comp Store and may be read back through the PID_TAPS command. If repeat mode is enabled, the first Auto Comp results after the first ramp will be stored; the values calculated periodically are not stored in the Auto Comp Store. When compensation values are saved in the Auto Comp Store, the device will use those compensation values on subsequent ramps. In repeat mode, the latest Auto Comp results will always be used during operation. Stored Auto Comp results can only be cleared by disabling Auto Comp Store, which is not permitted while the output is enabled. However, sending the AUTOCOMP_CONTROL command while enabled in Store mode will cause the next results to be stored, overwriting previously stored values. If auto compensation is disabled, the device will use the compensation parameters that are stored in the DEFAULT_STORE or USER_STORE.

If the PG assert parameter is set to "Use PG Delay," PG will be asserted according to the POWER_GOOD_DELAY command, after which Auto Comp will begin. When Auto Comp is enabled, the user must not program a Power-Good Delay that will expire before the ramp is finished. If PG assert is set to "After Auto Comp," PG will be asserted immediately after the first Auto Comp cycle completes (POWER_GOOD_DELAY will be ignored).

The routine can be set via the PMBus interface to execute one time after ramp or periodically while regulating, and have either PG assert behavior described earlier. Note that the auto compensation feature requires a minimum t_{ON_DELAY} as described in "Soft-Start Delay and Ramp Times" on page 17.

The Auto Comp Gain control scales the Auto Comp results to allow a trade-off between transient response and steady-state duty cycle jitter. A setting of 100% will provide the fastest transient response while a setting of 10% will produce the lowest jitter.

With resistor settings, auto compensation can only be set to execute one time after ramp with option to store auto comp values. With auto compensation disabled, PG is asserted according to POWER_GOOD_DELAY. With auto compensation executed once and auto comp values not stored, PG is asserted after auto compensation is complete at every start-up event. With auto compensation executed once and auto comp values stored, PG is asserted after auto compensation is complete at the first start-up event, and is asserted according to POWER_GOOD_DELAY for subsequent start-up event along with using the stored auto comp values from the first start-up. By default with FCO OPEN, auto compensation is configured to execute one time after ramp with 70% Auto Comp Gain, PG asserted immediately after the first Auto Comp cycle completes, and auto comp values not stored.

Note that if Auto Comp is enabled, for best results V_{IN} must be stable before Auto Comp begins, as shown in Equation 3.

$$\frac{\Delta Vin}{Vin_{Nom}}(in\%) \leq \frac{100\%}{1+\frac{256 \bullet Vout}{Vin_{Nom}}} \quad \text{(EQ. 3)}$$

The auto compensation function can also be configured via the AUTO_COMP_CONFIG command and controlled using the AUTO_COMP_CONTROL command over the PMBus interface. Please refer to "PMBus Commands Description" on page 32 for further details.

TABLE 9. FCO PIN-STRAP/RESISTOR SETTINGS

FCO PIN/ R_{FCO} (kΩ)	AUTOCOMP CONFIG			SYNC PIN CONFIG	SYNC OVERRIDE
	AC SINGLE/ DISABLE	AC GAIN	STORE VALUES		
LOW	Auto Comp Disabled			Auto Detect	
OPEN	Single	70	Not Stored		
HIGH			Store in Flash		
10	Single	50	Not Stored	Auto Detect	
11			Store in Flash		
12.1		90	Not Stored		
13.3			Store in Flash		
14.7	Auto Comp Disabled			Output	400kHz
16.2	Single	70	Not Stored		
17.8			Store in Flash		
19.6	Auto Comp Disabled				615kHz
21.5	Single	70	Not Stored		
23.7			Store in Flash		
26.1	Auto Comp Disabled				800kHz
28.7	Single	70	Not Stored		
31.6			Store in Flash		
34.8	Auto Comp Disabled				Depend on RSYNC
38.3	Single	70	Not Stored		
42.2			Store in Flash		

Adaptive Diode Emulation

Adaptive diode emulation mode turns off the low-side FET gate drive at low load currents to prevent the inductor current from going negative, reducing the energy losses and increasing overall efficiency. Diode emulation is available to single-phase devices only.

Note: the overall bandwidth of the device may be reduced when in diode emulation mode. Disabling the diode emulation prior to applying significant load steps is recommended.

Input Undervoltage Lockout

The input undervoltage lockout (UVLO) prevents the ZL9006M from operating when the input falls below a preset threshold, indicating the input supply is out of its specified range.

The UVLO threshold (V_{UVLO}) can be set between 2.85V and 16V using the PMBus interface.

Once an input undervoltage fault condition occurs, the device can respond in a number of ways, as follows:

1. Continue operating without interruption.
2. Continue operating for a given delay period, followed by shutdown if the fault still exists. The device remains in shutdown until instructed to restart.
3. Initiate an immediate shutdown until the fault is cleared. The user can select a specific number of retry attempts.

The default response from a UVLO fault is an immediate shutdown of the module. The controller continuously checks for the presence of the fault condition. If the fault condition is no longer present, the ZL9006M is re-enabled.

Output Overvoltage Protection

The ZL9006M offers an internal output overvoltage protection circuit that can be used to protect sensitive load circuitry from being subjected to a voltage higher than its prescribed limits. A hardware comparator is used to compare the actual output voltage (seen at the FB+ pin) to a threshold set to 15% higher than the target output voltage (the default setting). If the FB+ voltage exceeds this threshold, the PG pin deasserts, and the controller can then respond in a number of ways, as follows:

1. Initiate an immediate shutdown until the fault is cleared. The user can select a specific number of retry attempts.
2. Turn off the high-side and turn on the low-side MOSFETs until the device attempts a restart.

The default response from an overvoltage fault is to immediately shut down. The controller continuously checks for the presence of the fault condition, and when the fault condition no longer exists, the device is re-enabled.

For continuous overvoltage protection when operating from an external clock, the only allowed response is an immediate shutdown.

Please refer to "PMBus Commands Description" on page 32 for details on how to select specific overvoltage fault response options via PMBus.

Output Prebias Protection

An output prebias condition exists when an externally applied voltage is present on a power supply's output before the power supply's control IC is enabled. Certain applications require that the converter not be allowed to sink current during start-up if a prebias condition exists at the output. The ZL9006M provides prebias protection by sampling the output voltage prior to initiating an output ramp.

If a prebias voltage lower than the target voltage exists after the preconfigured delay period has expired, the target voltage is set to match the existing prebias voltage, and both drivers are enabled. The output voltage is then ramped to the final regulation value at the preconfigured ramp rate.

The actual time the output takes to ramp from the prebias voltage to the target voltage varies, depending on the prebias voltage, but the total time elapsed from when the delay period expires and when the output reaches its target value will match the preconfigured ramp time (see Figure 21).

If a prebias voltage higher than the target voltage exists after the preconfigured delay period has expired, the target voltage is set to match the existing prebias voltage, and both drivers are enabled with a PWM duty cycle that would ideally create the prebias voltage.

Once the preconfigured soft-start ramp period has expired, the PG pin is asserted (assuming the prebias voltage is not higher than the overvoltage limit). The PWM then adjusts its duty cycle to match the original target voltage, and the output ramps down to the preconfigured output voltage.

If a prebias voltage higher than the overvoltage limit exists, the device does not initiate a turn-on sequence and declares an overvoltage fault condition to exist. In this case, the device responds based on the output overvoltage fault response method that has been selected. See "Output Overvoltage Protection" on page 20 for response options due to an overvoltage condition.

Note that prebias protection is not offered for current sharing groups that also have tracking enabled. V_{DD} must be the same voltage as V_{IN} for proper prebias start-up in single module operation.

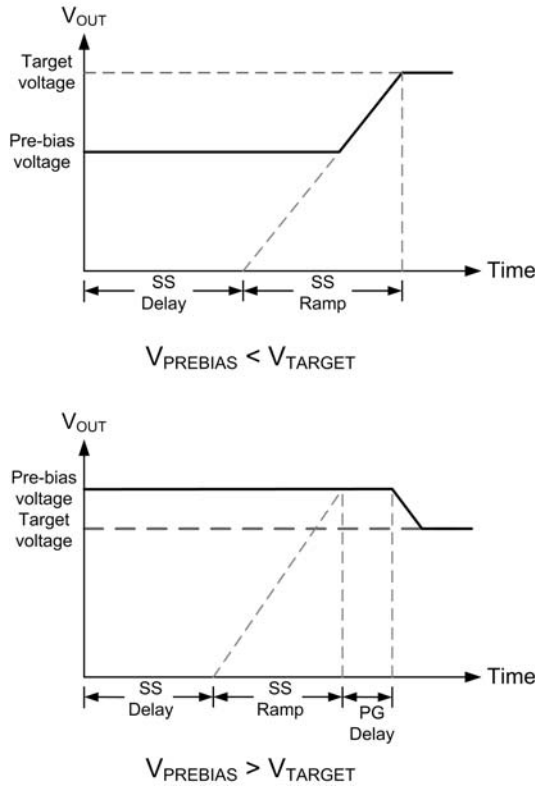


FIGURE 21. OUTPUT RESPONSES TO PREBIAS VOLTAGES

Output Overcurrent Protection

The ZL9006M can protect the power supply from damage if the output is shorted to ground or if an overload condition is imposed on the output. The following overcurrent protection response options are available:

1. Initiate a shutdown and attempt to restart an infinite number of times with a preset delay period between attempts.
2. Initiate a shutdown and attempt to restart a preset number of times with a preset delay period between attempts.
3. Continue operating for a given delay period, followed by shutdown if the fault still exists.
4. Continue operating through the fault (this could result in permanent damage to the power supply).
5. Initiate an immediate shutdown.

The default response from an overcurrent fault is an immediate shutdown of the controller. The controller continuously checks for the presence of the fault condition, and if the fault condition no longer exists, the device is re-enabled.

Please refer to "PMBus Commands Description" on page 32 for details on how to select specific overcurrent fault response options via PMBus.

Thermal Overload Protection

The ZL9006M includes a thermal sensor that continuously measures the internal temperature of the module and shuts down the controller when the temperature exceeds the preset limit. The default temperature limit is set to +125°C in the factory, but the user may set the limit to a different value if desired. See "PMBus Commands Description" on page 32 for details. Note that setting a higher thermal limit via the PMBus interface may result in permanent damage to the controller. Once the module has been disabled due to an internal temperature fault, the user may select one of several fault response options as follows:

1. Initiate a shutdown and attempt to restart an infinite number of times with a preset delay period between attempts.
2. Initiate a shutdown and attempt to restart a preset number of times with a preset delay period between attempts.
3. Continue operating for a given delay period, followed by shutdown if the fault still exists.
4. Continue operating through the fault (this could result in permanent damage to the power supply).
5. Initiate an immediate shutdown.

If the user has configured the module to restart, the controller waits the preset delay period (if configured to do so) and then checks the module temperature. If the temperature has dropped below a threshold that is approximately +15°C lower than the selected temperature fault limit, the controller attempts to restart. If the temperature still exceeds the fault limit, the controller waits the preset delay period and retries again.

The default response from a temperature fault is an immediate shutdown of the module. The controller continuously checks for the fault condition, and once the fault has cleared, the ZL9006M is re-enabled.

Please refer to "PMBus Commands Description" on page 32 for details on how to select specific temperature fault response options via PMBus.

Voltage Tracking

Numerous high performance systems place stringent demands on the order in which the power supply voltages are turned on. This is particularly true when powering FPGAs, ASICs, and other advanced processor devices that require multiple supply voltages to power a single die. In most cases, the I/O interface operates at a higher voltage than the core and therefore the core supply voltage must not exceed the I/O supply voltage according to the manufacturers' specifications. Voltage tracking protects these sensitive ICs by limiting the differential voltage between multiple power supplies during the power-up and power down sequence.

The ZL9006M integrates a lossless tracking scheme that allows its output to track a voltage that is applied to the VTRK pin with no external components required. The VTRK pin is an analog input that, when tracking mode is enabled, configures the voltage applied to the VTRK pin to act as a reference for the device's output regulation. Figure 22 illustrates the typical connection of two tracking modules.

The ZL9006M offers two modes of tracking as follows, and can be configured according to an external resistor, R_{SS}, connected between SS and SGND in Table 10 or via PMBus. The t_{ON_DELAY} time is set to 5ms, and t_{OFF_DELAY} time is set to 35ms. The RAMP time is set to 2ms, but can track to a slower RAMP time, i.e., >2ms.

TABLE 10. TRACKING RESISTOR SETTINGS

R_{SS} (kΩ)	TRACK RATIO (%)	UPPER TRACK LIMIT	RAMP-UP/DOWN BEHAVIOR
90.9	100	Limited by target	Output does not decrease before PG
100			Output always follows VTRK
110		Limited by VTRK	Output does not decrease before PG
121			Output always follows VTRK
133	50	Limited by target	Output does not decrease before PG
147			Output always follows VTRK
162		Limited by VTRK	Output does not decrease before PG
178			Output always follows VTRK

1. **Coincident**. This mode configures the module to ramp its output voltage at the same rate as the voltage applied to the VTRK pin. Two options are available for this mode:
   - Track at 100% V_{OUT} limited. Member rail tracks the reference rail and stops when the member reaches its target voltage (Figure 23A).
   - Track at 100% VTRK limited. Member rail tracks the reference at the instantaneous voltage value applied to the VTRK pin (Figure 23B).

2. **Ratiometric.** This mode configures the module to ramp its output voltage at a rate that is a percentage of the voltage applied to the VTRK pin. The default setting is 50%, but an external resistor string may be used to configure a different tracking ratio:
   - Track at 50% V_{OUT} limited. Member rail tracks the reference rail and stops when the member reaches 50% of the target voltage (Figure 24A).
   - Track at 50% VTRK limited. Member rail tracks the reference at the instantaneous voltage value applied to the VTRK pin until the member rail reaches 50% of the reference rail voltage, or if the member is configured to less than 50% of the reference the member will achieve its configured target (Figure 24B).

The master module device in a tracking group is defined as the device that has the highest target output voltage within the group. This master device will control the ramp rate of all tracking devices and is not configured for tracking mode. A delay of at least 6ms must be configured into the master device, and the user may also configure a specific ramp rate. Any device that is configured for tracking mode will ignore its soft-start delay and its output will take on the turn-on/turn-off characteristics of the reference voltage present at the VTRK pin. All of the ENABLE pins in the tracking group must be connected together and driven by a single logic source. Tracking is configured via the PMBus interface by using the TRACK_CONFIG PMBus command. Please refer to "PMBus Commands Description" on page 32 for further details on configuring tracking mode using PMBus.

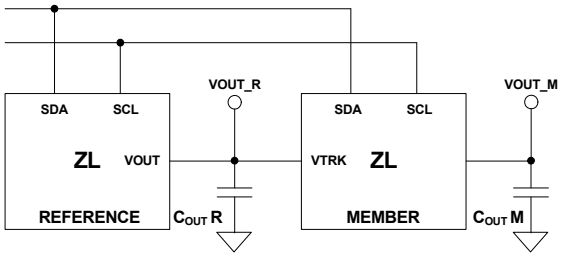


FIGURE 22. PMBus TRACKING CONFIGURATION

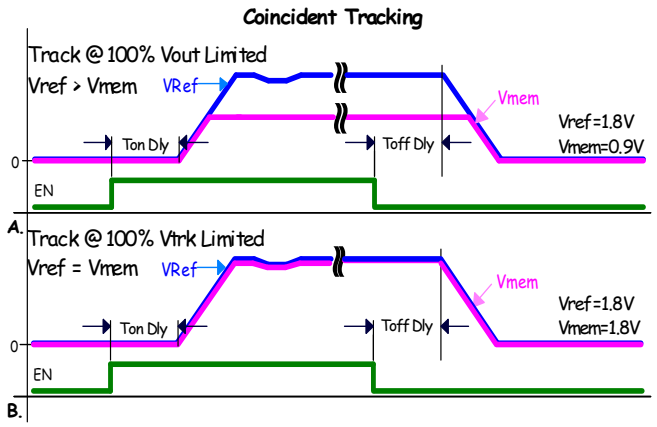


FIGURE 23. COINCIDENT TRACKING

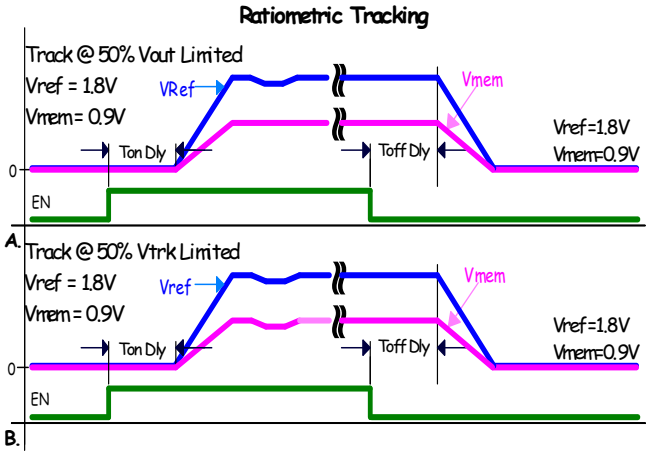


FIGURE 24. RATIOMETRIC TRACKING

When the ZL9006M is configured to the voltage tracking mode, the voltage applied to the VTRK pin acts as a reference for the member device(s) output regulation. When the Auto Compensation algorithm is used the soft-start values (rise/fall times) are used to calculate the loop gain used during the turn-on/turn-off ramps. If current sharing is used, constrain the rise/fall time between 5 and 20ms to ensure current sharing while ramping.

Tracking Groups

In a tracking group, the device configured to the highest voltage within the group is defined as the reference device. The device(s) that track the reference is called member device(s). The reference device will control the ramp delay and ramp rate of all tracking devices and is not placed in the tracking mode. The reference device is configured to the highest output voltage for the group and all other device(s)' output voltages are meant to track and never exceed the reference device output voltage. The reference device must be configured to have a minimum Time-On Delay and Time-On Rise as shown in Equation 4:

$$t_{ON_DLY}(REF) \geq t_{ON_DLY}(MEM) + t_{ON_RISE}(REF) + 5ms \geq t_{ON_DLY}(MEM) + 6ms \quad \text{(EQ. 4)}$$

This delay allows the member device(s) to prepare their control loops for tracking following the assertion of ENABLE.

The member device time-off delay has been redefined to describe the time that the VTRK pin will follow the reference voltage after enable is deasserted. The delay setting sets the timeout for the member's output voltage to turn off in the event that the reference output voltage does not achieve zero volts.

The member device(s) must have a minimum time-off delay of as shown in Equation 5:

$$t_{OFF_DLY}(MEM) \geq t_{OFF_DLY}(REF) + t_{OFF_FALL}(REF) + 5ms \quad \text{(EQ. 5)}$$

All of the ENABLE pins must be connected together and driven by a single logic source or a PMBus Broadcast Enable command may be used.

The configuration settings for Figures 23 and 24 are shown in Tables 11 through 14. In each case the reference and member rise times are set to the same value.

TABLE 11. TRACKING CONFIGURATION (Figure 23A)

RAIL	V_{OUT} (V)	t_{ON} DLY (ms)	t_{ON} RISE (ms)	t_{OFF} DLY (ms)	t_{OFF} FALL (ms)	MODE
Reference	1.8	15	5	5	5	Tracking Disabled
Member	0.9	5	5	15	5	100% V_{OUT} Limited

TABLE 12. TRACKING CONFIGURATION (Figure 23B)

RAIL	V_{OUT} (V)	t_{ON} DLY (ms)	t_{ON} RISE (ms)	t_{OFF} DLY (ms)	t_{OFF} FALL (ms)	MODE
Reference	1.8	15	5	5	5	Tracking Disabled
Member	1.8	5	5	15	5	100% V_{TRK} Limited

TABLE 13. TRACKING CONFIGURATION (Figure 24A)

RAIL	V_{OUT} (V)	t_{ON} DLY (ms)	t_{ON} RISE (ms)	t_{OFF} DLY (ms)	t_{OFF} FALL (ms)	MODE
Reference	1.8	15	5	5	5	Tracking Disabled
Member	0.9	5	5	15	5	50% V_{OUT} Limited

TABLE 14. TRACKING CONFIGURATION (Figure 24B)

RAIL	V_{OUT} (V)	t_{ON} DLY (ms)	t_{ON} RISE (ms)	t_{OFF} DLY (ms)	t_{OFF} FALL (ms)	MODE
Reference	1.8	15	5	5	5	Tracking Disabled
Member	1.8	5	5	15	5	50% V_{TRK} Limited

Voltage Margining

The ZL9006M offers a simple means to vary its output higher or lower than its nominal voltage setting in order to determine whether the load device is capable of operating over its specified supply voltage range. The MGN command is set through the PMBus interface.

The module's output will be forced higher than its nominal set point when the MGN command is set HIGH, and the output will be forced lower than its nominal set point when the MGN command is set LOW. Default margin limits of V_{NOM} ±5% are preloaded in the factory, but the margin limits can be modified through the PMBus interface to as high as V_{NOM} + 10% or as low as 0V, where V_{NOM} is the nominal output voltage set point determined by the V1 pin.

The margin limits and the MGN command can both be set individually through the PMBus interface. Additionally, the transition rate between the nominal output voltage and either margin limit can be configured through the PMBus interface. Please refer to "PMBus Commands Description" on page 32 for further instructions on modifying the margining configurations.

Digital-DC Bus

The Digital-DC Communications (DDC) bus is used to communicate between Intersil Digital-DC modules and devices. This dedicated bus provides the communication channel between devices for features such as sequencing, fault spreading, and current sharing. The DDC pin on all Digital-DC devices in an application should be connected together. A pull-up resistor is required on the DDC bus in order to guarantee the rise time as shown in Equation 6:

$$\text{Rise Time} = R_{PU} * C_{LOAD} \approx 1\mu s \quad \text{(EQ. 6)}$$

where R_{PU} is the DDC bus pull-up resistance and C_{LOAD} is the bus loading. The pull-up resistor may be tied to an external 3.3V or 5V supply as long as this voltage is present prior to or during device power-up. As a rule of thumb, each device connected to the DDC bus presents approximately 10pF of capacitive loading, and each inch of FR4 PCB trace introduces approximately 2pF. The ideal design uses a central pull-up resistor that is well-matched to the total load capacitance. The minimum pull-up resistance should be limited to a value that enables any device to assert the bus to a voltage that ensures a logic 0 (typically 0.8V at the device monitoring point), given the pull-up voltage and the pull-down current capability of the ZL9006M (nominally 4mA).

Output Sequencing

A group of Digital-DC modules or devices may be configured to power-up in a predetermined sequence. This feature is especially useful when powering advanced processors, FPGAs, and ASICs that require one supply to reach its operating voltage prior to another supply reaching its operating voltage in order to avoid latch-up. Multidevice sequencing can be achieved by configuring each device through the PMBus interface.

Multiple device sequencing is configured by issuing PMBus commands to assign the preceding device in the sequencing chain as well as the device that follows in the sequencing chain.

The Enable pins of all devices in a sequencing group must be tied together and driven high to initiate a sequenced turn-on of the group. Enable must be driven low to initiate a sequenced turnoff of the group.

Refer to "PMBus Commands Description" on page 32 for details on sequencing via the PMBus interface.

Fault Spreading

Digital DC modules and devices can be configured to broadcast a fault event over the DDC bus to the other devices in the group. When a nondestructive fault occurs and the device is configured to shut down on a fault, the device shuts down and broadcasts the fault event over the DDC bus. The other devices on the DDC bus shut down together, if configured to do so, and attempt to restart in their prescribed order.

Monitoring Via PMBus

A system controller can monitor a wide variety of different ZL9006M system parameters through the PMBus interface. The device can monitor for fault conditions by monitoring the SALRT pin, which will be pulled low when any number of preconfigured fault conditions occur.

The module can be monitored continuously for any number of power conversion parameters including the following:

- Input voltage
- Output voltage
- Output current
- Internal temperature
- External temperature
- Switching frequency
- Duty cycle

The PMBus host should respond to SALRT as follows:

1. ZL device pulls SALRT low.
2. PMBus host detects that SALRT is now low, performs transmission with Alert Response Address to find which ZL device is pulling SALRT low.
3. PMBus host talks to the ZL device that has pulled SALRT low. The actions that the host performs are up to the system designer.

If multiple devices are faulting, SALRT will still be low after doing the above steps and will require transmission with the Alert Response Address repeatedly until all faults are cleared.

Please refer to "PMBus Commands Description" on page 32 for details on how to monitor specific parameters via the PMBus interface.

Temperature Monitoring Using the XTEMP Pin

The ZL9006M supports measurement of an external device temperature using either a thermal diode integrated in a processor, FPGA or ASIC, or using a discrete diode-connected 2N3904 NPN transistor. Figure 25 illustrates the typical connections required.

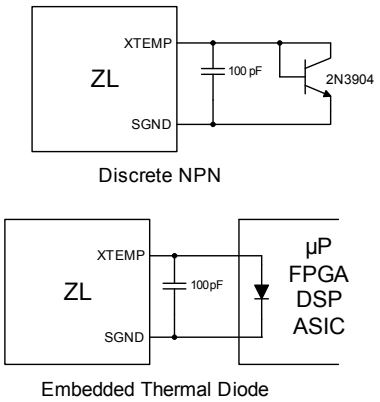


FIGURE 25. EXTERNAL TEMPERATURE MONITORING

SnapShot Parameter Capture

The ZL9006M offers a special feature that enables the user to capture parametric data during normal operation or following a fault. The SnapShot functionality is enabled by setting Bit 1 of MISC_CONFIG command to 1. The SnapShot feature enables the user to read parameters via a block read transfer through the SMBus. This can be done during normal operation, although it should be noted that reading the 32 bytes occupies the SMBus for a period of time.

The SNAPSHOT_CONTROL command enables the user to store the SnapShot parameters to flash memory in response to a pending fault, as well as to read the stored data from flash memory after a fault has occurred. In order to read the stored data from flash memory, two conditions must apply:

1. The module should be disabled.
2. SnapShot mode should be disabled by changing bit 1 of MISC_CONFIG to 0. This is to prevent firmware from updating RAM values after the fault with current values.

Table 15 describes the usage of SNAPSHOT_CONTROL command. Automatic writes to flash memory following a fault are triggered when any fault threshold level is exceeded, provided that the specific fault's response is to shut down (writing to flash memory is not allowed if the device is configured to retry following the specific fault conditions).

TABLE 15. SNAPSHOT_CONTROL COMMAND

DATA VALUE	DESCRIPTION
1	Copies current SNAPSHOT values from flash memory to RAM for immediate access using SNAPSHOT command.
2	Writes current SNAPSHOT values to Flash memory. Only available when device is disabled.

It should be noted that the device's VDD voltage must be maintained during the time when the device is writing the data to flash memory; a process that requires up to 1400µs. Undesirable results may be observed if the device's VDD supply drops below 3.0V during the process.

The following is a recommended procedure for using the SnapShot parameter capture after a fault:

1. Configure the module using config file (optional).
2. Enable the SnapShot mode by setting bit 1 of MISC_CONFIG command to 1. This can be done before or after the module is enabled. Note: do not store MISC_CONFIG: SNAPSHOT setting in default/user store.
3. At this point the module starts capturing operational parameters in RAM for SNAPSHOT, every firmware cycle.
4. The module is configured to capture operational parameters after a fault during operation.
5. After the fault, disable the SnapShot mode by setting bit 1 of MISC_CONFIG command to 0. This is to prevent firmware from updating RAM values after the fault with current values.
6. Disable the module.

7. Send SNAPSHOT_CONTROL command 1 to read the stored data from flash memory into RAM at any time. Issue a SNAPSHOT command to read the data from RAM via SMBus.
8. Repeat step 7 to retrieve SNAPSHOT parameters after a power cycle. It is important to make sure SnapShot mode is disabled in MISC_CONFIG command.

Nonvolatile Memory and Device Security Features

The ZL9006M has internal nonvolatile memory where user configurations are stored. Integrated security measures ensure that the user can only restore the module to a level that has been made available to them.

During the initialization process, the ZL9006M checks for stored values contained in its internal nonvolatile memory. The ZL9006M offers two internal memory storage units that are accessible by the user as follows:

1. Default Store: The ZL9006M has a default configuration that is stored in the default store in the controller. The module can be restored to its default settings by issuing a RESTORE_DEFAULT_ALL command over the PMBus.
2. User Store: The user can modify certain power supply settings as described in this data sheet. The user stores their configuration in the user store.

Please refer to "PMBus Commands Description" on page 32 for details on how to set specific security measures via the PMBus interface.

Layout Guide

To achieve stable operation, low losses, and good thermal performance, some layout considerations are necessary (Figure 26).

- Establish a continuous ground plane connecting the DGND pin and PGND pin F10 with via directly to the ground plane.
- Establish SGND island connecting (Pad 3, Pin C1) and the return path of analog signals and resistor programming pin signals.
- Establish PGND island connecting PGND (Pad 2, 5, Pin F10).
- Make a single point connection between SGND and PGND islands.
- Place a high frequency ceramic capacitor between (1) VIN and PGND (Pad 2) (2) VOUT and PGND (Pad 5) as close to the module as possible to minimize high frequency noise. High frequency ceramic capacitors close to the module between VOUT and PGND will help to minimize noise at the output ripple.
- Use large copper areas for power path (VIN, PGND, VOUT, SW) to minimize conduction loss and thermal stress. Also, use multiple vias to connect the power planes in different layers.
- Connect remote sensed traces FB+ and FB- to the regulation point to achieve a tight output voltage regulation, and keep them in parallel. Route a trace from FB- to a location near the load ground, and a trace from FB+ to the point-of-load where the tight output voltage is desired.
- Avoid routing any sensitive signal traces, such as the VOUT, FB+, FB- sensing point near the SW pad.

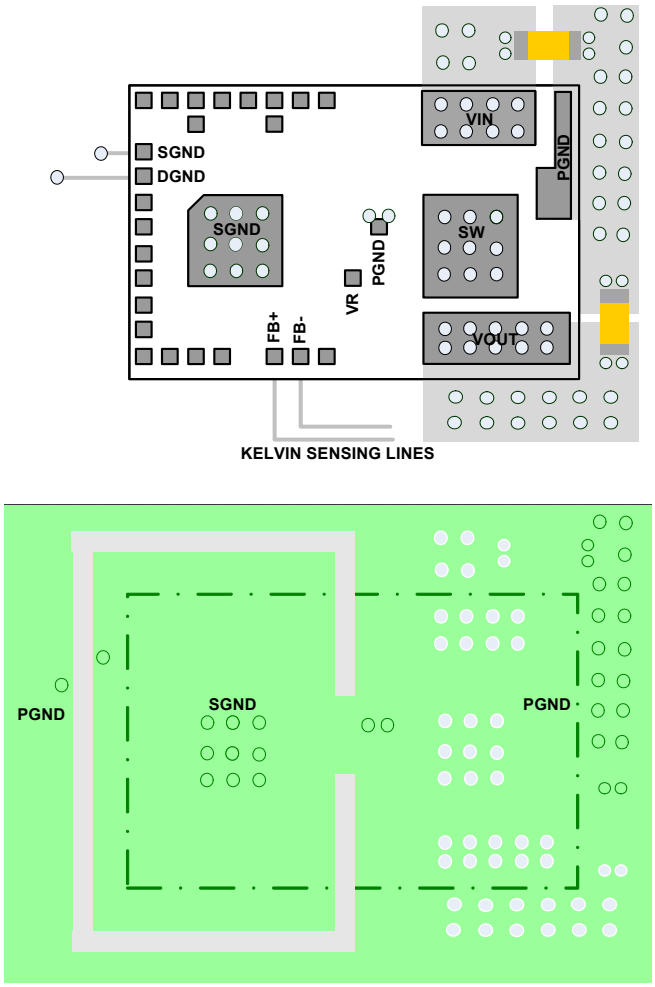


FIGURE 26. RECOMMENDED LAYOUT

Thermal Considerations

Experimental power loss curves along with θ_{JA} from thermal modeling analysis can be used to evaluate the thermal consideration for the module. The derating curves are derived from the maximum power allowed while maintaining the temperature below the maximum junction temperature of +125°C. In actual application, other heat sources and design margin should be considered.

Package Description

The structure of ZL9006M belongs to the High Density Array (HDA) package. This kind of package has advantages, such as good thermal and electrical conductivity, low weight and small size. The HDA package is applicable for surface mounting technology. The ZL9006M contains several types of devices, including resistors, capacitors, inductors and control ICs. The ZL9006M is a copper leadframe based package with exposed copper thermal pads, which have good electrical and thermal conductivity. The copper lead frame and multicomponent assembly is overmolded with polymer mold compound to protect these devices.

The package outline and typical PCB layout pattern design and typical stencil pattern design are shown in the package outline drawing Y32.17.2x11.45 on page 66. The module has a small size of 17.2mm x 11.45mm x 2.5mm. Figure 27 shows typical reflow profile parameters. These guidelines are general design rules. Users could modify parameters according to their application.

PCB Layout Pattern Design

The bottom of the ZL9006M is a leadframe footprint, which is attached to the PCB by surface mounting process. The PCB layout pattern is shown in the Package Outline Drawing Y32.17.2x11.45 on page 66. The PCB layout pattern is essentially 1:1 with the HDA exposed pad and I/O termination dimensions. The thermal lands on the PCB layout should match 1:1 with the package exposed die pads.

Thermal Vias

A grid of 1.0mm to 1.2mm pitch thermal vias, which drops down and connects to buried copper plane(s), should be placed under the thermal land. The vias should be about 0.3mm to 0.33mm in diameter with the barrel plated to about 1.0 ounce copper. Although adding more vias (by decreasing via pitch) will improve the thermal performance, diminishing returns will be seen as more and more vias are added. Simply use as many vias as practical for the thermal land size and your board design rules allow.

Stencil Pattern Design

Reflowed solder joints on the perimeter I/O lands should have about a 50µm to 75µm (2mil to 3mil) standoff height. The solder paste stencil design is the first step in developing optimized, reliable solder joins. Stencil aperture size to land size ratio should typically be 1:1. The aperture width may be reduced slightly to help prevent solder bridging between adjacent I/O lands. To reduce solder paste volume on the larger thermal lands, it is recommended that an array of smaller apertures be used instead of one large aperture. It is recommended that the stencil printing area cover 50% to 80% of the PCB layout pattern. A typical solder stencil pattern is shown in the Package Outline Drawing Y32.17.2x11.45 on page 66. The gap width pad to pad is 0.6mm. The user should consider the symmetry of the whole stencil pattern when designing its pads. A laser cut, stainless steel stencil with electropolished trapezoidal walls is recommended. Electropolishing “smooths” the aperture walls resulting in reduced surface friction and better paste release which reduces voids. Using a trapezoidal section aperture (TSA) also promotes paste release and forms a "brick-like" paste deposit that assists in firm component placement. A 0.1mm to 0.15mm stencil thickness is recommended for this large pitch (1.3mm) HDA.

Reflow Parameters

Due to the low mount height of the HDA, “No Clean” Type 3 solder paste per ANSI/J-STD-005 is recommended. Nitrogen purge is also recommended during reflow. A system board reflow profile depends on the thermal mass of the entire populated board, so it is not practical to define a specific soldering profile just for the HDA. The profile given in Figure 27 is provided as a guideline, to be customized for varying manufacturing practices and applications.

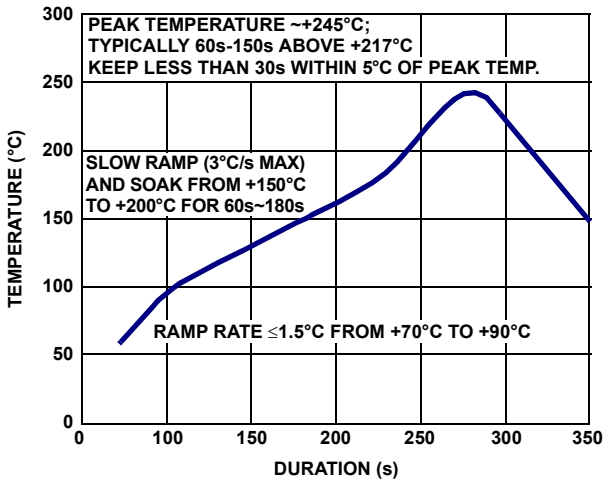


FIGURE 27. TYPICAL REFLOW PROFILE

PMBus Command Summary

COMMAND CODE	COMMAND NAME	DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE	DEFAULT SETTING	PAGE
01h	OPERATION	Sets Enable, Disable and VOUT margin modes.	R/W BYTE	BIT			page 32
02h	ON_OFF_CONFIG	Configures device to enable from EN pin or OPERATION command.	R/W BYTE	BIT	16h	Pin Enable Soft Off	page 33
03h	CLEAR_FAULTS	Clears fault indications.	SEND BYTE				page 33
11h	STORE_DEFAULT_ALL	Stores all PMBus values written since last restore at default level.	SEND BYTE				page 33
12h	RESTORE_DEFAULT_ALL	Restores PMBus settings that were stored at default level.	SEND BYTE				page 34
15h	STORE_USER_ALL	Stores all PMBus values written since last restore at user level.	SEND BYTE				page 34
16h	RESTORE_USER_ALL	Restores PMBus settings that were stored in user level.	SEND BYTE				page 34
20h	VOUT_MODE	Preset to defined data format of VOUT commands.	READ BYTE	BIT	13h	Linear Mode, Exponent = -13	page 34
21h	VOUT_COMMAND	Sets the nominal value of VOUT.	R/W WORD	L16u		Pin Strap	page 34
22h	VOUT_TRIM	Sets trim value of VOUT.	R/W WORD	L16s	0000h	0V	page 35
23h	VOUT_CAL_OFFSET	Applies a fixed offset voltage to the VOUT_COMMAND.	R/W WORD	L16s	0000h	0V	page 35
24h	VOUT_MAX	Sets the maximum possible value of VOUT.	R/W WORD	L16u		1.1*VOUT Pin Strap	page 35
25h	VOUT_MARGIN_HIGH	Sets the value of the VOUT during a margin high.	R/W WORD	L16u		1.05*VOUT Pin Strap	page 35
26h	VOUT_MARGIN_LOW	Sets the value of the VOUT during a margin low.	R/W WORD	L16u		0.95*VOUT Pin Strap	page 35
27h	VOUT_TRANSITION_RATE	Sets the transition rate during margin or other change of VOUT.	R/W WORD	L11	BA00h	1V/ms	page 36
28h	VOUT_DROOP	Sets the loadline (V/I Slope) resistance for the rail.	R/W WORD	L11	0000h	0mV/A	page 36
32h	MAX_DUTY	Sets the maximum allowable duty cycle.	R/W WORD	L11	EAD6h	90.75%	page 36
33h	FREQUENCY_SWITCH	Sets the switching frequency.	R/W WORD	L11		Pin Strap	page 36
37h	INTERLEAVE	Configures a phase offset between devices sharing a SYNC clock.	R/W WORD	BIT		Based on PMBus address	page 37
38h	IOUT_CAL_GAIN	Sense resistance for inductor DCR current sensing.	R/W WORD	L11	C2EEh	2.93mV/A	page 37
39h	IOUT_CAL_OFFSET	Sets the current-sense offset.	R/W WORD	L11	B667h	-0.4A	page 37
40h	VOUT_OV_FAULT_LIMIT	Sets the VOUT overvoltage fault threshold.	R/W WORD	L16u		1.15*VOUT Pin Strap	page 37
41h	VOUT_OV_FAULT_RESPONSE	Configures the VOUT overvoltage fault response.	R/W BYTE	BIT	80h	Disable and no retry	page 38
44h	VOUT_UV_FAULT_LIMIT	Sets the VOUT undervoltage fault threshold.	R/W WORD	L16u		0.8*VOUT Pin Strap	page 38
45h	VOUT_UV_FAULT_RESPONSE	Configures the VOUT undervoltage fault response.	R/W BYTE	BIT	80h	Disable and no retry	page 39

PMBus Command Summary (Continued)

COMMAND CODE	COMMAND NAME	DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE	DEFAULT SETTING	PAGE
46h	IOUT_OC_FAULT_LIMIT	Sets the IOUT average overcurrent fault threshold.	R/W WORD	L11	D340h	13A	page 39
4Bh	IOUT_UC_FAULT_LIMIT	Sets the IOUT average undercurrent fault threshold.	R/W WORD	L11	D4C0h	-13A	page 39
4Fh	OT_FAULT_LIMIT	Sets the over-temperature fault threshold.	R/W WORD	L11	EBE8h	+125°C	page 40
50h	OT_FAULT_RESPONSE	Configures the over-temperature fault response.	R/W BYTE	BIT	80h	Disable and no retry	page 40
51h	OT_WARN_LIMIT	Sets the over-temperature warning limit.	R/W WORD	L11	EB70h	+110°C	page 40
52h	UT_WARN_LIMIT	Sets the under-temperature warning limit.	R/W WORD	L11	E580h	-40°C	page 41
53h	UT_FAULT_LIMIT	Sets the under-temperature fault threshold.	R/W WORD	L11	E490h	-55°C	page 41
54h	UT_FAULT_RESPONSE	Configures the under-temperature fault response.	R/W BYTE	BIT	80h	Disable and no retry	page 41
55h	VIN__OV_FAULT_LIMIT	Sets the VIN overvoltage fault threshold.	R/W WORD	L11	D3A0h	14.5V	page 41
56h	VIN__OV_FAULT_RESPONSE	Configures the VIN overvoltage fault response.	R/W BYTE	BIT	80h	Disable and no retry	page 42
57h	VIN__OV_WARN_LIMIT	Sets the VIN overvoltage warning limit.	R/W WORD	L11	D360h	14.0V	page 42
58h	VIN_UV_WARN_LIMIT	Sets the VIN undervoltage warning limit.	R/W WORD	L11	CA40h	4.5V	page 42
59h	VIN_UV_FAULT_LIMIT	Sets the VIN undervoltage fault threshold.	R/W WORD	L11	CA00h	4.0V	page 43
5Ah	VIN_UV_FAULT_RESPONSE	Configures the VIN undervoltage fault response.	R/W BYTE	BIT	80h	Disable and no retry	page 43
5Eh	POWER_GOOD_ON	Sets the voltage threshold for power-good indication.	R/W WORD	L16u		0.9*VOUT Pin Strap	page 43
60h	TON_DELAY	Sets the delay time from ENABLE to start of VOUT rise.	R/W WORD	L11	CA80h	5ms	page 43
61h	TON_RISE	Sets the rise time of VOUT after ENABLE and TON_DELAY.	R/W WORD	L11	CA80h	5ms	page 44
64h	TOFF_DELAY	Sets the delay time from DISABLE to start of VOUT fall.	R/W WORD	L11	CA80h	5ms	page 44
65h	TOFF_FALL	Sets the fall time for VOUT after DISABLE and TOFF_DELAY.	R/W WORD	L11	CA80h	5ms	page 44
78h	STATUS_BYTE	Summary of most critical faults.	READ BYTE	BIT	00h	No Faults	page 44
79h	STATUS_WORD	Summary of critical faults.	READ WORD	BIT	0000h	No Faults	page 45
7Ah	STATUS_VOUT	Reports VOUT warnings/faults.	READ BYTE	BIT	00h	No Faults	page 45
7Bh	STATUS_IOUT	Reports IOUT warnings/faults.	READ BYTE	BIT	00h	No Faults	page 46
7Ch	STATUS_INPUT	Reports INPUT warnings/faults.	READ BYTE	BIT	00h	No Faults	page 46
7Dh	STATUS_TEMPERATURE	Reports temperature warnings/faults.	READ BYTE	BIT	00h	No Faults	page 46

PMBus Command Summary (Continued)

COMMAND CODE	COMMAND NAME	DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE	DEFAULT SETTING	PAGE
7Eh	STATUS_CML	Reports communication, memory, logic errors.	READ BYTE	BIT	00h	No Faults	page 47
80h	STATUS_MFR_SPECIFIC	Reports voltage monitoring/clock sync faults.	READ BYTE	BIT	00h	No Faults	page 47
88h	READ_VIN	Reports input voltage measurement.	READ WORD	L11			page 47
8Bh	READ_VOUT	Reports output voltage measurement.	READ WORD	L16u			page 48
8Ch	READ_IOUT	Reports output current measurement.	READ WORD	L11			page 48
8Dh	READ_TEMPERATURE_1	Reports temperature reading internal to the device.	READ WORD	L11			page 48
8Eh	READ_TEMPERATURE_2	Reports temperature reading external to the device.	READ WORD	L11			page 48
94h	READ_DUTY_CYCLE	Reports actual duty cycle.	READ WORD	L11			page 48
95h	READ_FREQUENCY	Reports actual switching frequency.	READ WORD	L11			page 48
98h	PMBUS_REVISION	Returns the revision of the PMBus.	READ BYTE	HEX			page 48
99h	MFR_ID	Sets a user defined identification.	R/W BLOCK	ASC		<null>	page 49
9Ah	MFR_MODEL	Sets a user defined model.	R/W BLOCK	ASC		<null>	page 49
9Bh	MFR_REVISION	Sets a user defined revision.	R/W BLOCK	ASC		<null>	page 49
9Ch	MFR_LOCATION	Sets a user defined location identifier.	R/W BLOCK	ASC		<null>	page 49
9Dh	MFR_DATE	Sets a user defined date.	R/W BLOCK	ASC		<null>	page 49
9Eh	MFR_SERIAL	Sets a user defined serialized identifier.	R/W BLOCK	ASC		<null>	page 50
B0h	USER_DATA_00	Sets a user defined data.	R/W BLOCK	ASC		<null>	page 50
BCh	AUTO_COMP_CONFIG	Configures the auto compensation features.	R/W BYTE	CUS	69h	Auto Comp enabled gain = 70%	page 50
BDh	AUTO_COMP_CONTROL	Causes the auto comp algorithm to initiate.	Send BYTE				page 50
BFh	DEADTIME_MAX	Sets the maximum deadtime values.	R/W WORD	CUS	3838h	H-L = 56ns L-H = 56ns	page 51
D0h	MFR_CONFIG	Configures several manufacturer-level features.	R/W WORD	BIT	6A11h	Refer to description	page 51
D1h	USER_CONFIG	Configures several user-level features.	R/W WORD	BIT	2011h	Refer to description	page 52
D2h	ISHARE_CONFIG	Configures the device for current sharing communication.	R/W WORD	BIT	0000h	Current share disabled	page 53
D3h	DDC_CONFIG	Configures the DDC bus.	R/W WORD	BIT	0001h	Set Based on PMBus Address	page 53
D4h	POWER_GOOD_DELAY	Sets the delay PG threshold and asserting the PG pin.	R/W WORD	L11	BA00h	1ms	page 53
D5h	PID_TAPS	Configures control loop compensator coefficients.	R/W BLOCK	CUS		Calculated by Auto Comp	page 54

PMBus Command Summary (Continued)

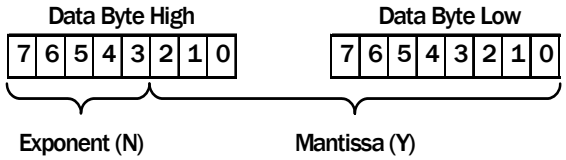
COMMAND CODE	COMMAND NAME	DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE	DEFAULT SETTING	PAGE
D6h	INDUCTOR	Informs the device of circuit's inductor value.	R/W WORD	L11	BA00h	1µH	page 54
D7h	NLR_CONFIG	Configures the nonlinear response control parameters.	R/W BLOCK	BIT	00000000h	Refer to description	page 55
D8h	OVUV_CONFIG	Configures output voltage OV/UV fault detection.	R/W BYTE	BIT	00h	Faster response, no crowbar	page 55
D9h	XTEMP_SCALE	Scalar value that is for calibrating the external temperature.	R/W WORD	L11	BA00h	1 °C	page 56
DAh	XTEMP_OFFSET	Offset value for calibrating the external temperature.	R/W WORD	L11	8000h	0 °C	page 56
DCh	TEMPCO_CONFIG	Sets Tempco settings.	R/W BYTE	CUS	28h	4000ppm/°C with internal temperature sensor correction	page 56
DDh	DEADTIME	Sets default deadtime settings.	R/W WORD	BIT	1014h	H-L = 16ns L-H = 20ns	page 57
DEh	DEADTIME_CONFIG	Configures the adaptive dead time optimization mode.	R/W WORD	CUS	8686h	Adaptive deadtime disabled	page 57
E0h	SEQUENCE	DDC rail sequencing configuration.	R/W WORD	BIT	0000h	Prequel and sequel Disabled	page 57
E1h	TRACK_CONFIG	Configures voltage tracking modes.	R/W BYTE	BIT	00h	Tracking disable	page 58
E2h	DDC_GROUP	Configures group ID, fault spreading, OPERATION and VOUT.	R/W BLOCK	BIT	00000000h	Ignore fault spread	page 58
E4h	DEVICE_ID	Returns the device identifier string.	READ BLOCK	ASC		Reads device version	page 58
E5h	MFR_IOUT_OC_FAULT_RESPONSE	Configures the IOUT overcurrent fault response.	R/W BYTE	BIT	80h	Disable and no retry	page 59
E6h	MFR_IOUT_UC_FAULT_RESPONSE	Configures the IOUT undercurrent fault response.	R/W BYTE	BIT	80h	Disable and no retry	page 59
E7h	IOUT_AVG_OC_FAULT_LIMIT	Sets IOUT average overcurrent fault threshold.	R/W WORD	L11	D249h	9.14A	page 60
E8h	IOUT_AVG_UC_FAULT_LIMIT	Sets IOUT average undercurrent fault threshold.	R/W WORD	L11	D5B7h	-9.14A	page 60
E9h	MISC_CONFIG	Sets options pertaining to advanced features.	R/W WORD	BIT	2000h	Broadcast disabled	page 60
EAh	SNAPSHOT	Returns 32-byte read-back of parametric and status values.	READ BLOCK	BIT		N/A	page 61
EBh	BLANK_PARAMS	Indicates recently saved parameter values.	READ BLOCK	BIT	FF...FFh		page 61
F0h	PHASE_CONTROL	Controls phase adding/dropping for current sharing configuration.	R/W BYTE	BIT	00h	All phases disabled	page 61
F3h	SNAPSHOT_CONTROL	Controls how SnapShot values are handled.	R/W BYTE	BIT			page 62
F4h	RESTORE_FACTORY	Restores device to the factory default values.	SEND BYTE				page 62

PMBus Command Summary (Continued)

COMMAND CODE	COMMAND NAME	DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE	DEFAULT SETTING	PAGE
FAh	SECURITY_LEVEL	Reports the security level.	READ BYTE	HEX	1	Public security level	page 62
FBh	PRIVATE_PASSWORD	Sets the private password string.	R/W BLOCK	ASC	00...00h		page 63
FCh	PUBLIC_PASSWORD	Sets the public password string.	R/W BLOCK	ASC	0000h		page 64
FDh	UNPROTECT	Identifies which commands are protected.	R/W BLOCK	CUS	FF...FFh		page 64

PMBus™ Data Formats

Linear-11 (L11)
L11 data format uses 5-bit two's compliment exponent (N) and 11-bit two's compliment mantissa (Y) to represent real world decimal value (X).



Relation between real world decimal value (X), N and Y is: $X = Y \cdot 2^{N}$

Linear-16 Unsigned (L16u)
L16u data format uses a fixed exponent (hard-coded to N = -13h) and a 16-bit unsigned integer mantissa (Y) to represent real world decimal value (X). Relation between real world decimal value (X), N and Y is: $X = Y \cdot 2^{-13}$

Linear-16 Signed (L16s)
L16s data format uses a fixed exponent (hard-coded to N = -13h) and a 16-bit two's compliment mantissa (Y) to represent real world decimal value (X).
Relation between real world decimal value (X), N and Y is: $X = Y \cdot 2^{-13}$

Bit Field (BIT)
Break down of Bit Field is provided in "PMBus Commands Description" on page 32.

Custom (CUS)
Break down of Custom data format is provided in "PMBus Commands Description" on page 32. A combination of Bit Field and integer are common type of Custom data format.

ASCII (ASC)
A variable length string of text characters uses ASCII data format.

PMBus Use Guidelines

The PMBus is a powerful tool that allows the user to optimize circuit performance by configuring devices for their application. When configuring a device in a circuit, the device should be disabled whenever most settings are changed with PMBus commands. Some exceptions to this recommendation are OPERATION, ON_OFF_CONFIG, CLEAR_FAULTS, VOUT_COMMAND, VOUT_MARGIN_HIGH, VOUT_MARGIN_LOW, and ASCCR_CONFIG. While the device is enabled any command can be read. Many commands do not take effect until after the device has been re-enabled, hence the recommendation that commands that change device settings are written while the device is disabled.

When sending the STORE_DEFAULT_ALL, STORE_USER_ALL, RESTORE_DEFAULT_ALL, and RESTORE_USER_ALL commands, it is recommended that no other commands are sent to the device for 100ms after sending STORE or RESTORE commands.

In addition, there should be a 2ms delay between repeated READ commands sent to the same device. When sending any other command, a 5ms delay is recommended between repeated commands sent to the same device.

Summary

All commands can be read at any time.

Always disable the device when writing commands that change device settings. Exceptions to this rule are commands intended to be written while the device is enabled, for example, VOUT_MARGIN_HIGH.

To be sure a change to a device setting has taken effect, write the STORE_USER_ALL command, then cycle input power and re-enable.

PMBus Commands Description

OPERATION (01h)

Definition: Sets Enable, Disable and V_{OUT} Margin settings. Data values of OPERATION that force margin high or low only take effect when the MGN pin is left open (i.e., in the NOMINAL margin state).

Data Length in Bytes: 1

Data Format: BIT

Type: R/W Byte

Default Value:

Units: N/A

COMMAND	OPERATION (01h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BITS 7:6	BITS 5:4	BITS 3:0 (NOT USED)	UNIT ON OR OFF	MARGIN STATE
00	00	0000	Immediate off (No sequencing)	N/A
01	00	0000	Soft off (With sequencing)	N/A
10	00	0000	On	Nominal
10	01	0000	On	Margin Low
10	10	0000	On	Margin High

NOTE: Bit combinations not listed above may cause command errors.

ON_OFF_CONFIG (02h)

Definition: Configures the interpretation and coordination of the OPERATION command and the ENABLE pin (EN).

Data Length in Bytes: 1

Data Format: BIT

Type: R/W Byte

Default Value: 16h (Device starts from ENABLE pin with immediate off)

Units: N/A

COMMAND	ON_OFF_CONFIG (02h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	1	0	1	1	1

BIT NUMBER	PURPOSE	BIT VALUE	MEANING
7:5	Not Used	000	Not Used
4:2	Sets the default to either operate any time power is present or for the on/off to be controlled by ENABLE pin, OPERATION command, or when both the Enable pin and OPERATION command are valid.	000	Device starts any time power is present regardless of ENABLE pin or OPERATION command states.
		101	Device starts from ENABLE pin only.
		110	Device starts from OPERATION command only.
		111	Device starts when the ENABLE pin is active and OPERATION “on” command has been sent.
1	Polarity of the ENABLE pin	0	Active low (Pull pin low to start the device)
		1	Active high (Pull pin high to start the device)
0	ENABLE pin action when commanding the unit to turn off	0	Use the programmed ramp down settings
		1	Turn off the output immediately

CLEAR_FAULTS (03h)

Definition: Clears all fault bits in all registers and releases the SALRT pin (if asserted) simultaneously. If a fault condition still exists, the bit will reassert immediately. This command will not restart a device if it has shut down, it will only clear the faults.

Data Length in Bytes: 0

Data Format: N/A

Type: Send Byte

Default Value: N/A

Units: N/A

Reference: N/A

STORE_DEFAULT_ALL (11h)

Definition: Stores, at the DEFAULT level, all PMBus values that were written since the last restore command. To clear the DEFAULT store, perform a RESTORE_FACTORY then STORE_DEFAULT_ALL. To add to the DEFAULT store, perform a RESTORE_DEFAULT_ALL, write commands to be added, then STORE_DEFAULT_ALL. Wait 20ms after a STORE command.

Data Length in Bytes: 0

Data Format: N/A

Type: Send Byte

Default Value: N/A

Units: N/A

RESTORE_DEFAULT_ALL (12h)

Definition: Restores PMBus™ settings from the nonvolatile DEFAULT Store memory into the operating memory. These settings are loaded at power-up if not superseded by settings in USER store. Security level is changed to level 1 following this command. This command should not be used during device operation.

Data Length in Bytes: 0

Data Format: N/A

Type: Send Byte

Default Value: N/A

Units: N/A

STORE_USER_ALL (15h)

Definition: Stores all PMBus settings from the operating memory to the nonvolatile USER store memory. To clear the USER store, perform a RESTORE_FACTORY then STORE_USER_ALL. To add to the USER store, perform a RESTORE_USER_ALL, write commands to be added, then STORE_USER_ALL. This command can be used during device operation, but the device will be unresponsive for 20ms while storing values.

Data Length in Bytes: 0

Data Format: N/A

Type: Send Byte

Default Value: N/A

Units: N/A

RESTORE_USER_ALL (16h)

Definition: Restores all PMBus settings from the USER store memory to the operating memory. Command performed at power-up. Security level is changed to Level 1 following this command. This command can be used during device operation.

Data Length in Bytes: 0

Data Format: N/A

Type: Send Byte

Default Value: N/A

Units: N/A

VOUT_MODE (20h)

Definition: Reports the V_{OUT} mode and prides the exponent used in calculating several V_{OUT} settings. Fixed with linear mode with default exponent (N) = -13

Data Length in Bytes: 1

Data Format: BIT

Type: Read Byte

Default Value: 13h (Linear Mode, N = -13)

Units: N/A

VOUT_COMMAND (21h)

Definition: This command sets or reports the target output voltage. This command cannot set a value higher than either VOUT_MAX or 110% of the pin strap V_{OUT} setting.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: Pin strap setting

Units: Volts

Range: 0V to VOUT_MAX

VOUT_TRIM (22h)

Definition: Sets VOUT trim value. The two bytes are formatted as a two's complement binary mantissa, used in conjunction with the exponent set in VOUT_MODE.

Data Length in Bytes: 2

Data Format: L16s

Type: R/W Word

Default Value: 0000h (0V)

Units: Volts

Range: -4V to 4V

VOUT_CAL_OFFSET (23h)

Definition: The VOUT_CAL_OFFSET command is used to apply a fixed offset voltage to the output voltage command value. This command is typically used by the user to calibrate a device in the application circuit.

Data Length in Bytes: 2

Data Format: L16s

Type: R/W Word

Default Value: 0000h (0V)

Units: Volts

Range: -4V to 4V

VOUT_MAX (24h)

Definition: The VOUT_ MAX command sets an upper limit on the output voltage the unit can command regardless of any other commands or combinations. The intent of this command is to pride a safeguard against a user accidentally setting the output voltage to a possibly destructive level rather than to be the primary output overprotection.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W Word

Default Value: 1.10xVOUT_COMMAND pin strap setting

Units: Volts

Range: 0V to 4V

VOUT_MARGIN_HIGH (25h)

Definition: Sets the value of the V_{OUT} during a margin high. This VOUT_MARGIN_HIGH command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to "Margin High".

Data Length in Bytes: 2

Data Format: L16u

Type: R/W Word

Default value: 1.05 x VOUT_COMMAND pin strap setting

Units: Volts

Range: 0V to VOUT_MAX

VOUT_MARGIN_LOW (26h)

Definition: Sets the value of the V_{OUT} during a margin low. This VOUT_MARGIN_LOW command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to "Margin Low".

Data Length in Bytes: 2

Data Format: L16u

Type: R/W Word

Default value: 0.95 x VOUT_COMMAND pin strap setting

Units: Volts

Range: 0V to VOUT_MAX

VOUT_TRANSITION_RATE (27h)

Definition: This command sets the rate at which the output should change voltage when the device receives an OPERATION command (Margin High, Margin Low) that causes the output voltage to change. The maximum possible positive value of the two data bytes indicates that the device should make the transition as quickly as possible.

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default value: BA00h (1.0 V/ms)

Units: V/ms

Range: 0.1 to 4V/ms

VOUT_DROOP (28h)

Definition: The VOUT_DROOP sets the effective load line (V/I slope) for the rail in which the device is used. It is the rate, in mV/A, at which the output voltage decreases (or increases) with increasing (or decreasing) output current for use with Adaptive Voltage Positioning requirements and passive current sharing schemes.

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default value: 0000h (0mV/A)

Units: mV/A

Range: 0 to 40 mV/A

MAX_DUTY (32h)

Definition: Sets the maximum allowable duty cycle of the switching frequency.

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default Value: EAD6h (90.75%)

Units: %

FREQUENCY_SWITCH (33h)

Definition: Sets the switching frequency of the device. Initial default value is defined by a pin strap and this value can be overridden by writing this command via PMBus. If an external SYNC is utilized, this value should be set as close as possible to the external clock value. The output must be disabled when writing this command.

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default Value: Pin strap setting

Units: kHz

Range: 300kHz to 1000kHz

INTERLEAVE (37h)

Definition: Configures the phase offset of a device that is sharing a common SYNC clock with other devices. A value of 0 for the Number in Group field is interpreted as 16, to allow for phase spreading groups of up to 16 devices. For current sharing rails, INTERLEAVE is used to set the initial phase of the rail. The current share devices then automatically distributes their phase relative to the INTERLEAVE setting.

Data Length in Bytes: 2

Data Format: BIT

Type: R/W Word

Default Value: Set based on pin-strap PMBus address

Units: N/A

BITS	PURPOSE	VALUE	DESCRIPTION
15:12	Reserved	0	Reserved
11:8	Group Number	0 to 15	Sets a number to a group of interleaved rails
7:4	Number in Group	0 to 15	Sets the number of rails in the group A value of 0 is interpreted as 16
3:0	Position in Group	0 to 15	Sets position of the device's rail within the group

IOUT_CAL_GAIN (38h)

Definition: Sets the effective impedance across the current sense circuit for use in calculating output current at +25°C.

Data Length in Bytes: 2

Data Format: L11.

Type: R/W Word

Default Value: C2EEh (2.93mΩ)

Units: mΩ

IOUT_CAL_OFFSET (39h)

Definition: Used to null out any offsets in the output current sensing circuit, and to compensate for delayed measurements of current ramp due to Isense blanking time.

Data Length in Bytes: 2

Data Format: L11.

Type: R/W Word

Default Value: B667h (-0.4A)

Units: A

VOUT__OV_FAULT_LIMIT (40h)

Definition: Sets the V_{OUT} overvoltage fault threshold.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W Word

Default Value: 1.15xVOUT_COMMAND pin strap setting

Units: Volts

Range: 0V to VOUT_MAX

VOUT__OV_FAULT_RESPONSE (41h)

Definition: Configures the V_{OUT} overvoltage fault response. Note that the device cannot be set to ignore this fault mode. The retry time is the time between restart attempts.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W Byte

Default Value: 80h (Disable and no retry)

Units: N/A

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior: Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Continuous operation (Ignore fault)
		01	Delay, disable and retry. Delay time is specified by Bits[2:0] and retry attempt is specified in Bits[5:3].
		10	Disable and retry according to the setting in Bits[5:3].
		11	Output is disabled while the fault is present. Output is enabled when the fault condition no longer exists.
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted.
		001-110	The PMBus device attempts to restart the number of times set by these bits. The time between the start is set by the value in Bits[2:0].
		111	Attempts to restart continuously, without checking if the fault is still present, until it is disabled, bias power is removed, or another fault condition causes the unit to shut down.
2:0	Retry and Delay Time	000-111	This time count is used for both the amount of time between retry attempts and for the amount of time a rail is to delay its response after a fault is detected. The retry time and delay time units are defined by the type of fault within each device.

VOUT_UV_FAULT_LIMIT (44h)

Definition: Sets the V_{OUT} undervoltage fault threshold. This fault is masked during ramp or when the device is disabled.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W Word

Default Value: 0.8xVOUT_COMMAND pin strap setting

Units: Volts

Range: 0V to VOUT_MAX

VOUT_UV_FAULT_RESPONSE (45h)

Definition: Configures the V_{OUT} undervoltage fault response.
Data Length in Bytes: 1
Data Format: BIT
Type: R/W Byte
Default Value: 80h (Disable, no retry)
Units: N/A

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior: Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Continuous operation (Ignore fault)
		01	Delay, disable and retry. Delay time is specified by Bits[2:0] and retry attempt is specified in Bits[5:3].
		10	Disable and retry according to the setting in Bits[5:3].
		11	Output is disabled while the fault is present. Output is enabled when the fault condition no longer exists.
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted.
		001-110	The PMBus device attempts to restart the number of times set by these bits. The time between the start is set by the value in Bits[2:0].
		111	Attempts to restart continuously, without checking if the fault is still present, until it is disabled, bias power is removed, or another fault condition causes the unit to shut down.
2:0	Retry and Delay Time	000-111	This time count is used for both the amount of time between retry attempts and for the amount of time a rail is to delay its response after a fault is detected. The retry time and delay time units are defined by the type of fault within each device.

IOUT_OC_FAULT_LIMIT (46h)

Definition: Sets the inductor peak overcurrent fault threshold. This limit is applied to current measurement samples taken after the current sense blanking time has expired. A fault occurs after this limit is exceeded for the number of consecutive samples as defined in MFR_CONFIG.

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default Value: D340h (13A)

Units: A

Range: -13 to 13A

IOUT_UC_FAULT_LIMIT (4Bh)

Definition: Sets the inductor valley undercurrent fault threshold. This limit is applied to current measurement samples taken after the current sense blanking time has expired. A fault occurs after this limit is exceeded for the number of consecutive samples as defined in MFR_CONFIG.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: D4C0h (-1xIOUT_OC_FAULT_LIMIT,-13A)

Units: A

Range: -13 to 13A

OT_FAULT_LIMIT (4Fh)

Definition: The OT_FAULT_LIMIT command sets the temperature at which the device should indicate an over-temperature fault. Note that the temperature must drop below OT_WARN_LIMIT to clear this fault.

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default Value: EBE8h (+125˚C)

Units: Celsius

Range: 0˚C to +175˚C

OT_FAULT_RESPONSE (50h)

Definition: Instructs the device on what action to take in response to an over-temperature fault. The delay time is the time between restart attempts.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W Byte

fault Value: 80h (Disable and no retry)

Units: N/A

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior: Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Continuous operation (Ignore fault)
		01	Delay, disable and retry. Delay time is specified by Bits[2:0] and retry attempt is specified in Bits[5:3].
		10	Disable and retry according to the setting in Bits[5:3].
		11	Output is disabled while the fault is present. Output is enabled when the fault condition no longer exists.
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted.
		001-110	The PMBus device attempts to restart the number of times set by these bits. The time between the start is set by the value in Bits[2:0].
		111	Attempts to restart continuously, without checking if the fault is still present, until it is disabled, bias power is removed, or another fault condition causes the unit to shut down.
2:0	Retry and Delay Time	000-111	This time count is used for both the amount of time between retry attempts and for the amount of time a rail is to delay its response after a fault is detected. The retry time and delay time units are defined by the type of fault within each device.

OT_WARN_LIMIT (51h)

Definition: The OT_WARN_LIMIT command sets the temperature at which the device should indicate an er-temperature warning alarm. In response to the OT_WARN_LIMIT being exceeded, the device: Sets the TEMPERATURE bit in STATUS_WORD, Sets the OT_WARNING bit in STATUS_TEMPERATURE, and notifies the host.

Data Length in Bytes: 2

Data Format: L11.

Type: R/W Word

Default Value: EB70h (+110˚C)

Units: Celsius

Range: 0˚C to +175˚C

UT_WARN_LIMIT (52h)

Definition: The UT_WARN_LIMIT command set the temperature at which the device should indicate an under-temperature Warning alarm. In response to the UT_WARN_LIMIT being exceeded, the device: Sets the TEMPERATURE bit in STATUS_WORD, Sets the UT_WARNING bit in STATUS_TEMPERATURE, and notifies the host.

Data Length in Bytes: 2

Data Format: L11.

Type: R/W Word

Default Value: E580h (-40°C)

Units: Celsius

Range: -55˚C to +25˚C

UT_FAULT_LIMIT (53h)

Definition: Sets the temperature at which the device should indicate an under-temperature fault. Note that the temperature must rise above UT_WARN_LIMIT to clear this fault.

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default Value: E490h (-55°C)

Units: Celsius

Range: -55˚C to +25˚C

UT_FAULT_RESPONSE (54h)

Definition: Instructs the device on what action to take in response to an under-temperature fault. The delay time is the time between restart attempts.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W Byte

Default Value: 80h (Disable, no retry)

Units: N/A

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior: Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Continuous operation (Ignore fault)
		01	Delay, disable and retry. Delay time is specified by Bits[2:0] and retry attempt is specified in Bits[5:3].
		10	Disable and retry according to the setting in Bits[5:3].
		11	Output is disabled while the fault is present. Output is enabled when the fault condition no longer exists.
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted.
		001-110	The PMBus device attempts to restart the number of times set by these bits. The time between the start is set by the value in Bits[2:0].
		111	Attempts to restart continuously, without checking if the fault is still present, until it is disabled, bias power is removed, or another fault condition causes the unit to shut down.
2:0	Retry and Delay Time	000-111	This time count is used for both the amount of time between retry attempts and for the amount of time a rail is to delay its response after a fault is detected. The retry time and delay time units are defined by the type of fault within each device.

VIN__OV_FAULT_LIMIT (55h)

Definition: Sets the VIN overvoltage fault threshold.

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default Value: D3A0h (14.5V)

Units: Volts

Range: 0V to 16V

VIN__OV_FAULT_RESPONSE (56h)

Definition: Configures the VIN overvoltage fault response. The delay time is the time between restart attempts.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W Byte

Default Value: 80h (Disable and no retry)

Units: N/A

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior: Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Continuous operation (Ignore fault)
		01	Delay, disable and retry. Delay time is specified by Bits[2:0] and retry attempt is specified in Bits[5:3].
		10	Disable and retry according to the setting in Bits[5:3].
		11	Output is disabled while the fault is present. Output is enabled when the fault condition no longer exists.
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted.
		001-110	The PMBus device attempts to restart the number of times set by these bits. The time between the start is set by the value in Bits[2:0].
		111	Attempts to restart continuously, without checking if the fault is still present, until it is disabled, bias power is removed, or another fault condition causes the unit to shut down.
2:0	Retry and Delay Time	000-111	This time count is used for both the amount of time between retry attempts and for the amount of time a rail is to delay its response after a fault is detected. The retry time and delay time units are defined by the type of fault within each device.

VIN__OV_WARN_LIMIT (57h)

Definition: Sets the VIN overvoltage warning threshold as defined by the table below. In response to the _WARN_LIMIT being exceeded, the device: Sets the NONE OF THE ABE and INPUT bits in STATUS_WORD, Sets the VIN__WARNING bit in STATUS_INPUT, and notifies the host.

Data Length in Bytes: 2

Data Format: L11.

Type: R/W Word

Default Value: D360h (14.0V)

Units: Volts

Range: 0V to 16V

VIN_UV_WARN_LIMIT (58h)

Definition: Sets the VIN undervoltage warning threshold. If a VIN_UV_FAULT occurs, the input voltage must rise above VIN_UV_WARN_LIMIT to clear the fault, which prides hysteresis to the fault threshold. In response to the UV_WARN_LIMIT being exceeded, the device: Sets the NONE OF THE ABE and INPUT bits in STATUS_WORD, Sets the VIN_UV_WARNING bit in STATUS_INPUT, and notifies the host.

Data Length in Bytes: 2

Data Format: Linear-11.

Type: R/W Word

Default Value: 4.5V

Units: Volts

Range: 0V to 12V

VIN_UV_FAULT_LIMIT (59h)

Definition: Sets the VIN undervoltage fault threshold.

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default Value: Pin strap setting

Units: Volts

Range: 0V to 12V

VIN_UV_FAULT_RESPONSE (5Ah)

Definition: Configures the V_{IN} undervoltage fault response as defined by the following table. The delay time is the time between restart attempts.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W Byte

Default Value: 80h (Disable and no retry)

Units: N/A

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior: Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Continuous operation (Ignore fault)
		01	Delay, disable and retry. Delay time is specified by Bits[2:0] and retry attempt is specified in Bits[5:3].
		10	Disable and retry according to the setting in Bits[5:3].
		11	Output is disabled while the fault is present. Output is enabled when the fault condition no longer exists.
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted.
		001-110	The PMBus device attempts to restart the number of times set by these bits. The time between the start is set by the value in Bits[2:0].
		111	Attempts to restart continuously, without checking if the fault is still present, until it is disabled, bias power is removed, or another fault condition causes the unit to shut down.
2:0	Retry and Delay Time	000-111	This time count is used for both the amount of time between retry attempts and for the amount of time a rail is to delay its response after a fault is detected. The retry time and delay time units are defined by the type of fault within each device.

POWER_GOOD_ON (5Eh)

Definition: Sets the voltage threshold for power-good indication. Power-good asserts when the output voltage exceeds POWER_GOOD_ON and de-asserts when the output voltage is less than VOUT_UV_FAULT_LIMIT.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W Word

Default Value: 0.9xVOUT_COMMAND pin strap setting

Units: Volts

TON_DELAY (60h)

Definition: Sets the delay time from when the device is enabled to the start of VOUT rise.

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default Value: CA80h (5ms)

Units: ms

Range: 0 to 500ms

TON_RISE (61h)

Definition: Sets the rise time of VOUT after ENABLE and TON_DELAY.
Data Length in Bytes: 2
Data Format: L11
Type: R/W Word
Default Value: CA80h (5ms)
Units: ms
Range: 0 to 200ms

TOFF_DELAY (64h)

Definition: Sets the delay time from DISABLE to start of VOUT fall.
Data Length in Bytes: 2
Data Format: L11
Type: R/W Word
Default Value: CA80h (5ms)
Units: ms
Range: 0 to 500ms

TOFF_FALL (65h)

Definition: Sets the fall time for VOUT after DISABLE and TOFF_DELAY.
Data Length in Bytes: 2
Data Format: L11
Type: R/W Word
Default Value: CA80h (5ms)
Units: ms
Range: 0 to 200ms

STATUS_BYTE (78h)

Definition: The STATUS_BYTE command returns one byte of information with a summary of the most critical faults.
Data Length in Bytes: 1
Data Format: BIT
Type: Read Byte
Default Value: 00h
Units: N/A

BIT	STATUS BIT NAME	MEANING
7	BUSY	A fault was declared because the device was busy and unable to respond.
6	OFF	This bit is asserted if the unit is not priding power to the output, regardless of the reason, including simply not being enabled.
5	VOUT__OV_FAULT	An output overvoltage fault has occurred.
4	IOUT_OC_FAULT	An output overcurrent fault has occurred.
3	VIN_UV_FAULT	An input undervoltage fault has occurred.
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communications, memory or logic fault has occurred.
0	NONE OF THE ABOVE	A fault or warning not listed in bits 7:1 has occurred.

STATUS_WORD (79h)

Definition: The STATUS_WORD command returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate status registers. The low byte of the STATUS_WORD is the same register as the STATUS_BYTE (78h) command.

Data Length in Bytes: 2

Data Format: BIT

Type: Read Word

Default Value: 0000h

Units: N/A

BIT	STATUS BIT NAME	MEANING
15	VOUT	An output voltage fault or warning has occurred.
14	IOUT/POUT	An output current or output power fault or warning has occurred.
13	INPUT	An input voltage, input current, or input power fault or warning has occurred.
12	MFG_SPECIFIC	A manufacturer specific fault or warning has occurred.
11	POWER_GOOD#	The POWER_GOOD signal, if present, is negated.
10	FANS	A fan or airflow fault or warning has occurred.
9	OTHER	A bit in STATUS_OTHER is set.
8	UNKNOWN	A fault type not given in bits 15:1 of the STATUS_WORD has been detected.
7	BUSY	A fault was declared because the device was busy and unable to respond.
6	OFF	This bit is asserted if the unit is not priding power to the output, regardless of the reason, including simply not being enabled.
5	VOUT__OV_FAULT	An output overvoltage fault has occurred.
4	IOUT_OC_FAULT	An output overcurrent fault has occurred.
3	VIN_UV_FAULT	An input undervoltage fault has occurred.
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communications, memory or logic fault has occurred.
0	NONE OF THE ABOVE	A fault or warning not listed in bits 7:1 has occurred.

STATUS_VOUT (7Ah)

Definition: The STATUS_VOUT command returns one data byte with the status of the output voltage.

Data Length in Bytes: 1

Data Format: BIT

Type: Read Byte

Default Value: 00h

Units: N/A

BIT	STATUS BIT NAME	MEANING
7	VOUT__OV_FAULT	Indicates an output overvoltage fault.
6	VOUT__WARNING	Indicates an output overvoltage warning.
5	VOUT_UV_WARNING	Indicates an output undervoltage warning.
4	VOUT_UV_FAULT	Indicates an output undervoltage fault.
3	VOUT_MAX_WARNING	An attempt has been made to set the output voltage to value higher than allowed by the VOUT_MAX command.
2	TON_MAX_FAULT	Indicates T_{ON} Max fault
1	TOFF_MAX_FAULT	Indicates T_{OFF} Max fault
0	VOUT_TRACKING_ERROR	Indicates V_{OUT} Tracking error. (Note 24)

NOTE:

24. The conditions that cause the VOUT Tracking Error bit to be set is defined by each device manufacturer. This status bit is intended to allow the device to notify the host that there was error in output voltage tracking during the most recent power or power-down event.

STATUS_IOUT (7Bh)

Definition: The STATUS_IOUT command returns one data byte with the status of the output current.

Data Length in Bytes: 1

Data Format: BIT

Type: Read Byte

Default Value: 00h

Units: N/A

BIT	STATUS BIT NAME	MEANING
7	IOUT_OC_FAULT	An output overcurrent fault has occurred.
6	IOUT_OC_LV_FAULT	An output overcurrent and low voltage fault has occurred.
5	IOUT_UC_WARNING	An output overcurrent warning has occurred.
4	IOUT_UC_FAULT	An output undercurrent fault has occurred.
3	ISHARE_FAULT	An current share fault occurred (Note 25).
2	POWER_LIMITING_MODE_FAULT	An P_{OUT} limiting mode fault occurred (Note 26).
1	POUT_OP_FAULT	An P_{OUT} over power fault occurred.
0	POUT_OP_WARNING	Indicates P_{OUT} over power warning.

NOTES:

25. The conditions that cause the Current Share Fault bit to be set are defined by each device manufacturer.

26. The bit is to be asserted when the unit is operating with the output in constant power mode at the power set by the POUT_MAX command

STATUS_INPUT (7Ch)

Definition: The STATUS_INPUT command returns input voltage and input current status information.

Data Length in Bytes: 1

Data Format: BIT

Type: Read Byte

Default Value: 00h

Units: N/A

BIT	STATUS BIT NAME	MEANING
7	VIN__OV_FAULT	An input overvoltage fault has occurred.
6	VIN__OV_WARNING	An input overvoltage warning has occurred.
5	VIN_UV_WARNING	An input undervoltage warning has occurred.
4	VIN_UV_FAULT	An input undervoltage fault has occurred.
3	UNIT OFF FOR LOW INPUT VOLTAGE	Unit is off for insufficient Input voltage.
2	IIN OC FAULT	An I_{IN} overcurrent fault occurred.
1	IIN OC WARNING	An I_{IN} overcurrent warning occurred
0	PIN OP WARNING	An P_{IN} overpower waning occurred.

STATUS_TEMP (7Dh)

Definition: The STATUS_TEMP command returns one byte of information with a summary of any temperature related faults or warnings.

Data Length in Bytes: 1

Data Format: BIT

Type: Read Byte

Default Value: 00h

Units: N/A

BIT	STATUS BIT NAME	MEANING
7	OT_FAULT	An over-temperature fault has occurred.
6	OT_WARNING	An over-temperature warning has occurred.
5	UT_WARNING	An under-temperature warning has occurred.
4	UT_FAULT	An under-temperature fault has occurred.
3:0	N/A	These bits are not used.

STATUS_CML (7Eh)

Definition: The STATUS_CML command returns one byte of information with a summary of any Communications, Logic and/or Memory errors.

Data Length in Bytes: 1

Data Format: BIT

Type: Read Byte

Default Value: 00h

Units: N/A

BIT	MEANING
7	Invalid or unsupported PMBus command was received.
6	The PMBus command was sent with invalid or unsupported data.
5	A packet error was detected in the PMBus command.
4	Memory fault detected (Note 27).
3	Processor fault detected (Note 28).
2	Reserved
1	A PMBus command tried to write to a read-only or protected command, or a communication fault other than the ones listed in this table has occurred.
0	Other Memory or Logic Fualt has occurred (Note 29).

NOTES:

27. The conditions that cause the memory fault detected bit to be set, and the response this condition, are defined by each device manufacturer. One example of an error that would cause this bit to be set is a CRC of the memory that does not match the initial CRC value.
28. The conditions that cause the processor fault detected bit to be set, and the response this condition, are defined by each device manufacturer.
29. The conditions that cause the other memory or logic fault detected bit to be set, and the response this condition, are defined by each device manufacturer.

STATUS_MFR_SPECIFIC (80h)

Definition: Returns the Communication, Logic and Memory specific status.

Data Length in Bytes: 1

Data Format: BIT

Type: Read Byte

Default value: 00h

Units: N/A

BIT	FIELD NAME	MEANING
7:6	Reserved	Reserved
5	Reserved	Reserved
4	Reserved	Reserved
3	TSW	Loss of external clock synchronization has occurred.
2	Reserved	Reserved
1	Reserved	Reserved
0	Reserved	Reserved

READ_VIN (88h)

Definition: Returns the input voltage reading.

Data Length in Bytes: 2

Data Format: L11

Type: Read Word

Units: Volts

READ_VOUT (8Bh)

Definition: Returns the output voltage reading.
Data Length in Bytes: 2
Data Format: L16u
Type: Read Word
Units: Volts

READ_IOUT (8Ch)

Definition: Returns the output current reading.
Data Length in Bytes: 2
Data Format: L11
Type: Read Word
Default Value: N/A
Units: A

READ_TEMPERATURE_1 (8Dh)

Definition: Returns the controller junction temperature reading from internal temperature sensor.
Data Length in Bytes: 2
Data Format: L11
Type: Read Word
Units: °C

READ_TEMPERATURE_2 (8Eh)

Definition: Returns the temperature reading from the external temperature device connected to XTEMP pins.
Data Length in Bytes: 2
Data Format: L11
Type: Read Word
Units: °C

READ_DUTY_CYCLE (94h)

Definition: Reports the actual duty cycle of the converter during the enable state.
Data Length in Bytes: 2
Data Format: L11
Type: Read Word
Units:%

READ_FREQUENCY (95h)

Definition: Reports the actual switching frequency of the converter during the enable state.
Data Length in Bytes: 2
Data Format: L11
Type: Read Word
Units: kHz

PMBUS_REVISION (98h)

Definition: Returns the revision of the PMBus implemented in the device
Data Length in Bytes: 1
Data Format: HEX
Type: Read Byte
Default Value: 01h
Units: N/A

MFR_ID (99h)

Definition: MFR_ID sets user defined identification. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL and USER_DATA_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Data Length in Bytes: user defined

Data Format: ASCII

Type: Block R/W

Default Value: null

Units: N/A

MFR_MODEL (9Ah)

Definition: MFR_MODEL sets a user defined model. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL and USER_DATA_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Data Length in Bytes: user defined

Data Format: ASC

Type: Block R/W

Default Value: null

Units: N/A

MFR_REVISION (9Bh)

Definition: MFR_REVISION sets a user defined revision. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL and USER_DATA_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Data Length in Bytes: user defined

Data Format: ASC

Type: Block R/W

Default Value: null

Units: N/A

MFR_LOCATION (9Ch)

Definition: MFR_LOCATION sets a user defined location identifier. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL and USER_DATA_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Data Length in Bytes: user defined

Data Format: ASC

Type: Block R/W

Default Value: null

Units: N/A

MFR_DATE (9Dh)

Definition: MFR_DATE sets a user defined date. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL and USER_DATA_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Data Length in Bytes: user defined

Data Format: ASC

Type: Block R/W

Default Value: null

Units: N/A

MFR_SERIAL (9Eh)

Definition: MFR_SERIAL sets a user defined serialized identifier. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL and USER_DATA_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Data Length in Bytes: user defined

Data Format: ASC

Type: Block R/W

Default Value: null

Units: N/A

USER_DATA_00 (B0h)

Definition: USER_DATA_00 sets a user defined data. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL and USER_DATA_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Data Length in Bytes: user defined

Data Format: ASCII

Type: Block R/W

Default Value: null

Units: N/A

AUTO_COMP_CONFIG (BCh)

Definition: Controls configuration of Auto Compensation features.

Data Length in Bytes: 1

Data Format: CUS

Type: R/W Byte

Default Value: 69h

Units: N/A

BITS	PURPOSE	VALUE	DESCRIPTION
7:4	Auto Comp Gain Percentage	G	Scale the Gain of the auto compensation results by a factor of (G+1)*10%, where 0 = G = 9. G = 0 yields lowest jitter; G = 9 yields tightest transient response.
3	Power-good Assertion	0	Use PG_DELAY.
		1	Assert PG after Auto Comp completes.
2	Auto Comp Store	0	Do not store Auto Comp results.
		1	Store Auto Comp results for use on future ramps.
1:0	Auto Comp Mode	0	Off (Disabled). Compensation stored in PID_TAPS will be used.
		1	Once (results are storable).
		2	Repeat every ~1 second (only the first results are storable).
		3	Repeat every ~1 minute (only the first results are storable).

AUTO_COMP_CONTROL (BDh)

Definition: Causes the Auto Comp algorithm to initiate, if the Auto Comp feature is enabled in AUTO_COMP_CONFIG.

Data Length in Bytes: 1

Data Format: BIT

Type: Send Byte

Default Value:

Units: N/A

DEADTIME_MAX (BFh)

Definition: Sets the maximum dead time value for the PWMH and PWML outputs. This limit applies during frozen or adaptive dead time algorithm modes (see DEADTIME_CONFIG).

Data Length in Bytes: 2

Data Format: CUS

Type: R/W Word

Default Value: 3838h (56ns)

Range: 0 to 60ns

Units: ns

BIT	PURPOSE	VALUE	DESCRIPTION
15	n/a	0	NOT used
14:8	Sets the Maximum H-to-L Deadtime	H	Limits the maximum allowed H-to-L dead time when using the adaptive dead time algorithm. dead time = Hns (signed).
7	n/a	0	Not used
6:0	Sets the Maximum L-to-H Deadtime	L	Limits the maximum allowed L-to-H dead time when using the adaptive dead time algorithm. dead time = Lns (signed).

MFR_CONFIG (D0h)

Definition: Configures several manufacturer-level features.

Data Length in Bytes: 2

Data Format: BIT

Type: R/W Word

Default Value: 6A11h

Units: N/A

BIT	PURPOSE	VALUE	DESCRIPTION
15:11	Current Sense Blanking Delay	D	Sets the delay, D, in 32ns steps.
10:8	Current Sense Fault Count	C	Sets the number of consecutive OC or UC violations required for a fault to 2C+1.
7	Enable XTEMP Measurements	0	No temperature measurements are performed on XTEMP.
		1	Temperature measurements are performed on XTEMP.
6	Temperature Sensor Control (Note 30)	0	The internal temperature sensor is used for warning and fault checks.
		1	An external 2N3904 NPN on XTEMP is used for warning and fault checks.
5:4	Current Sense Control	00	Current sense uses GND-referenced, down-slope sense.
		01	Current sense uses VOUT-referenced, down-slope sensing.
		10	Current sense uses VOUT-referenced, up-slope sensing.
		11	Reserved
3	NLR During Ramp	0	Wait for PG.
		1	Always on.
2	Alternate Ramp Control	0	Alternate Ramp Disabled.
		1	Alternate Ramp Enabled.
1	PG Pin Output Control	0	PG is open drain.
		1	PG is push-pull.
0	SYNC Pin Output Control	0	SYNC is open drain.
		1	SYNC is push-pull.

NOTE:

30. When selecting XTEMP (bit 6), be sure to have the XTEMP enabled in bit 7.

USER_CONFIG (D1h)

Definition: Configures several user-level features.

Data Length in Bytes: 2

Data Format: BIT

Type: R/W Word

Default Value: 2011h

Units: N/A

BIT	PURPOSE	VALUE	DESCRIPTION
15:14	Minimum Duty Cycle	N	Sets the minimum duty cycle ((N+1)/(2^8)) during a ramp when "Minimum Duty Cycle" (Bit 13) is enabled. For example, if Minimum Duty Cycle input N is set to 3, the minimum duty cycle is (3+1)/(2^8) = (1/64).
13	Minimum Duty Cycle Control	0	Minimum Duty Cycle is Disabled.
		1	Minimum Duty Cycle is Enabled.
12	Reserved	-	Reserved
11	SYNC Time-out Enable	0	SYNC output remains on after device is disabled.
		1	SYNC turns off 500ms after device is disabled.
10	Reserved	-	Reserved
9	PID Feed-Forward Control	0	PID Coefficients are corrected for VDD variations.
		1	PID Coefficients are not corrected for VDD variations.
8	Fault Spreading Mode	0	If sequencing is disabled, this device will ignore faults from other devices. If sequencing is enabled, the devices will sequence down from the failed device outward.
		1	Faults received from any device selected by the DDC_GROUP command will cause this device to shut down immediately.
7	Reserved	-	Reserved
6	SYNC Utilization Control	0	Auto-configure using the SYNC pin and FREQUENCY_SWITCH parameter.
		1	Switch using the SYNC input.
5	SYNC Output Control	0	Configure the SYNC pin as an input-only.
		1	Drive the switch clock out of SYNC when using the internal oscillator.
4	Reserved	-	Reserved
3	Reserved	-	Reserved
2	OFF Low-side Control	0	The low-side drive is off when device is disabled.
		1	The low-side drive is on when device is disabled.
1:0	Standby Mode	00	Enter low-power mode when device is disabled (no READ_xxxx data available).
		01	Monitor for faults when device is disabled (READ_xxxx data available).
		10	Reserved
		11	Monitor for faults using pulsed mode (READ_xxxx data available upon read command).

ISHARE_CONFIG (D2h)

Definition: Configures the device for current sharing communication over the DDC bus.

Data Length in Bytes: 2

Data Format: BIT

Type: R/W Word

Default Value: 0000h

Units: N/A

BIT	PURPOSE	VALUE	DESCRIPTION
15:8	IShare DDC ID	0 to 31 (0x00 to 0x1F)	Sets the current share rail's DDC ID for each device within a current share rail. Set to the same DDC ID as in DDC_CONFIG. This DDC ID is used for sequencing and fault spreading when used in a current share rail.
7:5	Number of Members	0 to 7	Number of devices in current share rail -1. Example: 3 device current share rail, use 3 – 1 = 2.
4:2	Member Position	0 to 7	Position of device within current share rail.
1	Reserved	0	Reserved
0	I-Share Control	1	Device is a member of a current share rail.
		0	Device is not a member of a current share rail.

DDC_CONFIG (D3h)

Definition: Configures DDC addressing.

Data Length in Bytes: 2

Data Format: BIT

Type: R/W Word

Default Value: 0001h

Units: N/A

BIT	FIELD NAME	VALUE	DESCRIPTION
15:13	Reserved	0	Reserved
12:8	Broadcast Group	0 to 31	Group number used for broadcast events. (i.e., Broadcast Enable and Broadcast Margin) Set this number to the same value for all rails/devices that should respond to each other's broadcasted event. This function is enabled by the bits 15 and 14 in the MISC_CONFIG command.
7:6	Reserved	0	Reserved
5	DDC TX Inhabit	0	DDC Transmission.
		1	DDC Transmission Enabled.
4:0	Rail ID	0 to 31 (00 to 1Fh)	Sets the rail's DDC ID for sequencing and fault spreading. For the current-sharing applications, set this value the same as the ID value in ISHARE_CONFIG for all devices in the current sharing rail.

POWER_GOOD_DELAY (D4h)

Definition: Sets the delay applied between the output exceeding the PG threshold (POWER_GOOD_ON) and asserting the PG pin. The delay time can range from 0ms up to 500s, in steps of 125ns. A 1ms minimum configured value is recommended to apply proper debounce to this signal.

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default Value: BA00h (1ms)

Units: ms

Range: 0 to 5s

PID_TAPS (D5h)

Definition: this command configures the control loop compensator coefficients.

Data Length in Bytes: 9

Data Format: CUS

Units: N/A

Type: R/W

Default Value: Auto Comp stores when algorithm is initiated during start up. When Auto Comp is disabled PID_TAPS can be stored via PMBus.

The PID algorithm implements the following Z-domain function in Equation 7:

$$\frac{A + Bz^{-1} + Cz^{-2}}{1 - z^{-1}} \quad \text{(EQ. 7)}$$

The coefficients A, B, and C are represented using a pseudo-floating point format similar to the V_{OUT} parameters (with the addition of a sign bit), defined as Equation 8:

$$A = (-1)^S \bullet 2^E \bullet M \quad \text{(EQ. 8)}$$

where M is a two-byte unsigned mantissa, S is a sign-bit, and E is a 7-bit two's-complement signed integer. The 9-byte data field is defined in table below. S is stored as the MSB of the E byte.

BYTE	PURPOSE	DEFINITION
8	Tap C - E	Coefficient C exponent + S
7	Tap C - M [15:8]	Coefficient C mantissa, high-byte
6	Tap C - M [7:0]	Coefficient C mantissa, low-byte
5	Tap B - E	Coefficient B exponent + S
4	Tap B - M [15:8]	Coefficient B mantissa, high-byte
3	Tap B - M [7:0]	Coefficient B mantissa, low-byte
2	Tap A - E	Coefficient A exponent + S
1	Tap A - M [15:8]	Coefficient A mantissa, high-byte
0	Tap A - M [7:0]	Coefficient A mantissa, low-byte

NOTE: Data bytes are transmitted on the PMBus in the order of Byte 0 through Byte 8.

INDUCTOR (D6h)

Definition: Informs the device of circuit's inductor value. This is used in adaptive algorithm calculations relating to the inductor ripple current.

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default Value: BA00h (1µH)

Units: µH

NLR_CONFIG (D7h)

Definition: Configures the non-linear response (NLR) control parameters.

Data Length in Bytes: 4

Data Format: BIT

Type: R/W

Default Value: 00000000h

Units: N/A

BIT	FIELD NAME	VALUE	DESCRIPTION
31:30	Outer Threshold Multiplier	O	Sets multiplier of inner threshold for outer threshold setting, O*LI and O*UI.
29:27	NLR Comparator Threshold: Loading-Inner	LI	Sets inner threshold for a loading event to ~0.5%*(LI+1)*V_{OUT}.
26:24	NLR Comparator Threshold: Unloading-Inner	UI	Sets inner threshold for an unloading event to ~0.5%*(UI+1)*V_{OUT}.
23:20	Loading-Outer Threshold Max Correction Time	LOT	Sets outer threshold, maximum correction time for a loading event to LOT*tsw/64(s).
19:16	Loading-Inner Threshold Max Correction Time	LIT	Sets inner threshold, maximum correction time for a loading event to LIT*tsw/64(s).
15:12	Unloading-Outer Threshold Max Correction Time	UOT	Sets outer threshold, maximum correction time for an unloading event to UOT*tsw/64(s).
11:8	Unloading-Inner Threshold Max Correction Time	UIT	Sets inner threshold, maximum correction time for an unloading event to UIT*tsw/64(s).
7:4	Load Blanking Time Control	LB	Sets NLR blanking time for a loading event.
3:0	Unload Blanking Time Control	UB	Sets NLR blanking time for an unloading event.

TABLE 16. LOADING/UNLOADING BLANKING TIMES

LB or UB	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
tsw/64 UNITS	1	2	3	5	9	17	33	49	65	81	97	129	161	177	193	225

OVUV_CONFIG (D8h)

Definition: Configures the output voltage OV and UV fault detection feature. The default value of 00h is recommended.

Data Length in Bytes: 1

Data Format: Bit

Type: R/W

Default Value: 00h

Units: N/A

BIT	PURPOSE	VALUE	DEFINITION
7	Controls How an OV Fault Response Shutdown Sets the Output Driver State	0	An OV fault does not enable the low-side power device
		1	An OV fault enables the low-side power device
6:4	Not used	0	Not used
3:0	Defines the Number of Consecutive Limit Violations Required to Declare an OV or UV Fault	N	N+1 consecutive OV or UV violations initiate a fault response

XTEMP_SCALE (D9h)

Definition: Sets a scalar value that is used for calibrating the external temperature. The constant is applied in Equation 9 to produce the read value of XTEMP via the PMBus command READ_TEMPERATURE_2.

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default Value: BA00h (1°C)

Units: °C

NOTE: This value must be = to 1.

$$READ_TEMPERATURE_2 = \left(External\ Temperature \cdot \frac{1}{XTEMP_SCALE}\right) + XTEMP_OFFSET \quad \text{(EQ. 9)}$$

XTEMP_OFFSET (DAh)

Definition: Sets an offset value that is used for calibrating the external temperature. The constant is applied in Equation 10 to produce the read value of XTEMP via the PMBus command READ_TEMPERATURE_2.

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default Value: 8000h (0°C)

Units: °C

$$READ_TEMPERATURE_2 = \left(External\ Temperature \cdot \frac{1}{XTEMP_SCALE}\right) + XTEMP_OFFSET \quad \text{(EQ. 10)}$$

TEMPCO_CONFIG (DCh)

Definition: Configures the correction factor and temperature measurement source when performing temperature coefficient correction for current sense. TEMPCO_CONFIG values are applied as negative correction to a positive temperature coefficient.

Data Length in Bytes: 1

Data Format: CUS

Type: R/W Byte

Default Value: 28h (4000ppm/°C)

Units: N/A

To determine the hex value of the Tempco Correction factor (TC) for current scale of a power stage using $r_{DC(ON)}$ current sensing, first determine the temperature coefficient of resistance for the conductor, α. This is found with Equation 11:

$$\alpha = \frac{R_{REF} - R}{R_{REF}(T_{REF} - T)} \quad \text{(EQ. 11)}$$

Where: R = Conductor resistance at temperature "T"

R_{REF} = Conductor resistance at reference temperature T

α = Temperature coefficient of resistance for the conductor material

T = Temperature measured by temperature sensor, in °C

T_{REF} = Reference temperature that α is specified at for the conductor material

After α is determined, convert the value in units of 100ppm/°C. This value is then converted to a hex value with Equation 12.

$$TC = \frac{\alpha \times 10^6}{100} \quad \text{(EQ. 12)}$$

Typical Values: Copper = 3900ppm/°C (27h), silicon = 4800ppm/°C (30h)

Range: 0 to 6300ppm/°C

BIT	PURPOSE	VALUE	DEFINITION
7	Selects the Temp Sensor Source for Tempco Correction	0	Selects the internal temperature sensor.
		1	Selects the XTEMP pin for temperature measurements.
6:0	Sets the Tempco Correction in Units of 100ppm/°C for IOUT_CAL_GAIN	TC	$R_{SEN(DCR)}$ = IOUT_CAL_GAIN*(1+TC*(T-25)) where R_{SEN} = resistance of sense element.

DEADTIME (DDh)

Definition: Sets the nonoverlap between PWM transitions using a 2-byte data field. The most significant byte controls the high-side to low-side dead time value as a single 2's-complement signed value in units of ns. The least significant byte controls the low-side to high-side dead time value. Positive values imply a non-overlap of the FET drive on-times. Negative values imply an overlap of the FET drive on-times. The device will operate at the dead time values written to this command when adaptive dead time is disabled, between the minimum dead time specified in DEADTIME_CONFIG and the maximum dead time specified in DEADTIME_MAX. When switching from adaptive dead time mode to frozen mode (by writing to bit 15 of DEADTIME_CONFIG) the frozen dead time will be whatever the last dead time was before the device switches to frozen dead time mode.

Data Length in Bytes: 2

Data Format: CUS

Type: R/W Word

Default Value: 1014h (H-L = 16ns, L-H = 20ns)

Units: ns

Range: -15ns to 60ns

DEADTIME_CONFIG (DEh)

Definition: Configures the deadtime optimization mode. Also sets the minimum deadtime value for the adaptive deadtime mode range.

Data Length in Bytes: 2

Data Format: CUS

Type: R/W Word

Default Value: 8686h (Adaptive deadtime disabled)

Units: N/A

BIT	PURPOSE	VALUE	DESCRIPTION
15	Sets the High to Low Transition Deadtime Mode	0	Adaptive H-to-L deadtime control.
		1	Freeze the H-to-L deadtime.
14:8	Sets the Minimum H-to-L Deadtime	0-126d	Limits the minimum allowed H-to-L dead time when using the adaptive dead time algorithm (2ns resolution).
7	Sets the Low to High Transition Deadtime Mode	0	Adaptive L-to-H deadtime control.
		1	Freezes the L-to-H deadtime.
6:0	Sets the Minimum L-to-H Deadtime	0-126d	Limits the minimum allowed L-to-H dead time when using the adaptive dead time algorithm (2ns resolution).

SEQUENCE (E0h)

Definition: Identifies the Rail DDC ID of the prequel and sequel rails when performing multi-rail sequencing. The device will enable its output when its EN or OPERATION enable states, as defined by ON_OFF_CONFIG, is set and the prequel device has issued a power-good event on the DDC bus. The device will disable its output (using the programmed delay values) when the sequel device has issued a power down event on the DDC bus.

The data field is a two-byte value. The most-significant byte contains the 5-bit Rail DDC ID of the prequel device. The least-significant byte contains the 5-bit Rail DDC ID of the sequel device. The most significant bit of each byte contains the enable of the prequel or sequel mode. This command overrides the corresponding sequence configuration set by the CONFIG pin settings.

Data Length in Bytes: 2

Data Format: BIT

Type: R/W Word

Default Value: 0000h (Prequel and Sequel disabled)

BIT	FIELD NAME	VALUE	SETTING	DESCRIPTION
15	Prequel Enable	0	Disable	Disable, no prequel preceding this rail.
		1	Enable	Enable, prequel to this rail is defined by bits 12:8.
14:13	Reserved	0	Reserved	Reserved
12:8	Prequel Rail DDC ID	0 to 31	DDC ID	Set to the DDC ID of the prequel rail.
7	Sequel Enable	0	Disable	Disable, no sequel following this rail.
		1	Enable	Enable, sequel to this rail is defined by bits 4:0.
6:5	Reserved	0	Reserved	Reserved
4:0	Sequel Rail DDC ID	0 to 31	DDC ID	Set to the DDC ID of the sequel rail.

TRACK_CONFIG (E1h)

Definition: Configures the voltage tracking modes of the device.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W Byte

Default Value: 00h (Tracking Disabled)

BIT	FIELD NAME	VALUE	SETTING	DESCRIPTION
7	Enables Voltage Tracking	0	Disable	Tracking is disabled.
		1	Enable	Tracking is enabled.
6:3	Reserved	-	Reserved	Reserved
2	Tracking Ratio Control	0	100%	Output tracks 100% ratio of VTRK input.
		1	50%	Output tracks 50% ratio of VTRK input.
1	Tracking Upper Limit	0	Target Voltage	Output Voltage is limited by Target Voltage.
		1	VTRK Voltage	Output Voltage is limited by VTRK Voltage.
0	Ramp-up Behavior	0	Track after PG	The output is not allowed to track VTRK down before power-good.
		1	Track always	The output is allowed to track VTRK down before power-good.

DDC_GROUP (E2h)

Definition: This command sets which rail DDC IDs a device should listen to for fault spreading information. A device can follow multiple DDC ID rails. Example is provided in following table.

DDC ID	CONFIGURATION	DDC_GROUP	DESCRIPTION
0	3xZL9006M Current Sharing	0000000Ah	This rail will listen to Rail-1 and Rail-3.
1	2xZL9006M Current Sharing	00000004h	This rail will listen to Rail-2.
2	1xZL9006M Single Phase	00000000h	This rail will ignore fault spread.
3	1xZL9006M Single Phase	00000002h	This rail will listen to Rail-1.

The device/rail's own DDC ID should not be set within the DDC_GROUP command for that device/rail. All devices in a current share rail must shutdown for the rail to report a shutdown.

If fault spread mode is enabled in USER_CONFIG (Bit8 set to 1), the device will immediately shut down if one of its DDC_GROUP members fail. The device/rail will attempt its configured restart only after all devices/rails within the DDC_GROUP have cleared their faults.

If fault spread mode disabled in USER_CONFIG (Bit 8 cleared to 0), the device will perform a sequenced shutdown as defined by the SEQUENCE command setting. The rails/devices in a sequencing set only attempt their configured restart after all faults have cleared within the DDC_GROUP. If fault spread mode is disabled and sequencing is also disabled, the device will ignore faults from other devices and stay enabled.

Data Length in Bytes: 4

Data Format: BIT

Type: R/W

Default Value: 00000000h (Ignore fault spread)

DEVICE_ID (E4h)

Definition: Returns the 16-byte (character) device identifier string.

Data Length in Bytes: 16

Data Format: ASC

Type: Read Block

Default Value: Current firmware revision

MFR_IOUT_OC_FAULT_RESPONSE (E5h)

Definition: Configures the I_{OUT} overcurrent fault response as defined by the following table. Sets the overcurrent status bit in STATUS_IOUT.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W Byte

Default Value: 80h (Disable, and no retry)

Units: N/A

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior: Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Continuous operation (Ignore fault).
		01	Delay, disable and retry. Delay time is specified by Bits[2:0] and retry attempt is specified in Bits[5:3].
		10	Disable and retry according to the setting in Bits[5:3].
		11	Output is disabled while the fault is present. Output is enabled when the fault condition no longer exists.
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted.
		001-110	The PMBus device attempts to restart the number of times set by these bits. The time between the start is set by the value in Bits[2:0].
		111	Attempts to restart continuously, without checking if the fault is still present, until it is disabled, bias power is removed, or another fault condition causes the unit to shut down.
2:0	Retry and Delay Time	000-111	This time count is used for both the amount of time between retry attempts and for the amount of time a rail is to delay its response after a fault is detected. The retry time and delay time units are defined by the type of fault within each device.

MFR_IOUT_UC_FAULT_RESPONSE (E6h)

Definition: Configures the IOUT undercurrent fault response as defined by the table below. Sets the undercurrent status bit in STATUS_IOUT.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W Byte

Default Value: 80h (Disable and no retry)

Units: N/A

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior: Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Continuous operation (Ignore fault).
		01	Delay, disable and retry. Delay time is specified by Bits[2:0] and retry attempt is specified in Bits[5:3].
		10	Disable and retry according to the setting in Bits[5:3].
		11	Output is disabled while the fault is present. Output is enabled when the fault condition no longer exists.
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted.
		001-110	The PMBus device attempts to restart the number of times set by these bits. The time between the start is set by the value in Bits[2:0].
		111	Attempts to restart continuously, without checking if the fault is still present, until it is disabled, bias power is removed, or another fault condition causes the unit to shut down.
2:0	Retry and Delay Time	000-111	This time count is used for both the amount of time between retry attempts and for the amount of time a rail is to delay its response after a fault is detected. The retry time and delay time units are defined by the type of fault within each device.

IOUT_AVG_OC_FAULT_LIMIT (E7h)

Definition: Sets the IOUT average overcurrent fault threshold. For down-slope sensing, this corresponds to the average of all the current samples taken during the (1-D) time interval, excluding the Current Sense Blanking time (which occurs at the beginning of the 1-D interval). For up-slope sensing, this corresponds to the average of all the current samples taken during the D time interval, excluding the Current Sense Blanking time (which occurs at the beginning of the D interval). This feature shares the OC fault bit operation (in STATUS_IOUT) and OC fault response with IOUT_ OC_FAULT_LIMIT.

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default Value: D249h (9.14A)

Units: A

IOUT_AVG_UC_FAULT_LIMIT (E8h)

Definition: Sets the IOUT average undercurrent fault threshold. For down-slope sensing, this corresponds to the average of all the current samples taken during the (1-D) time interval, excluding the Current Sense Blanking time (which occurs at the beginning of the 1-D interval). For up-slope sensing, this corresponds to the average of all the current samples taken during the D time interval, excluding the Current Sense Blanking time (which occurs at the beginning of the D interval). This feature shares the UC fault bit operation (in STATUS_IOUT) and UC fault response with IOUT_ UC_FAULT_LIMIT.

Data Length in Bytes: 2

Data Format: L11

Type: R/W WORD

Default Value: D5B7h (-9.14A)

Units: A

MISC_CONFIG (E9h)

Definition: This command is used to set options for SYNC output configurations.

Data Length in Bytes: 2

Data Format: BIT

Type: R/W Word

Units: N/A

Default Value: 2000h

BITS	PURPOSE	VALUE	DESCRIPTION
15	Broadcast Margin (see DDC_CONFIG)	0	Disabled
		1	Enable
14	Broadcast Enable (see DDC_CONFIG)	0	Disabled
		1	Enable
13	Phase Enable Select	0	Use PH_EN pin to add/drop current-share phases.
		1	Use PHASE_CONTROL command to add/drop phases.
12	Reserved	-	Reserved
11:10	Reserved	-	Reserved
9	Reserved	-	Reserved
8	Reserved	-	Reserved
7	Reserved	-	Reserved
6	Diode Emulation	0	Disabled
		1	Enabled, enter diode emulation at light loads to improve efficiency.
5:3	Reserved	-	Reserved
2	Minimum GL Pulse	0	Disabled
		1	Enabled, GL pulse width limited to 10%*T_{SW} minimum during diode emulation.
1	SnapShot	0	Disabled
		1	Enable
0	Reserved	-	Reserved

SNAPSHOT (EAh)

Definition: The SNAPSHOT command is a 32-byte read-back of parametric and status values. It allows monitoring and status data to be stored to flash either during a fault condition or via a system-defined time using the SNAPSHOT_CONTROL command. In case of a fault, last updated values are stored to the flash memory. Use SNAPSHOT_CONTROL command to read stored values.

Data Length in Bytes: 32

Data Format: Bit

Type: Block Read

BYTE NUMBER	VALUE	PMBUS COMMAND	FORMAT
31:22	Reserved	Reserved	00h
21	Manufacturer Specific Status Byte	STATUS_MFR_SPECIFIC (80h)	Byte
20	CML Status Byte	STATUS_CML (7Eh)	Byte
19	Temperature Status Byte	STATUS_TEMPERATURE (7Dh)	Byte
18	Input Status Byte	STATUS_INPUT (7Ch)	Byte
17	I_{OUT} Status Byte	STATUS_IOUT (7Bh)	Byte
16	V_{OUT} Status Byte	STATUS_VOUT (7Ah)	Byte
15:14	Switching Frequency	READ_FREQUENCY (95h)	L11
13:12	External Temperature	READ_EXTERNAL_TEMP_2 (8Eh)	L11
11:10	Internal Temperature	READ_INTERNAL_TEMP_1 (8Dh)	L11
9:8	Duty Cycle	READ_DUTY_CYCLE (94h)	L11
7:6	Peak Current	N/A	L11
5:4	Load Current	READ_IOUT (8Ch)	L11
3:2	Output Voltage	READ_VOUT (8Bh)	L16u
1:0	Input Voltage	READ_VIN (88h)	L11

BLANK_PARAMS (EBh)

Definition: Returns a 16-byte string which indicates which parameter values were either retrieved by the last RESTORE operation or have been written since that time. Reading BLANK_PARAMS immediately after a restore operation allows the user to determine which parameters are stored in that store. Index to read BLANK_PARAM is provided in "PMBus Command Summary" on page 27. One indicates the parameter is not present in the store and has not been written since the RESTORE operation.

Data Length in Bytes: 16

Data Format: BIT

Type: Block Read

Default Value: FF...FFh

Units: N/A

PHASE_CONTROL (F0h)

Definition: This command controls Phase adding/dropping when the device is setup for current sharing.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W Byte

Default Value: 00h

Units: N/A

VALUE	DESCRIPTION
00h	The device phase is disabled or dropped.
01h	The device phase is active or added.

SNAPSHOT_CONTROL (F3h)

Definition: Writing a 01 will cause the device to copy the current SnapShot values from NVRAM to the 32-byte SnapShot parameters. Writing a 02 will cause the device to write the current SnapShot values to NVRAM. Read from NVRAM (writing a 01) does not work if SNAPSHOT is enabled in MISC_CONFIG. To read from NVRAM, the device has to be disabled.

Data Length in Bytes: 1

Data Format: Bit

Type: R/W Byte

VALUE	DESCRIPTION
01h	Move parametric and status values from Flash to the RAM.
02h	Move latest parametric and status values from RAM to the Flash.

RESTORE_FACTORY (F4h)

Definition: Restores the device to the hard-coded Factory default values and pin strap definitions. The device retains the DEFAULT and USER stores for restoring. Security level is changed to Level 1 following this command.

Data Length in Bytes: 0

Data Format: N/A

Type: Send Byte

Default Value: N/A

Units: N/A

SECURITY_LEVEL (FAh)

Definition: The device provides write protection for individual commands. Each bit in the UNPROTECT parameter controls whether its corresponding command is writable (commands are always readable). If a command is not writable, a password must be entered in order to change its parameter (i.e., to enable writes to that command). There are two types of passwords, public and private. The public password provides a simple lock-and-key protection against accidental changes to the device. It would typically be sent to the device in the application prior to making changes. Private passwords allow commands marked as non-writable in the UNPROTECT parameter to be changed. Private passwords are intended for protecting Default-installed configurations and would not typically be used in the application. Each store (USER and DEFAULT) can have its own UNPROTECT string and private password. If a command is marked as non-writable in the DEFAULT UNPROTECT parameter (its corresponding bit is cleared), the private password in the DEFAULT Store must be sent in order to change that command. If a command is writable according to the Default UNPROTECT parameter, it may still be marked as non-writable in the User Store UNPROTECT parameter. In this case, the User private password can be sent to make the command writable.

The device supports four levels of security. Each level is designed to be used by a particular class of users, ranging from module manufacturers to end users, as discussed below. Levels 0 and 1 correspond to the public password. All other levels require a private password. Writing a private password can only raise the security level. Writing a public password will reset the level down to 0 or 1. Figure 28 shows the algorithm used by the device to determine if a particular command write is allowed.

Security Level 3 – Module Vendor

Level 3 is intended primarily for use by Module vendors to protect device configurations in the Default Store. Clearing a UNPROTECT bit in the Default Store implies that a command is writable only at Level 3 and above. The device's security level is raised to Level 3 by writing the private password value previously stored in the Default Store. To be effective, the module vendor must clear the UNPROTECT bit corresponding to the STORE_DEFAULT_ALL and RESTORE_DEFAULT commands. Otherwise, Level 3 protection is ineffective since the entire store could be replaced by the user, including the enclosed private password.

Security Level 2 – User

Level 2 is intended for use by the end user of the device. Clearing a UNPROTECT bit in the User Store implies that a command is writable only at Level 2 and above. The device's security level is raised to Level 2 by writing the private password value previously stored in the User Store. To be effective, the user must clear the UNPROTECT bit corresponding to the STORE_USER_ALL, RESTORE_DEFAULT_ALL, STORE_DEFAULT_ALL, and RESTORE_DEFAULT commands. Otherwise, Level 2 protection is ineffective since the entire store could be replaced, including the enclosed private password.

Security Level 1 – Public

Level 1 is intended to protect against accidental changes to ordinary commands by providing a global write-enable. It can be used to protect the device from erroneous bus operations. It provides access to commands whose UNPROTECT bit is set in both the Default and User Store. Security is raised to Level 1 by writing the public password stored in the User Store using the PUBLIC_PASSWORD command. The public password stored in the Default Store has no effect.

Security Level 0 - Unprotected

Level 0 implies that only commands, which are always writable (e.g., PUBLIC_PASSWORD) are available. This represents the lowest authority level and hence the most protected state of the device. The level can be reduced to 0 by using PUBLIC_PASSWORD to write any value which does not match the stored public password.

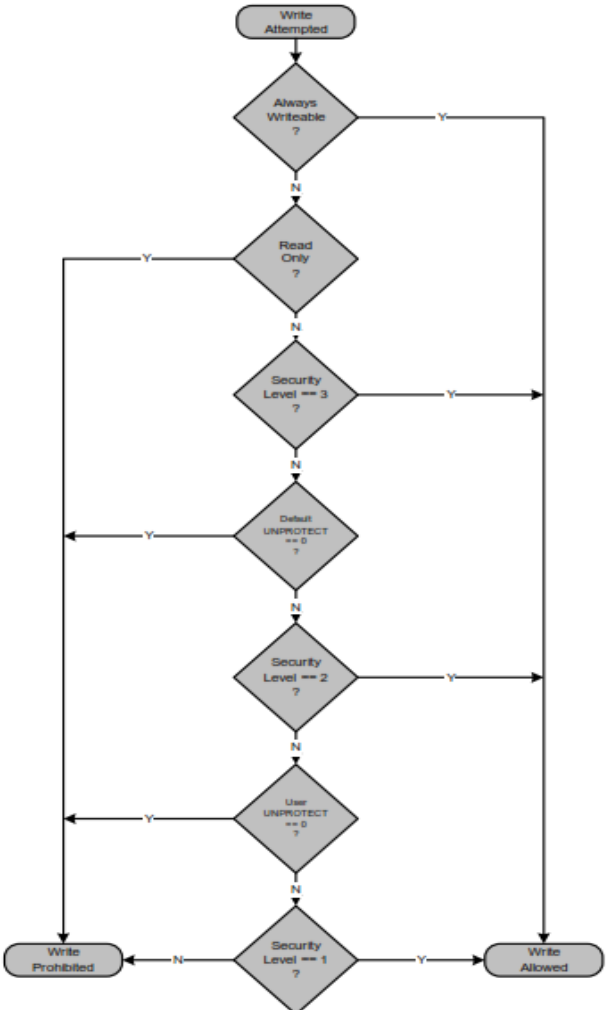


FIGURE 28. ALGORITHM USED TO DETERMINE WHEN A COMMAND IS WRITABLE

Data Length in Bytes: 1
Data Format: HEX
Type: Read Byte
Default Value: 01h

PRIVATE_PASSWORD (FBh)

Definition: Sets the private password string.
Data Length in Bytes: 9
Data Format: ASCII. ISO/IEC 8859-1
Type: R/W Block
Default Value: 000..00h

PUBLIC_PASSWORD (FCh)

Definition: Sets the public password string.

Data Length in Bytes: 4

Data Format: ASCII. ISO/IEC 8859-1

Type: R/W Block

Default Value: 00...00h

UNPROTECT (FDh)

Definition: Sets a 256-bit (32-byte) parameter which identifies which commands are to be protected against write-access at lower security levels. Each bit in this parameter corresponds to a command according to the command's code. The command with a code of 00h (PAGE) is protected by the least significant bit of the least significant byte, followed by the command with a code of 01h and so forth. Note that all possible commands have a corresponding bit regardless of whether they are protected or supported by the device. Clearing a command's UNPROTECT bit indicates that write access to that command is only allowed if the device's security level has been raised to an appropriate level. The UNPROTECT bits in the DEFAULT store require a security level 3 or greater to be writable. The UNPROTECT bits in the USER store require a security level of 2 or higher.

Data Length in Bytes: 32

Data Format: CUS

Type: Block R/W

Default Value: FF...FFh

Firmware Revision History

FIRMWARE REVISION CODE	CHANGE DESCRIPTION	NOTE
FE03		Not recommended for new designs.
FE04	3. VIN_OV_WARN_LIMIT = 14.0V 4. VIN_UV_FAULT_LIMIT = 4.0V 5. OT_WARN_LIMIT = 110°C 6. OT_FAULT_LIMIT = 125°C 7. VIN_UV_WARN_LIMIT = 4.5V 8. DEADTIME = 1014h (H-L = 16ns, L-H = 20ns) 9. DEADTIME_MAX = 3838h (Max H-L = 56ns, Max L-H = 56ns)	Recommended for new designs.

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Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
March 16, 2016	FN7959.2	Added “PMBus Use Guidelines” on page 32.
October 30, 2014	FN7959.1	Removed I^2C throughout entire datasheet. Removed all references to AN2033 and AN2034 throughout entire datasheet. Added references to refer to the “PMBus Commands Description” section throughout datasheet. On Page 1: Removed related literature. Added “overcurrent/undercurrent protection” bullet to the Features section. Removed “current sharing” from one of the Features bullets. Updated Figure 1 (removed EPAD, I2C, and RTN from diagram). On page 3: Added more verbiage to Pin description to be more accurate. On page 4: Updated Note 2 from “These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate -e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.” to “These Intersil plastic packaged products are RoHS compliant by EU exemption 7C-I and employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish which is compatible with both SnPb and Pb-free soldering operations. Intersil RoHS compliant products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.” Added Firmware Revision to Ordering Information table. Added Note 4. On page 6: Corrected typo of Note reference on Output Current Range, IOUT(DC) under Recommended Operating Conditions from “Note 19” to “Note 20”. Updated Charged Device Model ESD rating from “750V” to “1000V”. On page 24: “SnapShot Parameter Capture” section has been rewritten. From page 27 through page 64: Added “PMBus Command Summary”, “PMBus™ Data Formats” and “PMBus Commands Description” sections. On page 64: Added “Firmware Revision History” section. Updated About Intersil Verbiage.
March 5, 2013	FN7959.0	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

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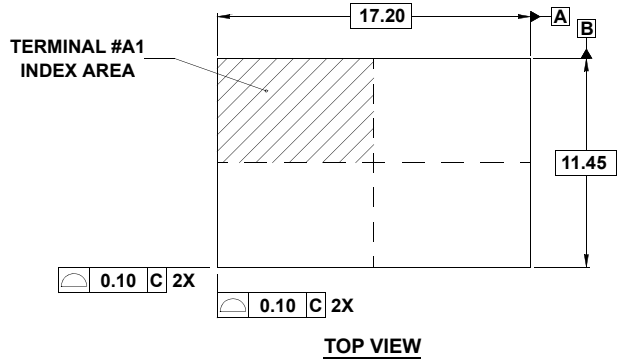
Reliability reports are also available from our website at www.intersil.com/support.

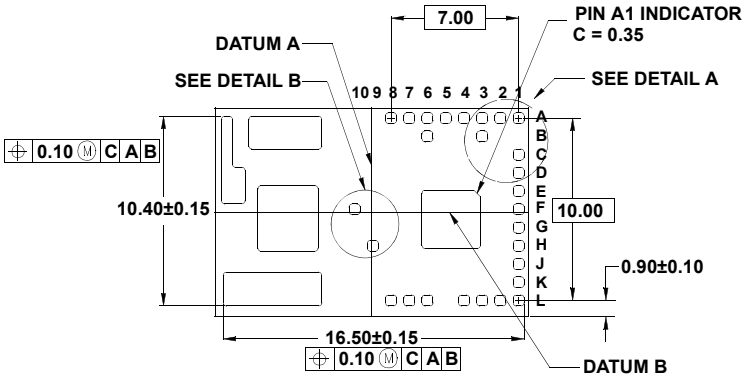
Package Outline Drawing
Y32.17.2x11.45

32 I/O 17.2mm x 11.45mm x 2.5mm HDA MODULE

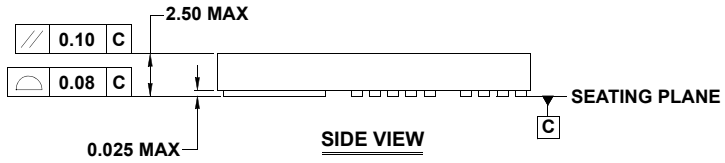
Rev 1, 11/12



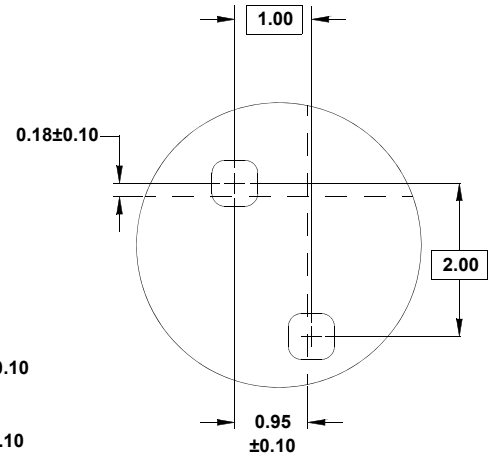
TOP VIEW



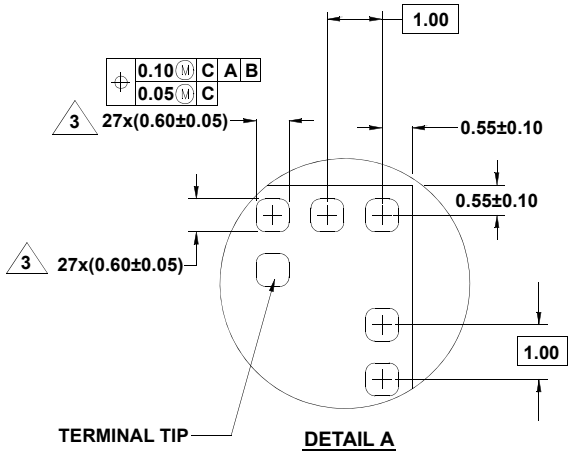
BOTTOM VIEW



SIDE VIEW



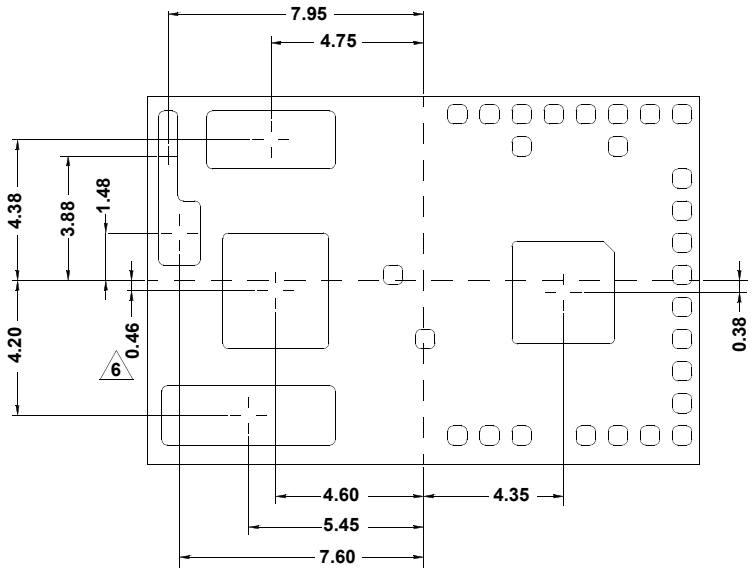
DETAIL B



DETAIL A

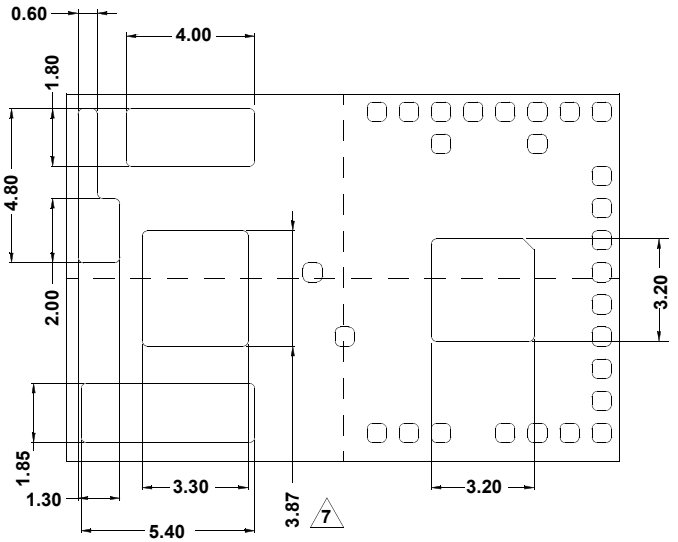
NOTES:

1. All dimensions are in millimeters.
2. 1.0mmx1.0mm represents the basic land grid pitch.
3. "27" is the total number of I/O (excluding large pads). All 27 I/O's are centered in a fixed row and column matrix at 1.0mm pitch BSC.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Tolerance for exposed DAP edge location dimension on page 2 is ±0.1mm.



CENTERLINE POSITION DETAILS FOR THE 5 EXPOSED DAPS

BOTTOM VIEW

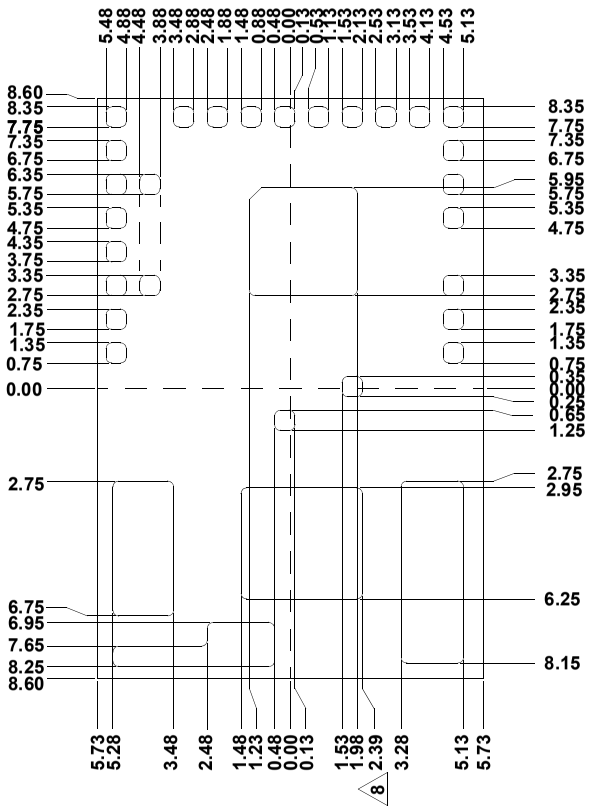


SIZE DETAILS FOR THE 5 EXPOSED DAPS

BOTTOM VIEW

NOTES:

6. Shown centerline measurement of 0.46mm applies to ZL9006M module. For the ZL9010M module, this measurement is 0.33mm. All other measures identical for both the ZL9006M and ZL9010M modules.
7. Shown pad edge measurement of 3.87mm applies to ZL9006M module. For the ZL9010M module, this measurement is 3.60mm. All other measurements are identical for both the ZL9006M and ZL9010M modules.

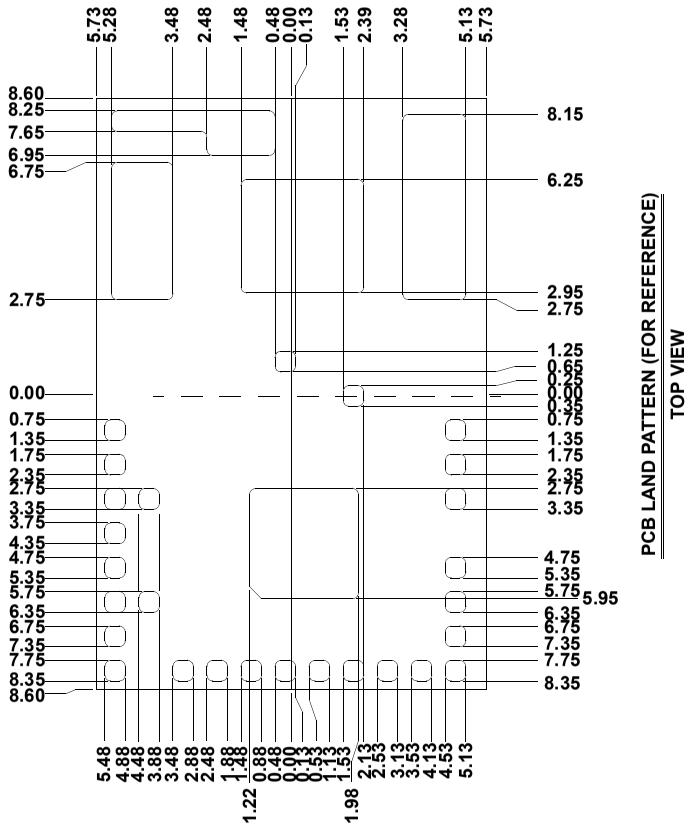


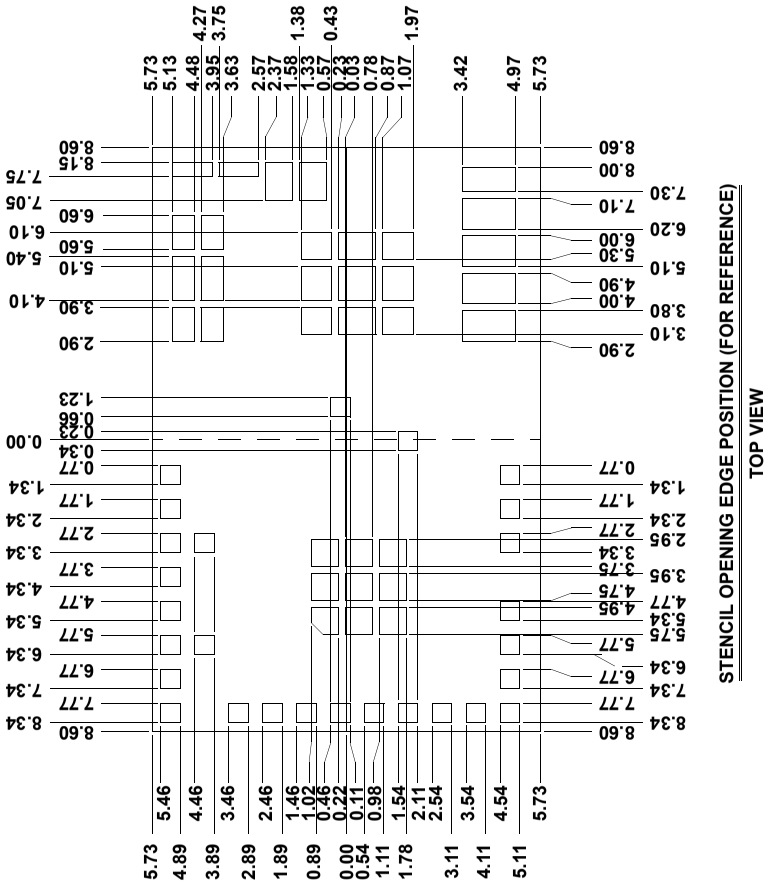
TERMINAL AND PAD EDGE DETAILS

BOTTOM VIEW

NOTES:

8. Shown edge pad measurement of 2.39mm applies to ZL9006M module. For the ZL9010M module, this measurement is 2.13mm. All other measurements are identical for both the ZL9006M & ZL9010M modules.


PCB LAND PATTERN (FOR REFERENCE)
TOP VIEW


STENCIL OPENING EDGE POSITION (FOR REFERENCE)
TOP VIEW