



**Absolute Maximum Ratings**

IN, UVEN to SGND .....	-0.3V to +52V	ICTRL, PWM, FB, and $\overline{\text{FLT}}$ to SGND.....	-0.3V to +6V
INN, INP, ISP, ISN, and $\overline{\text{DIMOUT}}$ to PGND .....	-0.3V to +65V	PGND to SGND.....	-0.3V to +0.3V
ISP to ISN.....	-0.3V to +0.6V	V <sub>CC</sub> Short-Circuit Duration.....	Continuous
LX1, LX2 to PGND .....	-1.0V to +65V	Continuous Power Dissipation (TQFN)	
BST_ to LX_ .....	-0.3V to +6V	(T <sub>A</sub> = +70°C, derate, 28.6mW/°C above +70°C).....	2285mW
DH_ to LX_ .....	-0.3V to V <sub>BST</sub> +0.3V	Continuous Power Dissipation (TSSOP)	
DL1, DL2 to PGND.....	-0.3V to (V <sub>VCC</sub> +0.3)V	(T <sub>A</sub> = +70°C, derate 27mW/°C above +70°C).....	2162mW
CSP, CSN to SGND .....	-2.5V to +6V	Operating Junction-Temperature Range	
CSP to CSN .....	-0.5V to +0.5V	(Note 1, 2).....	-40°C to +125°C
IOUTV, COMP, RT, SS .....	-0.3 to V <sub>VCC</sub> +0.3	Storage-Temperature Range.....	-40°C to +150°C
V <sub>CC</sub> to SGND .....	-0.3V to +6V	Soldering Temperature (reflow).....	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Package Information**

**28-TQFN**

PACKAGE CODE	T2855Y+5C
Outline Number	<a href="#">21-100130</a>
Land Pattern Number	<a href="#">90-0027</a>
<b>Thermal Resistance, Single-Layer Board:</b>	
Junction to Ambient (θ <sub>JA</sub> )	68°C/W
Junction to Case (θ <sub>JC</sub> )	11°C/W
<b>Thermal Resistance, Four-Layer Board:</b>	
Junction to Ambient (θ <sub>JA</sub> )	60°C/W
Junction to Case (θ <sub>JC</sub> )	11°C/W

**28-TSSOP**

PACKAGE CODE	U28E+1C
Outline Number	<a href="#">21-100182</a>
Land Pattern Number	<a href="#">90-100069</a>
<b>Thermal Resistance, Single-Layer Board:</b>	
Junction to Ambient (θ <sub>JA</sub> )	78°C/W
Junction to Case (θ <sub>JC</sub> )	13°C/W
<b>Thermal Resistance, Four-Layer Board:</b>	
Junction to Ambient (θ <sub>JA</sub> )	71.6°C/W
Junction to Case (θ <sub>JC</sub> )	13°C/W

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

## Electrical Characteristics

( $V_{IN} = 12V$ ,  $V_{UVEN} = 12V$ , limits are 100% tested at  $T_A = +25^\circ C$  and  $T_A = +125^\circ C$ . Limits over the operating temperature range and relevant supply-voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>SUPPLY VOLTAGE</b>						
INP Input Voltage Range	$V_{INP}$		5.0		60	V
Supply Current	$I_{INQ}$	No switching		3	6	mA
<b>UNDERVOLTAGE LOCKOUT</b>						
Undervoltage Lockout Rising	$V_{UVEN\_THR}$	$V_{UVEN}$ rising	1.12	1.24	1.37	V
Hysteresis				106		mV
Shutdown Current	$I_{SHTDN}$	$V_{UVEN} = 0$ , $V_{IN} = 12V$		6	20	$\mu A$
<b>V<sub>CC</sub> REGULATOR</b>						
Output Voltage	$V_{CC}$	$5.5V < V_{IN} < 40V$ ; $I_{VCC} = 1mA$	4.9	5.0	5.1	V
		$I_{VCC} = 30mA$ , $5.5V < V_{IN} < 36V$	4.9	5.0	5.1	
		$I_{VCC} = 1mA$ to $60mA$ , $6V < V_{IN} < 25V$	4.9	5.0	5.1	
Dropout Voltage	$V_{CC\_DROP}$	$V_{IN} = 4.5V$ , $I_{VCC} = 5mA$		60	110	mV
$V_{CC}$ UVLO Rising	$V_{CC\_UVLOR}$	Rising		4.0		V
$V_{CC}$ UVLO Falling	$V_{CC\_UVLOF}$	Falling		3.75		V
Short-Circuit Current Limit	$I_{VCC\_SC}$			70		mA
<b>INPUT CURRENT-SENSE AMPLIFIER</b>						
Input Current-Sense Common-Mode Range			5		60	V
Input Current-Sense Threshold		$3V < V_{INP} < 60V$	88	100	112	mV
INP Bias Current		$V_{INP} - V_{INN} = 100mV$ , $V_{INP} = 60V$		50		$\mu A$
INN Bias Current		$V_{INP} - V_{INN} = 100mV$ , $V_{INP} = 60V$		10		$\mu A$
<b>CSP, CSN CURRENT-SENSE AMPLIFIER</b>						
Voltage Gain (Boost, Buck modes)		$V_{CSP} = 100mV$ , $V_{CSN} = 0$	9.5	10	10.5	V/V
<b>ANALOG DIMMING</b>						
ICTRL Control Input Voltage Range	$ICTRL\_RNG$		0.2		1.2	V
ICTRL Zero Current Threshold	$ICTRLZC\_VTH$	$(V_{ISP} - V_{ISN}) < 5mV$	0.16	0.18	0.2	V
ICTRL Clamp Voltage	$ICTRL\_CLMP$	ICTRL sink = $1\mu A$	1.25	1.30	1.35	V
ICTRL Input Bias Current	$ICTRLI_{IN}$	$V_{ICTRL} = 0.2$ to $5.5V$		20	500	nA
<b>LED CURRENT-SENSE AMPLIFIER</b>						
Common-Mode Input Range			-0.3		+60	V
Differential Signal Range			0		200	mV
ISN Input Bias Current	$IB_{ISN}$	$V_{ISP} - V_{ISN} = 200mV$ , $V_{ISP} = 60V$		22	60	$\mu A$

**Electrical Characteristics (continued)**

( $V_{IN} = 12V$ ,  $V_{UVEN} = 12V$ , limits are 100% tested at  $T_A = +25^\circ C$  and  $T_A = +125^\circ C$ . Limits over the operating temperature range and relevant supply-voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ISP Input Bias Current	$I_{B_{ISP}}$	$V_{ISP} - V_{ISN} = 200mV$ , $V_{ISP} = 60V$		350	550	$\mu A$
Voltage Gain		$V_{ISP} - V_{ISN} = 200mV$ , $3V < V_{ISP}$ , $V_{ISN} < 60V$	4.9	5.00	5.1	V/V
LED Current-Sense Regulation Voltage		$V_{ICTRL} = 1.3V$ , $3V < (V_{ISP} - V_{ISN}) < 60V$	213.8	220	226.2	mV
		$V_{ICTRL} = 1.2V$ , $3V < (V_{ISP} - V_{ISN}) < 60V$	194	200	206	
		$V_{ICTRL} = 0.4V$ , $3V < (V_{ISP} - V_{ISN}) < 60V$	36	40	44	
LED Current-Sense Regulation Voltage (Low Range)		$V_{ICTRL} = 1.2V$ , $0V < (V_{ISP} - V_{ISN}) < 3V$	192	200	208	mV
		$V_{ICTRL} = 0.4V$ , $0V < (V_{ISP} - V_{ISN}) < 3V$	35	40	45	
Common-Mode Input Range Selector	$RNG_{SEL}$	$V_{ISP}$ rising	2.75	2.85	2.95	V
		$V_{ISP}$ falling	2.5	2.6	2.7	
<b>OSCILLATOR</b>						
Switching-Frequency Range			200		700	kHz
Bias Voltage at RT	$V_{RT}$			1.25		V
Oscillator Frequency Accuracy		Dither disabled	-10		+10	%
Frequency Dither	$f_{DITH}$	Dither enabled, $f_{SW} = 200kHz$ to $700kHz$		$\pm 6$		%
Switching Frequency	$f_{SW}$	$R_{RT} = 50K\Omega$	370	400	430	kHz
		$R_{RT} = 105K\Omega$	180	200	220	
		$R_{RT} = 25.5K\Omega$	630	700	770	
<b>SLOPE COMPENSATION ON CSP</b>						
Slope Compensation Current-Ramp Height	$I_{SLOPE\_PK}$	Peak-current ramp added to CSP input per switching cycle at 100% duty cycle	42.5	50	57.5	$\mu A$
<b>ERROR AMPLIFIER</b>						
Transconductance	$g_M$	$V_{ISP} - V_{ISN} = 200mV$	1170	1800	2430	$\mu S$
COMP Sink Current	$COMP_{ISINK}$	$V_{COMP} = 5V$		300		$\mu A$
COMP Source Current	$COMP_{ISRC}$	$V_{COMP} = 0V$		300		$\mu A$
COMP Clamp Boost Mode	$COMP_{CLBST}$			1.93		V
COMP Clamp Buck Mode	$COMP_{CLBK}$			1.74		V
<b>nMOS GATE DRIVERS</b>						
DH1 Sourcing Resistance	$R_{DH1\_SRC}$			2.2		$\Omega$
DH2 Sourcing Resistance	$R_{DH2\_SRC}$			1.3		$\Omega$
DH_ Sinking Resistance	$R_{DH\_SINK}$			0.9		$\Omega$
DL_ Sourcing Resistance	$R_{DL\_SRC}$	$DL\_ = high$		1.3		$\Omega$
DL_ Sinking Resistance	$R_{DL\_SINK}$	$DL\_ = low$		0.9		$\Omega$
DH_ to DL_ Dead Time		DH_ fall to DL_ rise		20		ns
DL_ to DH_ Dead Time		DL_ fall to DH_ rise		20		ns

**Electrical Characteristics (continued)**

( $V_{IN} = 12V$ ,  $V_{UVEN} = 12V$ , limits are 100% tested at  $T_A = +25^\circ C$  and  $T_A = +125^\circ C$ . Limits over the operating temperature range and relevant supply-voltage range are guaranteed by design and characterization.)

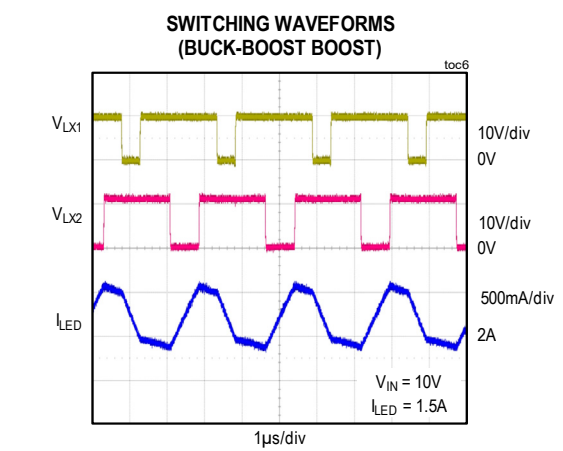
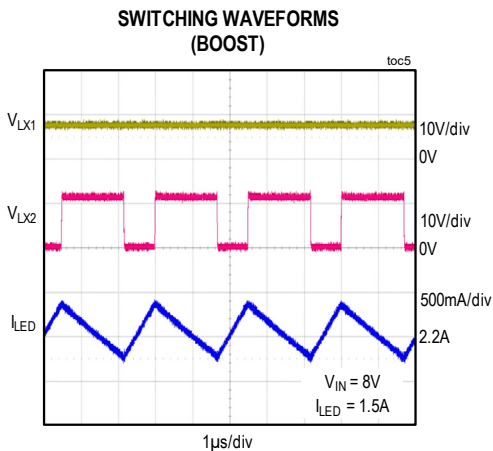
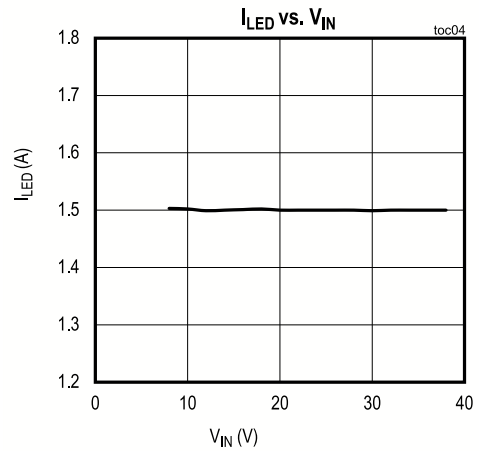
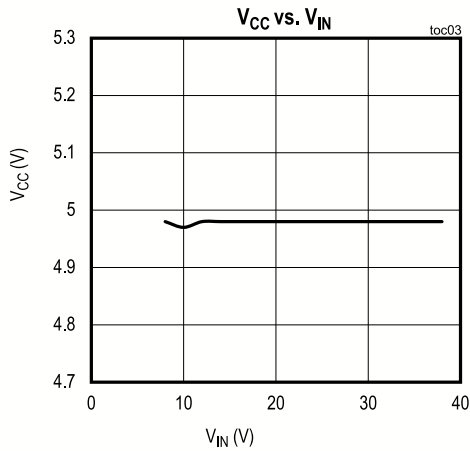
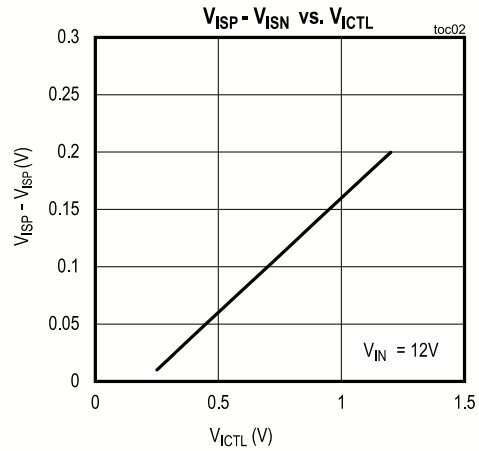
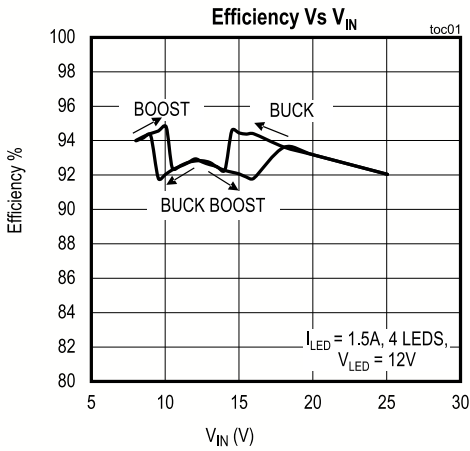
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>PWM DIMMING</b>						
Internal Ramp Frequency	$f_{RAMP}$		180	200	220	Hz
External Sync Frequency Range			30		2000	Hz
External Sync Low Level Voltage	$V_{LTH}$				0.4	V
External Sync High Level Voltage	$V_{HTH}$		2.2			V
DIM Comparator Offset Voltage			170	200	230	mV
Internal PWM Duty Cycle	$V_{PWM}$	$V_{PWM} = 1.0V$		28.6		%
		$V_{PWM} = 1.7V$		53.6		
DIM Voltage for 100% Duty Cycle			3.2			V
<b>DIMMING MOSFET GATE DRIVER</b>						
Peak Pullup Current	$I_{DIMOUTPU}$	PWM = 0V, ( $V_{ISP} - V_{DIMOUT}$ ) = 5V	30	50	85	mA
Peak Pulldown Current	$I_{DIMOUTPD}$	( $V_{ISP} - V_{DIMOUT}$ ) = 0V	10	25	45	mA
$\overline{DIMOUT}$ Low Voltage with Respect to ISP			-5.4	-5.0	-4.6	V
DIM Turn-On Comparator		ISP rising		5.7		V
DIM Turn-Off Comparator		ISP falling		5.3		V
<b>FAULT</b>						
Minimum On Time (Buck)	$t_{ON\_MIN}$			150	240	ns
FB Overvoltage Threshold	$V_{TH\_OVP}$	FB rising	1.22	1.24	1.28	V
FB Overvoltage Hysteresis				0.1		V
Short Fault Threshold		FB falling		150		mV
Soft-Start Pullup Current				15		$\mu A$
$\overline{FLT}$ Output Voltage		$I_{SINK}$ is 1mA after fault		0.05	0.3	V
$\overline{FLT}$ Leakage Current		$V_{\overline{FLT}} = 5.5V$			1	$\mu A$
Hiccup Activation Threshold				400		mV
<b>OFF TIME CONTROL</b>						
Linear Range of Pulse Doubler				5		$\mu s$
<b>THERMAL SHUTDOWN</b>						
Thermal Shutdown Threshold	$T_{SHUTDOWN}$	Temperature Rising		165		$^\circ C$
Thermal Shutdown Hysteresis	$T_{HYS}$			15		$^\circ C$

**Note 1:** The MAX25600 is guaranteed to meet performance specifications over the  $-40^\circ C$  to  $+125^\circ C$  operating junction-temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated for junction temperatures greater than  $+125^\circ C$ .

**Note 2:** The MAX25600 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating junction temperature when overtemperature protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability.

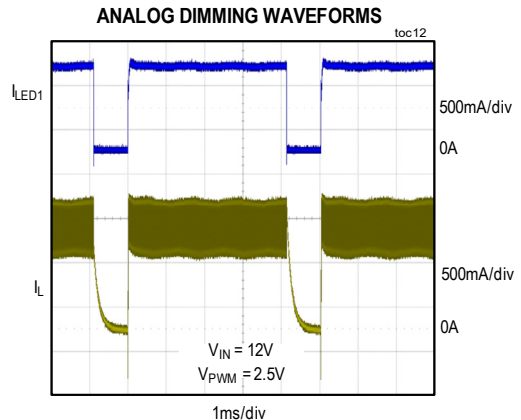
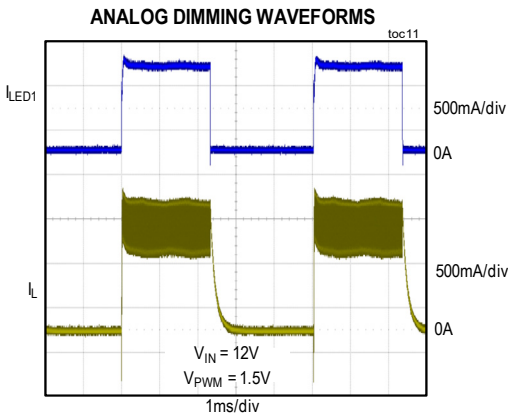
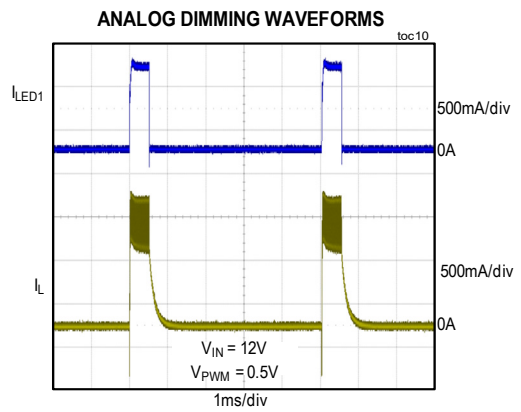
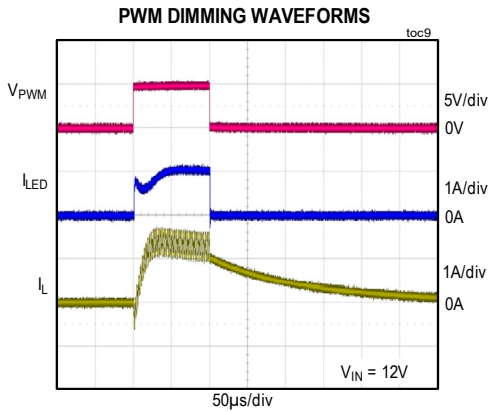
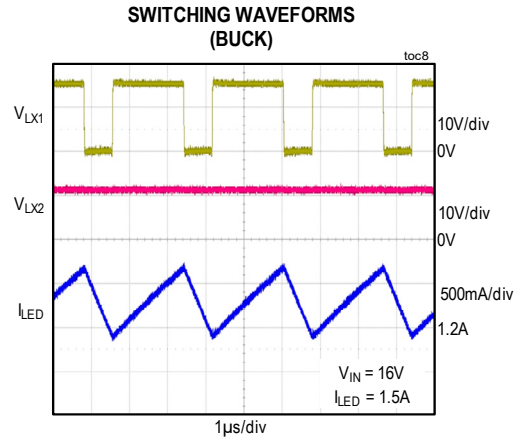
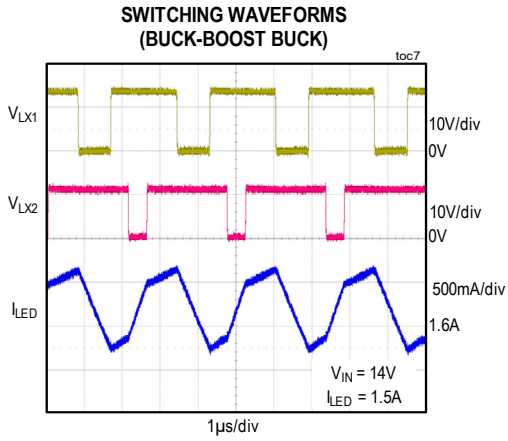
Typical Operating Characteristics

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

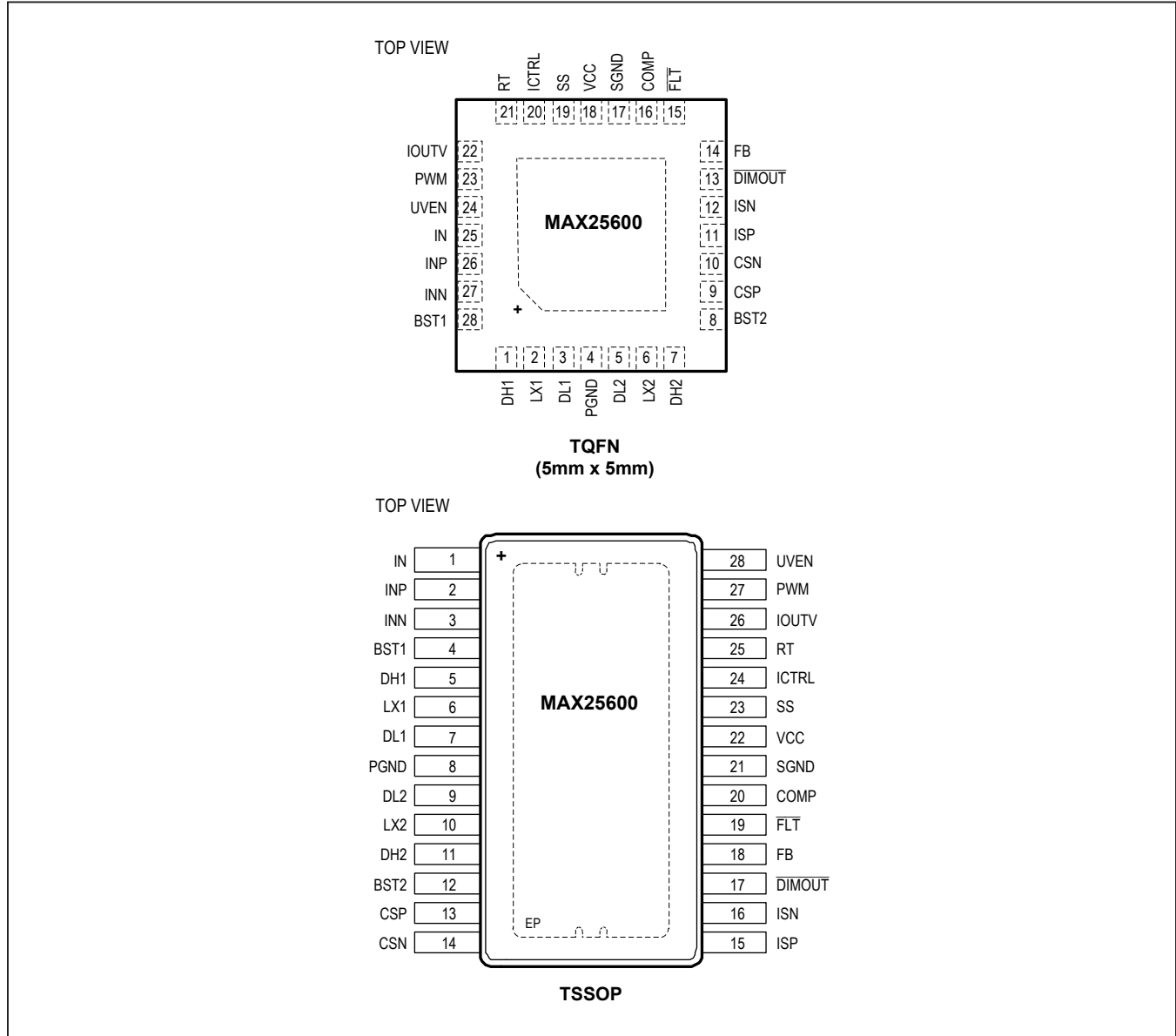


Typical Operating Characteristics (continued)

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)



Pin Configuration





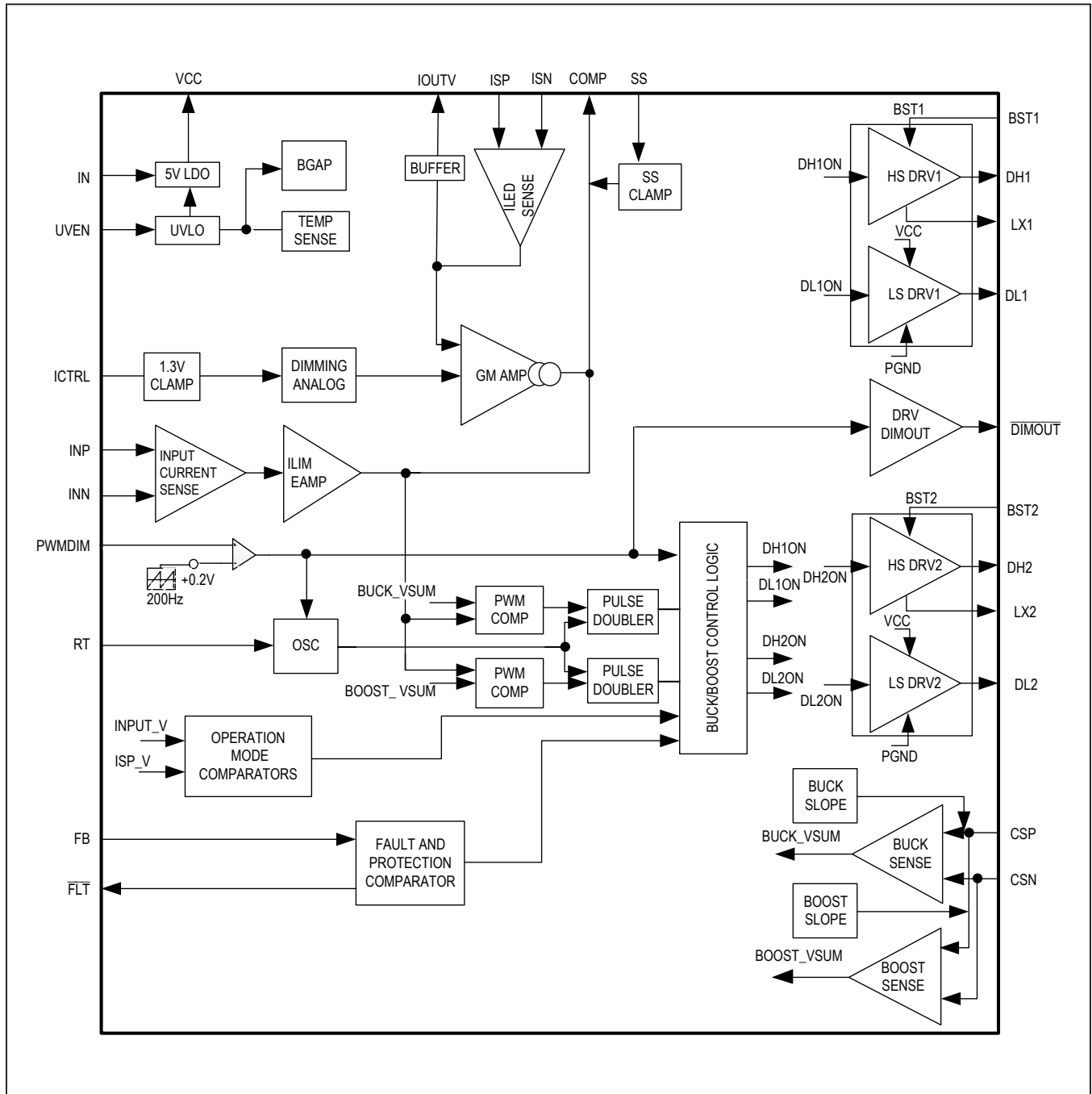
## Pin Description

PIN		NAME	FUNCTION
TQFN	TSSOP		
1	5	DH1	Top Gate Drive for <a href="#">Buck</a> Section of the MAX25600. Drives the gate of the top n-channel MOSFET.
2	6	LX1	Buck-Side Switching Node. LX1 pin swings from a diode voltage drop below ground up to $V_{IN}$ .
3	7	DL1	Bottom Gate Drive for <a href="#">Buck</a> Section of the MAX25600. Drives the gate of the bottom n-channel MOSFET.
4	8	PGND	Power Ground Connection
5	9	DL2	Bottom Gate Drive for the <a href="#">Boost</a> Section of the MAX25600. Drives the gate of the bottom n-channel MOSFET.
6	10	LX2	Switching Node of <a href="#">Boost</a> Section of the MAX25600. LX2 pin swings from a diode voltage drop below ground up to $V_{OUT}$ .
7	11	DH2	Top Gate Drive for <a href="#">Boost</a> Section of the MAX25600. Drives the gate of the top n-channel MOSFET.
8	12	BST2	High-Side Power Supply for High-Side Gate Drive for <a href="#">Boost</a> Section. Connect a 0.1 $\mu$ F ceramic capacitor from BST2 to LX2.
9	13	CSP	Positive Input to the Current-Sense Comparator for the Average-Current-Mode Controller
10	14	CSN	Negative Input to the Current-Sense Comparator for the Average-Current-Mode Controller
11	15	ISP	Positive LED Current-Sense Input. The voltage between ISP and ISN is proportionally regulated to 1.3V or $(V_{CTRL} - 0.2)/(5 \times RCS\_LED)$ , whichever is less.
12	16	ISN	Negative LED Current-Sense Input
13	17	$\overline{DIMOUT}$	External Dimming p-Channel MOSFET Gate Driver
14	18	FB	Overvoltage-Protection Input for the LED String. Connect a resistive divider between the output, FB, and GND. When the voltage on FB exceeds 1.23V, a fast-acting comparator immediately stops PWM switching and pulls $\overline{DIMOUT}$ high to disconnect the LED string from the output. $V_{OVP} = 1.23 \frac{(R_{FB1} + R_{FB2})}{R_{FB2}}$
15	19	$\overline{FLT}$	Active-Low, Open-Drain Fault Indicator Output. See the <a href="#">Fault Indicator (<math>\overline{FLT}</math>)</a> section.
16	20	COMP	Compensation-Network Connection. For proper compensation, connect a suitable RC network from COMP to SGND.
17	21	SGND	Signal Ground Connection
18	22	$V_{CC}$	5V Regulator Output. Connect a minimum 2.2 $\mu$ F ceramic capacitor from $V_{CC}$ to SGND for stable operation.
19	23	SS	Soft-Start Pin. A minimum 10nF capacitor is recommended on this pin.

## Pin Description (continued)

PIN		NAME	FUNCTION
TQFN	TSSOP		
20	24	ICTRL	<p>Analog Dimming-Control Input. Connect an analog voltage from 0 to 1.3V for analog dimming of LED current.</p> $I_{LED} = \frac{(V_{ICTRL} - 0.2V)}{5 \times R_{CS\_LED}}$ <p>Bypass ICTRL to GND with at least a 10nF ceramic capacitor for noise filtering. Not needed if <math>V_{REF1} &gt; 1.3V</math>.</p>
21	25	RT	Oscillator Switching-Frequency Programming. Connect a resistor ( $R_{RT}$ ) from RT to SGND to set the internal clock frequency. $f_{OSC}(kHz) = 20000/R_{RT} (k\Omega)$ .
22	26	IOUTV	Analog Voltage Indication of LED Current. Bypass to SGND with a 0.1µF ceramic capacitor.
23	27	PWM	<p>Dimming Control Input. Connect PWM to an external 3.3V or 5V PWM signal for PWM dimming. For analog-voltage-controlled PWM dimming, connect PWM to <math>V_{CC}</math> through a resistive voltage-divider with voltage between 0.2V and 3V. The dimming frequency is 200Hz under these conditions, and the duty cycle is <math>(V_{PWM} - 0.2)/2.8</math>.</p> <p>Connect PWM to SGND to turn off the LEDs. Connect PWM to <math>V_{CC}</math> for 100% duty cycle. Bypass PWM to SGND with a 0.1µF ceramic capacitor when using analog PWM.</p>
24	28	UVEN	<p>Undervoltage-Lockout (UVEN) Threshold/Enable Input. UVEN is a dual-function adjustable UVLO threshold input with an enable feature. Connect UVEN to <math>V_{IN}</math> through a resistive voltage-divider to program the UVLO threshold. The UVLO threshold is given by</p> $V_{UVLO} = 1.23 \frac{(R_{UVEN1} + R_{UVEN2})}{R_{UVEN2}}$
25	1	IN	Positive Power-Supply Input. Bypass IN to PGND with at least a 1µF ceramic capacitor.
26	2	INP	Positive Input for the Input Current Limit
27	3	INN	Negative Input for the Input Current Limit. Add an RC low-pass filter from INN to INP to provide a filtered DC voltage from INP to INN. The resistor should be 100Ω and the capacitor should be 0.1µF.
28	4	BST1	High-Side Power Supply for High-Side Gate Drive for <i>Buck</i> Section. Connect a 0.1µF ceramic capacitor from BST1 to LX1.
—	—	EP	Exposed Pad. Connect EP to a large-area contiguous copper ground plane for effective power dissipation. Do not use as the main IC ground connection. EP must be connected to SGND.

Functional Block Diagram



## Detailed Description

The MAX25600 is a synchronous 4-switch buck-boost LED driver controller. The controller regulates the LED current for LED string voltages from 0V to 60V. The MAX25600 can be used as a seamless buck-boost LED driver for applications that require an efficient buck-boost LED driver with synchronous rectification. The MAX25600 is ideal for high-power applications that require a current source with PWM dimming capability.

The device provides seamless transition between buck, boost, and buck-boost modes depending on the ratio of input to output voltage. The MAX25600 is ideal for LED driver applications in automotive, industrial, and other LED lighting applications. A fault flag indicates open LED, shorted LED, or thermal-shutdown conditions. The device uses Maxim's proprietary average-current-mode control scheme and allows adjustable 200kHz to 700kHz fixed-frequency operation. In addition,  $\pm 6\%$  triangular spread spectrum is added internally to the oscillator to improve EMI performance. The MAX25600 provides both analog and digital PWM dimming, and has built-in analog PWM dimming at a dimming frequency of 200Hz. Adjustable soft-start limits the current peaks and voltage overshoots at startup. The MAX25600 integrates a high-side p-channel dimming MOSFET driver for PWM dimming applications that require fast rising and falling edges of the LED current. It also features robust output open and short protection, is AEC qualified, and is suitable for automotive applications.

## V<sub>CC</sub> Regulator

The V<sub>CC</sub> supply is the low-voltage analog supply for the chip and derives power from the input voltage from IN to PGND. An internal power-on-reset (POR) monitors the V<sub>CC</sub> voltage and the IN voltage. A POR is generated when V<sub>CC</sub> drops below its UVLO threshold, causing the IC to reset. The chip exits reset state once the input voltage goes back up and the V<sub>CC</sub> linear regulator output is back in regulation.

## Undervoltage Lockout

The MAX25600 features an adjustable UVLO using the enable input (UVEN). Connect UVEN to V<sub>IN</sub> through a resistive divider to set the UVLO threshold. The MAX25600 is enabled when V<sub>UVEN</sub> exceeds the 1.24V (typ) threshold. UVEN also functions as an enable/disable input to the device. Drive UVEN low to disable the output, and high to enable the output.

## H-Bridge Operation

The H-bridge configuration using the MAX25600 is shown in [Figure 1](#). The H-bridge consists of the four switches N1, N2, N3, and N4. Switches N1 and N2 are in series with the input voltage, and switches N3 and N4 are connected to the output. Inductor L is connected as shown. There are four different configurations in which the circuit operates, depending on the ratio of the input and output voltage.

[Table 1](#) shows the status of the switches in the H-Bridge in each configuration.

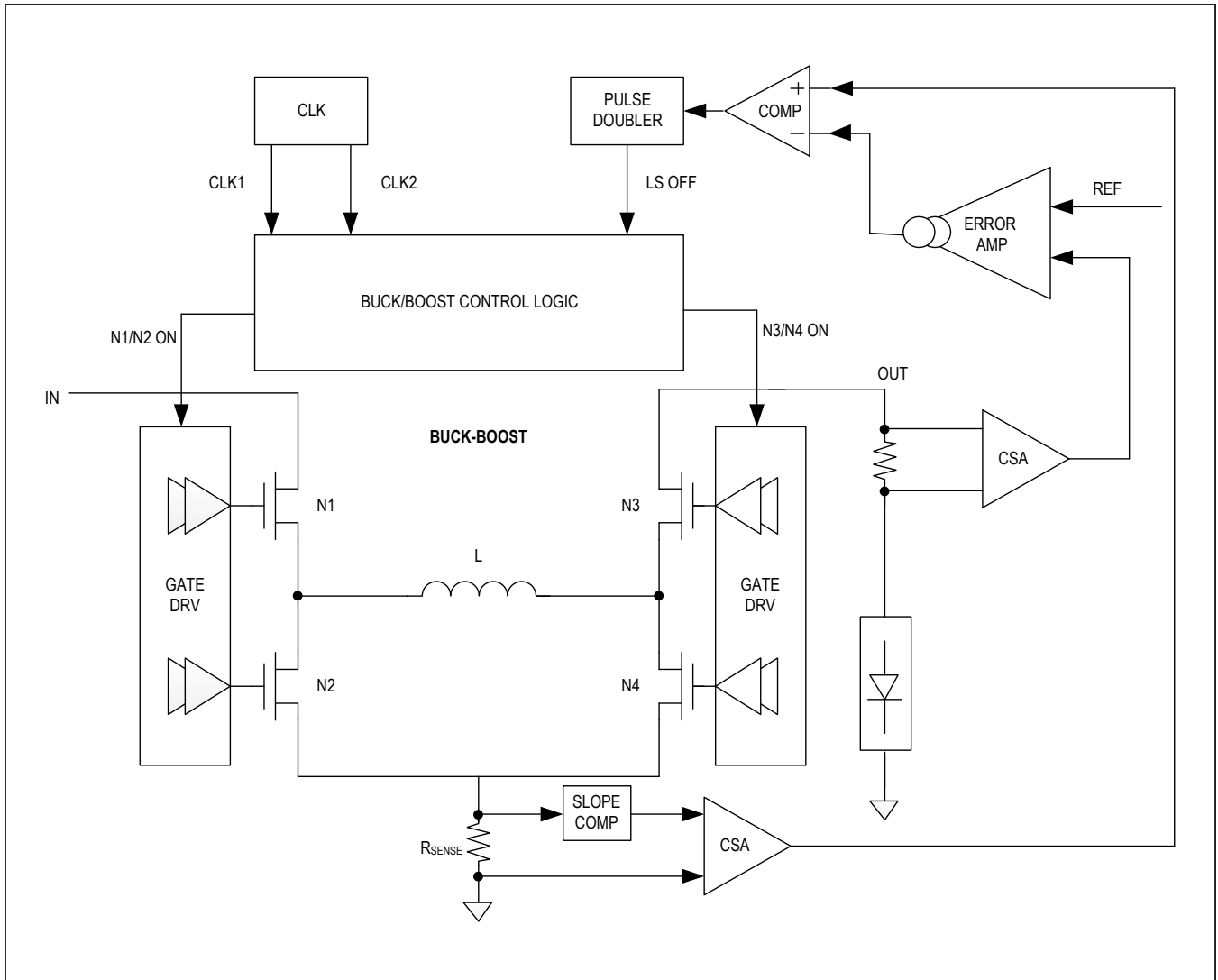


Figure 1. H-Bridge LED Driver

Table 1. Status of Switches in H-Bridge

SWITCH	BOOST MODE	BUCK-BOOST MODE (BOOST CONTROL)	BUCK-BOOST MODE (BUCK CONTROL)	BUCK MODE
N1	ON	PWM	PWM	PWM
N2	OFF	PWM	PWM	PWM
N3	PWM	PWM	PWM	ON
N4	PWM	PWM	PWM	OFF

**Buck Mode**

When the input voltage is much higher than the output voltage, then the MAX25600 operates in buck mode. In this configuration, switch N3 is always on and switch N4 is always off. Switch N2 is turned on at the beginning of the clock cycle (CLK1), and the inductor current ramps down. The MAX25600 uses an average-current-mode control scheme to determine the ON pulse width for switch N2. Once N2 is turned off, N1 is turned on. Switches N1 and N2 will alternate, behaving like a synchronous buck regulator.

**Boost Mode**

When the input voltage is much lower than the output voltage, then the MAX25600 operates in boost mode. In this configuration, switch N1 is always on and switch N2 is always off. Switch N4 is turned on at the beginning of the clock cycle (CLK2), and the inductor current ramps up. The MAX25600 uses an average-current-mode control scheme to determine the ON pulse width for switch N4. Once N4 is turned off, N3 is turned on. Switches N3 and N4 will alternate, behaving like a synchronous boost regulator.

**Buck-Boost Mode**

When  $V_{IN}$  is close to  $V_{OUT}$ , the MAX25600 operates in buck-boost configuration. In this configuration, all four switches have PWM voltages on the gates, and all four switches are switching at the switching frequency. There are two different configurations in the buck-boost mode.

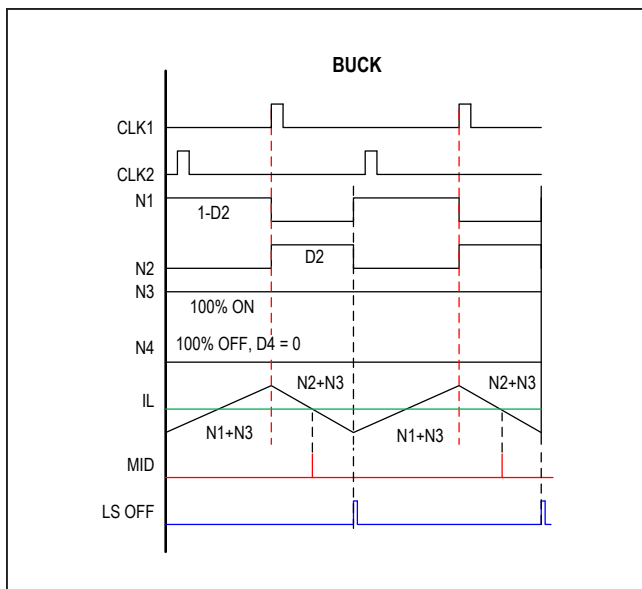


Figure 2. Buck-Mode Waveforms

When  $V_{IN}$  is slightly higher than  $V_{OUT}$ , the MAX25600 operates in the buck-boost region, where switch N2 is controlled by the PWM. Switch N4 is turned on for the beginning 16.7% cycle triggered by clock CLK2, and switch N3 is turned on for the remaining 83.3% cycle. Control of switch N2 is initiated by clock CLK1. N2 is turned on and N1 is turned off when CLK1 goes high. The MAX25600 uses average-current-mode control to determine the ON pulse width of N2. When N2 is turned off, N1 is turned on immediately

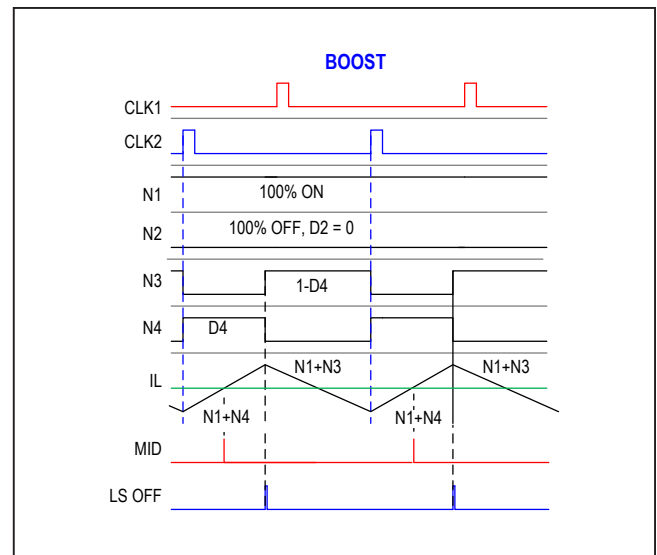


Figure 3. Boost-Mode Waveforms

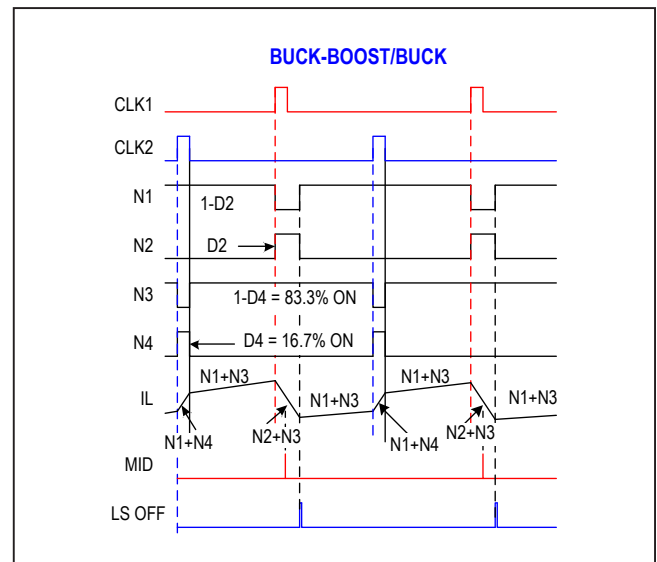


Figure 4. Buck-Boost Buck-Mode Waveforms

When  $V_{IN}$  is slightly lower than  $V_{OUT}$ , the MAX25600 operates in the buck-boost region where switch N4 is controlled by the PWM. Switch N2 is turned on for the beginning 16.7% cycle triggered by clock CLK1 and switch N1 is turned on for the remaining 83.3% cycle. Control of switch N4 is initiated by clock CLK2. N4 is turned on and N3 is turned off when CLK2 goes high. The MAX25600 uses average-current-mode control to determine the ON pulse width of N4. When N4 is turned off, N3 is turned on immediately.

**Maximum Proprietary Average-Current-Mode Control**

A novel average-current-mode control scheme is used in this current-mode buck-boost H-bridge converter. Instead of regulating the peak/valley current in buck/boost mode, average inductor current is regulated regardless of operating mode. As long as the inductor current is not changed abruptly during the mode transitions, the command signal remains at a nearly constant value unrelated to operating modes. As a result, seamless mode transition can be achieved. Since the converter is operating at a fixed switching frequency, additional slope compensation must be added to the inductor current-sense signal, which may require slight changes to the command signal to compensate for the error introduced by the slope compensation signal.

**Average-Current-Mode Buck**

When operating in buck mode, the pulse doubler controls the duty cycle of switch N2. The pulse width of switch N2 is  $2x$  tpw.

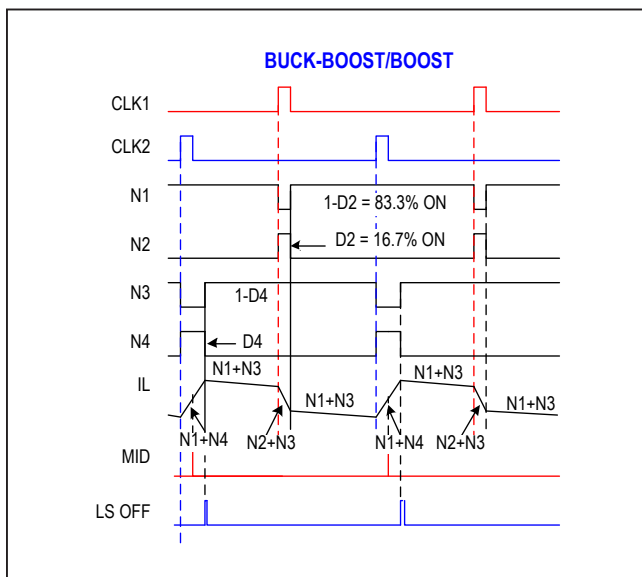


Figure 5. Buck-Boost Boost-Mode Waveforms

**Average Current Mode Boost**

When operating in boost mode, the pulse doubler controls the duty cycle of switch N4. The pulse width of switch N4 is  $2x$  tpw.

**Soft-Start**

The SS pin can be used to program soft-start by connecting an external capacitor from SS pin to ground. An internal  $15\mu A$  pullup current charges the capacitor on the SS pin, creating a voltage ramp. An internal diode from COMP to the SS pin clamps the voltage on the COMP pin. A ceramic capacitor of  $0.1\mu F$  or higher is recommended on the SS pin.

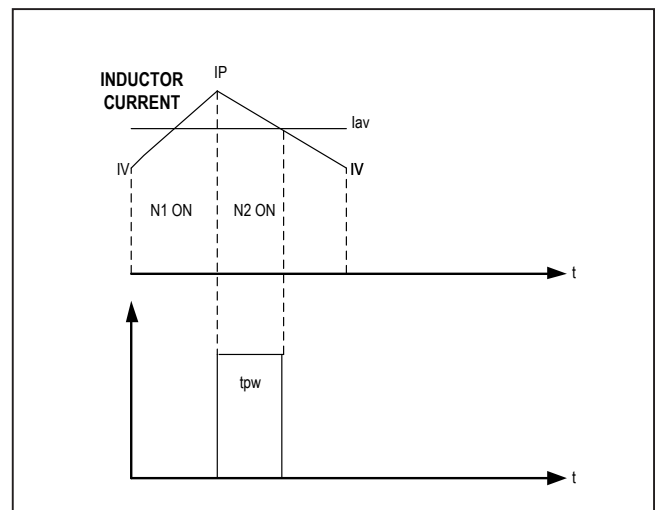


Figure 6. Pulse Doubler Buck

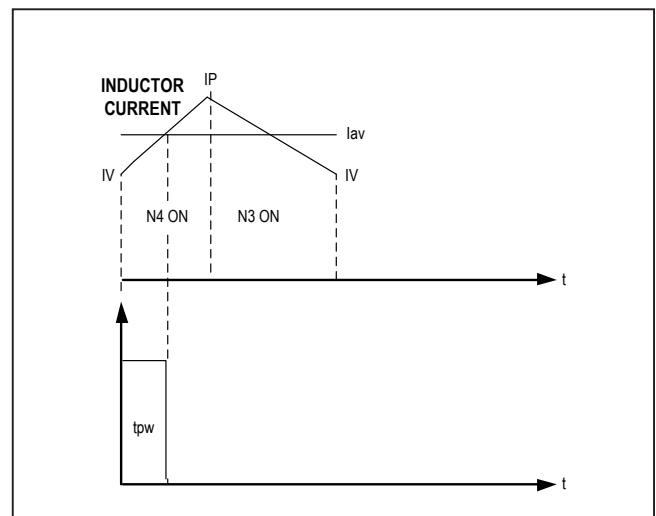


Figure 7. Pulse Doubler Boost

**Switching Frequency**

The internal oscillators of the MAX25600 are programmable from 200 kHz to 700 kHz using a single resistor at RT. Use the following formula to calculate the switching frequency:

$$f_{OSC}(kHz) = 20000/R_{RT}(k\Omega)$$

where  $R_{RT}$  is the resistor from RT to SGND.

The switching frequency oscillator in MAX25600 is synchronized to the leading edge of the PWM dimming pulse on input PWMDIM. The MAX25600 has built-in frequency dithering of  $\pm 6\%$  of the programmed frequency to alleviate EMI problems.

**Analog Dimming (ICTRL)**

The MAX25600 offers an analog dimming-control input (ICTRL). The voltage at ICTRL sets the LED current level when  $V_{ICTRL} < 1.2V$ . The LED current can be linearly adjusted from zero with the voltage on ICTRL. For  $V_{ICTRL} > 1.3V$ , an internal reference sets the LED current. The maximum withstand voltage of this input is 5.5V. The LED current is guaranteed to be at zero when the ICTRL voltage is at or below 0.18V. The LED current can be linearly adjusted from zero to full scale for the ICTRL voltage in the range of 0.2V to 1.2V.

**PWM Dimming (PWM)**

In the MAX25600, the PWM functions with either analog or PWM control signals. Once the internal pulse detector

detects three successive edges of a PWM signal with a frequency between 30Hz and 2kHz, the MAX25600 synchronizes to the external signal and pulse-width modulates the LED current at the external DIM input frequency with the same duty cycle as the PWM input. If an analog control signal is applied to the PWM pin, the MAX25600 compares the DC input to an internally generated 200Hz ramp to pulse-width-modulate the LED current ( $f_{DIM} = 200Hz$ ). The output-current duty cycle is linearly adjustable from 0% to 100% ( $0.2V < V_{PWM} < 3.0V$ ). Use the following formula to calculate the voltage  $V_{PWM}$  necessary for a given output-current duty cycle D:

$$V_{PWM} = (D \times 2.8) + 0.2V$$

where  $V_{PWM}$  is the voltage applied to PWM pin, in volts.

**Input-Current Limit**

The MAX25600 features circuitry that limits the input current during line dropouts. If desired, this circuitry can be disabled by shorting INN and INP pins together. If DC input-current limiting is desired during low input voltages, then a current-sense resistor  $R_{IN}$  should be used. Use the circuit shown in [Figure 8](#) to limit the input current.

An RC filter and a series resistor to INN should be used as shown. The input current is limited to  $I_{NMAX}$  where  $I_{NMAX}$  is given by the following equation:

$$I_{NMAX} = 0.1/R_{IN}$$

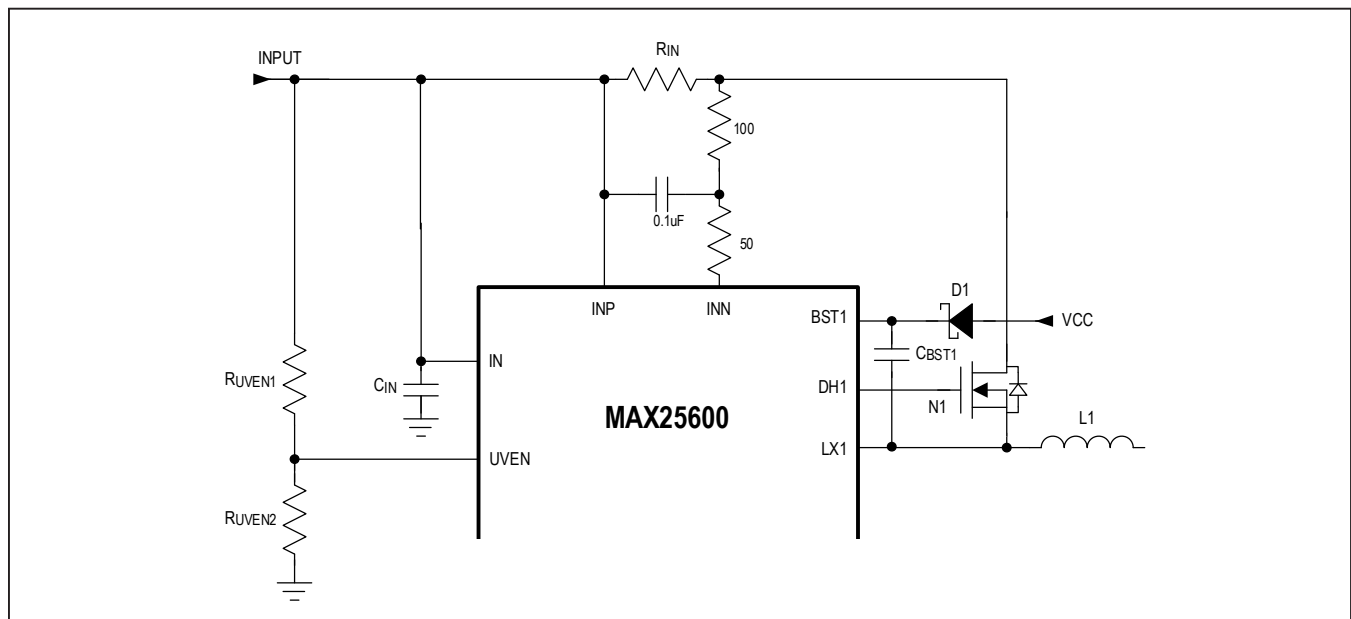


Figure 8. Input-Current Limit



**Output-Current Monitor (IOUTV)**

The MAX25600 includes a current monitor on the IOUTV pin. The IOUTV voltage is an analog voltage indication of the LED current when DIM is high. The voltage on the IOUTV pin is given by the following equation:

$$V_{IOUTV} = I_{LED} \times R_{CS\_LED} \times 5 + 0.2V$$

**Control Loop and Error Amplifier**

The sensed inductor current is controlled by the voltage on the COMP pin, which is the output of the error amplifier. The error amplifier has three inputs.

The control input ICTRL sets the LED current.

**Overvoltage Protection (FB)**

Pin FB sets the overvoltage-threshold limit across the LEDs. Use a resistive divider between ISP to FB and SGND to set the overvoltage-threshold limit. An internal overvoltage-protection comparator senses the differential voltage across FB and SGND. If the differential voltage is greater than 1.24V, the switching is turned off,  $\overline{DIMOUT}$

goes high, and  $\overline{FLT}$  asserts. When the differential voltage drops by 70mV, switching is enabled if PWM is high and  $\overline{DIMOUT}$  goes low.  $\overline{FLT}$  deasserts only if PWM is high and  $V_{(ISP - ISN)}$  is  $> 20mV$ .

**Fault Indicator  $\overline{FLT}$** 

The MAX25600 features an active-low, open-drain fault indicator ( $\overline{FLT}$ ).  $\overline{FLT}$  asserts when one of the following conditions occur:

- Overvoltage or open across the LED string
- Short-circuit condition across the LED string
- Overtemperature condition

For overvoltage or open across the LED string, the  $\overline{FLT}$  asserts only when an overvoltage occurs with the PWM in the high state. Once asserted, the  $\overline{FLT}$  remains low and will only change state if PWM is high, the overvoltage condition is removed, and the voltage across the LED current-sense resistor is greater than 20mV. The  $\overline{FLT}$  signal never changes state when PWM is low.



## Applications Information

Figure 10 shows a functional MAX25600 application circuit. External-component selection is driven by the input voltage range and LED string voltage and current requirements.

### V<sub>CC</sub> Regulator

The internal 5V regulator is used to power the internal control circuitry inside the MAX25600. This regulator can provide a load of 50mA to internal and external circuitry, and requires an external ceramic capacitor for stable operation. A 2.2μF ceramic capacitor is adequate for most applications. Place the ceramic capacitor close to the IC to minimize trace length to the internal V<sub>CC</sub> pin and also to the IC ground. Choose a low-ESR, X7R ceramic capacitor for optimal performance. The IC powers up once the voltage on V<sub>CC</sub> crosses the undervoltage lockout (V<sub>CC</sub> UVLO) rising threshold and shuts down when V<sub>CC</sub> falls below the (V<sub>CC</sub> UVLO) falling threshold.

### Programming Input UVLO Threshold

The input UVLO threshold is set by resistors R<sub>UVEN1</sub> and R<sub>UVEN2</sub> (see the Simplified Application Circuit). The MAX25600 turns on when the voltage across R<sub>UVEN2</sub> exceeds 1.24V, the UVLO threshold. Use the following equation to set the desired UVLO threshold:

$$V_{UVEN} = 1.24 \times (R_{UVEN1} + R_{UVEN2})/R_{UVEN2}, \text{ in volts}$$

The UVEN pin can also be used as a separate enable pin where an external logic signal can switch the MAX25600 on and off.

### Programming the LED Current

Normal sensing of the LED current should be done on the high side, where the LED current-sense resistor is connected to the anode of the LED string. The LED current is programmed using the resistor R<sub>LED</sub> (see the [Simplified Application Circuit](#)). The LED current can also be programmed by adjusting the voltage on ICTRL when V<sub>CTRL</sub> ≤ 1.2V (analog dimming). The current is given by the following equation:

$$I_{LED} = (V_{CTRL} - 0.2)/(5 \times R_{CS\_LED})$$

For voltages greater than 1.3V on the ICTRL pin, the LED current is clamped to the current given by the following equation:

$$I_{LED} = (1.3 - 0.2)/(5 \times R_{CS\_LED})$$

LED current can also be sensed on the ground side, if needed. In some applications, the LED current can be sensed by a current-sense resistor R<sub>LED</sub> to ground.

### Programming the Switching Frequency

The internal oscillator of the MAX25600 is programmable from 200kHz to 700kHz using a single resistor at RT. Use the following formula to calculate the value of the resistor

$$R_{RT}:R_{RT}(k\Omega) = 20000/f_{SW}(kHz)$$

where f<sub>SW</sub> is the desired switching frequency, in kHz.

An additional ±6% spread spectrum is added internally to the oscillator to improve EMI performance.

### Programming Input-Current Limit

The MAX25600 has an input current-sense amplifier that can be used to limit the input, as calculated by the following equation:

$$I_{IN} = 0.1/R_{IN}$$

A low-pass RC filter is needed for loop stability. For most applications, a 100Ω resistor R<sub>F</sub> and a 100nF capacitor C<sub>F</sub> is sufficient. An added 50Ω resistor R<sub>INN</sub> in series with the INN pin should be added, as shown in [Figure 10](#).

### Setting the Overvoltage Threshold

The overvoltage threshold is set by resistors R<sub>OVP1</sub> and R<sub>OVP2</sub> (see the Simplified Application Circuit). The overvoltage circuit in the MAX25600 is activated when the voltage on FB with respect to GND exceeds 1.24V. Use the following equation to set the desired overvoltage threshold:

$$V_{OVP} = 1.24 \times (R_{OVP1} + R_{OVP2})/R_{OVP2}$$

### Inductor Selection

In the boost converter, the average inductor current varies with the line voltage. The maximum average current occurs at the lowest line voltage. When operating the boost converter, the average inductor current is equal to the input current. Calculate maximum duty cycle using the following equation:

$$D_{MAX} = (V_{LED} - V_{INMIN})/V_{LED}$$

where V<sub>LED</sub> is the forward voltage of the LED string, in volts, and V<sub>INMIN</sub> is the minimum input supply voltage, in volts.

Use the following equations to calculate the maximum average inductor current (I<sub>LAVG</sub>), peak-to-peak inductor-current ripple (ΔI<sub>L</sub>), and peak inductor current (I<sub>LP</sub>):

Maximum average inductor current is given by

$$I_{LAVG} = I_{LED}/(1 - D_{MAX})$$

Allowing the peak-to-peak inductor ripple to be ΔI<sub>L</sub>, the peak inductor current is given by

$$I_{LP} = I_{LAVG} + 0.5 \times \Delta I_L$$

The inductance value (L) of inductor L1, in Henrys (H), is calculated as

$$L = V_{INMIN} \times D_{MAX} / (f_{SW} \times \Delta I_L)$$

where  $f_{SW}$  is the switching frequency in Hertz,  $V_{INMIN}$  is in volts, and  $\Delta I_L$  is in amperes.

Choose an inductor that has a minimum inductance greater than the calculated value. The current rating of the inductor should be higher than  $I_{LP}$  at the operating temperature.

When operating in buck mode, the average inductor current is the same as the LED current. The peak inductor current occurs at the maximum input line voltage where the duty cycle is at the minimum:

$$D_{MIN} = V_{LED} / V_{INMAX}$$

where  $V_{LED}$  is the forward voltage of the LED string, in volts, and  $V_{INMAX}$  is the maximum input supply voltage, in volts.

The peak inductor current is given by

$$I_{LP} = I_{LED} + 0.5 \times \Delta I_L$$

The inductance value (L) of inductor L1, in Henrys, is calculated as

$$L = (V_{INMAX} - V_{LED}) \times D_{MIN} / (f_{SW} \times \Delta I_L)$$

where  $f_{SW}$  is the switching frequency in Hertz,  $V_{INMAX}$  is in volts, and  $\Delta I_L$  is in amperes.

Choose an inductor that has a minimum inductance greater than the calculated value. The chosen inductor for the application should have an inductance that is the larger of the two calculated values from the boost and the buck configurations.

### Input Capacitor Selection

The discontinuous input-current waveform of the buck converter causes large ripple currents in the input capacitor. The switching frequency, peak inductor current, and the allowable peak-to-peak voltage ripple reflected back to the source dictate the capacitance requirement. The input ripple consists of  $\Delta V_Q$  (caused by the capacitor discharge) and  $\Delta V_{ESR}$  (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple-current capability at the input. A good starting point for selection of  $C_{IN}$  is to use an input-voltage ripple of 2% to 10% of  $V_{IN}$ .  $C_{IN\_MIN}$  can be selected as follows:

$$C_{IN\_MIN} = 2(I_{LED} \times t_{ON}) / \Delta V_{IN}$$

where  $t_{ON}$  is the on-time pulse width per switching cycle.

When selecting a ceramic capacitor, pay special attention to the operating conditions of the application. Ceramic capacitors can lose more than half of their capacitance at their rated DC-voltage bias and also lose capacitance with extremes in temperature. In applications with PWM

dimming where the input connections to the source have wiring inductance, additional electrolytic capacitors may need to be added at the input to prevent large sags and surges in the input voltages during the PWM rising and falling edges. These line sags and surges can also cause the H-bridge to switch between boost, buck-boost, and buck configurations in one dimming cycle, which is undesirable and can cause flicker problems.

### Output Capacitor Selection

The function of the output capacitor is to reduce the output ripple to acceptable levels. The ESR, ESL, and bulk capacitance of the output capacitor contribute to the output ripple. In most applications, the output ESR and ESL effects can be dramatically reduced by using low-ESR ceramic capacitors. To reduce the ESL and ESR effects, connect multiple ceramic capacitors in parallel to achieve the required bulk capacitance. To minimize audible noise generated by the ceramic capacitors during PWM dimming, it may be necessary to minimize the number of ceramic capacitors on the output. In these cases, an additional electrolytic or tantalum capacitor provides most of the bulk capacitance.

For simplicity, assume that the contributions from ESR and the bulk capacitance are equal, allowing 50% of the ripple for the bulk capacitance. The capacitance for boost configuration is given by

$$C_{BOOSTOUT} > (I_{LED} \times 2 \times D_{MAX}) / (V_{OUTRIPPLE} \times f_{SW})$$

where  $I_{LED}$  is in amperes,  $C_{OUT}$  is in farads,  $f_{SW}$  is in Hertz, and  $V_{OUTRIPPLE}$  is in volts.

The remaining 50% of allowable ripple is for the ESR of the output capacitor. Based on this, the ESR of the output capacitor is given by

$$ESR_{COUT} < (V_{OUTRIPPLE} \times V_{INMIN}) / (2 \times V_{LED} \times I_{LED})$$

When operating in buck configuration, the required capacitance is given by

$$C_{BUCKOUT} > (V_{INMIN} - V_{LED}) \times V_{LED} / (V_{OUTRIPPLE} \times 2 \times L \times V_{INMAX} \times f_{SW} \times 2)$$

Based on this, the ESR of the output capacitor is given by

$$ESR_{COUT} < (V_{OUTRIPPLE} \times L \times f_{SW}) / (2 \times V_{LED} \times (1 - D_{MIN}))$$

### H-Bridge Control Loop Current-Sense Selection ( $R_{SENSE}$ )

The current-sense resistor on the low side of the H-bridge is chosen based on maximum LED current and the total output power. The control loop uses average-current-mode control in both boost and buck mode to control the H-bridge switches. When operating in boost mode, the maximum average load current at minimum input voltage

$V_{INMIN}$  is given by  $I_{OUT(BOOST\_MAX)}$ .  $I_{OUT(BOOST\_MAX)}$  at minimum input voltage is given by

$$I_{OUT(BOOST\_MAX)} = \frac{50 \text{ mV}}{R_{SENSE}} \times \frac{V_{INMIN}}{V_{OUT}}$$

When operating in buck mode, the maximum average inductor current is given by  $I_{OUT(BUCK\_MAX)}$ . The maximum current occurs at the maximum LED current in buck mode.

$$I_{OUT(BUCK\_MAX)} = \frac{50 \text{ mV}}{R_{SENSE}}$$

### Slope Compensation

Slope compensation should be added to fixed-frequency converters operating in continuous-conduction mode with more than 50% duty cycle to avoid current-loop instability and sub-harmonic oscillations.

In the MAX25600, the slope-compensating ramp is added to the current-sense signal before it is fed to the PWM comparator. Connect a resistor ( $R_{SC}$ ) from CS to the switch current-sense resistor terminal for programming the amount of slope compensation.

The device generates a current ramp with a slope of  $50\mu\text{A}/t_{OSC}$  for slope compensation. The current-ramp signal is forced into an external resistor ( $R_{SC}$ ) connected between CS and the source of the external MOSFET, thereby adding a programmable slope-compensating voltage ( $V_{SLOPE}$ ) at the current-sense input CS. Therefore:

$$dV_{SLOPE}/dt = (R_{SC} \times 50\mu\text{A})/t_{OSC}$$

The slope-compensation voltage that must be added to the current signal at minimum line voltage, with margin of 1.5x, is as follows:

Boost configuration:

$$V_{SLOPE} = D_{MAX} \frac{(V_{LED} - 2V_{INMIN}) \times R_{SENSE}}{L \times f_{SW}} \times 2 \times 1.5$$

Buck configuration:

$$V_{SLOPE} = D_{MAX} \frac{V_{LED} \times R_{SENSE}}{L \times f_{SW}} \times 2 \times 1.5$$

### Control Loop Compensation

The LED current-control loop comprising the switching converter, LED current amplifier, and the error amplifier should be compensated for stable control of the LED current. For most applications the design needs to be stabilized for boost mode of operation and the buck mode

should be automatically stable. The switching converter small-signal transfer function has a right half-plane (RHP) zero for the boost configuration as the inductor current is in continuous-conduction mode. The RHP zero adds a 20dB/decade gain together with a 90° phase lag, which is difficult to compensate. The easiest way to avoid this zero is to roll off the loop gain to 0dB at a frequency less than 1/5 of the RHP zero frequency with a -20dB/decade slope. The worst-case RHP zero frequency ( $f_{ZRHP}$ ) is calculated as follows:

Boost configuration:

$$f_{ZRHP} = \frac{V_{LED} \times (1 - D_{MAX})^2}{2\pi \times L \times I_{LED}}$$

The switching converter small-signal transfer function also has an output pole for the boost configuration. The effective output impedance that determines the output pole frequency together with the output filter capacitance is calculated as:

Boost configuration:

$$R_{OUT} = \frac{(R_{LED} + R_{CS\_LED}) \times V_{LED}}{(R_{LED} + R_{CS\_LED}) \times I_{LED} + V_{LED}}$$

where  $R_{LED}$  is the dynamic impedance of the LED string at the operating current.

The output pole frequency is calculated as follows:

$$f_P = \frac{1}{2\pi R_{OUT} C_{OUT}}$$

The feedback-loop compensation is done by connecting a resistor ( $R_{COMP}$ ) and capacitor ( $C_{COMP}$ ) in series from COMP to GND.  $R_{COMP}$  is chosen to set the high frequency integrator gain for fast transient response, while  $C_{COMP}$  is chosen to set the integrator zero to maintain loop stability. For optimum performance, choose the components using the following equations:

$$f_C = 0.2 \times f_{ZRHP}$$

$$R_{COMP} = \frac{(f_{ZRHP} \times R_{SENSE})}{(f_p \times (1 - D_{MAX}) \times R_{CS\_LED} \times 5 \times G_M)}$$

where  $G_M = 1.8\text{mS}$  (transconductance of error amplifier),  $R_{SENSE}$  = Current-sense resistor on low side of H-Bridge, and  $R_{CS\_LED}$  = LED current-sense resistor.

$$C_{COMP} = \frac{1}{2 \times 3.14 \times R_{COMP} \times 5 \times f_p}$$

Typical Application Circuits

MAX25600 in Buck-Boost LED Driver Application

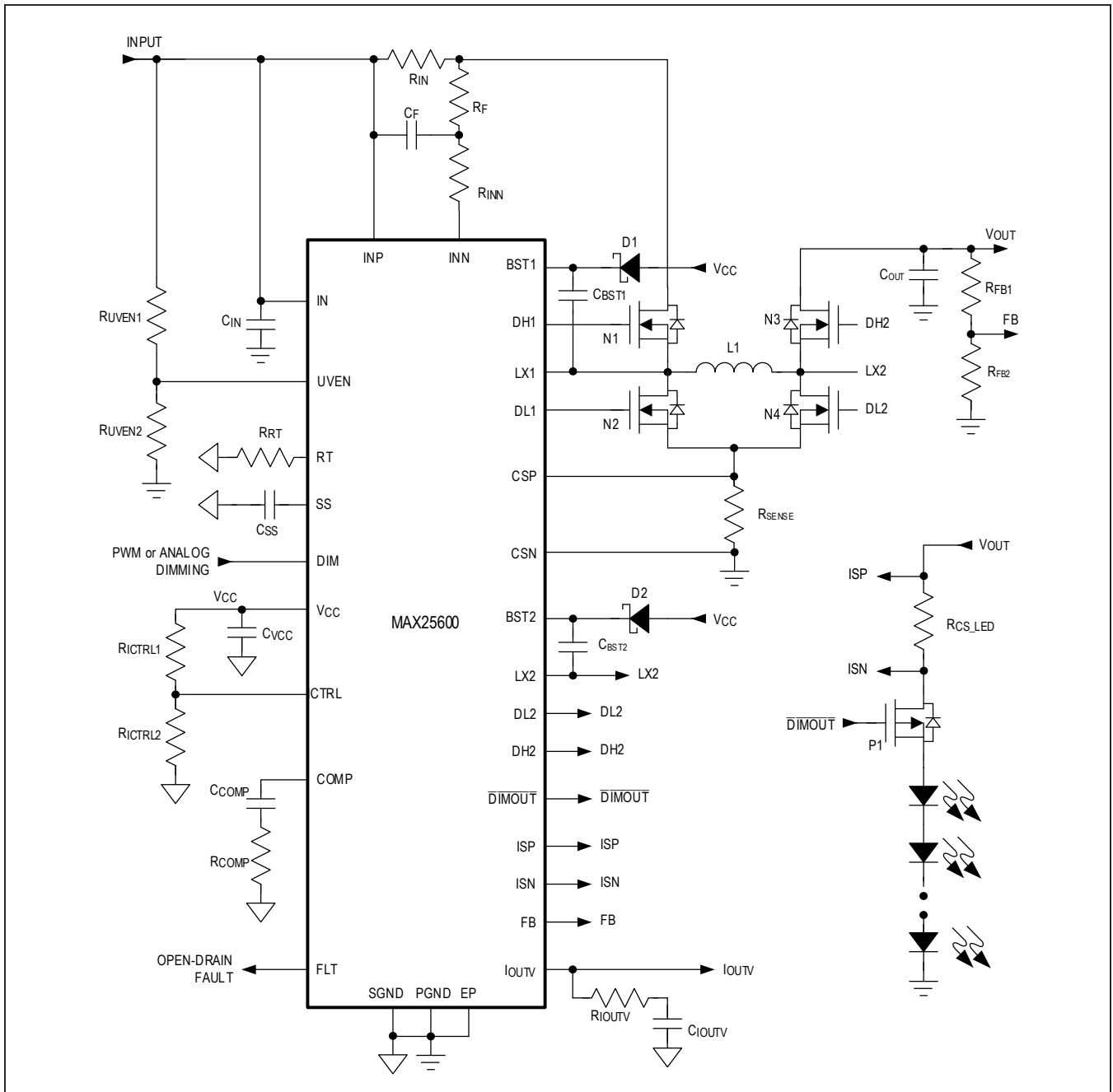


Figure 10. MAX25600 in Buck-Boost LED Driver Application

## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX25600ATI/VY+	-40°C to +125°C	28 TQFN-Cu
MAX25600AUI/V+	-40°C to +125°C	28 TSSOP-Cu

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

Y Denotes Side-Wettable

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/18	Initial release	—
1	1/19	Added future-product notation to MAX25600AUI/V+** in <a href="#">Ordering Information</a> table	23
2	10/19	Updated <a href="#">Electrical Characteristics</a> ; updated <a href="#">Applications Information</a> ; removed future-product notation from MAX25600AUI/V+** in <a href="#">Ordering Information</a> table	3–5, 21, 23

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at <https://www.maximintegrated.com/en/storefront/storefront.html>.

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