DEMO CIRCUIT 1704A
QUICK START GUIDE

LTC4280

Hot Swap Controller with I²C Compatible Monitoring

DESCRIPTION

Demonstration circuit DC1704A4A is a 12V rail circuit using the LTC4280, Hot Swap Controller with I2C Compatible Monitoring.

Included on a board is an input clamp, input and output voltage dividers for UV, OV, and PWRGD comparators, LEDs to indicate the presence of various voltages and turret terminals for critical signals to facilitate evaluation in a working system. Input and output connections are made by 93 mil turrets, which if removed, accommodate insertion of up to 12 gauge wires for in-situ testing. An I2C port designed to interface with DC590A allows control of DC1704A with LTC's QuickEval software.

DC1704A permits evaluating the LTC4280 during a turn on and turn off transients as well as during steady state and fault conditions. **Design files for this circuit board are available. Call the LTC factory.**

PERFORMANCE SUMMARY

Specifications are at TA = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD}	Input Supply Range		2.9		15.	V
$V_{OV(VDD)}$	Input Supply Overvoltage Threshold		15	15.6	16.5	V
$V_{DD(UVL)}$	Input Supply Undervoltage Lockout	V_{DD} Rising	2.75	2.84	2.89	V
$V_{DD(HYST)}$	Input Supply Undervoltage Lockout Hysteresis		75	100	125	mV
$INTV_{CC}$	Internal Regulator Voltage		2.9	3.1	3.4	V
$INTV_{CC(UVL)}$	$INTV_{CC}$ Undervoltage Lockout	$INTV_{CC}$ Rising	2.55	2.64	2.79	V
$INTV_{CC(HYST)}$	$INTV_{CC}$ Undervoltage Lockout Hysteresis		20	55	75	mV
$\Delta V_{SENSE(TH)}$	Circuit Breaker Threshold (V_{DD}-V_{SENSE})		22.5	25	27.5	mV
ΔV_{SENSE}	Current Limit Voltage	V_{DD}=1.3 V_{DD}=0	22.5 7	26 10	29.5 13.5	mV
ΔV_{GATE}	External N-Channel Gate Drive(V_{GATE}-V_{SOURCE})	V_{DD}=2.9 to 15V	4.7	5.9	6.5	V
$I_{GATE(UP)}$	External N-Channel Gate Pull-Up Current	Gate On, V_{GATE} =0V to 15V	15	20	30	µ A
$I_{GATE(DN)SLOW}$	External N-Channel Gate Pulldown Current	Gate Off, V_{GATE} =15V	0.8	1.0	1.6	mA
$I_{GATE(DN)FAST}$	Pulldown Current From GATE to SOURCE DuringOC/UVL	V_{DD} -V_{SENSE}=100mV, V_{GS}=4V	300	450	700	mA
$V_{ON(TH)}$	On pin Threshold	V_{ON} Rising	1.21	1.235	1.26	V
$V_{EN(TH)}$	EN Input Threshold	V_{EN} Rising	1.215	1.235	1.255	V
$V_{OV(TH)}$	OV pin Threshold Voltage	V_{OV} Rising	1.215	1.235	1.255	V
$V_{UV(TH)}$	UV pin Threshold Voltage	V_{UV} Rising	1.215	1.235	1.255	V
V_{FB}	Foldback Pin Power Good Threshold	V_{FB} Rising	1.215	1.235	1.255	V
RES	AD Converter Resolution		8			Bits
UVLO	Undervoltage Lockout	V_{IN} Rising, 0°C < T_A < 85°C V_{IN} Rising V_{IN} Falling	 1.6		2.5 2.6	V

OPERATING PRINCIPLES

The LTC4280 is a low voltage hot swap controller that has a 2.9V to 15V operating range and a 24V absolute maximum operating voltage for the VDD pin. This demo circuit is populated for +12V operation, but it can easily be readjusted for any voltage between 2.9V and 15V by replacing R1, R2 and R7 (top resistors in the UV and OV dividers and the FB divider). The DC1704A as supplied by the factory is populated with a Si4864DP MOSFET in an SO-8 package and a 4mΩ ,1/2W current sense resistor, providing a minimum of 5.4A load current. The current limit and circuit breaker thresholds can be adjusted by changing the sense resistor, RS. To enable demonstration of higher current applications up to 100A, provisions have been made to replace RS with up to three 1W, 2512 size sense resistors in parallel connection and replace Q1 MOSFET with one in the D2Pack or PowerSO-10 packages.

QUICK START PROCEDURE

Demonstration circuit DC1704A4A is easy to set up to evaluate the performance of the LTC4280. Refer to the Figure 1 for proper measurement equipment setup and follow the procedure below:

1. The DC1704A is a factory setup to operate in a 12 volt rail with current level up to 5 A. If the LTC4280 is to be evaluated at different operating conditions, follow 2-3 below, otherwise skip to 4.

2. If evaluating at a voltage other than 12V, the following Demo board component must be adjusted:

- R1 and R2 for proper UV and OV PIN response,

- R7 for proper foldback configuration and power-good detection.

Select $R2=V_{MAX}/V_{MIN}$•13.7K*1.235/1.205-13.7K, and $R1= V_{MIN}$ *(13.7K+R2)/1.235-13.7-R2, where V_{MIN} and V_{MAX} are the minimum and maximum output voltages for which power is determined to be good.

Select $R7= V_{MIN}$•3.01K.7K-3.01K.

3. If the DC1704A should operate at other than 5A max, change the value of R_{SENSE}=0.99•22.5mV/$I_{LOAD(MAX)}$ for a 1% tolerance current sense resistor.

If the DC1704A should operate above 10Amps, replace Q1 with a suitable MOSFET. There are pads for D2Pack and PowerSO-10 packages. The SO-8 pad on the front of the board includes an extra area for better heat-sinking this package requires. Alternately, for low power applications, Q1 may be replaced with a MOSFET in a SSOT-6 package using the alternate pad on the back of the board.

4. . The 'TIMER SELECT' jumper can be used to choose a startup timer period between the time defined the external timer capacitor, CT, or 100ms (built in internal startup time). CT is stuffed with a 0.82uF capacitor at the factory, which provides a 10.1ms±2.8ms startup time. To customize the startup time, select $CT=T_{START}/12.3(ms/uF)$.

5. The LTC4280 does not require an RC network on the GATE pin for compensation. However, an RC network may be used to limit the rate at which the GATE rises to provide an inrush current below the internal current limit. Pads for R6 and CG on the back of the board are available for this purpose. R6 and CG may be stuffed with a 15k resistor, and $CG=C_{LOAD}$ * $20uA/I_{INRUSH}$ for this purpose.

6. The ADIN pin may be used as an input to take voltage for 8 bit measurement. Jumper 'ADIN SELECT' selects between measuring the input voltage or measuring the voltage on the ADIN turret. The input voltage is measured through a resistor divider, which defaults to a 15.4V full scale range to match the range of the SOURCE pin measurement. To change the full scale of the input measurement, select $R11=V_{RANGE}$*12.4k/1.23-12.4k. The ADIN turret signal is also measured through a voltage divider, but the bottom resistor is not stuffed at the factory, defaulting

to a 1.23V full scale voltage. To select a larger full scale voltage, choose R17=1.23*10k/(V_{RANGE}-1.23).

7. If your system uses a short pin to sense board insertion, move the $\overline{EN}$ jumper to SHORT PIN position and using the SHORT PIN turret, connect the aforementioned short pin. This is a direct connection to the LTC4280's $\overline{EN}$ pin. If deleterious voltages are anticipated, add a series resistor and clamping. $\overline{EN}$ is good for -0.3 to +12V on its own. $\overline{EN}$ is also logic compatible, with a 1.235V threshold and 130mV hysteresis.

8. The I2C address is selected on the board by using **JP4 (ADR0), JP5 (ADR1), and JP6 (ADR2)** to pull the address pins high, low, or allowing them to float. An address table is shown in the data sheet. The evaluation software automatically scans and identifies the I2C address, regardless of the setting.

9. After any necessary component changes have been made, connect a suitable load between VOUT and GND. This may be a passive resistive load or an active electronic load box. If long leads are present between the DC1704A and load bypassing, install 10µF or more bypassing at COUT to eliminate the chance of MOSFET oscillation and large negative excursions at +12V/5A OUTPUT.

10. Connect a power supply capable of supplying 1.5•I_{LOAD} between the +12V input and GND turrets. The minimum current capability of the supply must accommodate the tolerance of the circuit breaker threshold of ±12%. With the 4mΩ, 1%, factory installed sense resistor, the overload circuit breaker will trip at between 5.4A to 7.1Amp (6.25Amp nominal).

11. Connect the ribbon cable from a DC590 to the I2C PORT on the DC1704A. LTC's QuickEval software will automatically recognize the DC1704A and load software to read and write to the LTC4280's registers. During an I2C transaction, D5-7 will flicker faintly. If the I2C port (JP7) is disconnected, the turret terminals SDAO, SDAI, and SCL can be connected directly to an I2C bus. Power for D4-7 is supplied by JP7**, pin 2**, so in this mode the LEDs will not light, unless 5V is connected to this pin. Resistor R24 shorts SDAO and SDAI pins together for communication to a non-isolated bus. Removing R24 splits SDAO and SDAI to facilitate optically isolated applications (see the LTC4280 data sheet).

12. The following experiments can be run:

- Turn on into a nominal load;
- Turn on into an overload;
- Turn on into a short circuit;
- Turn on into a nominal load and increase the load until the LTC4280 trips off.

A digital storage scope provides a convenient means of observing the turn on and overload events. Observe the input or output current using a current probe. A probe ground turret is provided to make a low current connection to the LTC4280.

USING THE I²C PORT WITH QUICKEVAL

1) Register Display Options

Register options allows detailed bits demonstration of the bits registers A, B, C, or D, (Figure 2A, 2B 2C, and 2D), depending on the option selected. For the registers A, B, and D checking a box to the left of the each bit name sets the respective bit of the Read/Write registers, while unchecking a box clears the bit. The display of the STATUS register and the Register List demonstrate the bit status description and its binary value after every refresh of the interface (Figures 2C and 2E). The Clear button for register D clears out the bits in this register.

The Reg Send option (Figure 2F) allows for the user to enter and send data to a particular register. Select the register to be written to in the drop down menu. Enter the data in hex and click on Send Data to send the data or Send/Refresh so send and refresh the interface.

2) *START/Refresh Buttons*

Click on the START button to enable a timer that continuously updates the interface with the latest data from the LTC4280 approximately every 500ms. This button will display STOP when the timer is unable. Click on STOP to stop the timer. Click on Refresh for a single update.

3) FET Control

The status of the FET is shown with a color display. When the FET On the bit (C3) is read as high and the FET On Control bit (A3) is set, the FET is on, the shape display will be green and the FET control button will read "Turn FET Off". If C3 is low and A3 is set, the FET is off, the shape display will be color red, and the FET control button will read "Clear Faults". In all other cases, the FET is off, the shape display is red and the FET control button will read "Turn FET On". The "Turn FET On" control button sets bits A3 logic high. "Turn FET Off" or "Clear Faults" clears bit A3 to logic low.

4) Address Selection

Select in the drop down list box the Write address byte of the LTC4280 that is to be communicated with. If multiple LTC4280s are on the bus lines, the Mass Write address BEh can be selected to communicate with all LTC4280s at the same time. The Auto find button will scan through the 9 individual LTC4280 addresses and list which addresses responded with an acknowledge. The ARA button sends the Alert Response protocol and displays the address of the device that replies with its address.

5) Data Display Option

The Fixed option (Figure 3A) shows the data byte in hex for registers E, F, and G and displays the calculated Vdd-sense, Source voltage, and ADIN values using the following equations:

Vdd-sense = Sense(data) * SenseScale mV

Source voltage = Source(data) * SourceScale V

Source voltage = Source(data) * SourceScale V

ADIN voltage = ADIN(data) * ADINScale V

The Adjusted option allows the user to enter Rs, R14 and R17. The calculated values are shown using the following equations:

Idd sense = Vdd sense / Rs mA

ADIN full = ADIN voltage * (R14 + R17) / R17 V

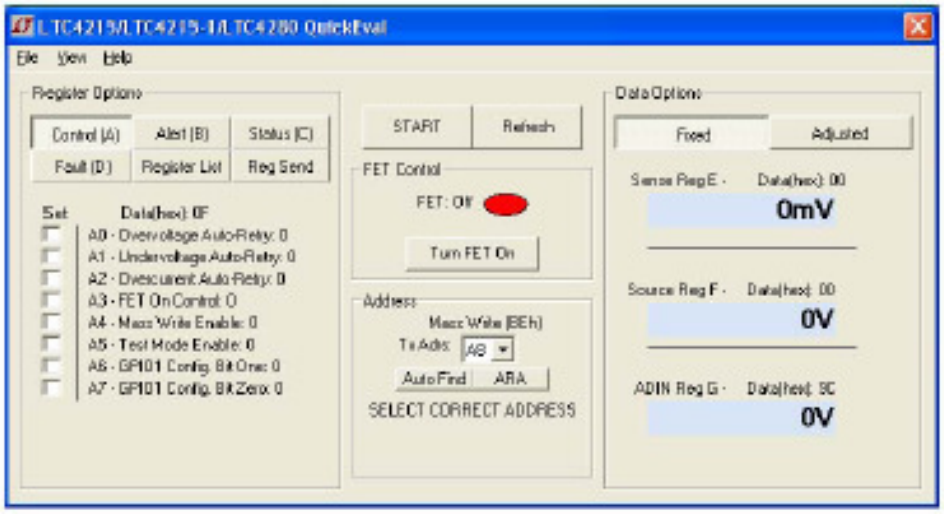


Figure 1. Defolt LTC4280 QuickEval Interface

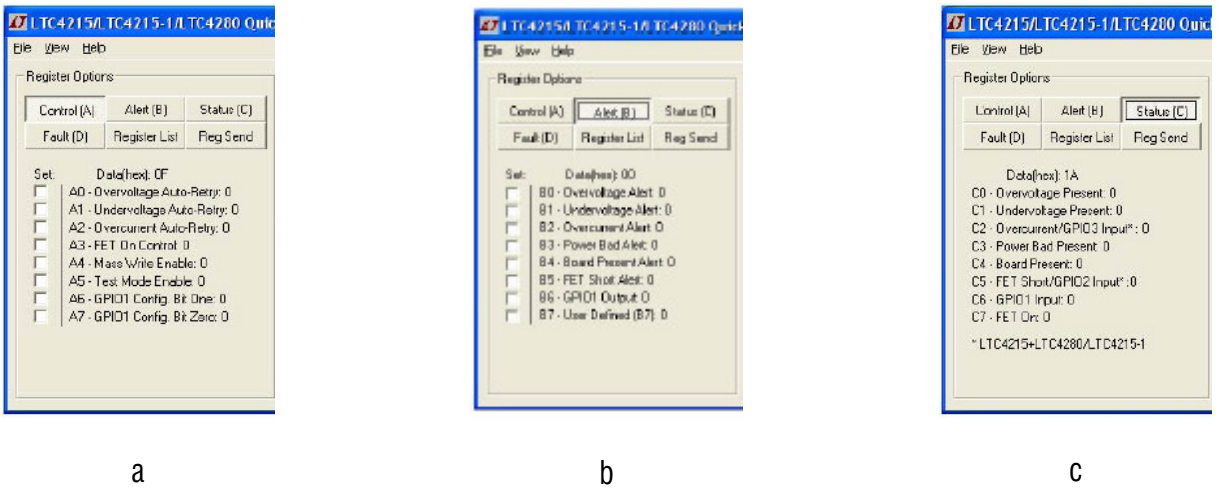
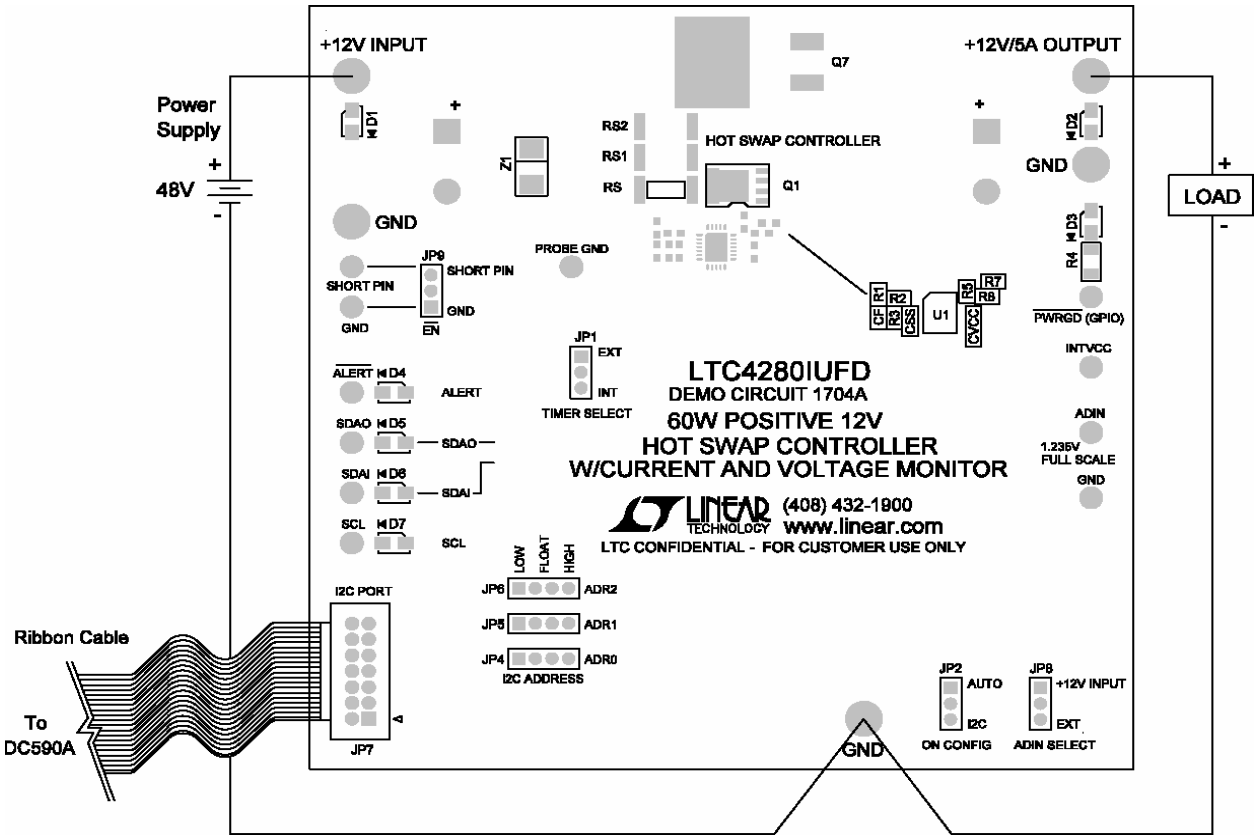
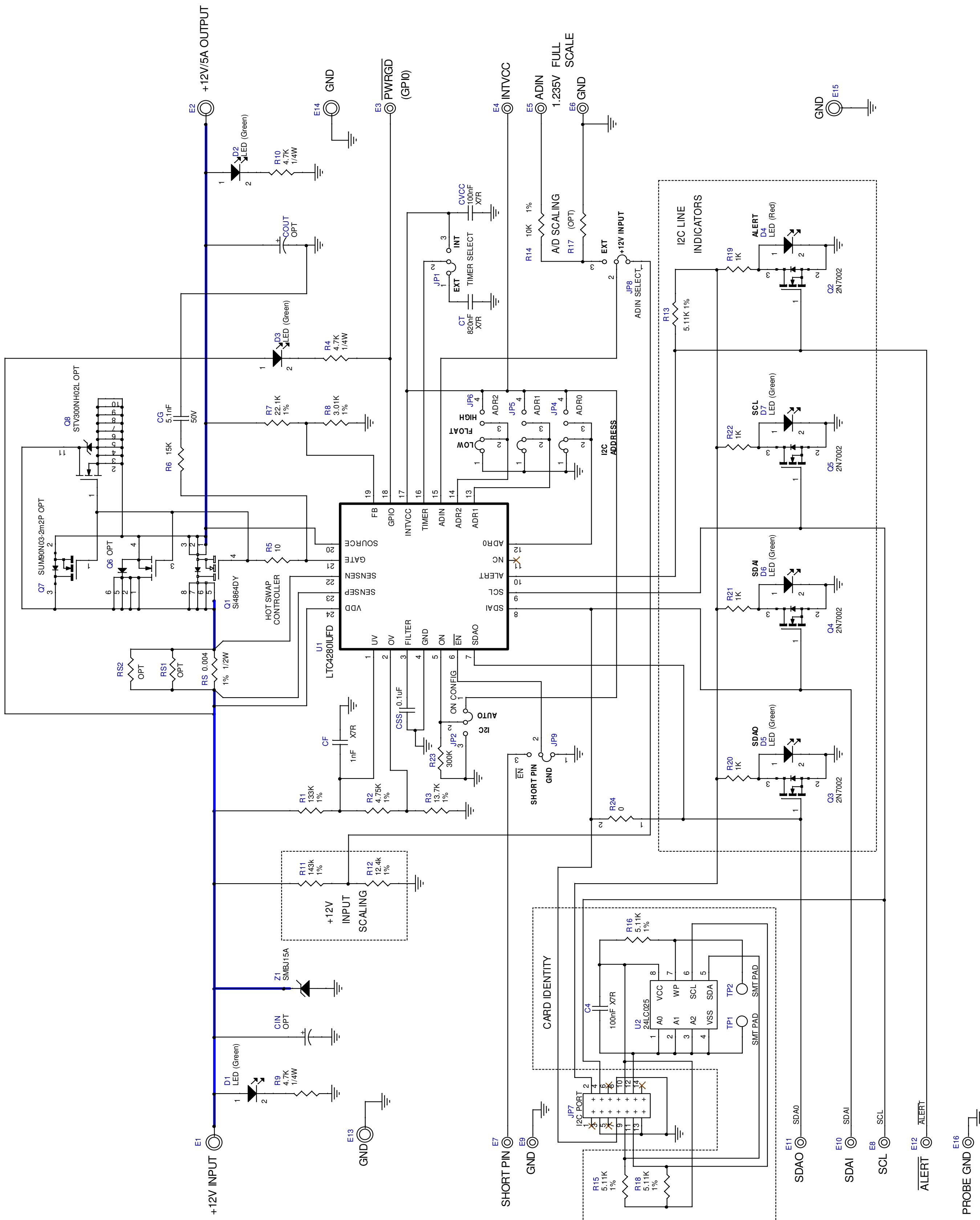


Figure 2. Register Display Options

Figure 3. Data Display Options





+12V/5A OUTPUT
+12V INPUT
GND
PWRGD (GPI0)
INTVCC
ADIN 1.235V FULL SCALE
HOT SWAP CONTROLLER
U1 LTC4280IUFD
A/D SCALING
TIMER SELECT
ON CONFIG
I2C ADDRESS
I2C LINE INDICATORS
+12V INPUT SCALING
CARD IDENTITY
U2 24LC025
JP7 I2C PORT
SHORT PIN
SDAO
SDAI
SCL
ALERT
PROBE GND