

N-channel 800 V, 2.1 Ω typ., 3 A MDmesh™ K5 Power MOSFET in a PowerFLAT™ 5x6 VHV package

Datasheet - preliminary data

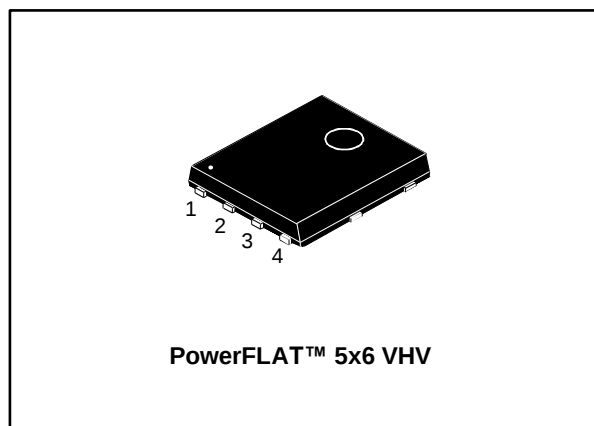
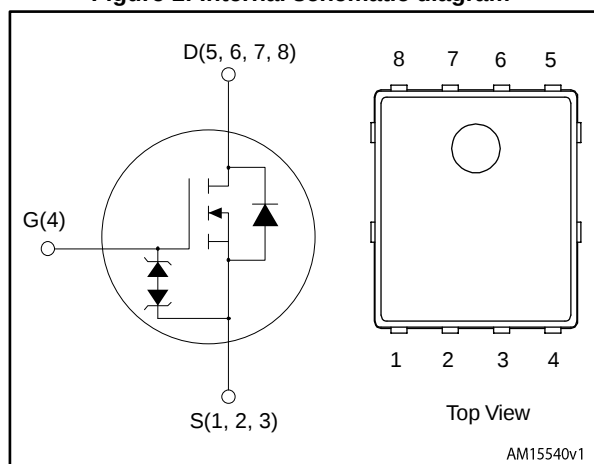


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STL4LN80K5	800 V	2.6 Ω	3 A

- Industry's lowest R_{DS(on)} * area
- Industry's best FoM (figure of merit)
- Ultra low-gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STL4LN80K5	4LN80K5	PowerFLAT™ 5x6 VHV	Tape and reel

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
3	Test circuits	6
4	Package information	7
	4.1 PowerFLAT™ 5x6 VHV package information	8
	4.2 PowerFLAT™ 5x6 packing information	11
5	Revision history	13

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	3	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	1.9	A
$I_{DM}^{(1)}$	Drain current (pulsed)	12	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	38	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	
T_j	Operating junction temperature	- 55 to 150	$^{\circ}\text{C}$
T_{stg}	Storage temperature		

Notes:⁽¹⁾Pulse width limited by safe operating area⁽²⁾ $I_{SD} \leq 3\text{ A}$, $dv/dt \leq 100\text{ A}/\mu\text{s}$; $V_{DS\text{ peak}} < V_{(BR)DSS}$ ⁽³⁾ $V_{DS} \leq 640\text{ V}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	3.3	$^{\circ}\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	59	$^{\circ}\text{C}/\text{W}$

Notes:⁽¹⁾When mounted on FR-4 board of 1 inch², 2 oz Cu

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	TBD	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	TBD	mJ

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified

Table 5: On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	800			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 800\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 800\text{ V}$ $T_C = 125\text{ °C}$			50	μA
I_{GSS}	Gate body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 1.2\text{ A}$		2.1	2.6	Ω

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	110	-	pF
C_{oss}	Output capacitance		-	9.5	-	pF
C_{rss}	Reverse transfer capacitance		-	0.4	-	pF
$C_{oss(eq)}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }640\text{ V}$, $V_{GS} = 0\text{ V}$	-	TBD	-	pF
R_g	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	18	-	Ω
Q_g	Total gate charge	$V_{DD} = 640\text{ V}$, $I_D = 2\text{ A}$ $V_{GS} = 10\text{ V}$, see Figure 3: "Gate charge test circuit"	-	4	-	nC
Q_{gs}	Gate-source charge		-	TBD	-	nC
Q_{gd}	Gate-drain charge		-	TBD	-	nC

Notes:

⁽¹⁾ $C_{oss\ eq}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$, $I_D = 1.6\text{ A}$, $R_G = 4.7\text{ }\Omega$ $V_{GS} = 10\text{ V}$ (See Figure 2: "Switching times test circuit for resistive load" and Figure 7: "Switching time waveform")	-	TBD	-	ns
t_r	Rise time		-	TBD	-	ns
$t_{d(off)}$	Turn-off delay time		-	TBD	-	ns
t_f	Fall time		-	TBD	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		3	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		12	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 3 \text{ A}$, $V_{GS} = 0 \text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 3 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 60 \text{ V}$, (see Figure 4: "Test circuit for inductive load switching and diode recovery times")	-	TBD		ns
Q_{rr}	Reverse recovery charge		-	TBD		μC
I_{RRM}	Reverse recovery current		-	TBD		A
t_{rr}	Reverse recovery time	$I_{SD} = 3 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 60 \text{ V}$, $T_J = 150 \text{ }^\circ\text{C}$ (Figure 4: "Test circuit for inductive load switching and diode recovery times")	-	TBD		ns
Q_{rr}	Reverse recovery charge		-	TBD		μC
I_{RRM}	Reverse recovery current		-	TBD		A

Notes:⁽¹⁾Pulse width limited by safe operating area⁽²⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%

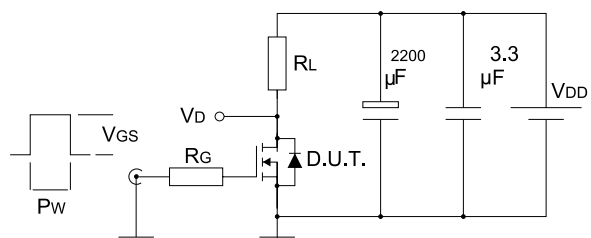
Table 9: Gate source-Zener diode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit.
$V_{(BR)GS0}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}$, $I_D = 0 \text{ A}$	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance the device's ESD capability. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

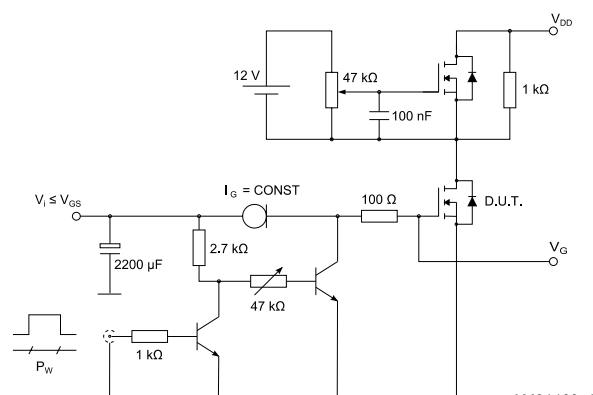
3 Test circuits

Figure 2: Switching times test circuit for resistive load



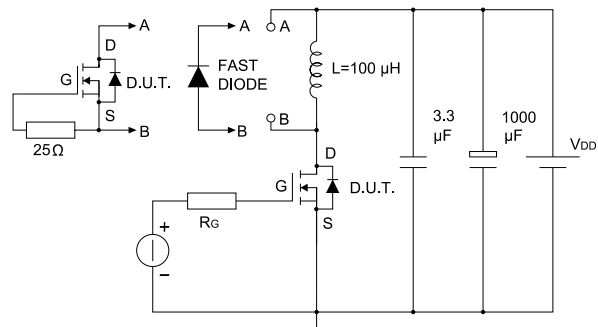
AM01468v1

Figure 3: Gate charge test circuit



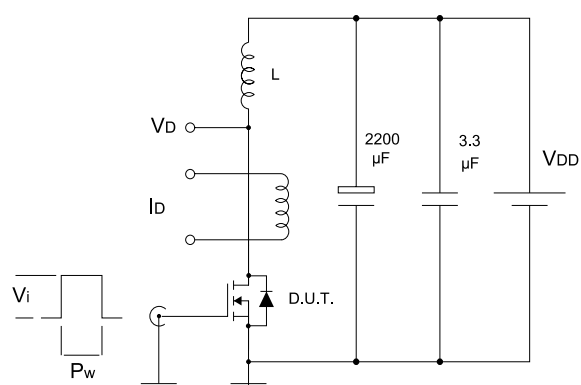
AM01469v1

Figure 4: Test circuit for inductive load switching and diode recovery times



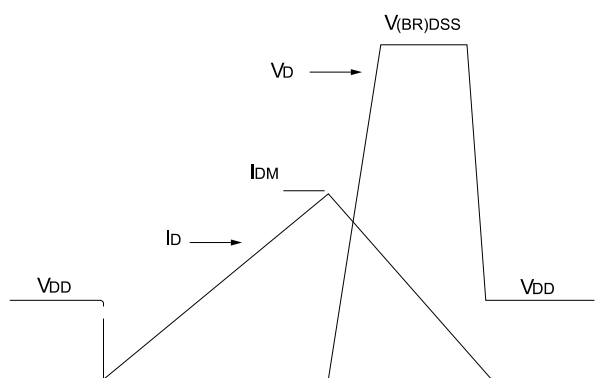
AM01470v1

Figure 5: Unclamped inductive load test circuit



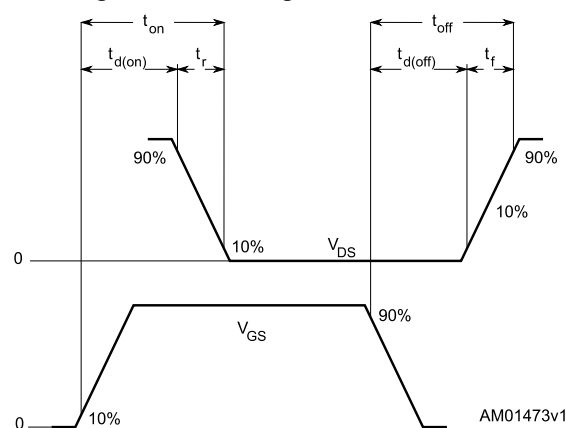
AM01471v1

Figure 6: Unclamped inductive waveform



AM01472v1

Figure 7: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK[®] is an ST trademark.

4.1 PowerFLAT™ 5x6 VHV package information

Figure 8: PowerFLAT™ 5x6 VHV Package outline

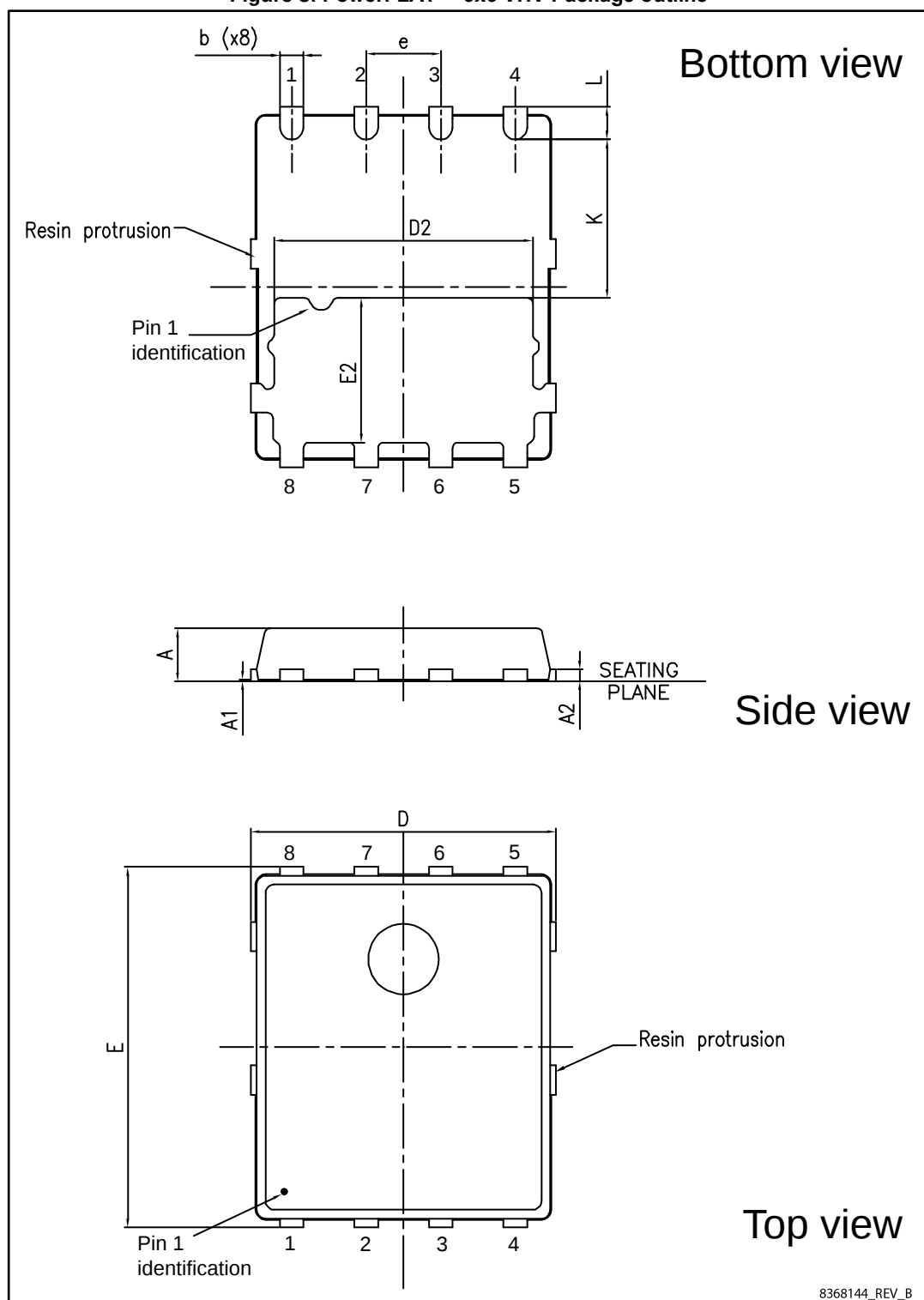
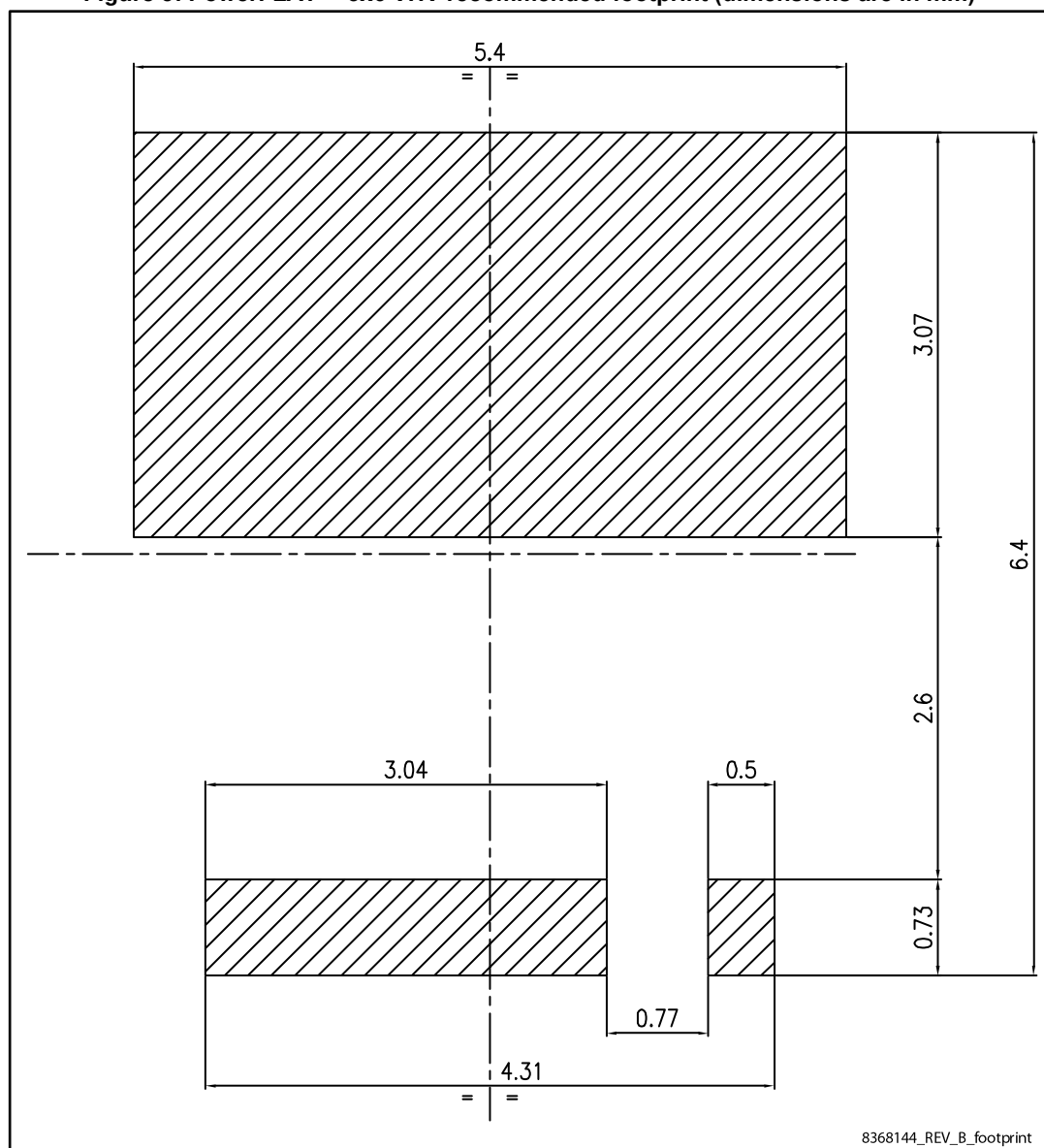


Table 10: PowerFLAT™ 5x6 VHV package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	5.95	6.15	6.35
D2	4.30	4.40	4.50
E2	2.40	2.50	2.60
e		1.27	
L	0.50	0.55	0.60
K	2.60	2.70	2.80

Figure 9: PowerFLAT™ 5x6 VHV recommended footprint (dimensions are in mm)



4.2 PowerFLAT™ 5x6 packing information

Figure 10: PowerFLAT™ 5x6 tape (dimensions are in mm)

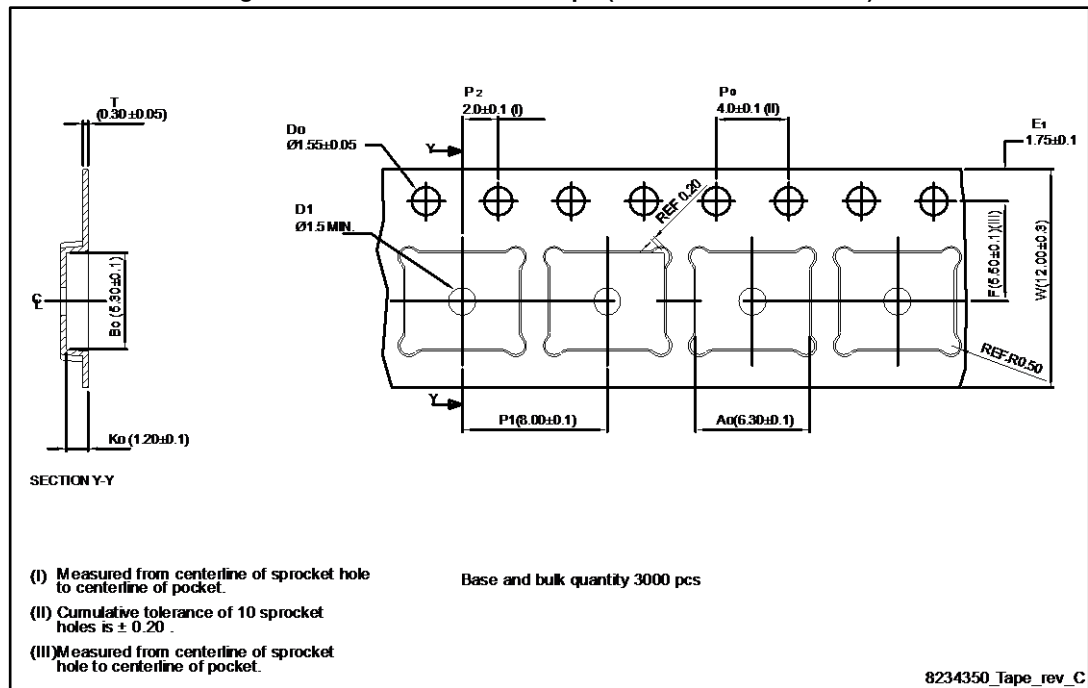


Figure 11: PowerFLAT™ 5x6 package orientation in carrier tape

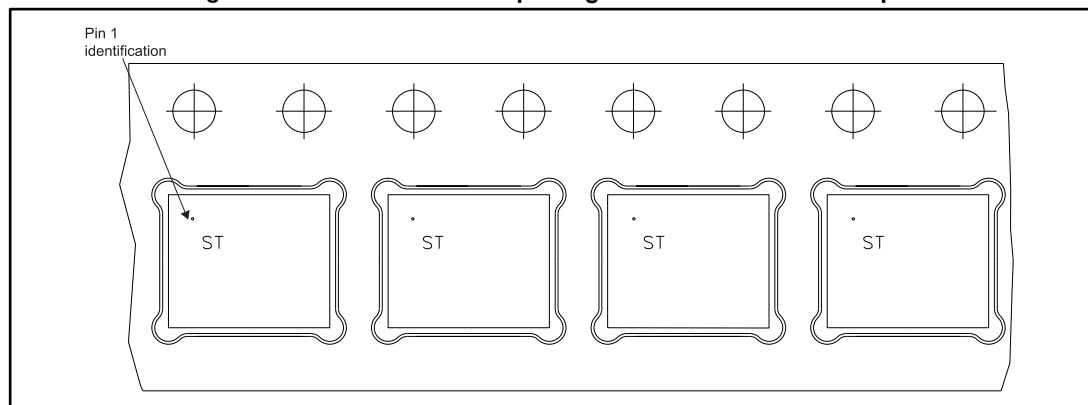
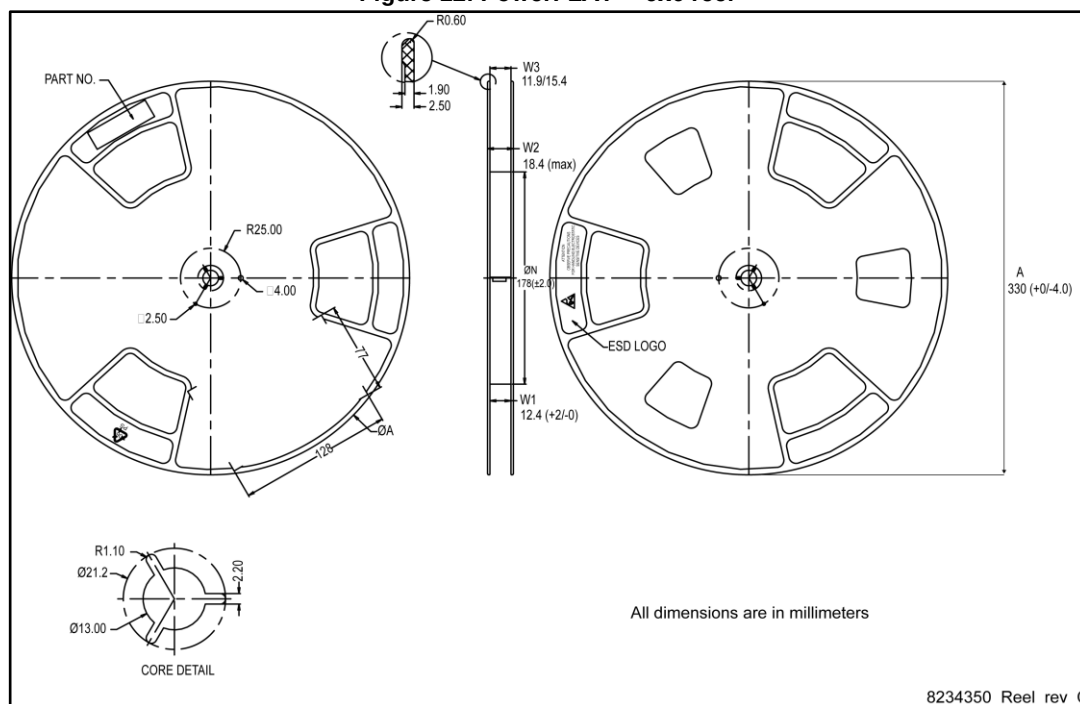


Figure 12: PowerFLAT™ 5x6 reel



5 Revision history

Table 11: Document revision history

Date	Revision	Changes
29-May-2015	1	First release.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2015 STMicroelectronics – All rights reserved