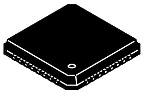
Advanced Doherty Alignment Module (ADAM)

MMDS20254HT1

1800-2200 MHz
ADAM – ADVANCED DOHERTY
ALIGNMENT MODULE



QFN 6 × 6

The MMDS20254H is an integrated module designed for use in base station transmitters in conjunction with high power Doherty amplifiers. The device is designed to enable accurate alignment of phase and amplitude on the carrier and peaking amplifiers to ensure performance consistency, in particular for asymmetric implementations. The MMDS20254H enables superior linearity-efficiency trade-off while improving output power. It contains a 90° coupler, digitally selectable phase shifters and step attenuators, and operates from a single voltage supply. The MMDS20254H is suitable for transmit protocols such as GSM, W-CDMA, UMTS and LTE using frequencies from 1800 to 2200 MHz, and is controlled using a serial peripheral interface (SPI).

Features

- Frequency: 1800-2200 MHz
- Maximum RF Input Power: 25 dBm (CW)
- Low Loss Power Splitter
- 0.5 dB Step Programmable Attenuators with 7.5 dB Maximum Range
- 7° per Bit Phase Shifters with 49° Maximum Range
- Power up into a Selectable State
- Single 5 Volt Supply
- Supply Current: 12 mA
- 50 Ohm Operation (no external matching required)
- TTL/CMOS/SPI Interface (1.8 V, 3.3 V Logic)
- Cost-effective 32-Pin, 6 mm QFN Surface Mount Plastic Package
- In Tape and Reel. R1 Suffix = 1,000 Units, 16 mm Tape Width, 7-inch Reel.

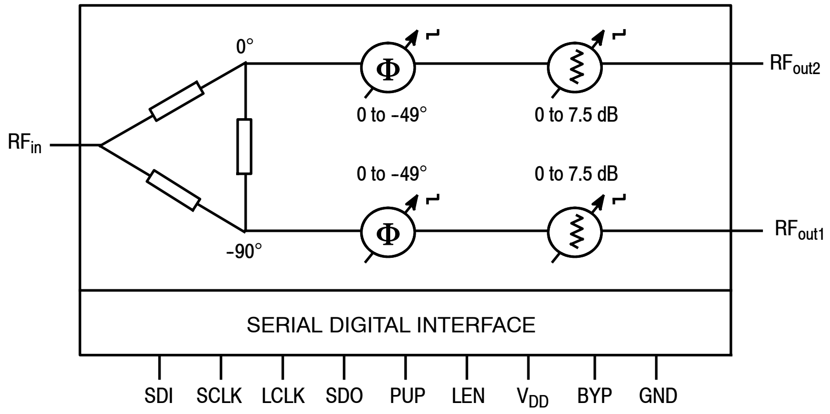


Figure 1. Functional Block Diagram

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	6	V
Logic Inputs (SCLK, LCLK, LEN, PUP, SDI)	V_{in}	-0.5 to +3.63	V
RF Input Power (CW)	P_{in}	25	dBm
Storage Temperature Range	T_{stg}	-65 to +150	°C
Junction Temperature	T_J	150	°C

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	4.5	5.5	V
DC Input Voltage (SCLK, LCLK, LEN, SDI)	V_{in}	0	3.3	V

Table 3. Electrical Characteristics (V_{DD} = 5 Vdc, 2140 MHz, T_A = 25°C, 50 ohm system, in Freescale Application Circuit)

Characteristic	Symbol	Min	Typ	Max	Unit
Insertion Loss (Includes 3 dB power division and 2.5 dB loss)	I_L	—	5.5	—	dB
Max Transition Time (Rising Edge of LCLK to RF_{out})	$t_{transition}$	—	350	—	ns
Power Input @ 1dB Compression	P1dB	—	35	—	dBm
Supply Current	I_{DD}	10	12	13	mA
Isolation (S32)	|S32|	—	20	—	dB
Input Return Loss (S11)	IRL	—	13	—	dB
Output Return Loss (S22)	ORL	—	15	—	dB
Third Order Input Intercept Point	IIP3	—	40	—	dBm
Phase Step	$\Delta\Phi$ ⌐	—	7	—	°/bit
Phase Control Range	$\Delta\Phi$	—	49	—	°
Attenuation Step	ΔR ⌐	—	0.5	—	dB
Attenuation Control Range	ΔR	—	7.5	—	dB
Max Input Voltage Logic Low	V_{IL}	—	—	0.4	V
Min Input Voltage Logic High	V_{IH}	1.6	—	—	V
SDO Output Voltage High	V_{OH}	1.8 (1)	—	0.6 × V_{DD}	V
SDO Output Voltage Low	V_{OL}	0	—	0.4	V
Max Clock Frequency (50% Duty Cycle)	f_{SCLK}	—	—	26	MHz

1. Load = 20 pF @ maximum clock frequency.

Table 4. Thermal Characteristics

Characteristics	Symbol	Value (2)	Unit
Thermal Resistance, Junction to Case Case Temperature 106°C, P_{out} = 0.02 W, Maximum Phase and Attenuation State, P_{in} = 25 dBm CW, 2140 MHz, V_{DD} = 5 Vdc, I_{DD} = 11 mA	$R_{\theta JC}$	16	°C/W

Table 5. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1B
Machine Model (per EIA/JESD22-A115)	A
Charge Device Model (per JESD22-C101)	III

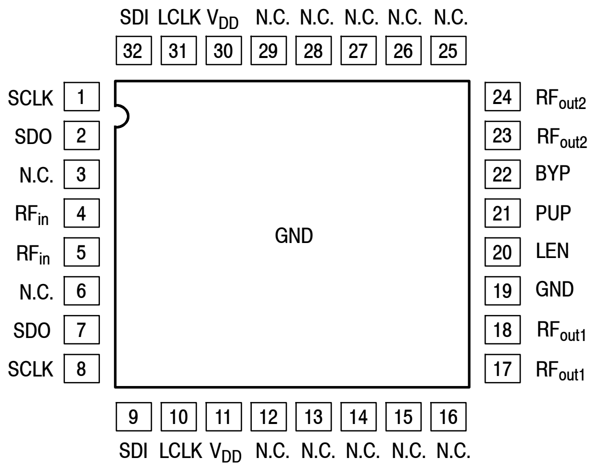
Table 6. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf.
Select Documentation/Application Notes - AN1955.

Table 7. Functional Pin Description

Pin Number	Pin Function	Pin Description
1, 8 (1)	SCLK	Serial Data Clock
2, 7 (1)	SDO	Serial Data Output
3, 6, 12, 13, 14, 15, 16, 25, 26, 27, 28, 29	N.C.	No Connection
4, 5 (2)	RF_{in}	RF Input (DC Block Needed)
9, 32 (1)	SDI	Serial Data Input
10, 31 (1)	LCLK	Latch Clock
11, 30 (1)	V_{DD}	Supply Voltage
17, 18 (2)	RF_{out1}	RF Output 1
19	GND	Ground
20 (3)	LEN	Logic Enable
21 (5)	PUP	Power-up Programming State
22 (4)	BYP	Decoupling Node
23, 24 (2)	RF_{out2}	RF Output 2



(Top View)

Note: Exposed backside of the package is DC and RF ground.

Figure 2. Pin Connections

1. Redundant pins are internally connected. User can connect to either of the internally connected paired pins: 1 and 8, 2 and 7, 9 and 32, 10 and 31, 11 and 30.
2. Each RF pin pair should be tied together.
3. Logic low enables normal SPI operation. Logic high disables SPI and places device at 0 dB attenuation and 0° phase shift.
4. Requires external capacitive decoupling to ground.
5. Logic low places device at 0 dB attenuation and 0° phase shift at power up. Logic high places device at 7.5 dB attenuation and –49° phase shift. Because PUP pin has internal pull up, logic high can be set by no connection to pin. Alternatively, it can be connected to BYP or a user-controlled V_{in}.

Table 8. Serial Interface Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units
t_{SCLK}	Serial Clock Period	38.5	—	—	ns
t_{SCLKH}	Serial Clock Pulse Width High	10	—	—	ns
t_{SCLKL}	Serial Clock Pulse Width Low	10	—	—	ns
t_{SU}	Serial Data Input Setup Time to SCLK Rising Edge	—	—	5	ns
t_{H}	Serial Data Input Hold Time from SCLK Rising Edge	—	—	2	ns
t_{OH}	Serial Data Output Hold Time from SCLK Rising Edge	1.6	—	—	ns
t_{OV} (10 pF)	Serial Data Output Propagation Delay from SCLK Rising Edge	—	5	9	ns
t_{OV} (50 pF)	Serial Data Output Propagation Delay from SCLK Rising Edge	—	15	26	ns
t_{OV} (150 pF)	Serial Data Output Propagation Delay from SCLK Rising Edge	—	35	65	ns
t_{SETTLE}	Serial Clock Rising Edge Setup Time to Latch Clock Rising Edge	—	—	27	ns
t_{LCLKH}	Latch Clock Pulse Width High	10	—	—	ns

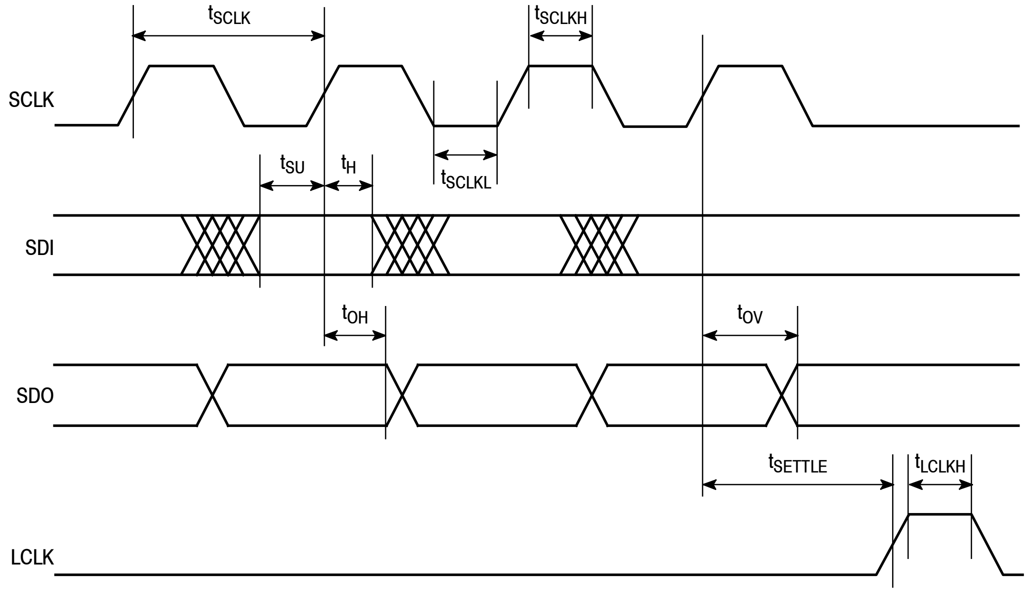
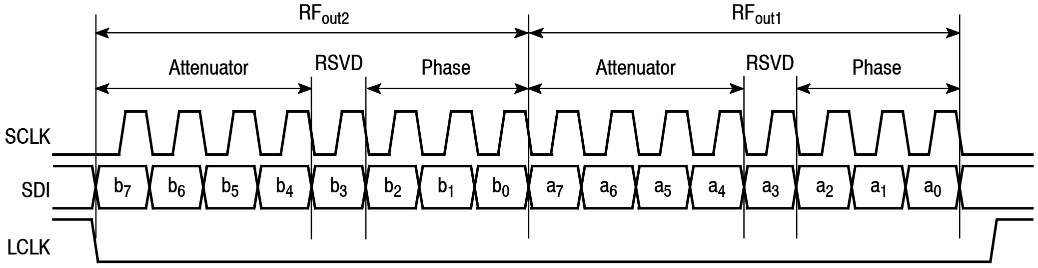


Figure 3. Serial Interface Timing Diagram



Note: Bits a3/b3 are reserved (RSVD) for future use. Always write these bits as zero (0).

Figure 4. Serial Interface Bits Diagram

Table 9. Logic Truth Table — RF_{In} to RF_{out1}

a7	a6	a5	a4	Attenuation (dB)
L	L	L	L	0
L	L	L	H	0.5
L	L	H	L	1.0
L	L	H	H	1.5
L	H	L	L	2.0
L	H	L	H	2.5
L	H	H	L	3.0
L	H	H	H	3.5
H	L	L	L	4.0
H	L	L	H	4.5
H	L	H	L	5.0
H	L	H	H	5.5
H	H	L	L	6.0
H	H	L	H	6.5
H	H	H	L	7.0
H	H	H	H	7.5

a2	a1	a0	Phase Shift (°)
L	L	L	0
L	L	H	-7
L	H	L	-14
L	H	H	-21
H	L	L	-28
H	L	H	-35
H	H	L	-42
H	H	H	-49

Table 10. Logic Truth Table — RF_{In} to RF_{out2}

b7	b6	b5	b4	Attenuation (dB)
L	L	L	L	0
L	L	L	H	0.5
L	L	H	L	1.0
L	L	H	H	1.5
L	H	L	L	2.0
L	H	L	H	2.5
L	H	H	L	3.0
L	H	H	H	3.5
H	L	L	L	4.0
H	L	L	H	4.5
H	L	H	L	5.0
H	L	H	H	5.5
H	H	L	L	6.0
H	H	L	H	6.5
H	H	H	L	7.0
H	H	H	H	7.5

b2	b1	b0	Phase Shift (°)
L	L	L	0
L	L	H	-7
L	H	L	-14
L	H	H	-21
H	L	L	-28
H	L	H	-35
H	H	L	-42
H	H	H	-49

Table 11. Power-up Programming (PUP) State

LCLK	PUP	Function
X	0	Minimum attenuation/minimum phase (0 dB/0°)
X	1	Maximum attenuation/maximum phase (7.5 dB/-49°)
On 1st rising edge	X	Normal operation on 1st rising edge LCLK and subsequent rising edges

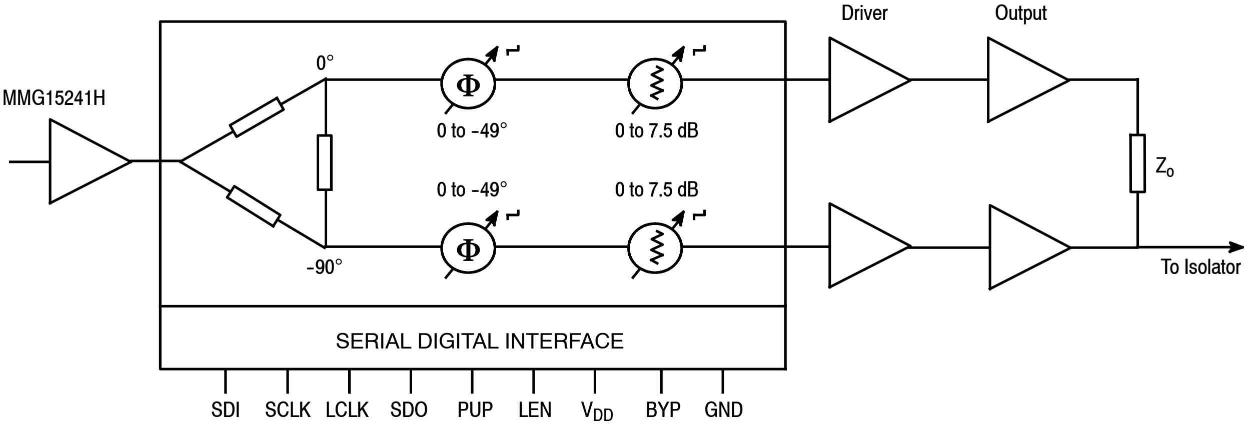


Figure 5. Typical Doherty Base Station Alignment Block Diagram

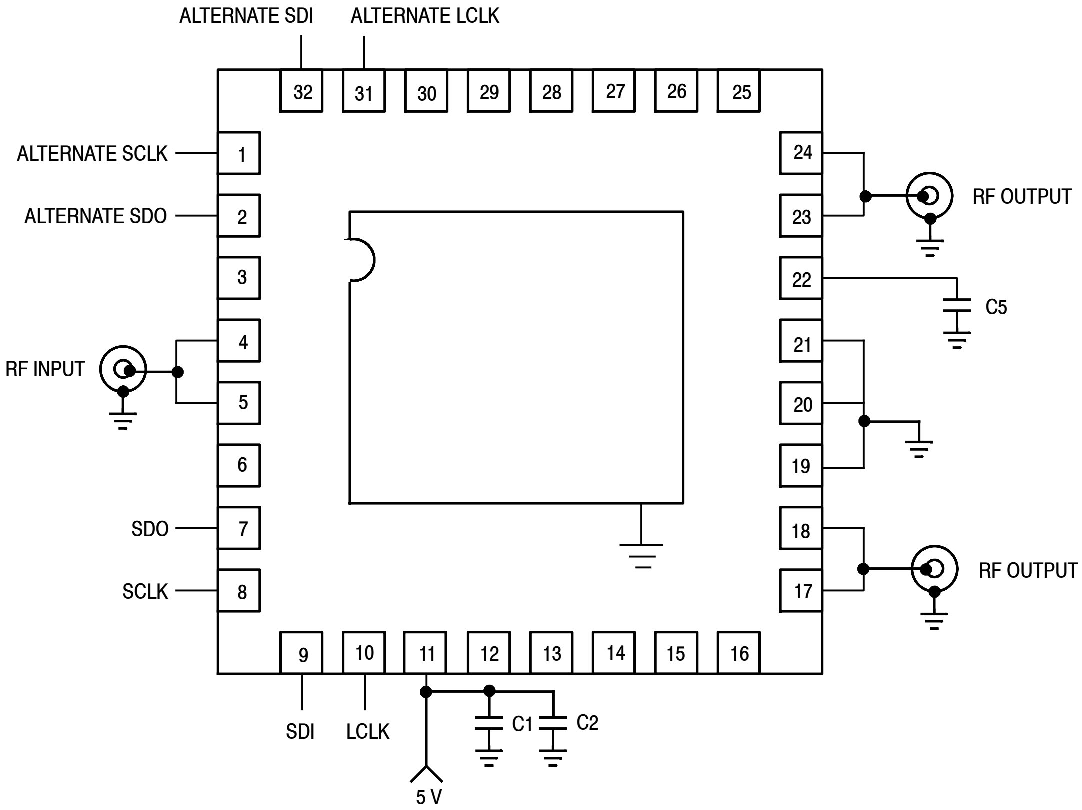
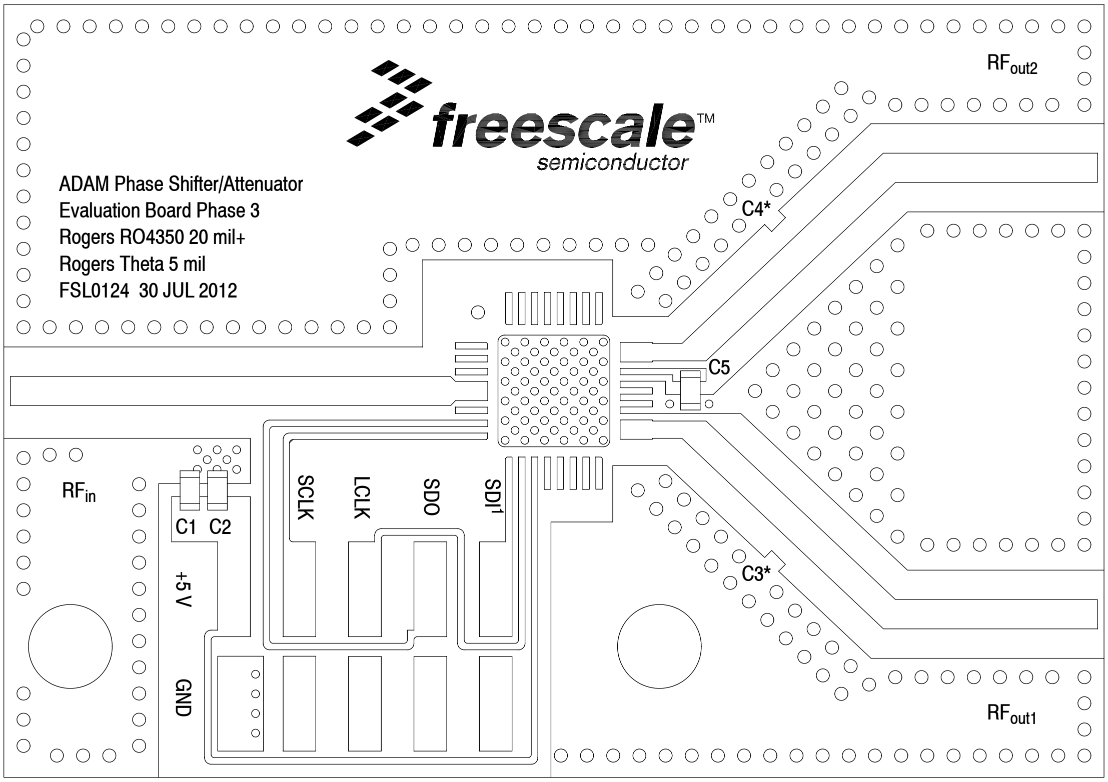


Figure 6. MMDS20254H Test Circuit Schematic

Table 12. MMDS20254H Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	22 pF Chip Capacitor	GRM1885C1H220JA01J	Murata
C2	100 pF Chip Capacitor	GRM1885C1H101JA01J	Murata
C3, C4	Components Not Placed		
C5	0.1 μF Chip Capacitor	GRM155R61A104KA01D	Murata
PCB	0.02″, ε_r = 3.48	RO4350	Rogers



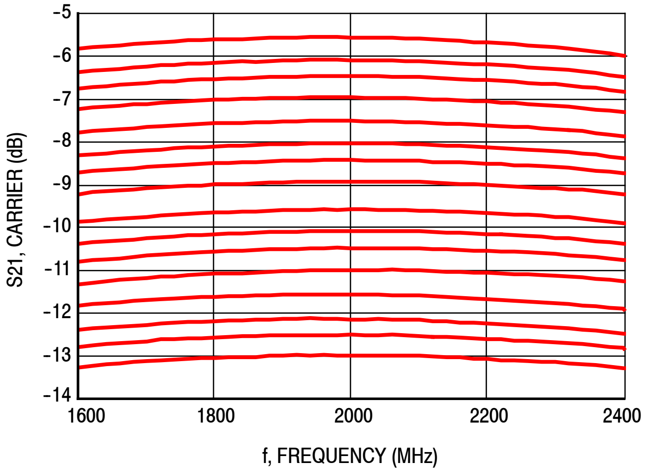
Note: Component numbers C3* and C4* are labeled on board but not placed.

Figure 7. MMDS20254H Test Circuit Component Layout

Table 12. MMDS20254H Test Circuit Component Designations and Values

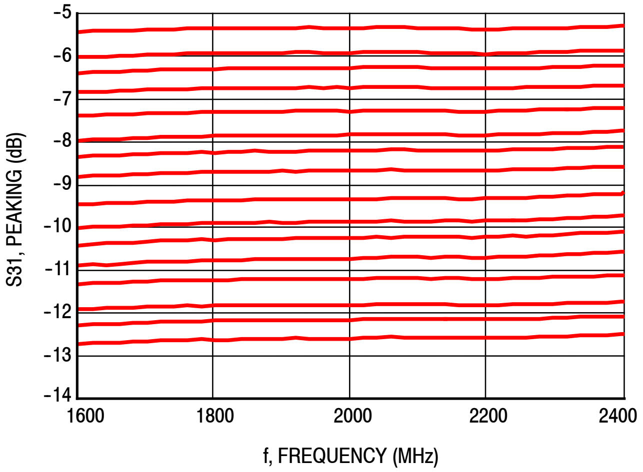
Part	Description	Part Number	Manufacturer
C1	22 pF Chip Capacitor	GRM1885C1H220JA01J	Murata
C2	100 pF Chip Capacitor	GRM1885C1H101JA01J	Murata
C3, C4	Components Not Placed		
C5	0.1 μF Chip Capacitor	GRM155R61A104KA01D	Murata
PCB	0.02″, $\varepsilon_r = 3.48$	RO4350	Rogers

(Test Circuit Component Designations and Values repeated for reference.)



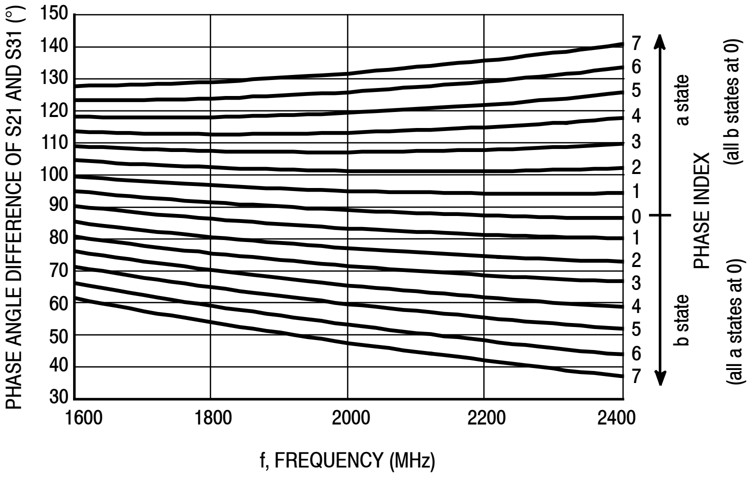
Note: S21 is a combination of static insertion loss and selected path attenuation.

Figure 8. S21 versus Attenuation State versus Frequency



Note: S31 is a combination of static insertion loss and selected path attenuation.

Figure 9. S31 versus Attenuation State versus Frequency



Note: The phase angle difference is a combination of insertion phase and selected phase adjustment.

Figure 10. Phase Angle Difference of S21 and S31 versus Phase State versus Frequency

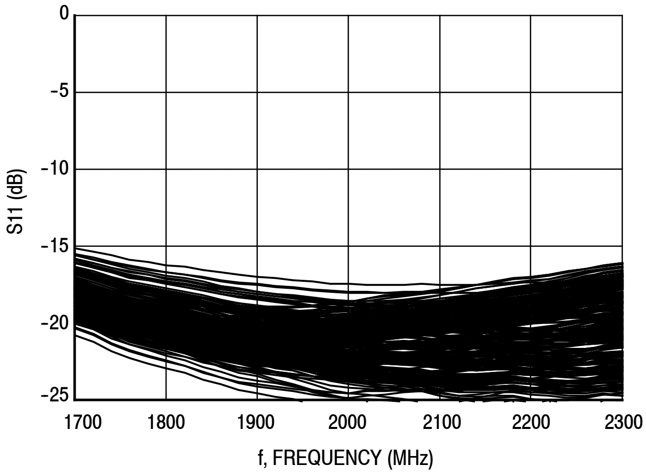


Figure 11. S11 versus Frequency

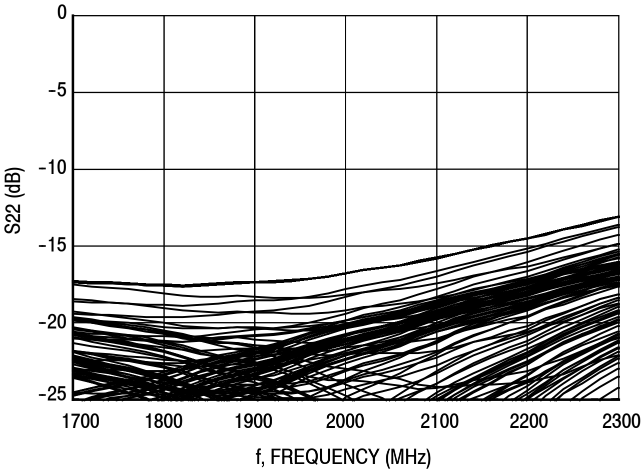


Figure 12. S22 versus Frequency

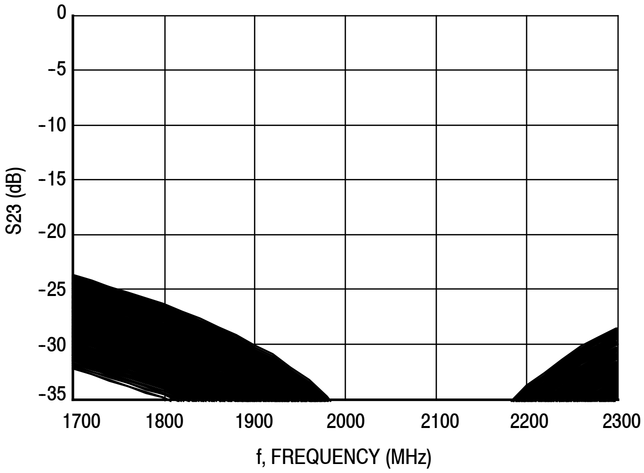


Figure 13. S23 versus Frequency

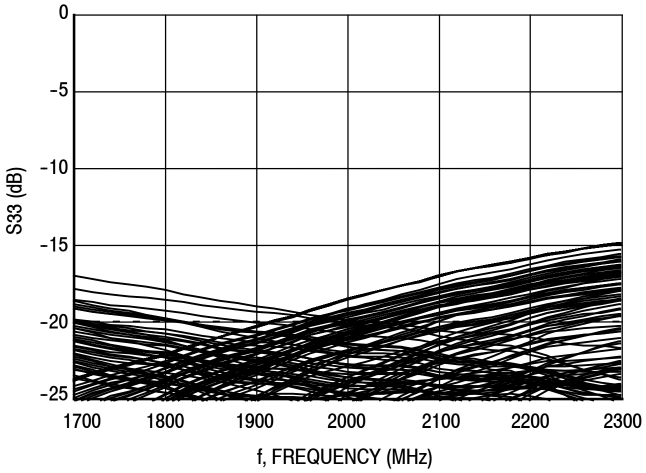


Figure 14. S33 versus Frequency

Note: A total of 256 states are plotted in Figures 11 to 14. Graph measurements include 128 states for the carrier side (combinations of all phase and amplitude states), with the peaking side set to 0 dB attenuation and 0° phase. Measurements also include 128 states for the peaking side (combinations of all phase and amplitude states) with the carrier side set to 0 dB attenuation and 0° phase.

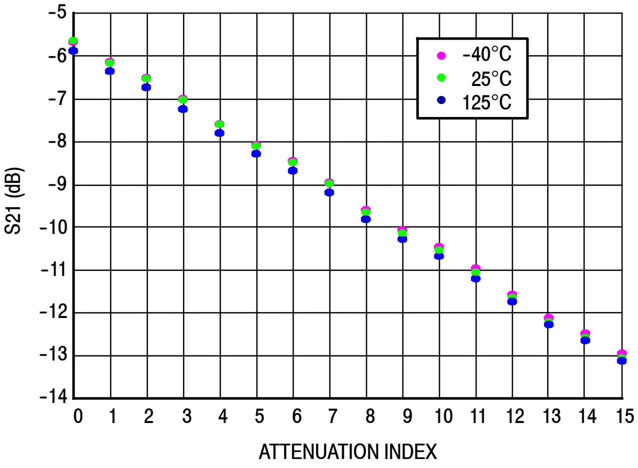


Figure 15. S21 versus Attenuation State versus Temperature

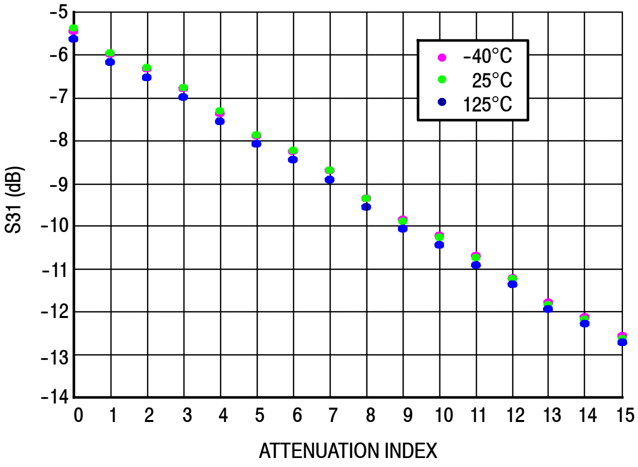


Figure 16. S31 versus Attenuation State versus Temperature

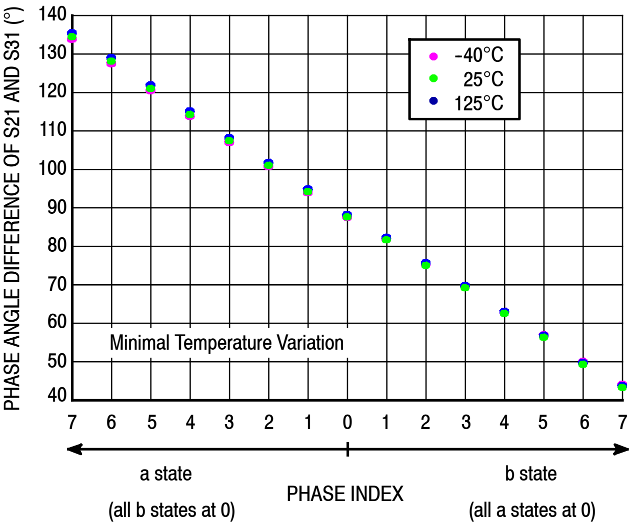


Figure 17. Phase Angle Difference of S21 and S31 versus Phase State versus Temperature

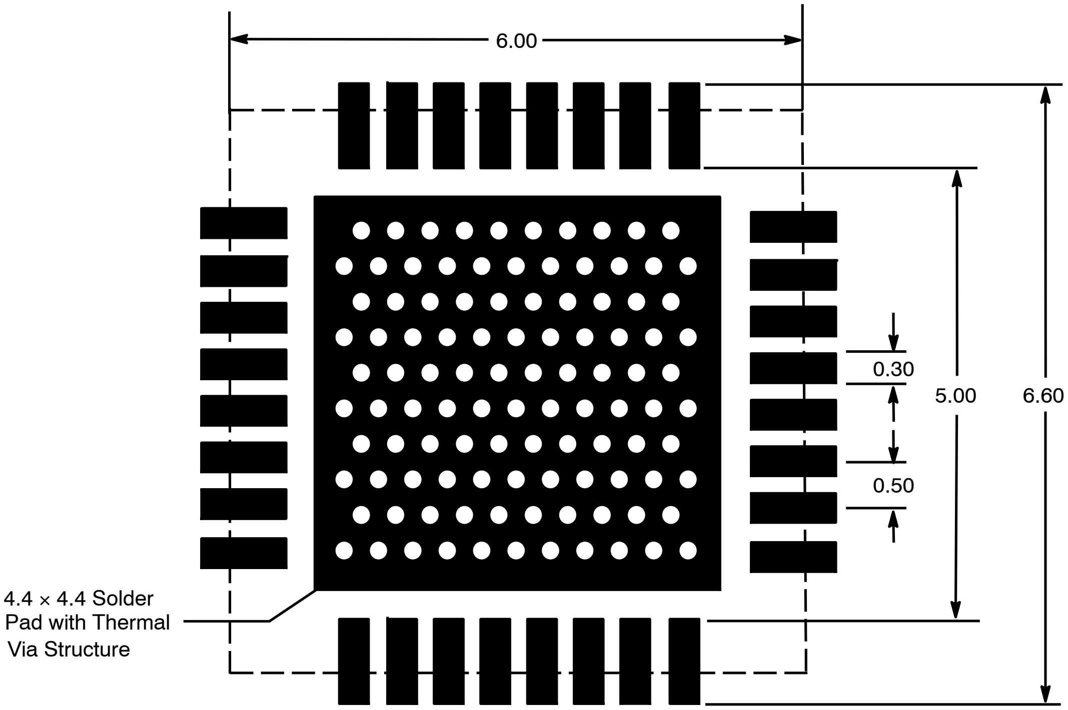
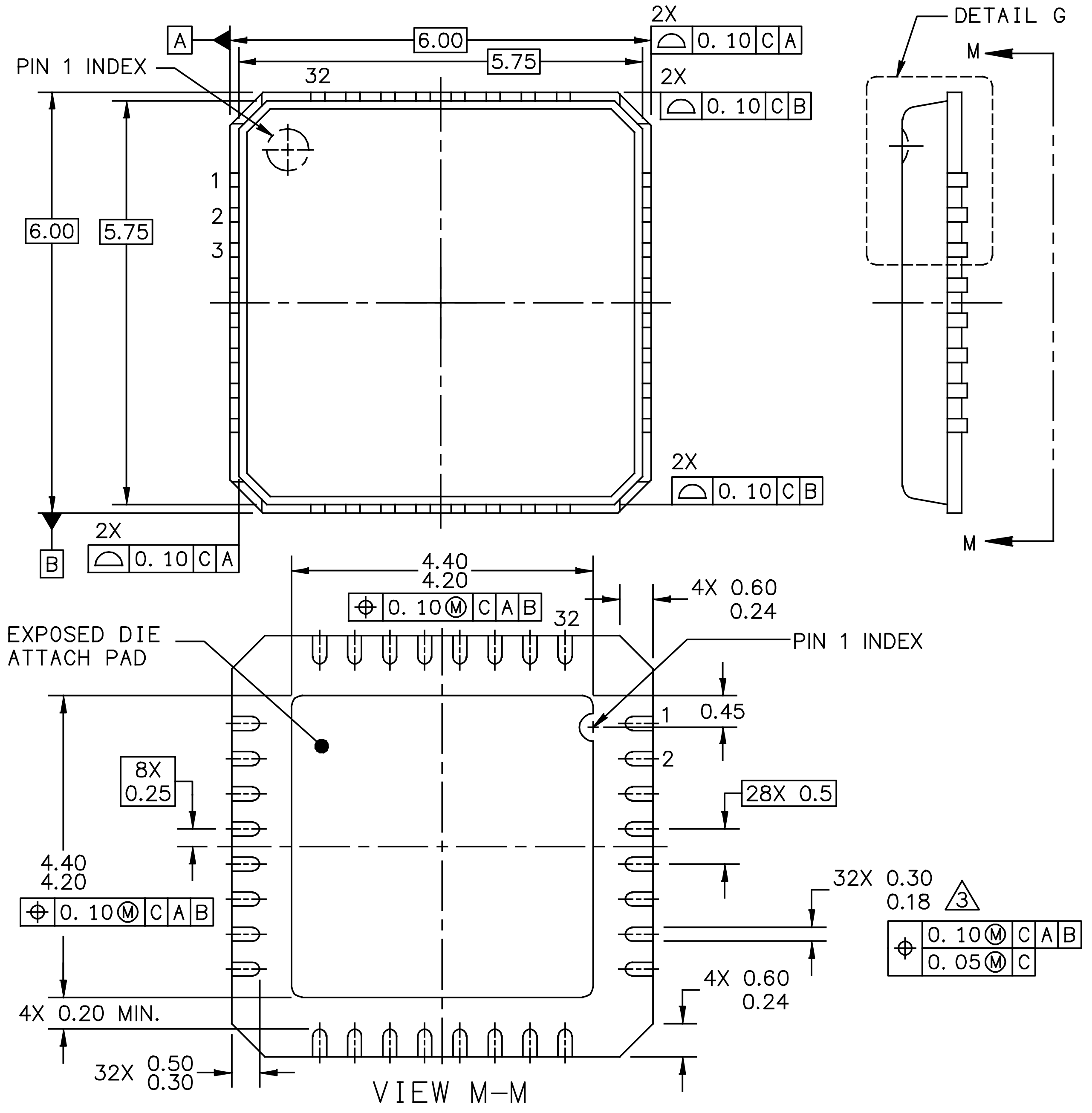


Figure 18. PCB Pad Layout for PQFN 6 × 6

Figure 19. Product Marking

PACKAGE DIMENSIONS



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MECHANICAL OUTLINE

PRINT VERSION NOT TO SCALE

TITLE:
THERMALLY ENHANCED QUAD
FLAT NON–LEADED PACKAGE (QFN)
6 X 6 X 0.85, 32 I/O, 0.5 PITCH

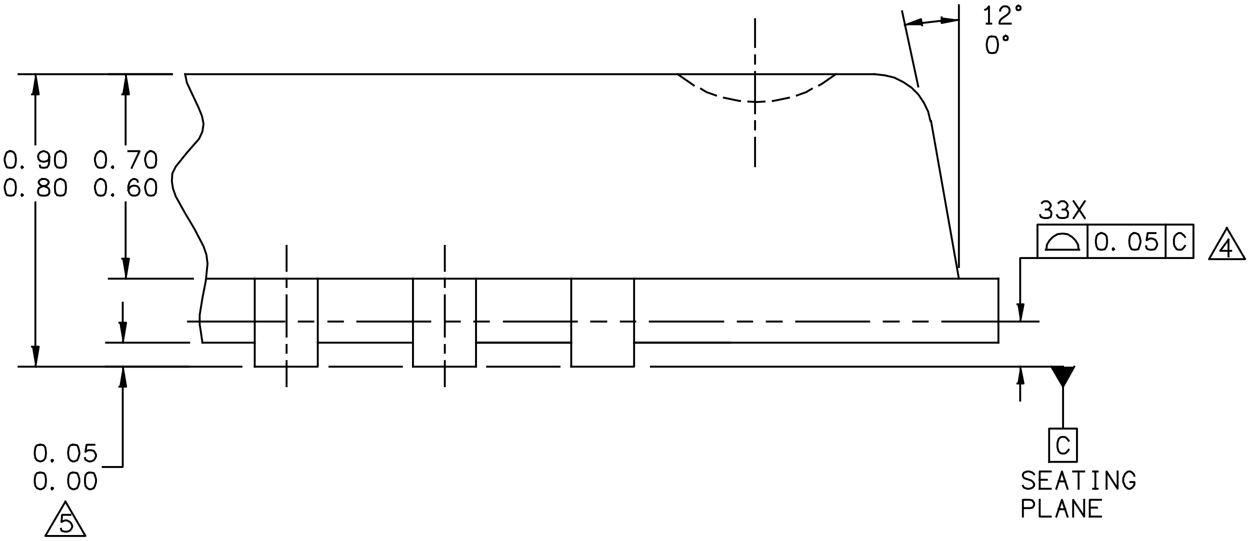
DOCUMENT NO: 98ASA00395D

REV: 0

CASE NUMBER: 2235–01

03 NOV 2011

STANDARD: NON–JEDEC



DETAIL G
VIEW ROTATED 90° CW

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TITLE: THERMALLY ENHANCED QUAD FLAT NON-LEADED PACKAGE (QFN) 6 X 6 X 0.85, 32 I/O, 0.5 PITCH	DOCUMENT NO: 98ASA00395D	REV: 0
	CASE NUMBER: 2235-01	03 NOV 2011
	STANDARD: NON-JEDEC	

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING & TOLERANCING PER ASME Y14.5 – 2009.
3. THIS DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. THIS DIMENSION APPLIES ONLY FOR TERMINALS.
6. MOLD FLASH OR PLATING COVERAGE ON THE RING PAD AREA SHALL BE ALLOWABLE

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Software

- .s3p File
- Large Signal Simulation

Development Tools

- Printed Circuit Boards
- Evaluation/Development Boards and Systems (file includes ADAM User's Guide)

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the "Part Number" link. Go to Software & Tools on the part's Product Summary page to download the respective tool.

FAILURE ANALYSIS

At this time, because of the physical characteristics of the part, failure analysis is limited to electrical signature analysis. In cases where Freescale is contractually obligated to perform failure analysis (FA) services, full FA may be performed by third party vendors with moderate success. For updates contact your local Freescale Sales Office.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	May 2013	• Initial release of data sheet
1	Aug. 2013	• Removed Freescale confidential statement, p. 1–16
2	Jan. 2015	• Table 7, Functional Pin Description, for pins 4 and 5: pin description for RF_{in} (pins 4 and 5) updated to include additional information needed for pin connection configuration, p. 3

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