TLE7183QU

3 Phase Driver IC

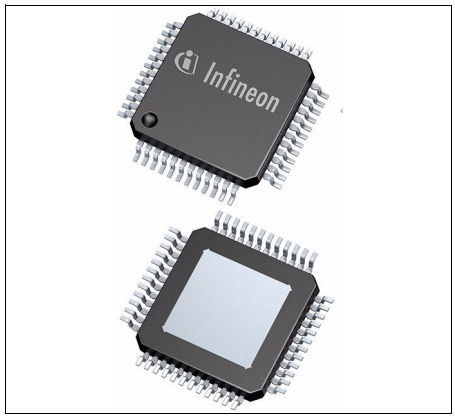
Automotive Power

Never stop thinking

Table of Contents

Table of Contents . . . 2
1 Overview . . . 3
2 Block Diagram . . . 4
3 Pin Configuration . . . 5
3.1 Pin Assignment TLE7183QU . . . 5
3.2 Pin Definitions and Functions . . . 6
4 General Product Characteristics . . . 8
4.1 Absolute Maximum Ratings . . . 8
4.2 Functional Range . . . 9
4.3 Default State of Inputs . . . 10
5 Description and Electrical Characteristics . . . 11
5.1 MOSFET Driver . . . 11
5.1.1 Output Stages . . . 11
5.1.2 Operation at Vs<12V - Integrated Charge Pumps . . . 12
5.1.3 Sleep Mode . . . 12
5.1.4 Electrical Characteristics . . . 13
5.2 Protection and Diagnostic Functions . . . 16
5.2.1 Short Circuit Detection . . . 16
5.2.2 Overcurrent Warning . . . 16
5.2.3 Dead Time and Shoot Through Protection . . . 16
5.2.4 Undervoltage Shut Down . . . 16
5.2.5 Overvoltage Shutdown . . . 17
5.2.6 Overtemperature Warning . . . 17
5.2.7 ERRx pins . . . 17
5.2.8 Electrical Characteristics . . . 18
5.3 Shunt Signal Conditioning . . . 20
5.3.1 Electrical Characteristics . . . 21
5.4 Phase Voltage Feedback . . . 23
5.4.1 Electrical Characteristics . . . 23
6 Application Description . . . 24
6.1 Layout Guide Lines . . . 25
6.2 Further Application Information . . . 25
7 Package Outlines . . . 26
8 Revision History . . . 27

1 Overview



PG-TQFP-48

Features

- Compatible with very low ohmic normal level input N-Channel MOSFETs
- Separate input for each MOSFET
- PWM frequency up to 30kHz
- Fulfils specification down to 5.5V supply voltage
- Optimized Electromagnetic Compatibility (EMC)
- TQFP-48 package with exposed heat slug
- Control inputs with TTL characteristics
- Separate source connection for each MOSFET
- Integrated minimum dead time
- Shoot through protection
- Short circuit protection with 5 fixed detection levels available
- Disable and sleep mode features
- 2-bit error diagnosis
- Thermal overload warning for driver IC
- Integrated overcurrent warning
- Integrated current sense amplifier
- 0 to 100% duty cycle
- Green Product (RoHS compliant)
- AEC Qualified

Description

The TLE7183QU driver IC is designed to control 6 to 12 external MOSFETs forming the converter for high current 3 phase motor drives in the automotive sector. It includes features like short circuit detection, 2-bit error diagnosis and high output performance. It meets the typical requirements of automotive applications, e.g. full functionality even at low battery voltages. Its 3 high side and 3 low side output stages are powerful enough to drive MOSFETs with a gate charge of 400 nC with rise and fall times of approximately 150 ns.

Typical applications are cooling fan, water pump, electro-hydraulic and electric power steering. The TLE7183QU is designed for a 12 V power net.

Several options are available for the fixed short circuit detection level.

Option	Typ. SCD level	Marking	Availability
SCD1	0.5V	TLE7183QU SCD1	please contact Infineon
SCD2	0.75V	TLE7183QU SCD2	available
SCD3	1V	TLE7183QU SCD3	please contact Infineon
SCD4	1.5V	TLE7183QU SCD4	please contact Infineon
SCD5	2.0V	TLE7183QU SCD5	available

2 Block Diagram

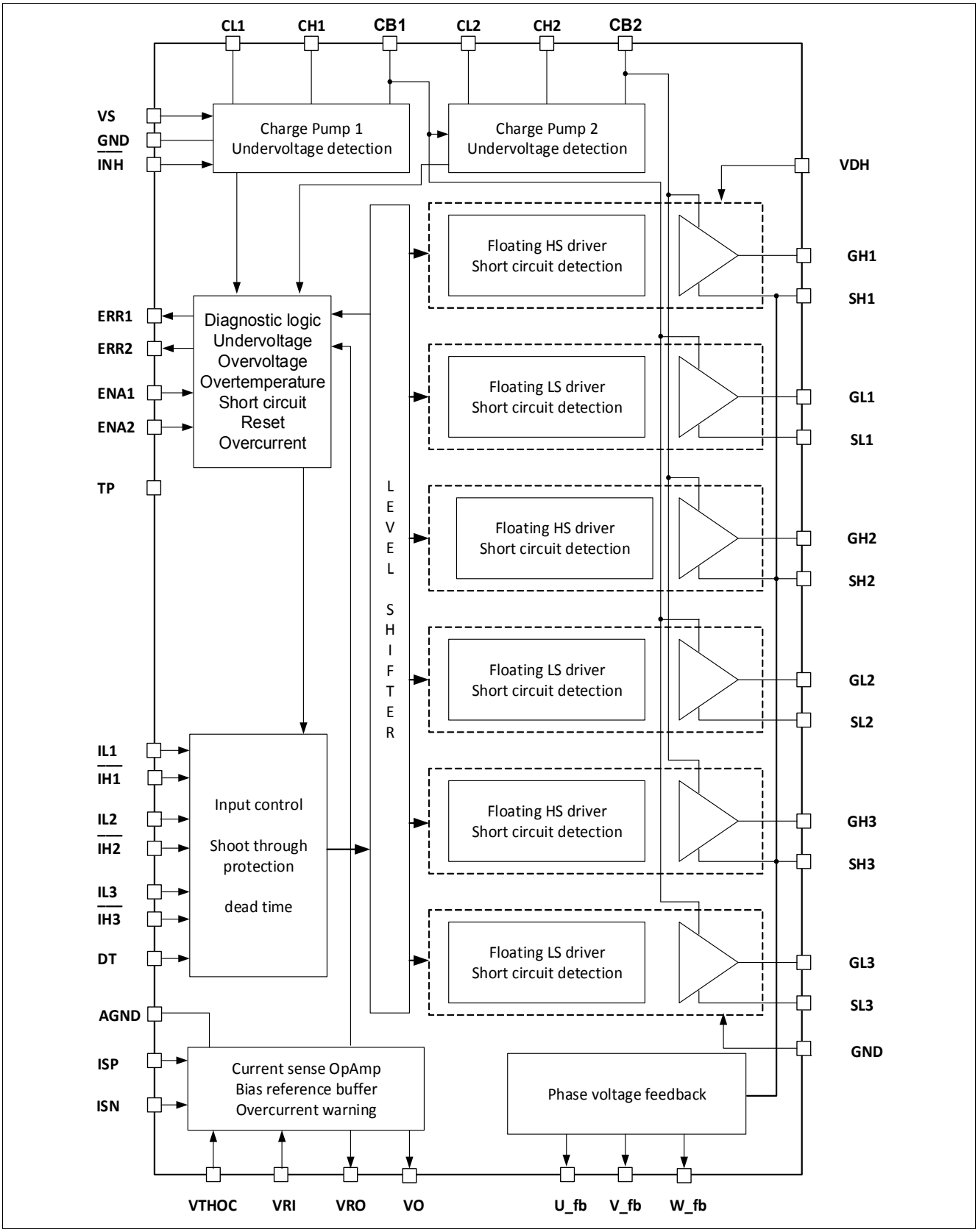


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment TLE7183QU

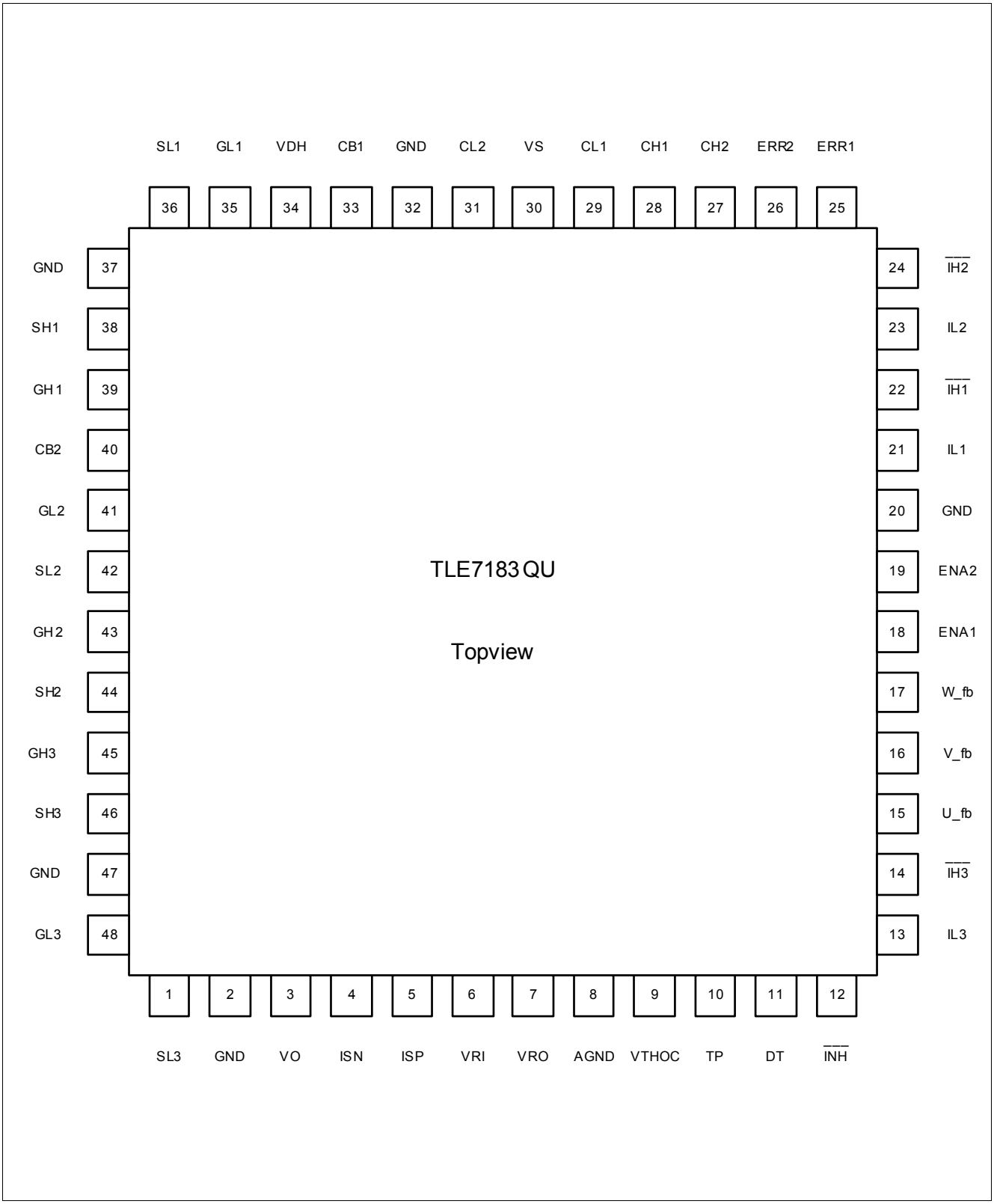


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	SL3	Connection to source low side switch 3
2	GND	Logic and power ground
3	VO	Output of OpAmp for shunt signal amplification
4	ISN	- Input of OpAmp for shunt signal amplification
5	ISP	+ Input of OpAmp for shunt signal amplification
6	VRI	Input of bias reference amplifier
7	VRO	Output of bias reference amplifier
8	AGND	Analog ground especially for the current sense OpAmp
9	VTHOC	Threshold voltage for overcurrent detection
10	TP	test pin, connect to GND of driver IC
11	DT	Dead time program pin
12	$\overline{\text{INH}}$	Inhibit pin (active low)
13	IL3	Input for low side switch 3 (active high)
14	$\overline{\text{IH3}}$	Input for high side switch 3 (active low)
15	U_fb	Digital logic representation of the voltage phase U; positive logic
16	V_fb	Digital logic representation of the voltage phase V; positive logic
17	W_fb	Digital logic representation of the voltage phase W; positive logic
18	ENA1	Enable pin (active high)
19	ENA2	Enable pin (active high)
20	GND	Logic and power ground
21	IL1	Input for low side switch 1 (active high)
22	$\overline{\text{IH1}}$	Input for high side switch 1 (active low)
23	IL2	Input for low side switch 2 (active high)
24	$\overline{\text{IH2}}$	Input for high side switch 2 (active low)
25	ERR1	Error signal 1
26	ERR2	Error signal 2
27	CH2	+ terminal for pump capacitor of charge pump 2
28	CH1	+ terminal for pump capacitor of charge pump 1
29	CL1	- terminal for pump capacitor of charge pump 1
30	VS	Voltage supply
31	CL2	- terminal for pump capacitor of charge pump 2
32	GND	Logic and power ground
33	CB1	Buffer capacitor for charge pump 1
34	VDH	Connection to drain of high side switches for short circuit detection
35	GL1	Output to gate low side switch 1
36	SL1	Connection to source low side switch 1
37	GND	Logic and power ground
38	SH1	Connection to source high side switch 1
39	GH1	Output to gate high side switch 1
40	CB2	Buffer capacitor for charge pump 2

Pin	Symbol	Function
41	GL2	Output to gate low side switch 2
42	SL2	Connection to source low side switch 2
43	GH2	Output to gate high side switch 2
44	SH2	Connection to source high side switch 2
45	GH3	Output to gate high side switch 3
46	SH3	Connection to source high side switch 3
47	GND	Logic and power ground
48	GL3	Output to gate low side switch 3

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]

40 °C ≤ T_j ≤ 150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Voltages						
4.1.1	Supply voltage	V_S	-4.0	45	V	with 10Ohm and 1µF
4.1.2	Supply voltage	V_S	-0.3	45	V	–
4.1.3	Supply voltage	V_S	-0.3	47	V	t_p<200ms
4.1.4	Voltage range at $\overline{IHx}$,ILx,ERRx, VO, DT, VTHOC, ENAx, VRI, VRO	V_{DP}	-0.3	6.0	V	–
4.1.5	Voltage range at $\overline{INH}$	V_{INH}	-0.3	18.0	V	–
4.1.6	Voltage range at TP	V_{TP}	-0.3	2	V	
4.1.7	Voltage range at SLx	V_{SL}	-7	7	V	–
4.1.8	Voltage range at SHx	V_{SH}	-7	45	V	–
4.1.9	Voltage range at GLx	V_{GL}	-7	18	V	–
4.1.10	Voltage range at GHx	V_{GH}	-7	55	V	–
4.1.11	Voltage difference Gxx-Sxx	V_{GS}	-0.3	15	V	–
4.1.12	Voltage range at VDH	V_{VDH}	-0.3	55	V	$\overline{INH}$=high
4.1.13	Voltage range at VDH	V_{VDH}	-4.0	55	V	$\overline{INH}$=high; with R_{VDH} >70Ω; 200ms, 5x
4.1.14	Voltage range at VDH	V_{VDH}	-0.3	28	V	$\overline{INH}$=low
4.1.15	Voltage range at VDH	V_{VDH}	-4.0	28	V	$\overline{INH}$=low; with R_{VDH} >70Ω; 200ms, 5x
4.1.16	Voltage range at CL1	V_{CL1}	-0.3	25	V	–
4.1.17	Voltage range at CH1, CB1	V_{CH1}	-0.3	25	V	–
4.1.18	Voltage difference CH1-CL1	V_{DC1}	-0.3	25	V	–
4.1.19	Voltage range at CL2	V_{CL2}	-0.3	25	V	–
4.1.20	Voltage range at CH2, CB2	V_{CH2}	-0.3	45	V	–
4.1.21	Voltage difference CH2-CL2	V_{CP2}	-0.3	25	V	–
4.1.22	Voltage range at ISP, ISN	V_{ISI}	-5	5	V	–
4.1.23	Output current range at VO	I_{VO}	-20	20	mA	–
4.1.24	Gate resistor	R_{Gate}	2	–	Ω	–
4.1.25	Voltage range at U_fb, V_fb and W_fb	V_{X_fb}	-0.3	6	V	–
Temperatures						
4.1.26	Junction temperature	T_j	-40	150	°C	–
4.1.27	Storage temperature	T_{stg}	-55	150	°C	–

Absolute Maximum Ratings (cont'd)[1)]

40 °C ≤ T_j ≤ 150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.1.28	Lead soldering temperature (1/16'' from body)	T_{sol}	–	260	°C	–
4.1.29	Peak reflow soldering temperature[2)]	T_{ref}	–	260	°C	–
Thermal Resistance						
4.1.30	Junction to case	R_{thjC}	–	5	K/W	–
Power Dissipation						
4.1.31	Power Dissipation (DC) @ T_{CASE}=125°C	P_{tot}	–	2	W	–
ESD Susceptibility						
4.1.32	ESD Resistivity[3)]	V_{ESD}	–	2	kV	
4.1.33	ESD Resistivity to GND	V_{ESD}	-500	500	V	CDM[4)]
4.1.34	ESD Resistivity Pin 1, 12, 13, 24, 25, 36, 37,48 (corner pins) to GND	$V_{ESD1, 12, 13, 24, 25, 36, 37, 48}$	-750	750	V	CDM[4)]

1) Not subject to production test, specified by design.
2) Reflow profile IPC/JEDEC J-STD-020C
3) ESD susceptibility HBM according to EIA/JESD 22-A 114B
4) ESD susceptibility, Charged Device Model "CDM" ESDA STM5.3.1

Attention: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Attention: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Supply voltage[1)2)]	V_S	5.5 5.5	20 28	V	DC t<1s
4.2.2	Duty cycle[3)]	D	0	100	%	–
4.2.3	PWM frequency	f_{PWM}	0	25	kHz	Total gate charge 400nC
4.2.4	Quiescent current[4)]	I_Q	–	30	µA	V_S,V_{DH}<20 V
4.2.5	Quiescent current into VDH	I_{Q_VDH}	–	30	µA	V_{DH}<20V; V_S pin open
4.2.6	Supply current at Vs	I_{Vs}	 – – 	 175 175 110 110	mA	f_{PWM}=25kHz Q_G=250nC: V_S = 5.5V V_S = 14V V_S = 17V V_S = 20V

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.7	Supply current at Vs(device disabled by ENA)	$I_{Vs(o)}$	–	60 50	mA	Vs=5.5V..17V Vs=17V..20V
4.2.8	Currrent into VDH (device not in sleep mode)	I_{VDH}		1.5	mA	V_{VDH}=5.5..20V $\overline{INH}$=high
4.2.9	Voltage difference CB2-VDH	V_{CB2}	-0.3	25	V	Operation mode
4.2.10	Junction temperature	T_j	-40	150	°C	

1) max ratings for Tj has to be considered as well
2) For proper start up minimum Vs=6.5V is required
3) Duty cycle is referred to the high side input command ($\overline{IHx}$); The duty cycles can be driven continuously and fully operational
4) total current consumption from power net (Vs and VDH)

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Default State of Inputs

Table 1 Default State of Inputs

Characteristic	State	Remark
Default state of ILx (if ILx left open)	Low	Low side MOSFETs off
Default state of $\overline{IHx}$ (if $\overline{IHx}$ left open)	High	High side MOSFETs off
Default state of ENA (if ENA1 left open)	Low	Device outputs disabled
Default state of ENA (if ENA2 left open)	Low	Device outputs disabled
Default state of $\overline{INH}$ (if $\overline{INH}$ left open)	Low	Sleep mode, I_Q < 30 µA
Default State of sense amplifier output V_O (ISP=ISN=0V)	Zero ampere equivalent	–
Status of the device and the outputs when ENA1=ENA2=$\overline{INH}$=high	Device active and outputs functional	Vs=5.5..28V
Pull up or pull down integrated resistors Ixx, ENA	30kΩ +/-50%	–
Pull down integrated resistor $\overline{INH}$	45kΩ +/-50%	–

Note: The load condition "C=22nF; R_{Load}=1Ω" in the paragraph "Electrical characteristics / Dynamic characersitic" means that R_{Load} is connected between the output Gxx and the positive terminal of the C. The negative terminal of the C is connected to GND and the corresponding Sxx. The voltage is measured at the positive terminal of the C.

5 Description and Electrical Characteristics

5.1 MOSFET Driver

5.1.1 Output Stages

The six powerful push-pull output stages of the TLE7183QU are floating blocks, each one of them with its own source pin which can be directly connected to the source pin of an external MOSFET. This enables a perfect control of each MOSFET's gate-source voltage even if a current of 200A is driven in the bridge.

All output stages have the same high output power. A single output stage is able to drive a single MOSFET with 400nC gate charge (or two MOSFETs with 200nC) achieving rise and fall times of approx. 150ns.

They can be switched with a frequency of up to 30kHz. The usability at higher frequencies is limited by the maximum allowed power dissipation, the max. junction temperature and the limited current capabilities of the charge pump.

Each output stage has its own short circuit detection block. Please see **Chapter 5.2.1** for short circuit detection details.

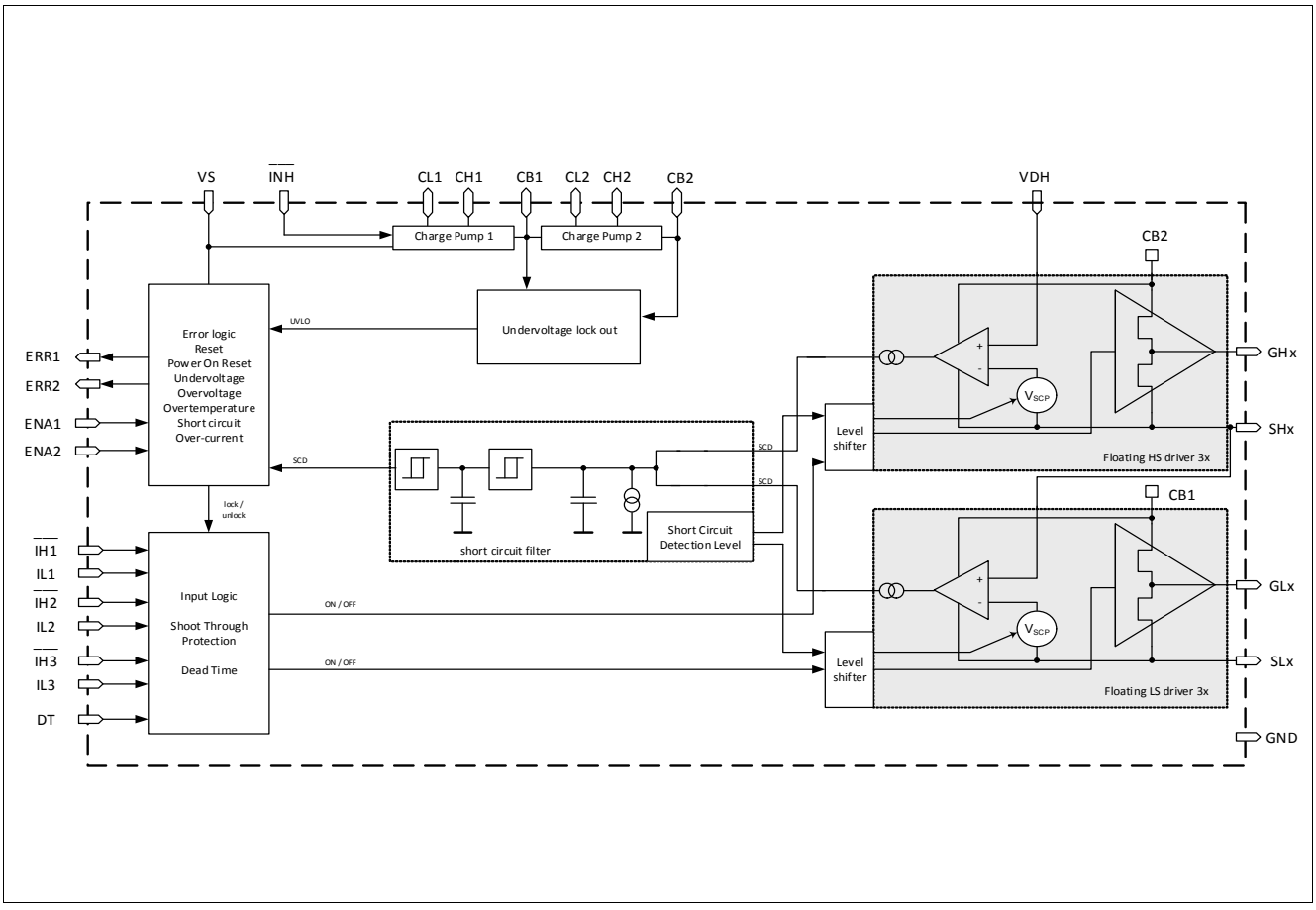


Figure 3 Block Diagram of Driver Ouput Stages including Short Circuit Detection

5.1.2 Operation at Vs<12V - Integrated Charge Pumps

In 12V automotive applications, correct operation has to be assured also at lower supply voltages, even at 9V. At low supply voltages conventional bridge drivers provide clearly less than 9V to the gate of an external MOSFET. However low gate-source voltage increases R_{DSon} of the MOSFET. This leads to an undesired, higher power dissipation.

The two charge pumps circuitries of TLE7183QU address this problem enabling operation even at lower supply voltages. Their operational capability does not depend on a specific pulse pattern of the MOSFETs overcoming duty cycle limitations which are inherent to drivers that use the bootstrap principle instead. Therefore TLE7183QU supports the complete duty cycle range from 0 to 100%. This simplifies the usabilty in all applications and especially when used with block wise commutation. The charge pumps are only deactivated if the device is set to sleep mode using $\overline{INH}$.

The first charge pump supplies the low side MOSFETs and the corresponding output stages with sufficient voltage to assure 10V gate-source voltage even if Vs<10V. In addition it also supplies most of the internal circuitries, including the second charge pump.

The second charge pump supplies the high side MOSFETs and the corresponding output stages. It is pumped on the voltage of Vs.

Each charge pump circuitry requires external pump (CPx) and buffer (CBx) capacitors. The output of the first charge pump is CB1 which is referenced to GND. The output of the second charge pump is CB2 which is referenced to VDH. VDH and Vs are usually in the same voltage range. The driver is not designed to have significant higher voltages at VDH compared to Vs. This would lead to reduced supply voltages for the high side output stages.

The outputs of both charge pumps are regulated. The first charge pump doubles the supply voltage for Vs<8V. For 8V<Vs<15V, its output is regulated to a typical voltage of 15V. For Vs>15V, its output increases linearly but does not exceed 25V.

For a proper wake up of the device at V_{VsWU}, it is not permitted to have any PWM patterns at the input pins ILx and $\overline{IHx}$ before the charge pumps have ramped up to their final values unless the output stages have been switched off by setting one of the ENAx pins to low.

The size of the charge pump capacitors (pump capacitors CPx as well as buffer capacitors CBx) can be varied between 1 µF and 4.7 µF. Yet, larger capacitor values result in higher charge pump voltages and less voltage ripple on the charge pump buffer capacistors CBx (which supply the internal circuits as well as the external MOSFETs, pls. see above). Besides the capacitance values the ESR of the buffer capacitors CBx determines the voltage ripple as well. It is recommended to use buffer capacitors CBx that have small ESR.

Please see also **Chapter 5.1.3** for capacitor selection.

5.1.3 Sleep Mode

If the $\overline{INH}$ pin is set to low, the driver will be set to sleep mode. The $\overline{INH}$ pin switches off the complete supply structure of the device and finally leads to an undervoltage shut down of the complete driver. Enabling the device with the $\overline{INH}$ pin means to switch on the supply structure. The device will run through power on reset during wake up. It is recommended to perform a reset using ENAx after wake up to remove possible $\overline{ERRx}$ signals. Reset is performed by keeping one or more ENAx pins low until the charge pump voltages have ramped up.

Enabling and disabling with the $\overline{INH}$ pin is not very fast. Please consider using the ENAx pins to speed things up.

If the TLE7183QU is in sleep mode or if the supply voltage Vs is not available, then the driver IC is not supplied, the charge pumps are inactive and the charge pump capacitors are discharged. Pin CB2 (+ terminal of buffer capacitor 2) will decay to GND. If the battery voltage is still applied to VDH (- terminal of buffer capacitor 2) the buffer capacitor 2 will slowly be charged to battery voltage with reversed polarity compared to the one during regular operation. Hence, it is important to use a buffer capacitor 2 (CB2) that can withstand both, +25 V in regular operation mode and $-V_{BAT}$ in sleep mode, e.g. a ceramic capacitor. If there is load dump in sleep mode, then the negative voltage across CB2 will be clamped to -31 V (CB2 referenced to VDH).

5.1.4 Electrical Characteristics

Electrical Characteristics MOSFET drivers - DC Characteristics

V_S = 5.5 to 20V, T_j = -40 to +150°C, f_{PWM} < 25kHz, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.1.1	Low Level Output Voltage	V_{G_LL}	–	–	0.2	V	I=30mA
5.1.2	High Level Output Voltage, Low Side	V_{G_HL}	7.5	–	13	V	I=-2mA; Vs=5.5..8V
5.1.3	High Level Output Voltage, High Side	V_{G_HL}	6.5	–	13	V	I=-2mA; Vs=5.5..8V
5.1.4	High Level Output Voltage	V_{G_HL}	9	–	13	V	I=-2mA; Vs=8..20V
5.1.5	High Level Output Voltage Difference	dV_{G_H}	–	–	1.0	V	I=-100mA; Vs=20V
5.1.6	Gate Drive Output Voltage (device disabled via ENAx)	$V_{G(DIS)}$	–	–	0.2	V	Disabled; Vs=5.5..20V; I=10mA
5.1.7	Gate Drive Output Voltage Tj=-40°C Tj=25°C Tj=150°C	V_{G_5}	–	–	 1.4 1.2 1.0	V	UVLO; Vs<=5.5V
5.1.8	Gate Drive Output Voltage High Side Tj=-40°C Tj=25°C Tj=150°C	V_{G_HS}	–	–	 1.4 1.2 1.0	V	Overvoltage
5.1.9	Gate Drive Output Voltage Low Side	V_{G_LS}	–	–	0.2	V	Overvoltage
5.1.10	Low Level Input Voltage of Ixx, ENAx	V_{I_LL}	–	–	1.0	V	–
5.1.11	High Level Input Voltage of Ixx, ENAx	V_{I_HL}	2.0	–	–	V	–
5.1.12	Low Level Input Voltage of $\overline{INH}$	V_{I_LL}	–	–	0.75	V	–
5.1.13	High Level Input Voltage of $\overline{INH}$	V_{I_HL}	2.1	–	–	V	–
5.1.14	Input Hysteresis of $\overline{IHx}$, ILx, ENAx	dV_I	50	–	–	mV	Vs=5.5..8V
5.1.15	Input Hysteresis of $\overline{IHx}$, ILx, ENAx	dV_I	100	200	–-	mV	Vs=8..20V
5.1.16	Output Bias Current SHx	I_{SHx}	-1.6	-1.0	-0.3	mA	VSHx=0..(Vs+1); ILx=low; $\overline{IHx}$=high
5.1.17	Output Bias Current SLx	I_{SLx}	-1.6	-1.0	-0.3	mA	VSLx=0..7V; ILx=low; $\overline{IHx}$=high

Electrical Characteristics MOSFET drivers - Dynamic Characteristics

V_S = 5.5 to 20V, T_j = -40 to +150°C, f_{PWM} < 25kHz, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.1.18	Minimum Internal Dead Time	t_{DT_MIN}	50	–	200	ns	DT pin to GND (R_{DT}=0Ω)
5.1.19	Programmable Internal Dead Time	t_{DT}	0.26 0.64 1.07 2.02	0.41 1.05 1.85 3.82	0.56 1.45 2.63 5.62	µs	R_{DT}=10 kΩ R_{DT}=47 kΩ R_{DT}=100 kΩ R_{DT}=1000 kΩ
5.1.20	Maximum Internal Dead Time	t_{DT_MAX}	2.33	–	6.35	µs	DT pin open
5.1.21	Turn On Current, Peak	$I_{G(on)}$	–	-0.8	–	A	VGxx-VSxx=0V; Vs=5.5..8V; C=22nF; R_{Load}=1Ω
5.1.22	Turn On Current, Peak	$I_{G(on)}$	–	-1.5	–	A	VGxx-VSxx=0V; Vs=8..20V C=22nF; R_{Load}=1Ω
5.1.23	Turn Off current, Peak	$I_{G(off)}$	–	1.5	–	A	VGxx-VSxx=10V; Vs=8..20V C=22nF; R_{Load}=1Ω
5.1.24	Rise Time (20-80%) T_j = -40°C T_j = 25°C T_j = 150°C	t_{G_rise}	–	 150	 400 400 700	ns	C=22nF; R_{Load}=1Ω
5.1.25	Fall Time (20-80%) T_j = -40°C T_j = 25°C T_j = 150°C	t_{G_fall}	–	 150	 230 230 500	ns	C=22nF; R_{Load}=1Ω
5.1.26	Input Propagation Time (Low on)	$t_{P(ILN)}$	90	190	290	ns	C=22nF; R_{Load}=1Ω
5.1.27	Input Propagation Time (Low off)	$t_{P(ILF)}$	0	100	200	ns	C=22nF; R_{Load}=1Ω
5.1.28	Input Propagation Time (High on)	$t_{P(IHN)}$	90	190	290	ns	C=22nF; R_{Load}=1Ω
5.1.29	Input Propagation Time (High off)	$t_{P(IHF)}$	0	100	200	ns	C=22nF; R_{Load}=1Ω
5.1.30	Absolute Input Propagation Time Difference (all channels turn on)	$t_{P(an)}$	–	–	70	ns	C=22nF; R_{Load}=1Ω
5.1.31	Absolute Input Propagation Time Difference (all channels turn off)	$t_{P(af)}$	–	–	50	ns	C=22nF; R_{Load}=1Ω
5.1.32	Absolute Input Propagation Time Difference (1channel High off - Low on)	$t_{P(1hfln)}$	–	–	150	ns	C=22nF; R_{Load}=1Ω
5.1.33	Absolute Input Propagation Time Difference (1channel Low off - High on)	$t_{P(1lfhn)}$	–	–	150	ns	C=22nF; R_{Load}=1Ω

Electrical Characteristics MOSFET drivers - Dynamic Characteristics

V_S = 5.5 to 20V, T_j = -40 to +150°C, f_{PWM} < 25kHz, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.1.34	Absolute Input Propagation Time Difference (all channels High off - Low on)	$t_{P(ahfln)}$	–	–	150	ns	C=22nF; R_{Load}=1Ω
5.1.35	Absolute Input Propagation Time Difference (all channels Low off - High on)	$t_{P(alfhn)}$	–	–	150	ns	C=22nF; R_{Load}=1Ω
5.1.36	Wake Up Time; $\overline{INH}$ Low to High	t_{INH_Pen}	–	–	20	ms	Driver fully functional; Vs=6.5...8V; ENAx=low; CPx=CBx=4.7µF
5.1.37	Wake Up Time; $\overline{INH}$ Low to High	t_{INH_Pen}	–	–	10	ms	Driver fully functional; VS=8..20V; ENAx=low; CPx=CBx=4.7µF;
5.1.38	Wake Up Time Logic Functions; $\overline{INH}$ Low to High	t_{INH_log}	–	–	10	ms	diagnostic, OpAmp working; Vs=6.5...8V; ENAx=low; CPx=CBx=4.7µF
5.1.39	Wake Up Time Logic Functions; $\overline{INH}$ Low to High	t_{INH_log}	–	–	5	ms	diagnostic, OpAmp working; VS=8..20V; ENAx=low; CPx=CBx=4.7µF
5.1.40	$\overline{INH}$ Propagation Time to Disable the Output Stages	$t_{INH_P(O)}$	–	–	10	µs	Vs=5.5..8V
5.1.41	$\overline{INH}$ Propagation Time to Disable the Output Stages	$t_{INH_P(O)}$	–	–	8	µs	Vs=8..20V
5.1.42	$\overline{INH}$ Propagation Time to Disable the entire Driver IC	$t_{INH_P(IC)}$	–	–	300	µs	–
5.1.43	Supply Voltage V_s for Wake Up	V_{VsWU}	6.5	–	–	V	diagnostic, OpAmp working;
5.1.44	Charge Pump Frequency	f_{CP}	38	55	72	kHz	–

5.2 Protection and Diagnostic Functions

5.2.1 Short Circuit Detection

The TLE7183QU provides a short circuit detection for the external MOSFETs. It monitors their drain-source voltage. It is active as soon as the corresponding input is set to "on" and the dead time has elapsed.

If the drain-source voltage is higher than the short circuit detection level, a timer will be started. After a delay of about 6 µs all external MOSFETs will be switched off. The ERRx pins will indicate a short circuit. This error is not self-clearing. The driver has to be reset using one of the ENAx pins.

The short circuit detection level is a fixed setting of the chip. Several options are available and described in **Chapter 5.2.8**.

5.2.2 Overcurrent Warning

The TLE7183QU offers the possibility to have a warning at the ERRx pins if a current threshold is reached. (see **Figure 4**).

The output of the current sense OpAmp is connected to an integrated comparator. It compares the amplified current sense signal with an external adjustable threshold. After the comparator a blanking time (1.5 µs typ.) is implemented to avoid false triggering caused by an overshoot of the current sense signal. If the overcurrent situation is detected, there is a warning at the ERRx pins.

The driver remains in normal operation mode. The overcurrent warning is self-clearing. It will be cleared if the current drops below the overcurrent limit set on the VTHOC pin. The overcurrent warning is also cleared if the current commutates from the low side MOSFET to the associated high side MOSFET (no current through the shunt resistor).

It is up to the user to react on the overcurrent warning by modifying the Ixx patterns to lower the current.

5.2.3 Dead Time and Shoot Through Protection

In bridge applications it has to be assured that the external high side and low side MOSFETs in a single half bridge are not switched on at the same time. This would lead to a direct connection from battery voltage to GND. The integrated mechanisms of TLE7183QU preventing this are called shoot through protection and minimum dead time generation.

The shoot through protection is a locking mechanism which deals with faulty input commands at the Ixx pins. If the command is given to switch on the high side and the low side MOSFET of a single half bridge at same time, it is ignored. The driver output stages remain unchanged.

The dead time of a half bridge is the time after the command to switch off a MOSFET has been given during which the command to switch on the other MOSFET is not executed. A minimum dead time has to be applied because switching does not happen instantly. If both MOSFETs of a single half bridge start to switch at the same time, both of them may be on at the same time causing the critical connection from battery voltage to ground. The dead time assures that a MOSFET is only switched on after the other one has been switched off.

The exact dead time of the bridge is usually set by the PWM generation unit of the µC. The minimum dead time generation of TLE7183QU assures a minimum dead time if the input signals from the µC are faulty. If the DT pin is connected to GND, the generated minimum dead time is fixed to 50..200ns .

It can be increased by connecting the DT pin via a dead time resistor R_{DT} to GND - the larger the dead time resistor, the larger the dead time (please see **Programmable Internal Dead Time** for details).

5.2.4 Undervoltage Shut Down

The TLE7183QU has an integrated undervoltage shut down, to assure that the behavior of the device is predictable in all supply voltage ranges.

If the voltage of a charge pump buffer capacitors CBx reaches the undervoltage shut down level for a minimum specified filter time, the gate-source voltage of all external MOSFETs will be actively pulled to low. In this situation the short circuit detection of this output stage is deactivated to avoid a latching shut down of the driver.

If the charge pump buffer voltage recovers, the status of the output stages will match the input patterns again. This allows an operation of the motor in case of undervoltage shut down without a reset by the µC.

Undervoltage shut down will not occur if V_S > 6 V, Q_G < 250 nC, f_{PWM} < 25 kHz, and the charge pump capacitors CPx, CBx = 4.7 µF.

5.2.5 Overvoltage Shutdown

The TLE7183QU has an integrated overvoltage shut down to avoid destruction of the IC at high supply voltages. The voltages at the pins Vs and VDH are monitored. The external MOSFETs will be switched off if one or both of them exceed the overvoltage shut down level for more than the specified filter time. In addition, the overvoltage condition will lead to a shut down of the charge pumps and a discharge of the charge pump capacitors. This results in an undervoltage condition which will be indicated at the ERRx pins. During overvoltage shut down the external MOSFETs and the charge pumps remain off until a reset is performed.

5.2.6 Overtemperature Warning

If the junction temperature is exceeding typ. 170°C, an overtemperature warning is reported at the ERRx pins. However the driver IC will continue to operate in order not to disturb the application.

This warning is self-clearing and will be cleared if the junction temperature cools down again. It is up to the user to protect the device from overtemperature destruction.

5.2.7 ERRx pins

The TLE7183QU has two status pins to provide diagnostic feedback to a µC. The outputs of these pins are 5V push pull stages which are either high or low. **Table 2** contains an overview. Some errors require a full reset of the driver using one of the ENAx pins to return to normal operation. Please see **Table 3** for details.

If multiple errors occur at the same time, only the one with the highest priority listed in **Table 4** is reported. If the device is disabled using one of the ENAx pins, only the errors Undervoltage and Overtemperature Warning are reported. Other errors are not reported.

Table 2 Overview of Error Conditions

ERR1	ERR2	Driver conditions
Low	Low	no errors
High	Low	Overtemperature Warning or Overvoltage Shut Down
High	High	Undervoltage Shut Down
Low	High	Short Circuit Detection or Overcurrent Warning

Table 3 Behavior at different Error Conditions

Error condition	restart behavior	Shuts down...
Short Circuit Detection	Latch, reset must be performed at ENAx pin	All external Power -MOSFETs
Overcurrent Warning	Self clearing	Nothing
Undervoltage Shut Down	Auto restart	All external Power -MOSFETs
Overvoltage Shut Down	Latch, reset must be performed at ENAx pin	All external Power -MOSFETs
Overtemperature Warning	Self clearing	Nothing

Note: Errors do NOT lead to sleep mode. Sleep mode is only initiated with the $\overline{INH}$ pin. The latch and restart behavior allows to distinguish between the different combined error types reported at the ERRx pins.

Table 4 Prioritization of Errors

Priority	Error
1	Short Circuit Detection
2	Undervoltage Shut Down
3	Overvoltage Shut Down
4	Overtemperature Warning Overcurrent Warning

5.2.8 Electrical Characteristics

Electrical Characteristics - Protection and diagnostic functions

V_S = 5.5 to 20V, T_j = -40 to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Overtemperature							
5.2.1	Overtemperature Warning	$T_{j(OW)}$	150	170	190	°C	–
5.2.2	Hysteresis for Overtemperature Warning	$dT_{j(OW)}$	–	20	–	°C	–
Overcurrent warning							
5.2.3	Overcurrent Threshold	V_{THOC}	2	–	4.5	V	Vs=5.5..8V
5.2.4	Overcurrent Threshold	V_{THOC}	2	–	4.8	V	Vs=8..20V
5.2.5	Input Offset Voltage of OC Comp	V_{OCOF}	-50	–	50	mV	–
5.2.6	Input Offset Voltage Temperature Drift of OC Comp[1)]	V_{IO}	-5	–	5	mV	–
5.2.7	Overcurrent Warning Threshold Hysteresis	dV_{THOC}	25		–	mV	Vs=5.5..8V
5.2.8	Overcurrent Warning Threshold Hysteresis	dV_{THOC}	50	80	–	mV	Vs=8..20V
5.2.9	Filter Time of Overcurrent Warning	t_{OC}	1.0	1.5	3.0	µs	
Short Circuit Protection							
5.2.10	Filter Time of Short Circuit Protection	$t_{SCP(off)}$	4.5	6.8	9	µs	default
5.2.11	Maximum Duty Cycle for no SCD[2)]	$D_{ySCDmax}$	–	–	6	%	f_{PWM}=20kHz at $\overline{IHx}$ or ILx and at static applied SC
5.2.12	Minimum Duty Cycle for Periodic SCD[2)]	$D_{ySCDmin}$	13	–	–	%	f_{PWM}=20kHz at $\overline{IHx}$ or ILx and at static applied SC
5.2.13	Short Circuit Detection Level SCD1	$V_{SCP1(off)}$	0.3	0.5	0.65	V	please contact Infineon
5.2.14	Short Circuit Detection Level SCD2	$V_{SCP2(off)}$	0.6	0.75	0.9	V	–
5.2.15	Short Circuit Detection Level SCD3	$V_{SCP3(off)}$	0.85	1.0	1.15	V	please contact Infineon

Electrical Characteristics - Protection and diagnostic functions (cont'd)

V_S = 5.5 to 20V, T_j = -40 to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.2.16	Short Circuit Detection Level SCD4	$V_{SCP4(off)}$	1.35	1.5	1.65	V	please contact Infineon
5.2.17	Short Circuit Detection Level SCD5	$V_{SCP5(off)}$	1.8	2.0	2.2	V	–
ERRx pins							
5.2.18	High Level Output Voltage of ERRx	V_{OHERR}	4.0	–	5.2	V	I= -0.2mA
5.2.19	Low Level Output Voltage of ERRx	V_{OLERR}	-0.1	–	0.4	V	I= 0.2mA
5.2.20	Propagation Time Difference ERR1 to ERR2	$t_{PD(ERR)}$		–	200	ns	–
5.2.21	Rise Time ERRx (20 - 80 %)	$t_{r(ERR)}$	50	–	600	ns	C_{LOAD}=100pF
5.2.22	Fall Time ERRx (80 - 20 %)	$t_{f(ERR)}$	50	–	400	ns	C_{LOAD}=100pF
Over- and undervoltage							
5.2.23	Overvoltage Shut Down	$V_{OV(off)}$	28	–	33	V	on Vs and/or VDH
5.2.24	Overvoltage Filter Time	t_{OV}	30	–	65	µs	–
5.2.25	Undervoltage Shut Down CB1	V_{UV1}	6.75	–	8.25	V	CB1 to GND
5.2.26	Undervoltage Shut Down CB2	V_{UV2}	3.9	–	5.7	V	CB2 to VDH
5.2.27	Undervoltage Shut Down Hysteresis of CB1 and CB2	V_{DUV}	–	1.0	–	V	–
5.2.28	Undervoltage Filter Time	t_{UV}	1	–	3	µs	–
Reset and Enable							
5.2.29	Reset Time to clear ERRx Registers	t_{Res1}	2.0	–	–	µs	–
5.2.30	Low Time of ENAx Signal without Reset	t_{Res0}	–	–	0.5	µs	–
5.2.31	ENAx Propagation Time (High --> Low)	t_{PENA_H-L}	–	–	2.0	µs	–
5.2.32	ENAx Propagation Time (Low --> High)	t_{PENA_L-H}	–	–	0.5	µs	–
5.2.33	Return Time to Normal Operation at Auto-Restart	t_{AR}	–	–	1.0	µs	–

1) Not subject to production test; specified by design

2) Parameters describe the behavior of the internal SCD circuit. Therefore only internal delay times are considered. In application dead-/ delay times determined by application circuit (switching times of MOSFETs, adjusted dead time) have to be considered as well.

5.3 Shunt Signal Conditioning

The TLE7183QU incorporates a fast and precise operational amplifier for conditioning and amplification of the current sense shunt signal. A reference bias buffer is integrated to provide an adjustable bias reference for the three OpAmps. The voltage divider connected to the VRI pin should be less than 50 kOhm. If required at all, the filtering capacitor should be less than 1.2 µF. The gain of the OpAmp can be adjusted by external resistors within a range of 5 to 15.

If V(ISP) equals V(ISN), VO provides the reference voltage VRO. Using a voltage divider VRO is usually set to half of the regulated voltage to allow bi-directional current sensing. The additional buffer permits the adaptation of the reference bias to different µC I/O voltages.

The output of the I-DC link Opamp VO is not short-circuit proof.

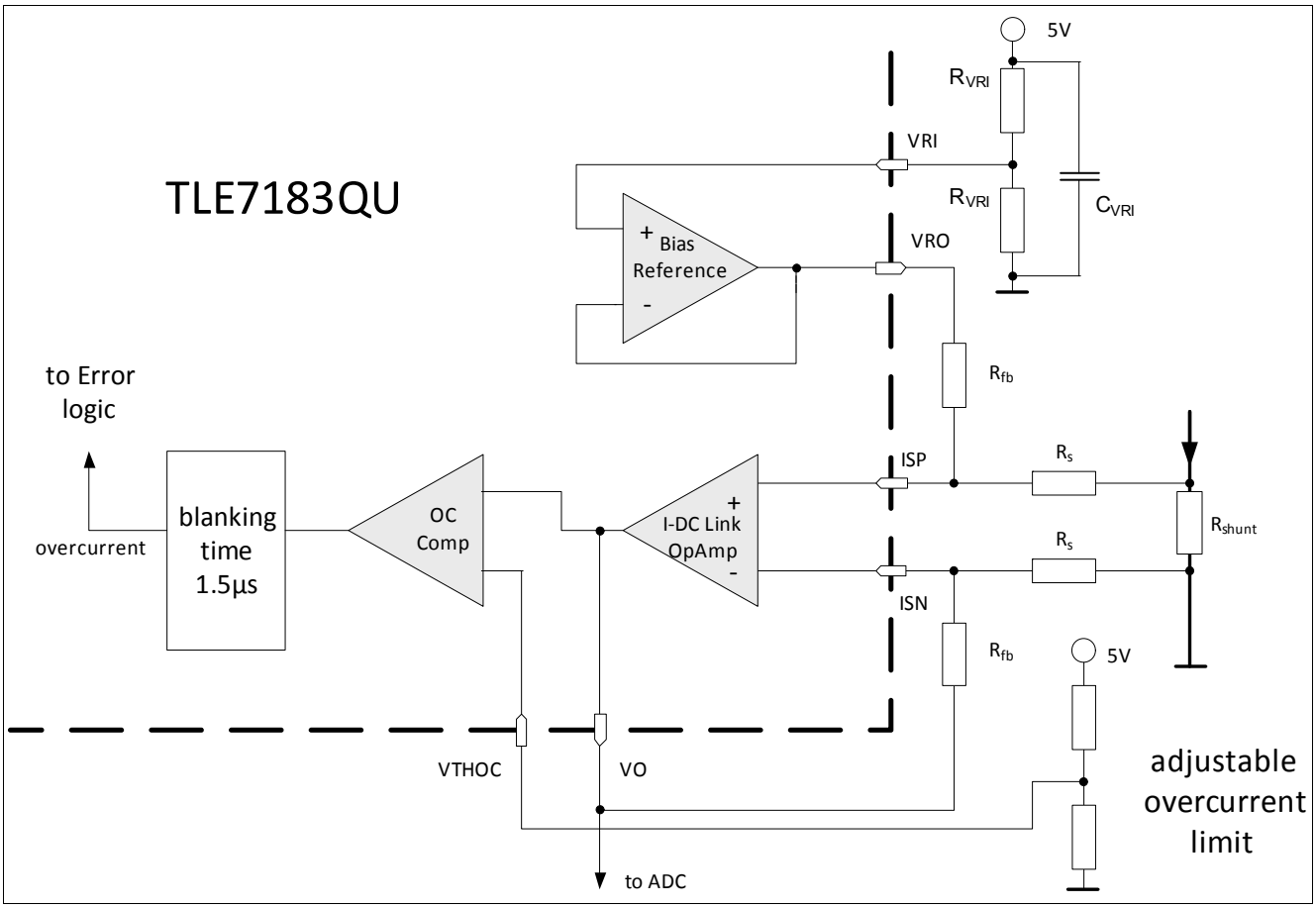


Figure 4 Shunt Signal Conditioning Block Diagram and Overcurrent Limitation

For overcurrent warning, please see **Chapter 5.2.2**.

5.3.1 Electrical Characteristics

Electrical Characteristics - Current sense signal conditioning

V_S = 5.5 to 20V, T_j = -40 to +150°C, f_{PWM} < 25kHz, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.3.1	Series Resistors	R_S	100	500	1000	Ω	–
5.3.2	Feedback Resistor Limited by the Output Voltage Dynamic Range	R_{fb}	2000	7500	–	Ω	–
5.3.3	Resistor Ratio (Gain Ratio)	R_{fb}/R_S	5	–	15	–	–
5.3.4	Steady State Differential Input Voltage Range across VIN[1)]	$V_{IN(ss)}$	-400	–	400	mV	–
5.3.5	Transient Differential Input Voltage Range across VIN	$V_{IN(tr)}$	-800	–	800	mV	–
5.3.6	Input Differential Voltage (ISP - ISN)	V_{IDR}	-800	–	800	mV	–
5.3.7	Input Voltage (Both Inputs - GND) (ISP - GND) or (ISN -GND)	V_{LL}	-800	–	1500	mV	Vs=5.5..8V
5.3.8	Input Voltage (Both Inputs - GND) (ISP - GND) or (ISN -GND)	V_{LL}	-800	–	2000	mV	Vs=8..20V
5.3.9	Input Offset Voltage of the I-DC link OpAmp	V_{IO}	–	1	+/-5	mV	R_S=500Ω; V_{CM}=0V; V_O=1.65V; V_{RI}=1.65V
5.3.10	Input Offset Voltage Temperature Drift of the I-DC link OpAmp[2)]	V_{IO}	–	1	2	mV	R_S=500Ω; V_{CM}=0V; V_O=1.65V; V_{RI}=1.65V
5.3.11	Input Offset Voltage of the Reference Buffer	V_{IO}		1	+/-5	mV	–
5.3.12	Input Offset Voltage Temperature Drift of the Reference Buffer[2)]	V_{IO}		1	2	mV	–
5.3.13	Input Range at VRI	V_{IO}	1.2	–	2.8	V	–
5.3.14	Input Bias Current (ISx to GND)	I_{IB}	-300	–	–	µA	V_{CM}=0V; V_O=open
5.3.15	High Level Output Voltage of VO	V_{OH}	4.8	–	5.2	V	V_{RI}=1.65V/2.5V; I_{OH}=-3mA
5.3.16	Low Level Output Voltage of VO	V_{OL}	-0.1	–	0.2	V	V_{RI}=1.65V/2.5V; I_{OH}=3mA
5.3.17	Output Voltage of VO[3)] V_{RI}= 2.5V, V_{RI}=1.65V	V_{OR}	2.42 1.58	2.50 1.65	2.58 1.73	V	$V_{IN(SS)}$=0V; Gain=15;
5.3.18	Temperature Drift of Output Voltage of VO[3)]	V_O	0	–	32	mV	$V_{IN(SS)}$=0V; Gain=15
5.3.19	Guaranteed Output Current Capability	I_{GOC}	-5	–	5	mA	–
5.3.20	Differential Input Resistance[2)]	R_I	100	–	–	kΩ	–
5.3.21	Common Mode Input apacitance[2)]	C_{CM}	–	–	10	pF	10kHz

Electrical Characteristics - Current sense signal conditioning (cont'd)

V_S = 5.5 to 20V, T_j = -40 to +150°C, f_{PWM} < 25kHz, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.3.22	Common Mode Rejection Ratio at DC CMRR = 20*Log((Vout_diff/Vin_diff) * (Vin_CM/Vout_CM))	CMRR	80	100	–	db	–
5.3.23	Common Mode Suppression[4] with CMS = 20*Log(Vout_CM/Vin_CM) Freq =100kHz Freq = 1MHz Freq = 10MHz	*CMS*	–	 62 43 33	–	db	VIN=360mV* sin(2*π*freq*t); Rs=500Ω; Rfb=7500Ω; VRI=1.65/2.5V
5.3.24	Slew Rate	*dV/dt*	3	10	–	V/µs	Gain>= 5; R_L=1.0kΩ; C_L=500pF
5.3.25	Large Signal Open Loop Voltage Gain (DC)	A_{OL}	80	100	–	dB	–
5.3.26	Unity Gain Bandwidth	GBW	10	20	–	MHz	R_L=1kΩ; C_L=100pF
5.3.27	Phase Margin [2]	Φ_M	–	50	–	°	Gain>= 5; R_L=1kΩ; C_L=100pF
5.3.28	Gain Margin [2]	A_M	–	12	–	db	R_L=1kΩ; C_L=100pF
5.3.29	Bandwidth	BW_G	1.6	–	–	MHz	Gain=15; R_L=1kΩ; C_L=500pF; R_s=500Ω
5.3.30	Output Settle Time to 98% [1]	t_{set}	–	1	1.8	µs	Gain=15; R_L=1kΩ; C_L=500pF; 0.3<VO< 4.8V; R_s=500Ω
5.3.31	Output Rise Time 10% to 90% [1]	t_{lrise}	–	–	1	µs	Gain=15; R_L=1kΩ;C_L=500pF; 0.3<VO< 4.8V; R_s=500Ω
5.3.32	Output Fall Time 90% to 10%[1]	t_{lfall}	–	–	1	µs	Gain=15; R_L=1kΩ;C_L=500pF; 0.3<VO< 4.8V; R_s=500Ω;

1) Input current and output amplifier characteristics:
"Output signal must be amplified and available at 2µs after input signal change (Gain 5...15)

2) Not subject to production test; specified by design

3) calculated out of **5.3.9**, **5.3.10**, **5.3.11** and **5.3.12**

4) Without considering any offsets such as input offset voltage, internal mismatch and assuming no tolerance error in external resistors.

5.4 Phase Voltage Feedback

The TLE7183QU incorporates a fast conversion of the phase voltages to logic signals. The threshold values are proportional to V_{DH}. The outputs are 5V push pull stages. If they are not used they can be left open.

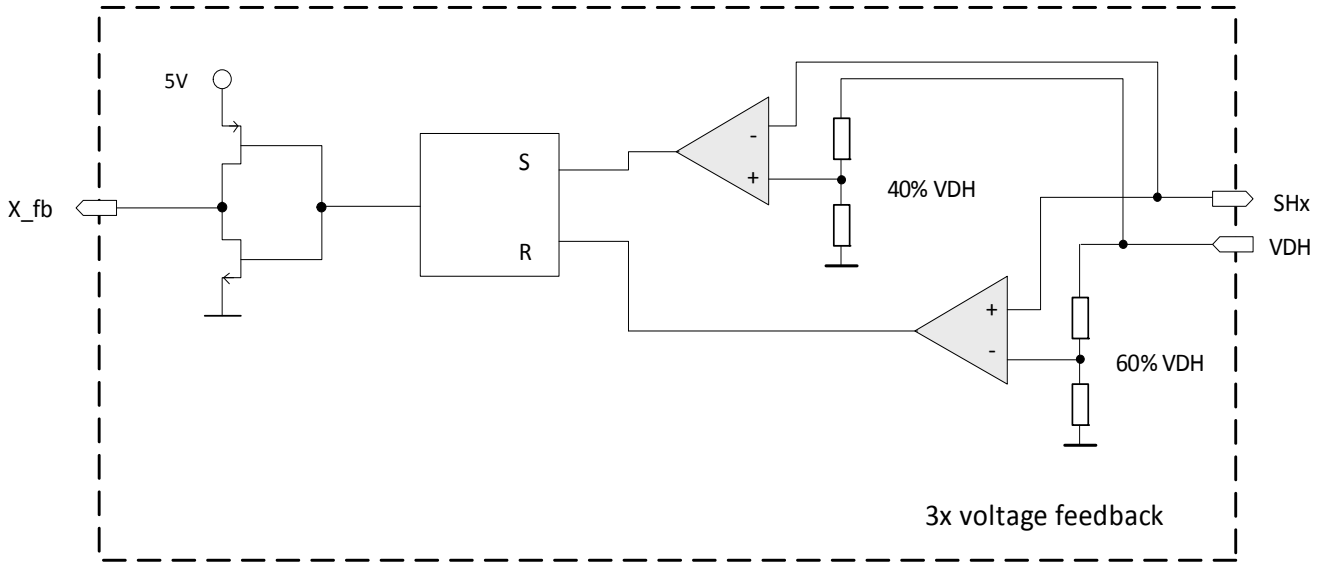


Figure 5 Block Diagram Phase Voltage Feedback

5.4.1 Electrical Characteristics

Electrical Characteristics - Phase Voltage Feedback

V_S = 5.5 to 20V, T_j = -40 to +150°C, f_{PWM} < 25kHz, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.4.1	Low Level Threshold	V_{ILfb}	35	40	45	% of VDH	VDH>5.5V V_{SHX} decreasing
5.4.2	High Level Threshold	V_{IHfb}	55	60	65	% of VDH	VDH>5.5V V_{SHX} decreasing
5.4.3	High Level Output Voltage of X_fb	V_{OHfb}	4.0	–	5.2	V	I= -0.5mA
5.4.4	Low Level Output Voltage of X_fb	V_{OLfb}	-0.1	–	0.2	V	I= 0.5mA
5.4.5	Propagation Delay Time incl. Rise or Fall Time	t_{PDfb}	–	–	110	ns	C_{LOAD}<100pF
5.4.6	Matching of Propagation Delay Time	t_{dPDfb}	–	–	30	ns	

6 Application Description

In the automotive sector there are more and more applications requiring high performance motor drives, such as electro-hydraulic or electric power steering. In these applications 3 phase motors, synchronous and asynchronous, are used, combining high output performance, low space requirements and high reliability.

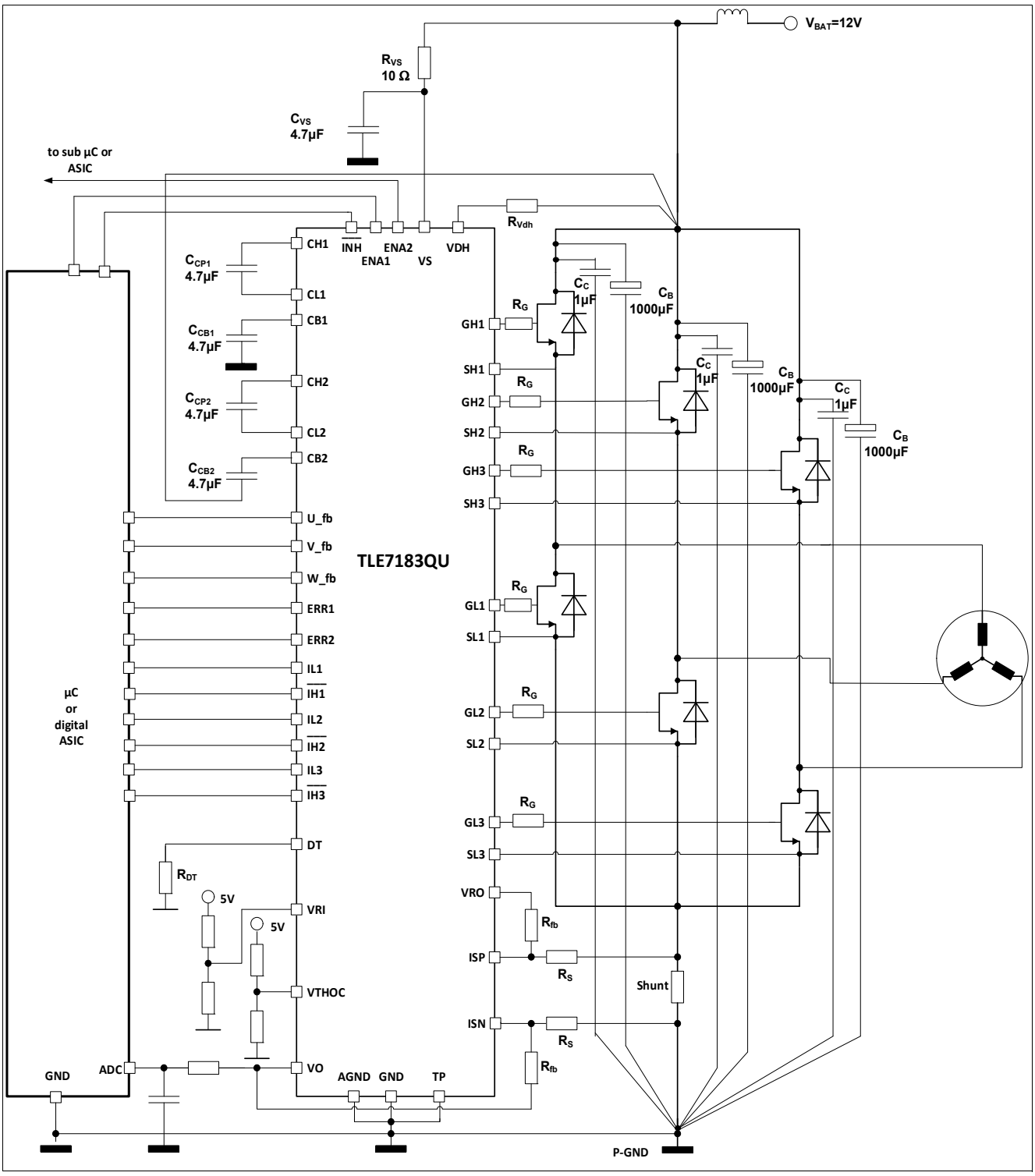


Figure 6 Application Circuit

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

6.1 Layout Guide Lines

Please refer also to the simplified application example.

- Three separate bulk capacitors C_B should be used - one per half bridge
- Three separate ceramic capacitors C_C should be used - one per half bridge
- Each of the 3 bulk capacitors C_B and each of the 3 ceramic capacitors C_C should be assigned to one of the half bridges and should be placed very close to it
- The components within one half bridge should be placed close to each other: high side MOSFET, low side MOSFET, bulk capacitor C_B and ceramic capacitor C_C (C_B and C_C are in parallel) and the shunt resistor form a loop that should be as small and tight as possible. The traces should be short and wide
- The three half bridges can be seperated but if there is one common GND referenced shunt resistor for the three half bridges the sources of the three low side MOSFETs should be close to each other and close to the common shunt resistor
- VDH is the sense pin used for short circuit detection; VDH should be routed (via Rvdh) to the common point of the drains of the high side MOSFETs to sense the voltage of the drain high side
- CB2 is the buffer capacitor of charge pump 2; its negative terminal should be routed to the common point of the drains of the high side MOSFETs as well - this connection should be low inductive / resistive
- Additional R-C snubber circuits (R and C in series) can be placed to attenuate/suppress oscillations during switching of the MOSFETs, there may be one or two snubber circuits per half bridge, R (several Ohm) and C (several nF) must be low inductive in terms of routing and packaging (ceramic capacitors)
- the exposed pad on the backside of the package should be connected to GND

6.2 Further Application Information

- For further information you may contact **http://www.infineon.com/**

7 Package Outlines

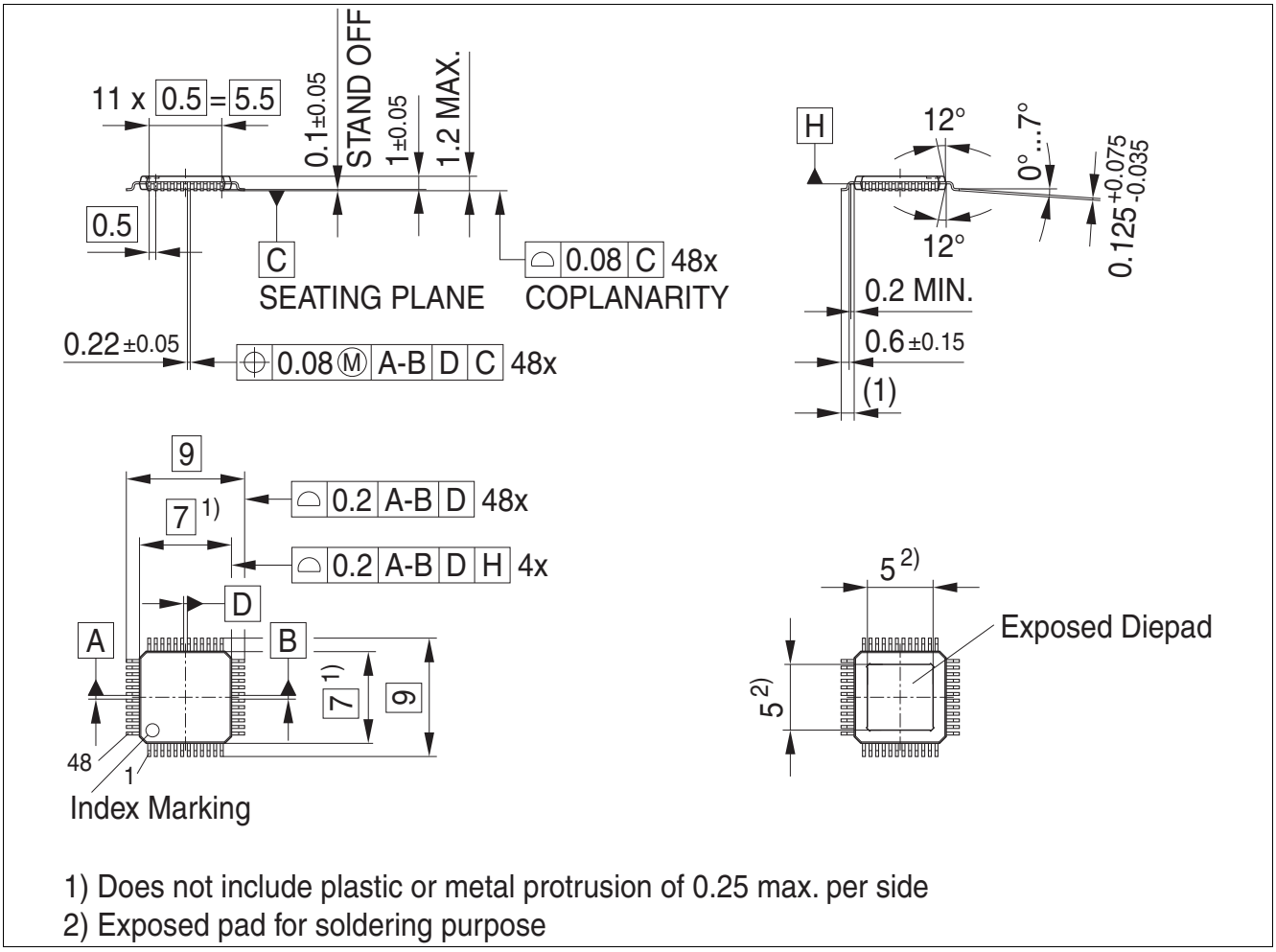


Figure 7 PG-TQFP-48

Green Product

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

Dimensions in mm

8 Revision History

Version	Date	Changes
1.1	2016-01-28	- package adjustments - replaced misleading term $\overline{\text{ERR}}$x with ERRx
1.0	2011-09-09	Data Sheet

Edition 2016-01-28

Published by
Infineon Technologies AG
81726 München, Germany

© Infineon Technologies AG 2016.
All Rights Reserved.

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics (“Beschaffenheitsgarantie”). With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.