

FEATURES

18-bit resolution with no missing codes

Throughput: 1 MSPS

Low power dissipation

4 mW at 1 MSPS (VDD only)

7 mW at 1 MSPS (total)

70 μ W at 10 kSPS

INL: ± 1 LSB typical, ± 2 LSB maximum

Dynamic range: 99 dB typical

True differential analog input range: $\pm V_{REF}$

0 V to V_{REF} with V_{REF} between 2.5 V to 5.0 V

Allows use of any input range

Easy to drive with the ADA4941-1 or ADA4940-1

No pipeline delay

Single-supply 2.5 V operation with 1.8 V, 2.5 V, 3 V, and 5 V logic interface

Proprietary serial interface SPI-/QSPI™/ MICROWIRE™-/DSP-compatible¹

Ability to daisy-chain multiple ADCs and busy indicator
10-Lead MSOP and 3 mm $\times$ 3 mm 10-Lead LFCSP

APPLICATIONS

Battery-powered equipment

Data acquisition systems

Medical instruments

Seismic data acquisition systems

FUNCTIONAL BLOCK DIAGRAM

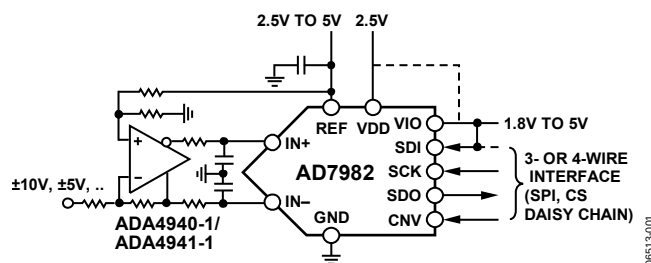


Figure 1.

GENERAL DESCRIPTION

The AD7982 is an 18-bit, successive approximation, analog-to-digital converter (ADC) that operates from a single power supply, VDD. The AD7982 contains a low power, high speed, 18-bit sampling ADC and a versatile serial interface port. On the CNV rising edge, the AD7982 samples the voltage difference between the IN+ and IN- pins. The voltages on these pins usually swing in opposite phases between 0 V and V_{REF} . The reference voltage, V_{REF} , is applied externally and can be set independent of the supply voltage, VDD. Its power scales linearly with throughput.

The serial peripheral interface (SPI)-compatible serial interface also features the ability, using the SDI input, to daisy-chain several ADCs on a single 3-wire bus and provides an optional busy indicator. The AD7982 is compatible with 1.8 V, 2.5 V, 3 V, and 5 V logic, using the separate VIO supply.

The AD7982 is available in a 10-lead MSOP or a 10-lead LFCSP with operation specified from -40°C to $+85^{\circ}\text{C}$.

Table 1. MSOP and LFCSP 14-/16-/18-Bit PulSAR® ADCs

Bits	100 kSPS	250 kSPS	400 kSPS to 500 kSPS	≥ 1000 kSPS
18 ¹	AD7989-1	AD7691	AD7690 AD7989-5	AD7982 AD7984
16 ¹	AD7684	AD7687	AD7688 AD7693 AD7916	AD7915
16 ²	AD7680 AD7683 AD7988-1	AD7685 AD7694	AD7686 AD7988-5	AD7980 AD7983
14 ²	AD7940	AD7942	AD7946	

¹ True differential.

² Pseudo differential.

¹ Protected by U.S. Patent 6,703,961.

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REVISION HISTORY

1/2017—Rev. C to Rev. D

Deleted QFN	Throughout
Changes to Features Section, Figure 1, and Table 1	1
Changed to VIO = 2.3 V to 5.5 V to VIO = 1.71 V to 5.5 V	3
Changes to Table 2	3
Deleted VIO Range Parameter, Table 3	4
Changed to VIO = 2.3 V to 5.5 V to VIO = 1.71 V to 5.5 V	4
Changes to VIO Parameter, Table 3	4
Changes to Table 4	5
Added Table 5; Renumbered Sequentially	6
Changes to Figure 5 and Table 7	8
Moved Typical Performance Characteristics Section	9
Changes to Figure 9	9
Changes to Figure 23	14
Changes to Analog Inputs Section and Table 9	15
Change to Single-Ended to Differential Driver Section Title	16
Changes to Power Supply Section	16
Changes to Figure 30	18
Changes to Figure 32	19
Changes to Figure 34	20
Changes to Figure 36	21
Changes to Chain Mode with Busy Indicator	23
Changes to Applications Information Section	24
Changes to Ordering Guide	25

6/2014—Rev. B to Rev. C

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Added Patent Footnote	1
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7/2013—Rev. A to Rev. B

Added Low Power Dissipation of 4 mW at 1 MSPS (VDD only) to Features Section	1
Changes to Power Dissipation; Table 3	4
Added EPAD Notation to Figure 5 and Table 6	7
Updated Outline Dimensions	24
Changes to Ordering Guide	24

10/2007—Rev. 0 to Rev. A

Changes to Table 1 and Layout	1
Changes to Table 2	3
Changes to Layout	5
Changes to Layout	6
Changes to Figure 5	7
Changes to Figure 18 and Figure 20	11
Changes to Figure 23	13
Changes to Figure 26	15
Changes to Digital Interface Section	16
Changes to Figure 38	21
Changes to Figure 40	22
Updated Outline Dimensions	24
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3/2007—Revision 0: Initial Version

SPECIFICATIONS

VDD = 2.5 V, VIO = 1.71 V to 5.5 V, VREF = 5 V, TA = -40°C to +85°C, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		18			Bits
ANALOG INPUT					
Voltage Range	IN+ – IN–	–VREF		+VREF	V
Absolute Input Voltage	IN+ and IN–	–0.1		VREF + 0.1	V
Common-Mode Input Range	IN+ and IN–	VREF × 0.475	VREF × 0.5	VREF × 0.525	V
Analog Input Common Mode Rejection Ratio (CMRR)	fIN = 450 kHz		67		dB
Leakage Current at 25°C	Acquisition phase		200		nA
Input Impedance			See the Analog Inputs section		
ACCURACY					
No Missing Codes		18			Bits
Differential Linearity Error (DNL)		–0.85	±0.5	+1.5	LSB ¹
Integral Linearity Error (INL)		–2	±1	+2	LSB ¹
Transition Noise	VREF = 5 V		1.05		LSB ¹
Gain Error, TMIN to TMAX ²		–0.023	+0.004	+0.023	% of FS
Gain Error Temperature Drift			±1		ppm/°C
Zero Error, TMIN to TMAX ²			±100	+700	μV
Zero Temperature Drift			0.5		ppm/°C
Power Supply Rejection Ratio (PSRR)	VDD = 2.5 V ± 5%		90		dB
THROUGHPUT					
Conversion Rate	VIO ≥ 2.3 V	0		1	MSPS
	VIO ≥ 1.71 V	0		800	kSPS
Transient Response	Full-scale step			290	ns
AC ACCURACY					
Dynamic Range	VREF = 5 V	97	99		dB ³
	VREF = 2.5 V		93		dB ³
Oversampled Dynamic Range ⁴	FO = 1 kSPS		129		dB ³
Signal-to-Noise Ratio (SNR)	fIN = 1 kHz, VREF = 5 V	95.5	98		dB ³
	fIN = 1 kHz, VREF = 2.5 V		92.5		dB ³
Spurious-Free Dynamic Range (SFDR)	fIN = 10 kHz		–115		dB ³
Total Harmonic Distortion ⁵ (THD)	fIN = 10 kHz		–120		dB ³
Signal-to-Noise-and-Distortion (SINAD)	fIN = 1 kHz, VREF = 5 V		97		dB ³

¹ LSB means least significant bit. With the ±5 V input range, 1 LSB is 38.15 μV.

² See Terminology section. These specifications include full temperature range variation but not the error contribution from the external reference.

³ All specifications expressed in decibels are referred to a full-scale input range (FSR) and tested with an input signal at 0.5 dB below full scale, unless otherwise specified.

⁴ Dynamic range is obtained by oversampling the ADC running at a throughput FS of 1 MSPS followed by postdigital filtering with an output word rate of FO.

⁵ Tested fully in production at fIN = 1 kHz.

VDD = 2.5 V, VIO = 1.71 V to 5.5 V, VREF = 5 V, TA = –40°C to +85°C, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
REFERENCE					
Voltage Range		2.4		5.1	V
Load Current	1 MSPS, VREF = 5 V		350		μA
SAMPLING DYNAMICS					
–3 dB Input Bandwidth			10		MHz
Aperture Delay	VDD = 2.5 V		2		ns
DIGITAL INPUTS					
Logic Levels					
VIL	VIO > 3 V	–0.3		+0.3 × VIO	V
VIH	VIO > 3 V	0.7 × VIO		VIO + 0.3	V
VIL	VIO ≤ 3 V	–0.3		+0.1 × VIO	V
VIH	VIO ≤ 3 V	0.9 × VIO		VIO + 0.3	V
IIL		–1		+1	μA
IiH		–1		+1	μA
DIGITAL OUTPUTS					
Data Format		Serial 18 bits, twos complement			
Pipeline Delay		Conversion results available immediately after completed conversion			
VOL	ISINK = +500 μA			0.4	V
VOH	ISOURCE = –500 μA	VIO – 0.3			V
POWER SUPPLIES					
VDD		2.375	2.5	2.625	V
VIO		1.71		5.5	V
Standby Current ^{1,2}	VDD and VIO = 2.5 V, 25°C		0.35		μA
Power Dissipation	VDD = 2.625 V, VREF = 5 V, VIO = 3 V				
Total	10 kSPS throughput		70	86	μW
	1 MSPS throughput		7	8.6	mW
VDD Only			4		mW
REF Only			1.7		mW
VIO Only			1.3		mW
Energy per Conversion			7.0		nJ/sample
TEMPERATURE RANGE ³					
Specified Performance	TMIN to TMAX	–40		+85	°C

¹ With all digital inputs forced to VIO or GND as required.

² During acquisition phase.

³ Contact an Analog Devices, Inc., sales representative for the extended temperature range.

TIMING SPECIFICATIONS

VDD = 2.37 V to 2.63 V, VIO = 2.3 V to 5.5 V, T_A = -40°C to +85°C, unless otherwise noted.¹

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit
CONVERSION AND ACQUISITION TIMES					
Conversion Time: CNV Rising Edge to Data Available	t _{CONV}	500		710	ns
Acquisition Time	t _{ACQ}	290			ns
Time Between Conversions	t _{CYC}	1000			ns
CNV PULSE WIDTH (CS MODE)	t _{CNVH}	10			ns
SCK					
SCK Period (CS Mode)	t _{SCK}				
VIO Above 4.5 V		10.5			ns
VIO Above 3 V		12			ns
VIO Above 2.7 V		13			ns
VIO Above 2.3 V		15			ns
SCK Period (Chain Mode)	t _{SCK}				
VIO Above 4.5 V		11.5			ns
VIO Above 3 V		13			ns
VIO Above 2.7 V		14			ns
VIO Above 2.3 V		16			ns
SCK Low Time	t _{SCKL}	4.5			ns
SCK High Time	t _{SCKH}	4.5			ns
SCK Falling Edge to Data Remains Valid	t _{HSDO}	3			ns
SCK Falling Edge to Data Valid Delay	t _{DSO}				
VIO Above 4.5 V				9.5	ns
VIO Above 3 V				11	ns
VIO Above 2.7 V				12	ns
VIO Above 2.3 V				14	ns
CS MODE					
CNV or SDI Low to SDO D17 MSB Valid	t _{EN}				
VIO Above 3 V				10	ns
VIO Above 2.3 V				15	ns
CNV or SDI High or Last SCK Falling Edge to SDO High Impedance	t _{DIS}			20	ns
SDI Valid Setup Time from CNV Rising Edge	t _{SSDICNV}	5			ns
SDI Valid Hold Time from CNV Rising Edge	t _{HSDICNV}	2			ns
CHAIN MODE					
SDI Valid Hold Time from CNV Rising Edge	t _{HSDICNV}	0			ns
SCK Valid Setup Time from CNV Rising Edge	t _{SSCKCNV}	5			ns
SCK Valid Hold Time from CNV Rising Edge	t _{HSCKCNV}	5			ns
SDI Valid Setup Time from SCK Falling Edge	t _{SSDISCK}	2			ns
SDI Valid Hold Time from SCK Falling Edge	t _{HSDISCK}	3			ns
SDI High to SDO High (Chain Mode with Busy Indicator)	t _{DSDOSDI}			15	ns

¹ See Figure 2 and Figure 3 for load conditions.

VDD = 2.37 V to 2.63 V, VIO = 1.71 V to 2.3 V, -40°C to $+85^{\circ}\text{C}$, unless otherwise stated.¹

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit
THROUGHPUT RATE				800	kSPS
CONVERSION AND ACQUISITION TIMES					
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}	500		800	ns
Acquisition Time	t_{ACQ}	290			ns
Time Between Conversions	t_{CYC}	1.25			μs
CNV PULSE WIDTH ($\overline{\text{CS}}$ MODE)	t_{CNVH}	10			ns
SCK					
SCK Period ($\overline{\text{CS}}$ Mode)	t_{SCK}	22			ns
SCK Period (Chain Mode)	t_{SCK}	23			ns
SCK Low Time	t_{SCKL}	6			ns
SCK High Time	t_{SCKH}	6			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	3			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}		14	21	ns
$\overline{\text{CS}}$ MODE					
CNV or SDI Low to SDO D17 MSB Valid	t_{EN}		18	40	ns
CNV or SDI High or Last SCK Falling Edge to SDO High Impedance	t_{DIS}			20	ns
SDI Valid Setup Time from CNV Rising Edge	t_{SSDICNV}	5			ns
SDI Valid Hold Time from CNV Rising Edge	t_{HSDICNV}	10			ns
CHAIN MODE					
SDI Valid Hold Time from CNV Rising Edge	t_{HSDICNV}	0			ns
SCK Valid Setup Time from CNV Rising Edge	t_{SSCKCNV}	5			ns
SCK Valid Hold Time from CNV Rising Edge	t_{HSCKCNV}	5			ns
SDI Valid Setup Time from SCK Falling Edge	t_{SSDISCK}	2			ns
SDI Valid Hold Time from SCK Falling Edge	t_{HSDISCK}	3			ns
SDI High to SDO High (Chain Mode with Busy Indicator)	t_{DSDOSDI}			22	ns

¹ See Figure 2 and Figure 3 for load conditions.

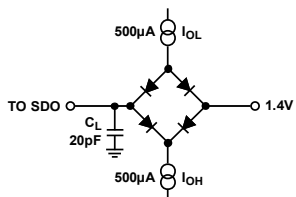
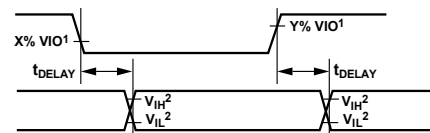


Figure 2. Load Circuit for Digital Interface Timing



¹FOR VIO ≤ 3.0V, X = 90, AND Y = 10; FOR VIO > 3.0V, X = 70, AND Y = 30.

²MINIMUM VIH AND MAXIMUM VIL USED. SEE DIGITAL INPUTS SPECIFICATIONS IN TABLE 3.

Figure 3. Voltage Levels for Timing

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Analog Inputs IN+, IN– to GND ¹	–0.3 V to $V_{REF} + 0.3$ V or ± 130 mA
Supply Voltage REF, VIO to GND	–0.3 V to +6.0 V
VDD to GND	–0.3 V to +3.0 V
VDD to VIO	+3 V to –6 V
Digital Inputs to GND	–0.3 V to VIO + 0.3 V
Digital Outputs to GND	–0.3 V to VIO + 0.3 V
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	
10-Lead MSOP	200°C/W
10-Lead LFCSP	48.7°C/W
θ_{JC} Thermal Impedance	
10-Lead MSOP	44°C/W
10-Lead LFCSP	2.96°C/W
Lead Temperatures	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

¹ See the Analog Inputs section for an explanation of IN+ and IN–.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

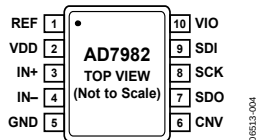
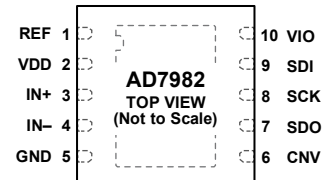


Figure 4. 10-Lead MSOP Pin Configuration



NOTES
 1. EXPOSED PAD. FOR THE LEAD FRAME CHIP SCALE PACKAGE (LFCSP), THE EXPOSED PAD MUST BE CONNECTED TO GND. THIS CONNECTION IS NOT REQUIRED TO MEET THE ELECTRICAL PERFORMANCES.

Figure 5. 10-Lead LFCSP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type ¹	Description
1	REF	AI	Reference Input Voltage. The REF range is 2.4 V to 5.1 V. This pin is referred to the GND pin and must be decoupled closely to the GND pin with a 10 μ F capacitor.
2	VDD	P	Power Supply.
3	IN+	AI	Differential Positive Analog Input.
4	IN–	AI	Differential Negative Analog Input.
5	GND	P	Power Supply Ground.
6	CNV	DI	Convert Input. This input has multiple functions. On its leading edge, it initiates the conversions and selects the interface mode of the device: chain mode or $\overline{CS}$ mode. In $\overline{CS}$ mode, the SDO pin is enabled when CNV is low. In chain mode, the data must be read when CNV is high.
7	SDO	DO	Serial Data Output. The conversion result is output on this pin. It is synchronized to SCK.
8	SCK	DI	Serial Data Clock Input. When the device is selected, the conversion result is shifted out by this clock.
9	SDI	DI	Serial Data Input. This input provides multiple features. It selects the interface mode of the ADC as follows: Chain mode is selected if SDI is low during the CNV rising edge. In this mode, SDI is a data input that daisy-chains the conversion results of two or more ADCs onto a single SDO line. The digital data level on SDI is the output on SDO with a delay of 18 SCK cycles. $\overline{CS}$ mode is selected if SDI is high during the CNV rising edge. In this mode, either SDI or CNV can enable the serial output signals when low. If SDI or CNV is low when the conversion is complete, the busy indicator feature is enabled.
10	VIO EPAD	P	Input/Output Interface Digital Power. Nominally at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V). Exposed Pad. For the lead frame chip scale package (LFCSP), the exposed pad must be connected to GND. This connection is not required to meet the electrical performances.

¹AI means analog input, DI means digital input, DO means digital output, and P means power.

TYPICAL PERFORMANCE CHARACTERISTICS

VDD = 2.5 V, V_{REF} = 5.0 V, VIO = 3.3 V.

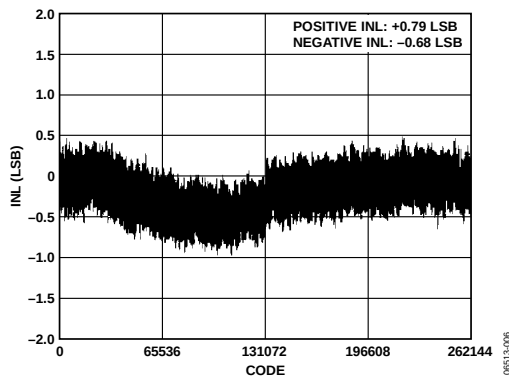


Figure 6. INL vs. Code

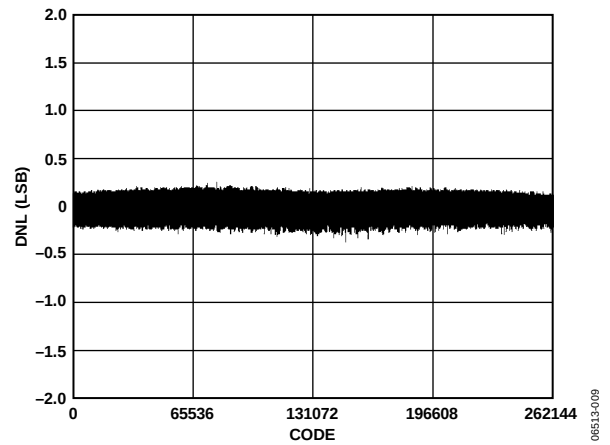


Figure 9. DNL vs. Code

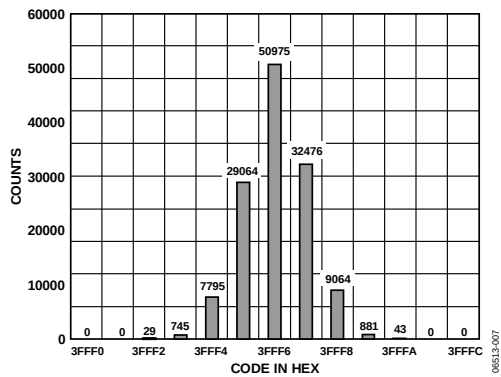


Figure 7. Histogram of a DC Input at the Code Center

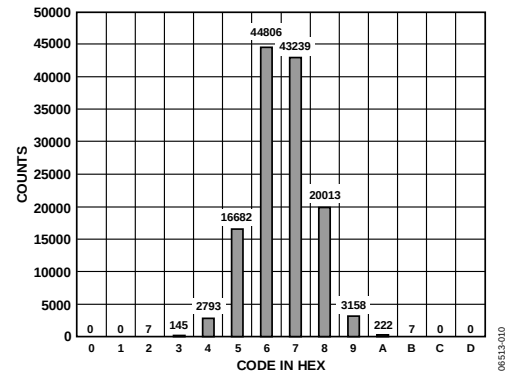


Figure 10. Histogram of a DC Input at the Code Transition

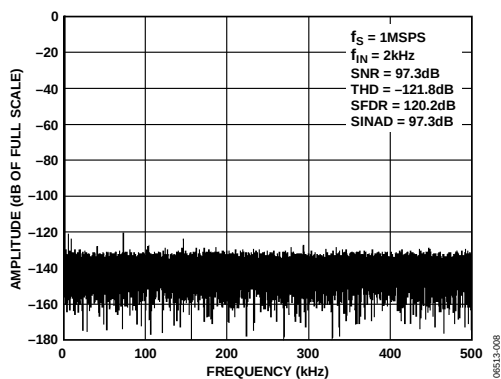


Figure 8. Fast Fourier Transform (FFT) Plot

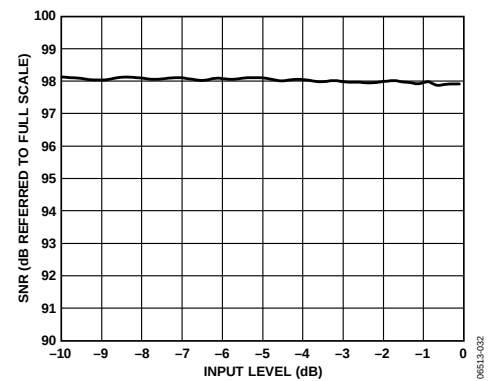


Figure 11. SNR vs. Input Level

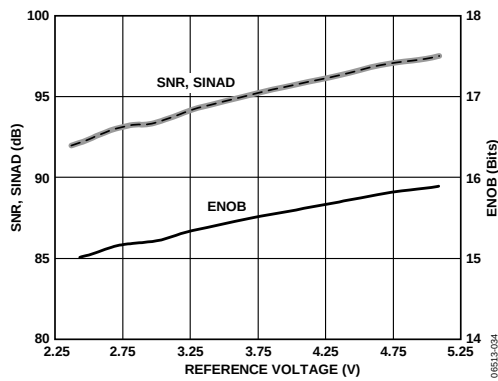


Figure 12. SNR, SINAD, and ENOB vs. Reference Voltage

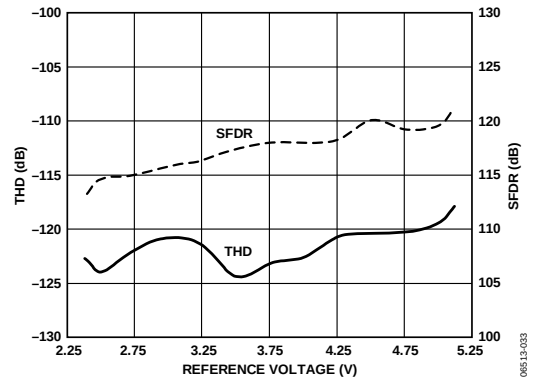


Figure 15. THD and SFDR vs. Reference Voltage

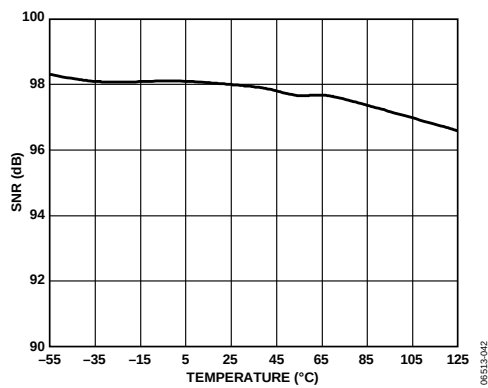


Figure 13. SNR vs. Temperature

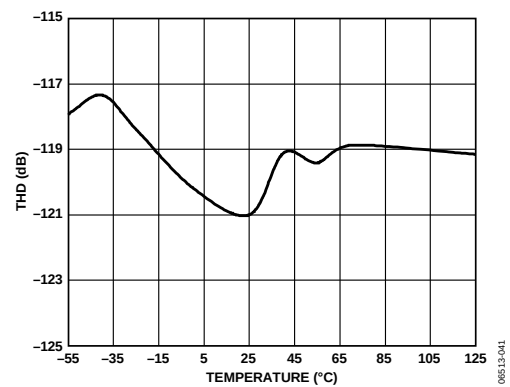


Figure 16. THD vs. Temperature

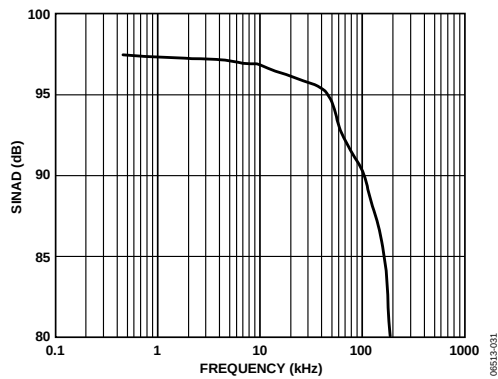


Figure 14. SINAD vs. Frequency

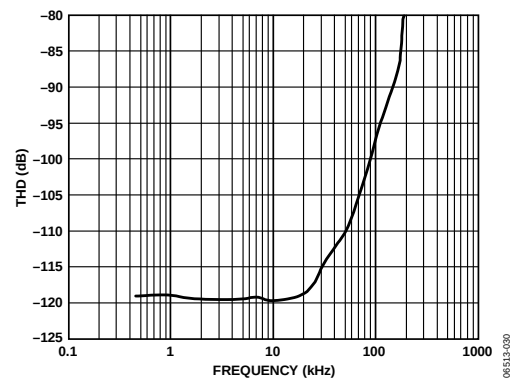


Figure 17. THD vs. Frequency

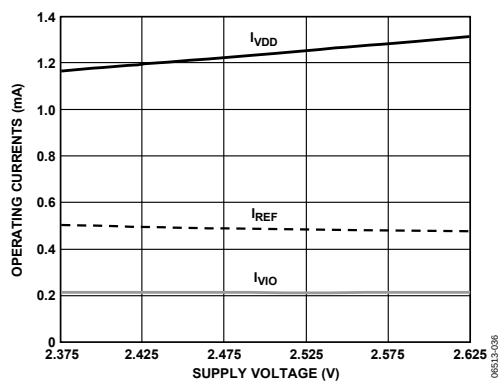


Figure 18. Operating Currents vs. Supply Voltage

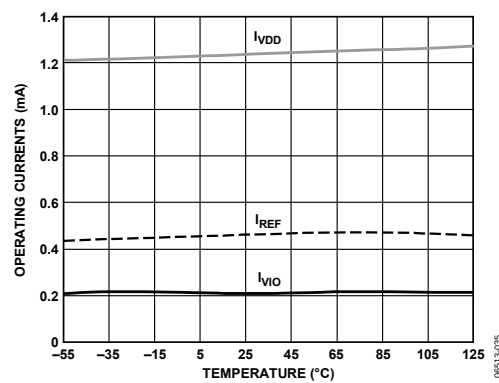


Figure 20. Operating Currents vs. Temperature

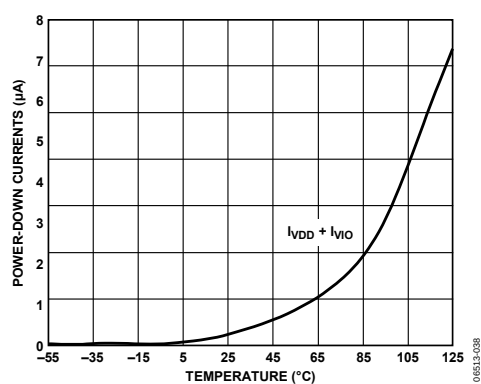


Figure 19. Power-Down Currents vs. Temperature

TERMINOLOGY

Integral Nonlinearity Error (INL)

INL refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs $\frac{1}{2}$ LSB before the first code transition. Positive full scale is defined as a level $1\frac{1}{2}$ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line (see Figure 22).

Differential Nonlinearity Error (DNL)

In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Zero Error

Zero error is the difference between the ideal midscale voltage, that is, 0 V, from the actual voltage producing the midscale output code, that is, 0 LSB.

Gain Error

The first code transition (from 100 ... 00 to 100 ... 01) must occur at a level $\frac{1}{2}$ LSB above nominal negative full scale (-4.999981 V for the ± 5 V range). The last transition (from 011 ... 10 to 011 ... 11) must occur for an analog voltage $1\frac{1}{2}$ LSB below the nominal full scale ($+4.999943$ V for the ± 5 V range). The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in decibels, between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)

ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD as follows:

$$ENOB = (SINAD_{dB} - 1.76)/6.02$$

and is expressed in bits.

Noise Free Code Resolution

Noise free code resolution is the number of bits beyond which it is impossible to distinctly resolve individual codes. It is calculated as

$$Noise\ Free\ Code\ Resolution = \log_2(2^N/Peak\text{-}to\text{-}Peak\ Noise)$$

and is expressed in bits.

Effective Resolution

Effective resolution is calculated as

$$Effective\ Resolution = \log_2(2^N/RMS\ Input\ Noise)$$

and is expressed in bits.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Dynamic Range

Dynamic range is the ratio of the rms value of the full scale to the total rms noise measured with the inputs shorted together. The value for dynamic range is expressed in decibels. It is measured with a signal at -60 dB so it includes all noise sources and DNL artifacts.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-Noise-and-Distortion Ratio (SINAD)

SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components that are less than the Nyquist frequency, including harmonics but excluding dc. The value of SINAD is expressed in decibels.

Aperture Delay

Aperture delay is the measure of the acquisition performance and is the time between the rising edge of the CNV input and when the input signal is held for a conversion.

Transient Response

Transient response is the time required for the ADC to accurately acquire its input after a full-scale step function is applied.

THEORY OF OPERATION

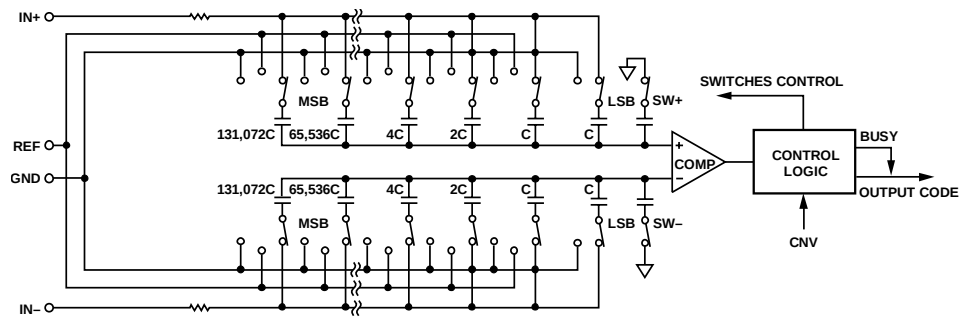


Figure 21. ADC Simplified Schematic

CIRCUIT INFORMATION

The [AD7982](#) is a fast, low power, single-supply, precise 18-bit ADC using a successive approximation architecture.

The [AD7982](#) is capable of converting 1,000,000 samples per second (1 MSPS) and powers down between conversions. When operating at 10 kSPS, for example, it typically consumes 70 μ W, making it ideal for battery-powered applications.

The [AD7982](#) provides the user with an on-chip track-and-hold and does not exhibit any pipeline delay or latency, making it ideal for multiple multiplexed channel applications.

The [AD7982](#) can interface to any 1.8 V to 5 V digital logic family. It is available in a 10-lead MSOP or a tiny 10-lead LFCSP that allows space savings and flexible configurations.

It is pin for pin compatible with the 16-bit [AD7980](#).

CONVERTER OPERATION

The [AD7982](#) is a successive approximation ADC based on a charge redistribution DAC. Figure 21 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 18 binary weighted capacitors, which are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the input of the comparator are connected to GND via Switch SW+ and Switch SW-. All independent switches are connected to the analog inputs. Therefore, the capacitor arrays are used as sampling capacitors and acquire the analog signal on the IN+ input and the IN- input. When the acquisition phase completes and the CNV input goes high, a conversion phase initiates. When the conversion phase begins, SW+ and SW- open first. The two capacitor arrays then disconnect from the inputs and connect to the GND input. Therefore, the differential voltage between the IN+ and IN- inputs captured at the end of the acquisition phase applies to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between GND and REF, the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4 \dots V_{REF}/262,144$). The control logic toggles these switches, starting with the MSB, to bring the comparator back into a balanced condition. After the completion of the conversion phase process, the device returns to the acquisition phase and the control logic generates the ADC output code and a busy signal indicator.

Because the [AD7982](#) has an on-board conversion clock, the serial clock, SCK, is not required for the conversion process.

Transfer Functions

The ideal transfer characteristic for the AD7982 is shown in Figure 22 and Table 8.

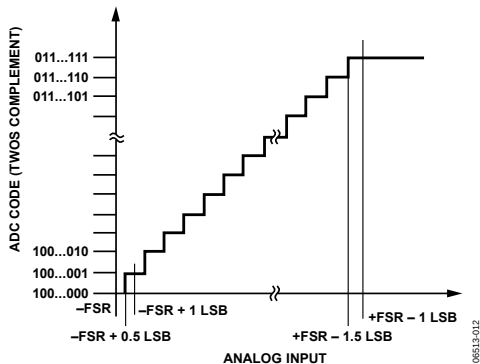


Figure 22. ADC Ideal Transfer Function Characteristic

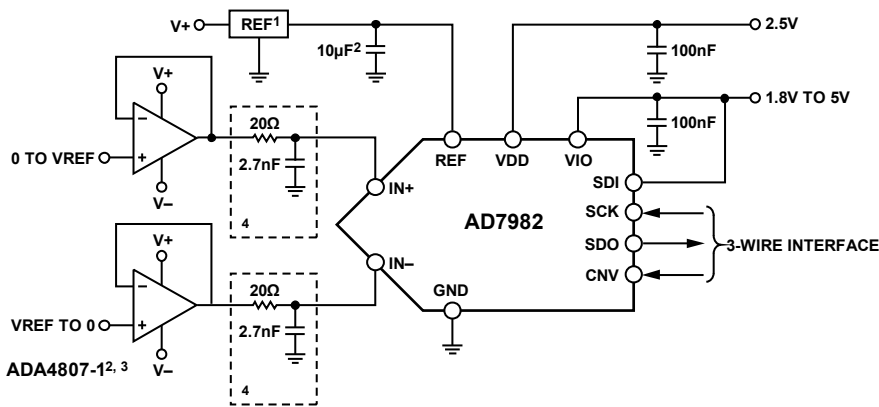
Table 8. Output Codes and Ideal Input Voltages

Description	Analog Input $V_{REF} = 5\text{ V}$	Digital Output Code (Hex)
FSR – 1 LSB	+4.999962 V	0x1FFFF ¹
Midscale + 1 LSB	+38.15 μV	0x00001
Midscale	0 V	0x00000
Midscale – 1 LSB	–38.15 μV	0x3FFFF
–FSR + 1 LSB	–4.999962 V	0x20001
–FSR	–5 V	0x20000 ²

¹ This is also the code for an overranged analog input ($V_{IN+} - V_{IN-}$ above $V_{REF} - V_{GND}$).
² This is also the code for an underranged analog input ($V_{IN+} - V_{IN-}$ below V_{GND}).

TYPICAL CONNECTION DIAGRAM

Figure 23 shows an example of the recommended connection diagram for the AD7982 when multiple supplies are available.



- NOTES
- ¹SEE VOLTAGE REFERENCE INPUT SECTION FOR REFERENCE SELECTION.
 - ²C_{REF} IS USUALLY A 10µF CERAMIC CAPACITOR (X5R).
 - SEE RECOMMENDED LAYOUT FIGURE 41 AND FIGURE 42.
 - ³SEE DRIVER AMPLIFIER CHOICE SECTION.
 - ⁴OPTIONAL FILTER. SEE ANALOG INPUT SECTION.

Figure 23. Typical Application Diagram with Multiple Supplies

ANALOG INPUTS

Figure 24 shows an equivalent circuit of the input structure of the AD7982.

The two diodes, D1 and D2, provide electrostatic discharge (ESD) protection for the IN+ analog input and the IN− analog input. Take care to ensure the analog input signal does not exceed the reference input voltage (REF) by more than 0.3 V. If the analog input signal exceeds the 0.3 V level, the diodes become forward-biased and begin conducting current. These diodes can handle a forward-biased current of 130 mA maximum. However, if the supplies of the input buffer (for example, the supplies of the ADA4807-1 in Figure 23) are different from those of the REF, the analog input signal can eventually exceed the supply rails by more than 0.3 V. In such a case (for example, an input buffer with a short-circuit), the current limitation can protect the device.

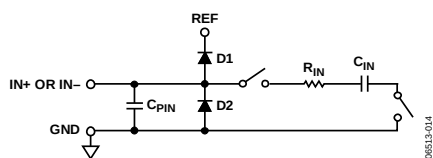


Figure 24. Equivalent Analog Input Circuit

The analog input structure allows the sampling of the true differential signal between IN+ and IN−. By using these differential inputs, signals common to both inputs are rejected.

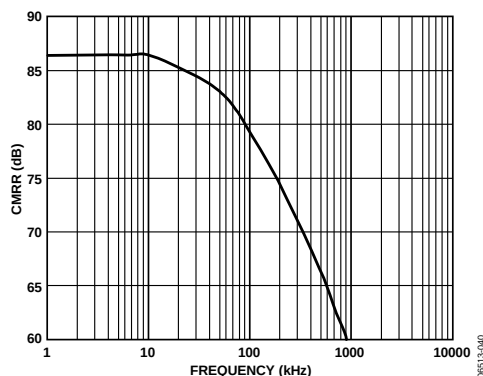


Figure 25. Analog Input CMRR vs. Frequency

During the acquisition phase, the impedance of the analog inputs (IN+ or IN−) can be modeled as a parallel combination of Capacitor C_{PIN} and the network formed by the series connection of R_{IN} and C_{IN} . C_{PIN} is primarily the pin capacitance. R_{IN} is typically 400 Ω and is a lumped component composed of serial resistors and the on resistance of the switches. C_{IN} is typically 30 pF and is mainly the ADC sampling capacitor.

During the sampling phase where the switches are closed, the input impedance is limited to C_{PIN} . R_{IN} and C_{IN} make a 1-pole, low-pass filter that reduces undesirable aliasing effects and limits noise.

When the source impedance of the driving circuit is low, the AD7982 can be driven directly. Large source impedances significantly affect the ac performance, especially THD. The dc performances are less sensitive to the input impedance. The maximum source impedance depends on the amount of THD that can be tolerated. The THD degrades as a function of the source impedance and the maximum input frequency.

DRIVER AMPLIFIER CHOICE

Although the AD7982 is easy to drive, the driver amplifier must meet the following requirements:

- The noise generated by the driver amplifier must be kept as low as possible to preserve the SNR and transition noise performance of the AD7982. The noise from the driver is filtered by the analog input circuit of the AD7982 1-pole, low-pass filter made by R_{IN} and C_{IN} , or by the external filter, if one is used. Because the typical noise of the AD7982 is 40 $\mu\text{V rms}$, the SNR degradation due to the amplifier is

$$\text{SNR}_{\text{LOSS}} = 20 \log \left(\frac{40}{\sqrt{40^2 + \frac{\pi}{2} f_{-3\text{dB}} (Ne_N)^2}} \right)$$

where:

$f_{-3\text{dB}}$ is the input bandwidth, in megahertz, of the AD7982 (10 MHz) or the cutoff frequency of the input filter, if one is used.

N is the noise gain of the amplifier (for example, 1 in buffer configuration).

e_N is the equivalent input noise voltage of the op amp in $\text{nV}/\sqrt{\text{Hz}}$.

- For ac applications, the driver must have a THD performance commensurate with the AD7982.
- For multichannel, multiplexed applications, the driver amplifier and the AD7982 analog input circuit must settle for a full-scale step onto the capacitor array at an 18-bit level (0.0004%, 4 ppm). In the data sheet of the amplifier, settling at 0.1% to 0.01% is more typically specified. Settling time can differ significantly from the settling time at an 18-bit level and must be verified prior to driver selection.

Table 9. Recommended Driver Amplifiers

Amplifier	Typical Application
ADA4941-1	Very low noise, low power, single to differential
ADA4940-1	Very low noise, low power, single to differential
ADA4807-2	Very low noise and low power
ADA4627-1	Precision, low noise and low input bias
ADA4522-2	Precision, zero drift, and electromagnetic interference (EMI) enhanced
ADA4500-2	Precision, rail-to-rail input and output (RRIO), and zero input crossover distortion

POWER SUPPLY

The AD7982 uses two power supply pins: a core supply (VDD) and a digital input/output interface supply (VIO). VIO allows direct interface with any logic between 1.8 V and 5.5 V. To reduce the number of supplies needed, tie VIO and VDD together. The AD7982 is independent of power supply sequencing between VIO and VDD. Additionally, it is very insensitive to power supply variations over a wide frequency range, as shown in Figure 27.

Frequency (kHz)	PSRR (dB)
1	90
10	90
100	75
1000	60

06513-039

6513-015

Figure 10 is a log-log plot showing the relationship between Operating Currents (mA) and Sampling Rate (SPS) for the AD7714. The y-axis represents Operating Currents (mA) on a logarithmic scale from 0.001 to 10.000. The x-axis represents Sampling Rate (SPS) on a logarithmic scale from 10,000 to 1,000,000. Three curves are plotted: I_{VDD} (solid line), I_{REF} (dashed line), and I_{VIO} (solid line). All three currents increase with increasing sampling rate.

Sampling Rate (SPS)	I_{VDD} (mA)	I_{REF} (mA)	I_{VIO} (mA)
10,000	~0.015	~0.005	~0.002
100,000	~0.10	~0.04	~0.015
1,000,000	~1.0	~0.4	~0.15

06513-037

Regardless, there is no need for an additional lower value ceramic decoupling capacitor (for example, 100 nF) between the REF and GND pins.

DIGITAL INTERFACE

Although the AD7982 has a reduced number of pins, it offers flexibility in its serial interface modes.

When in $\overline{\text{CS}}$ mode, the AD7982 is compatible with SPI, QSPI, digital hosts, and digital signal processors (DSPs). In $\overline{\text{CS}}$ mode, the AD7982 can use either a 3-wire or 4-wire interface. A 3-wire interface using the CNV, SCK, and SDO signals minimizes wiring connections useful, for instance, in isolated applications. A 4-wire interface using the SDI, CNV, SCK, and SDO signals allows CNV, which initiates the conversions, to be independent of the readback timing (SDI). The 4-wire interface is useful in low jitter sampling or simultaneous sampling applications.

When in chain mode, the AD7982 provides a daisy-chain feature using the SDI input for cascading multiple ADCs on a single data line similar to a shift register.

The mode in which the device operates depends on the SDI level when the CNV rising edge occurs. The $\overline{\text{CS}}$ mode is selected if SDI is high, and the chain mode is selected if SDI is low. The SDI hold time is such that when SDI and CNV are connected together, the chain mode is always selected.

In either mode, the AD7982 offers the option of forcing a start bit in front of the data bits. The start bit can be used as a busy signal indicator to interrupt the digital host and trigger the data reading. Otherwise, without a busy indicator, the user must timeout the maximum conversion time prior to readback.

The busy indicator feature is enabled

- In the $\overline{\text{CS}}$ mode if CNV or SDI is low when the ADC conversion ends (see Figure 32 and Figure 36).
- In the chain mode if SCK is high during the CNV rising edge (see Figure 40).

$\overline{\text{CS}}$ MODE, 3-WIRE WITHOUT BUSY INDICATOR

$\overline{\text{CS}}$ mode, 3-wire without busy indicator is usually used when a single AD7982 is connected to an SPI-compatible digital host. The connection diagram is shown in Figure 29, and the corresponding timing is given in Figure 30.

With SDI tied to VIO, a rising edge on CNV initiates a conversion, selects the $\overline{\text{CS}}$ mode, and forces SDO to high impedance. After a conversion is initiated, it continues until completion irrespective of the state of CNV. This feature can be useful, for instance, to bring CNV low to select other SPI devices, such as analog multiplexers; however, CNV must be returned high before the minimum conversion time elapses and then held high for the maximum possible conversion time to avoid the generation of the busy signal indicator.

When the conversion completes, the AD7982 enters the acquisition phase and powers down. When CNV goes low, the MSB is output onto SDO. The remaining data bits are clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the 18th SCK falling edge or when CNV goes high (whichever occurs first), SDO returns to high impedance.

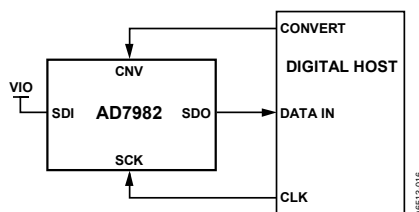


Figure 29. $\overline{\text{CS}}$ Mode, 3-Wire Without Busy Indicator Connection Diagram (SDI High)

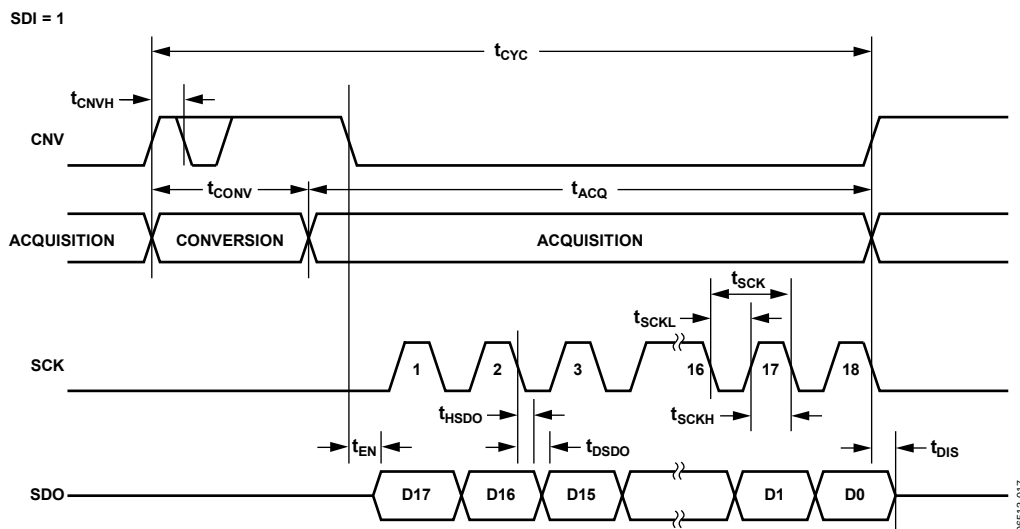


Figure 30. $\overline{\text{CS}}$ Mode, 3-Wire Without Busy Indicator Serial Interface Timing (SDI High)

$\overline{\text{CS}}$ MODE, 3-WIRE WITH BUSY INDICATOR

$\overline{\text{CS}}$ mode, 3-wire with busy indicator is usually used when a single AD7982 is connected to an SPI-compatible digital host having an interrupt input.

The connection diagram is shown in Figure 31, and the corresponding timing is given in Figure 32.

With SDI tied to VIO, a rising edge on CNV initiates a conversion, selects the $\overline{\text{CS}}$ mode, and forces SDO to high impedance. SDO is maintained in high impedance until the completion of the conversion irrespective of the state of CNV. Prior to the minimum conversion time, CNV can be used to select other SPI devices, such as analog multiplexers, but CNV must be returned low before the minimum conversion time elapses and then held low for the maximum possible conversion time to guarantee the generation of the busy signal indicator.

When the conversion completes, SDO goes from high impedance to low impedance. With a pull-up resistor on the SDO line, the high impedance to low impedance transition can be used as an interrupt signal to initiate the data reading controlled by the digital host. The AD7982 then enters the acquisition phase and powers down. The data bits are then clocked out, MSB first, by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the optional 19th SCK falling edge or when CNV goes high (whichever occurs first), SDO returns to high impedance.

If multiple AD7982 devices are selected at the same time, the SDO output pin handles this contention without damage or induced latch-up. Meanwhile, it is recommended to keep this contention as short as possible to limit extra power dissipation.

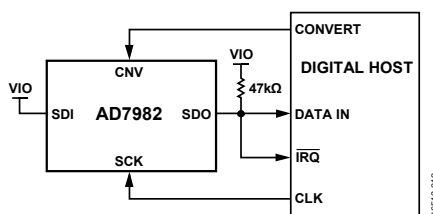


Figure 31. $\overline{\text{CS}}$ Mode, 3-Wire with Busy Indicator Connection Diagram (SDI High)

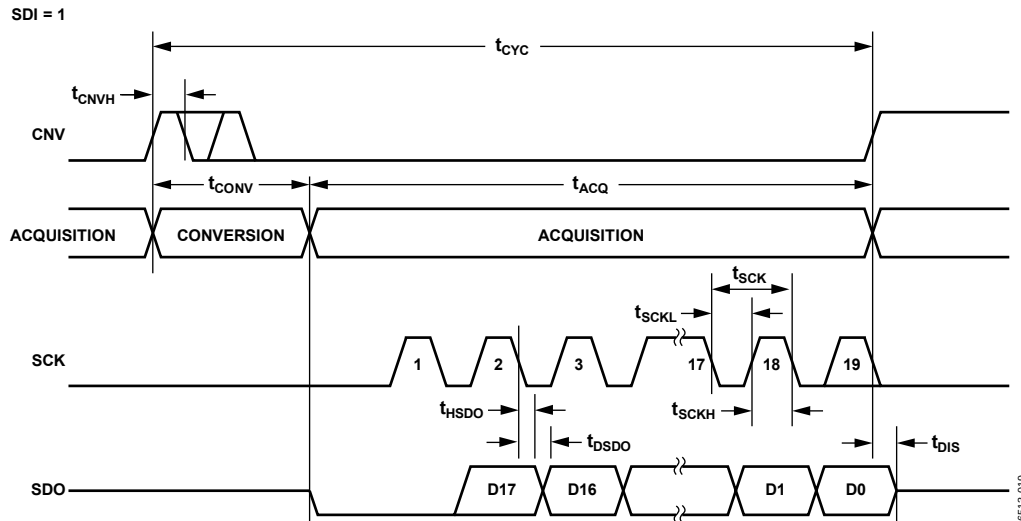


Figure 32. $\overline{\text{CS}}$ Mode, 3-Wire with Busy Indicator Serial Interface Timing (SDI High)

CS MODE, 4-WIRE WITHOUT BUSY INDICATOR

CS mode, 4-wire without busy indicator is usually used when multiple [AD7982](#) devices are connected to an SPI-compatible digital host.

A connection diagram example using two [AD7982](#) devices is shown in Figure 33, and the corresponding timing is given in Figure 34.

With SDI high, a rising edge on CNV initiates a conversion, selects the $\overline{\text{CS}}$ mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback. If SDI and CNV are low, SDO is driven low. Prior to the minimum conversion time, SDI can select other SPI devices, such as analog multiplexers, but SDI must be returned high before the minimum conversion time elapses and then held high for the maximum possible conversion time to avoid the generation of the busy signal indicator.

When the conversion completes, the [AD7982](#) enters the acquisition phase and powers down. Each ADC result can be read by bringing its SDI input low, which consequently outputs the MSB onto SDO. The remaining data bits are then clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the 18th SCK falling edge or when SDI goes high (whichever occurs first), SDO returns to high impedance and another [AD7982](#) can be read.

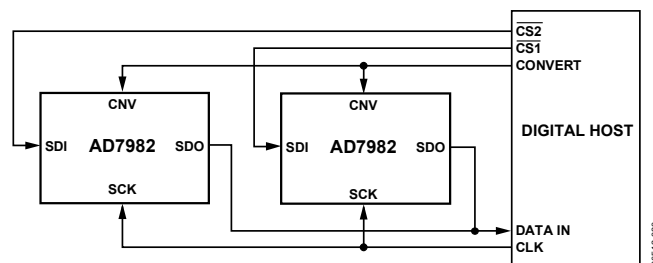
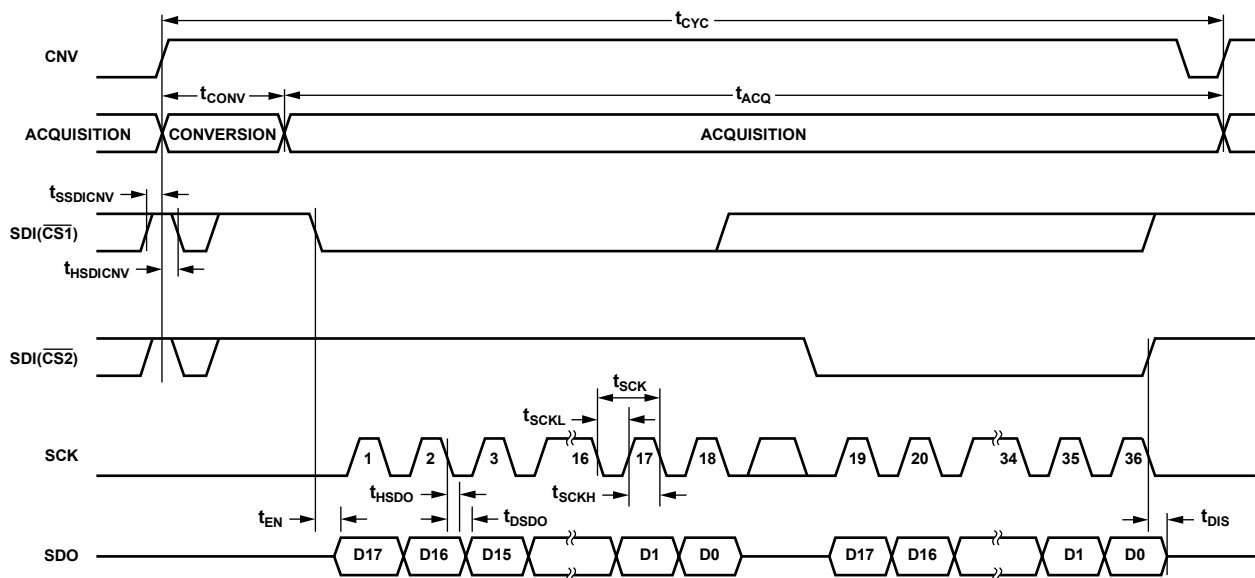


Figure 33. $\overline{CS}$ Mode, 4-Wire Without Busy Indicator Connection Diagram

Figure 34. $\overline{CS}$ Mode, 4-Wire Without Busy Indicator Serial Interface Timing

$\overline{\text{CS}}$ MODE, 4-WIRE WITH BUSY INDICATOR

$\overline{\text{CS}}$ mode, 4-wire with busy indicator is usually used when a single AD7982 is connected to an SPI-compatible digital host with an interrupt input and when it is desired to keep CNV, which samples the analog input, independent of the signal used to select the data reading. This independence is particularly important in applications where low jitter on CNV is desired.

The connection diagram is shown in Figure 35, and the corresponding timing is given in Figure 36.

With SDI high, a rising edge on CNV initiates a conversion, selects the $\overline{\text{CS}}$ mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback. If SDI and CNV are low, SDO is driven low.

Prior to the minimum conversion time, SDI can select other SPI devices, such as analog multiplexers, but SDI must be returned low before the minimum conversion time elapses and then held low for the maximum possible conversion time to guarantee the generation of the busy signal indicator.

When the conversion is complete, SDO goes from high impedance to low impedance. With a pull-up on the SDO line, the high impedance to low impedance transition can be used as an interrupt signal to initiate the data readback controlled by the digital host. The AD7982 then enters the acquisition phase and powers down. The data bits then clock out, MSB first, by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the optional 19th SCK falling edge or SDI going high (whichever occurs first), SDO returns to high impedance.

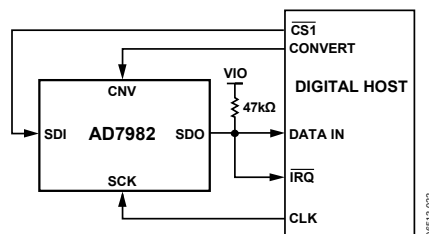


Figure 35. $\overline{\text{CS}}$ Mode, 4-Wire with Busy Indicator Connection Diagram

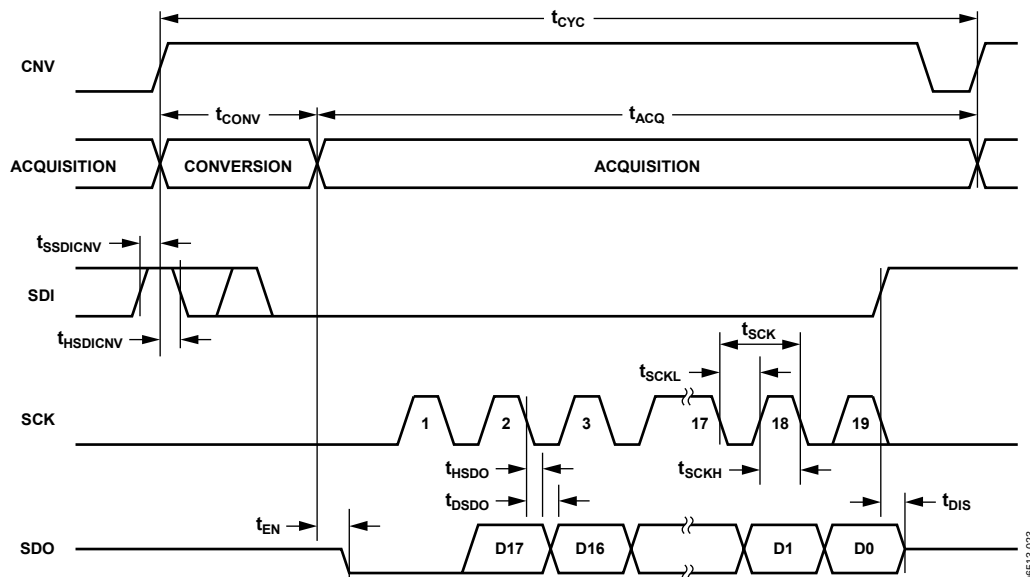


Figure 36. $\overline{\text{CS}}$ Mode, 4-Wire with Busy Indicator Serial Interface Timing

CHAIN MODE WITHOUT BUSY INDICATOR

Chain mode without busy indicator can be used to daisy-chain multiple AD7982 devices on a 3-wire serial interface. The chain mode without busy indicator feature reduces component count and wiring connections, for example, in isolated multiconverter applications or for systems with a limited interfacing capacity. Data readback is analogous to clocking a shift register.

Figure 37 shows a connection diagram example using two AD7982 devices, and Figure 38 shows the corresponding timing.

When SDI and CNV are low, SDO is driven low. With SCK low, a rising edge on CNV initiates a conversion, selects the chain mode, and disables the busy indicator.

In this mode, CNV is held high during the conversion phase and the subsequent data readback.

When the conversion completes, the MSB is output onto SDO and the AD7982 enters the acquisition phase and powers down. The remaining data bits stored in the internal shift register are clocked by subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register and is clocked by the SCK falling edge. Each ADC in the chain outputs its data MSB first, and $18 \times N$ clocks are required to read back the N ADCs. The data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate and consequently more AD7982 devices in the chain, provided the digital host has an acceptable hold time. The maximum conversion rate can be reduced due to the total readback time.

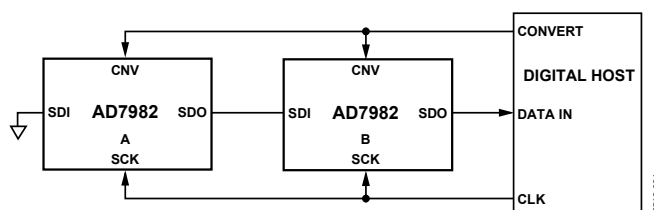


Figure 37. Chain Mode Without Busy Indicator Connection Diagram

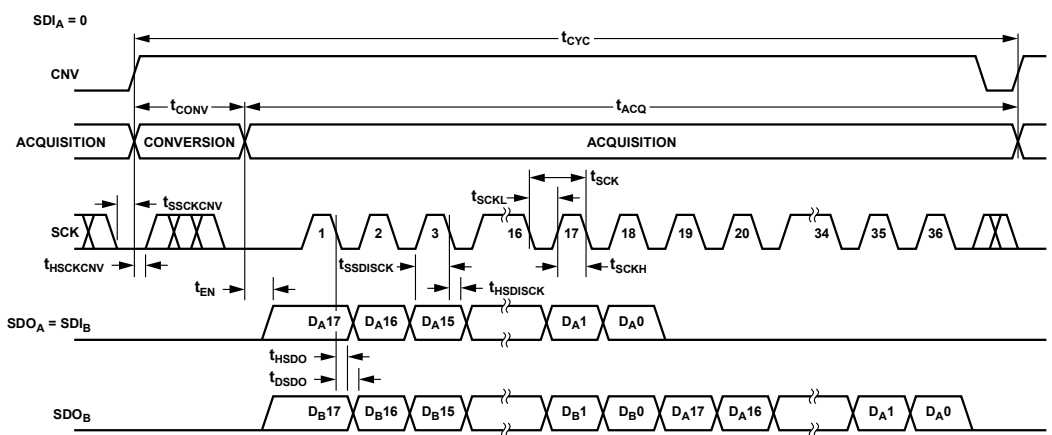


Figure 38. Chain Mode Without Busy Indicator Serial Interface Timing

CHAIN MODE WITH BUSY INDICATOR

Chain mode with busy indicator can also daisy-chain multiple AD7982 devices on a 3-wire serial interface while providing a busy indicator. This chain mode with busy indicator feature reduces component count and wiring connections, for example, in isolated multiconverter applications or for systems with a limited interfacing capacity. Data readback is analogous to clocking a shift register.

Figure 39 shows a connection diagram example using three AD7982 devices, and Figure 40 shows the corresponding timing.

When SDI and CNV are low, SDO is driven low. With SCK high, a rising edge on CNV initiates a conversion, selects the chain mode, and enables the busy indicator feature.

In this mode, CNV is held high during the conversion phase and the subsequent data readback. When all ADCs in the chain have completed their conversions, the SDO pin of the ADC closest to the digital host (see the AD7982 ADC labeled C in Figure 39) is driven high. The transition of driving the SDO pin of the ADC to high can be used as a busy indicator to trigger the data readback controlled by the digital host. The AD7982 then enters the acquisition phase and powers down. The data bits stored in the internal shift register are clocked out, MSB first, by subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register and is clocked by the SCK falling edge. Each ADC in the chain outputs its data MSB first, and $18 \times N + 1$ clocks are required to read back the N ADCs. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate and consequently more AD7982 devices in the chain, provided the digital host has an acceptable hold time.

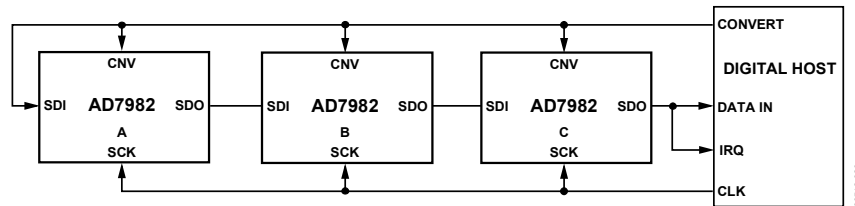


Figure 39. Chain Mode with Busy Indicator Connection Diagram

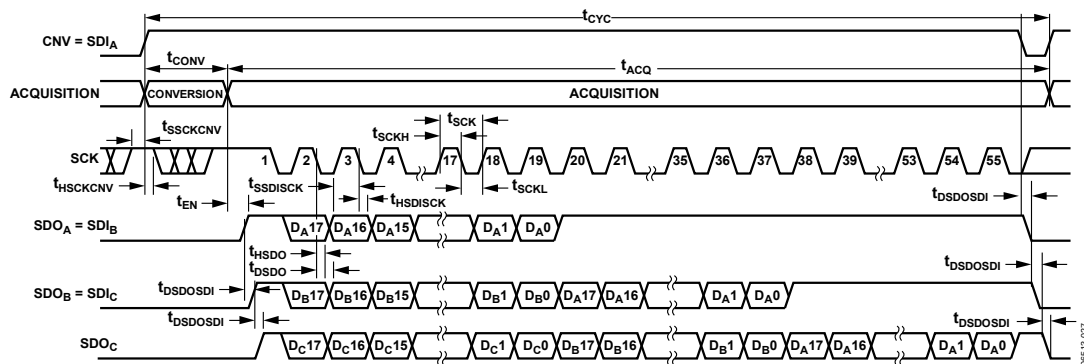


Figure 40. Chain Mode with Busy Indicator Serial Interface Timing

APPLICATIONS INFORMATION

LAYOUT

The printed circuit board (PCB) that houses the [AD7982](#) must be designed so the analog and digital sections are separated and confined to certain areas of the PCB. The pin configuration of the [AD7982](#), with its analog signals on the left side and its digital signals on the right side, eases the task of separating the analog and digital circuitry on a PCB.

Avoid running digital lines under the device; these couple noise onto the die, unless a ground plane under the [AD7982](#) is used as a shield. Fast switching signals, such as CNV or clocks, must not run near analog signal paths. Crossover of digital and analog signals must be avoided.

It is recommended to use at least one ground plane. It can be common or split between the digital and analog sections. In the latter case, the planes must be joined underneath the [AD7982](#) devices.

The [AD7982](#) voltage reference input REF has a dynamic input impedance and must be decoupled with minimal parasitic inductances. Decoupling is done by placing the reference decoupling ceramic capacitor close to, ideally right up against, the REF and GND pins and connecting them with wide, low impedance traces.

Finally, decouple the power supplies of the [AD7982](#), VDD and VIO, with ceramic capacitors, typically 100 nF, placed close to the [AD7982](#) and connected using short, wide traces to provide low impedance paths and to reduce the effect of glitches on the power supply lines.

An example of layout following these rules is shown in Figure 41 and Figure 42.

EVALUATING THE PERFORMANCE OF THE [AD7982](#)

Other recommended layouts for the [AD7982](#) are outlined in the [UG-340](#) user guide for the [EVAL-AD7982SDZ](#). The evaluation board package includes a fully assembled and tested evaluation board, the user guide, and software for controlling the evaluation board from a PC via the [EVAL-SDP-CB1Z](#).

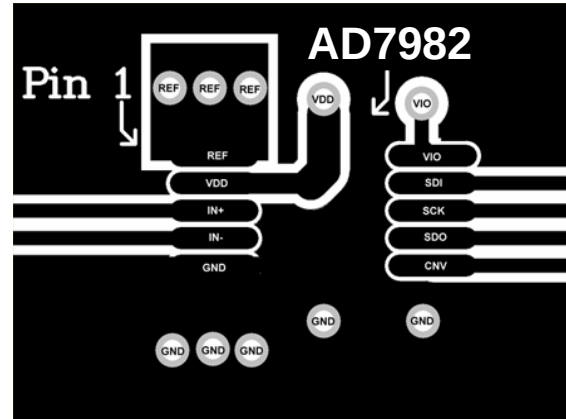


Figure 41. Example Layout of the [AD7982](#) (Top Layer)

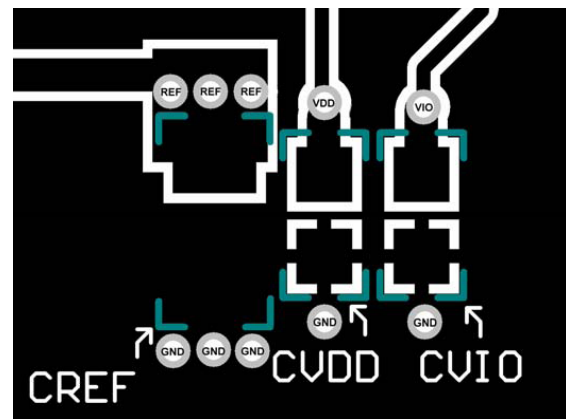
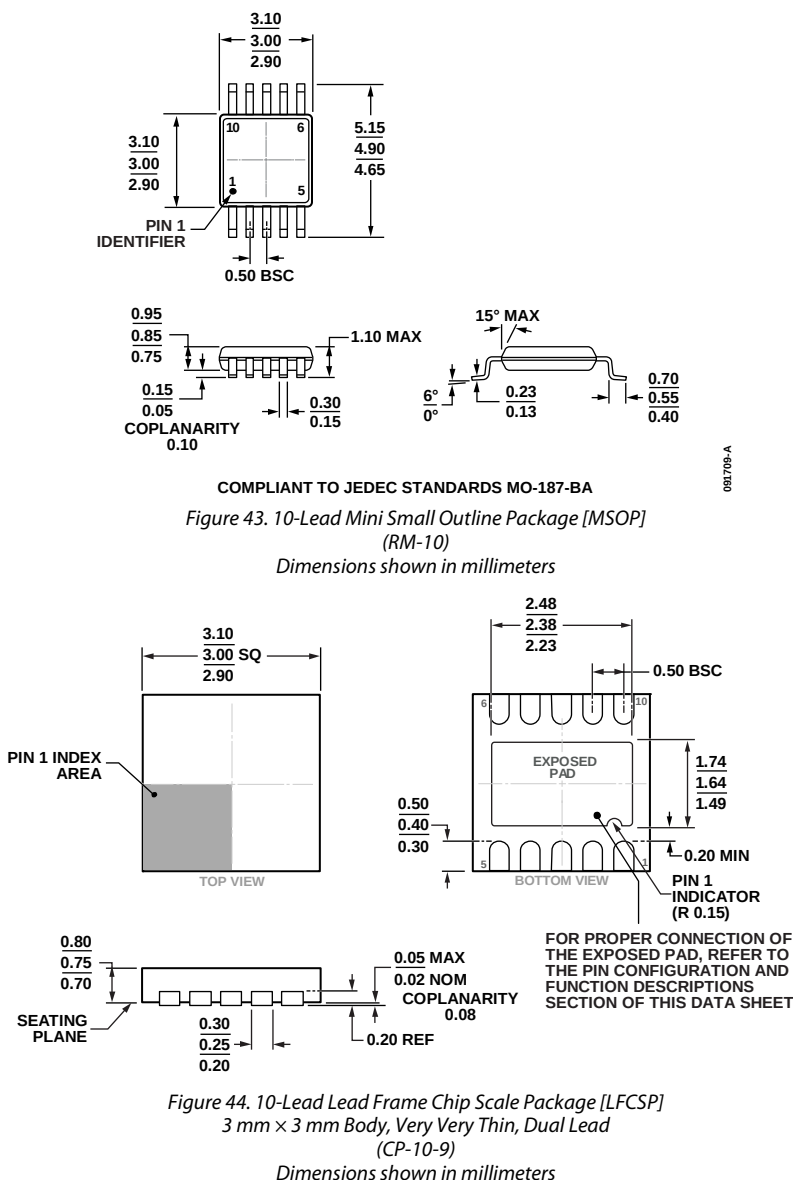


Figure 42. Example Layout of the [AD7982](#) (Bottom Layer)

OUTLINE DIMENSIONS



ORDERING GUIDE

Model ^{1, 2, 3}	Temperature Range	Package Description	Package Option	Branding	Ordering Quantity
AD7982BRMZ	−40°C to +85°C	10-Lead MSOP, Tube	RM-10	C5F	50
AD7982BRMZRL7	−40°C to +85°C	10-Lead MSOP, 7" Reel	RM-10	C5F	1,000
AD7982BCPZ-RL7	−40°C to +85°C	10-Lead LFCSP, 7" Reel	CP-10-9	C5F	1,500
AD7982BCPZ-RL	−40°C to +85°C	10-Lead LFCSP, 13" Reel	CP-10-9	C5F	5,000
EVAL-AD7982SDZ		Evaluation Board			
EVAL-SDP-CB1Z		Controller Board			

¹ Z = RoHS compliant part.

² The EVAL-AD7982SDZ board can be used as a standalone evaluation board or in conjunction with the EVAL-SDP-CB1Z for evaluation/demonstration purposes.

³ The EVAL-SDP-CB1Z board allows a PC to control and communicate with all Analog Devices evaluation boards ending in the SDZ designator.