

## Differential Clock Buffer/Driver

### Features

- Phase-locked loop clock distribution for Double Data Rate Synchronous DRAM applications
- 1:10 differential outputs
- External Feedback pins (FBINT, FBINC) are used to synchronize the outputs to the clock input
- SSCG: Spread Aware™ for EMI reduction
- 48-pin SSOP and TSSOP packages
- Conforms to JEDEC JC40 and JC42.5 DDR specifications

### Description

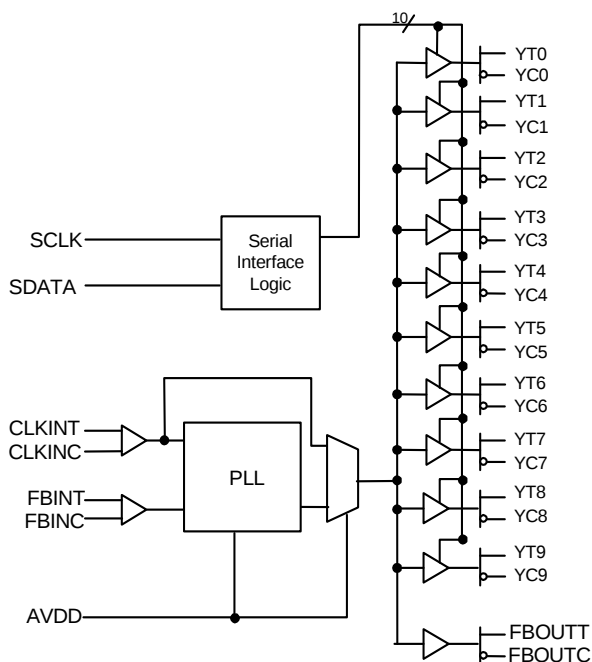
This PLL clock buffer is designed for 2.5 VDD and 2.5 AVDD operation and differential data input and output levels.

This device is a zero-delay buffer that distributes a differential clock input pair (CLKINT, CLKINC) to ten differential pairs of clock outputs (YT[0:9], YC[0:9]) and one differential pair feedback clock output (FBOUTT, FBOUTC). The clock outputs are individually controlled by the serial inputs SCLK and SDATA.

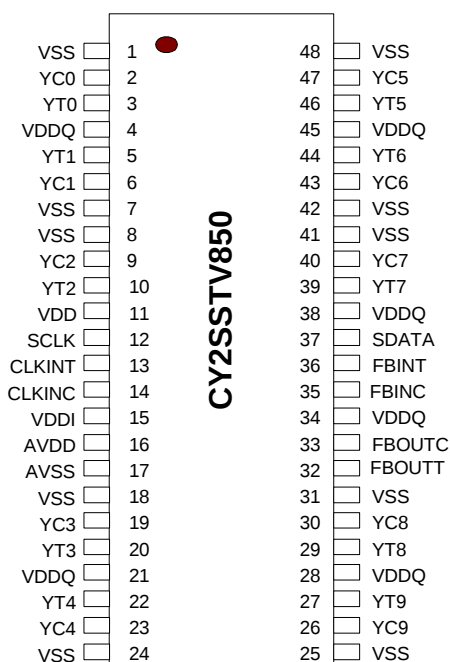
The two-line serial bus can set each output clock pair (YT[0:9], YC[0:9]) to the Hi-Z state. When AVDD is grounded, the PLL is turned off and bypassed for test purposes.

The PLL in this device uses the input clocks (CLKINT, CLKINC) and the feedback clocks (FBINT, FBINC) to provide high-performance, low-skew, low-jitter output differential clocks.

### Block Diagram



### Pin Configuration



**Pin Description<sup>[1, 2]</sup>**

| Pin                                    | Name    | I/O     | Description                                                                                                                                                                  | Electrical Characteristics                        |
|----------------------------------------|---------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------|
| 13                                     | CLKINT  | I       | <b>Complementary Clock Input.</b>                                                                                                                                            | LV Differential Input                             |
| 14                                     | CLKINC  | I       | <b>Complementary Clock Input.</b>                                                                                                                                            |                                                   |
| 35                                     | FBINC   | I       | <b>Feedback Clock Input.</b> Connect to FBOUTC for accessing the PLL.                                                                                                        | Differential Input                                |
| 36                                     | FBINT   | I       | <b>Feedback Clock Input.</b> Connect to FBOUTT for accessing the PLL.                                                                                                        |                                                   |
| 3, 5, 10, 20, 22<br>46, 44, 39, 29,27  | YT(0:9) | O       | <b>Clock Outputs</b>                                                                                                                                                         | Differential Outputs                              |
| 2, 6, 9, 19, 23<br>47, 43, 40,30,26    | YC(0:9) | O       | <b>Clock Outputs</b>                                                                                                                                                         |                                                   |
| 32                                     | FBOUTT  | O       | <b>Feedback Clock Output.</b> Connect to FBINT for normal operation. A bypass delay capacitor at this output will control Input Reference/Output Clocks phase relationships. | Differential Outputs                              |
| 33                                     | FBOUTC  | O       | <b>Feedback Clock Output.</b> Connect to FBINC for normal operation. A bypass delay capacitor at this output will control Input Reference/Output Clocks phase relationships. |                                                   |
| 12                                     | SCLK    | I, PU   | <b>Serial Clock Input.</b> Clocks data at SDATA into the internal register.                                                                                                  | Data Input for the two-line serial bus            |
| 37                                     | SDATA   | I/O, PU | <b>Serial Data Input.</b> Input data is clocked to the internal register to enable/disable individual outputs. This provides flexibility in power management.                | Data Input and Output for the two-line serial bus |
| 11                                     | VDD     |         | <b>2.5V power Supply for Logic</b>                                                                                                                                           | 2.5V Nominal                                      |
| 4, 21, 28, 34, 38, 45                  | VDDQ    |         | <b>2.5V Power Supply for Output Clock Buffers</b>                                                                                                                            | 2.5V Nominal                                      |
| 16                                     | AVDD    |         | <b>2.5V Power Supply for PLL</b>                                                                                                                                             | 2.5V Nominal                                      |
| 15                                     | VDDI    |         | <b>Power Supply for two-line serial Interface</b>                                                                                                                            | 2.5V or 3.3V Nominal                              |
| 1, 7, 8, 18, 24, 25,<br>31, 41, 42, 48 | VSS     |         | <b>Common Ground</b>                                                                                                                                                         | 0.0V Ground                                       |
| 17                                     | AVSS    |         | <b>Analog Ground</b>                                                                                                                                                         | 0.0V Analog Ground                                |

**Notes:**

1. PU= internal pull-up
2. A bypass capacitor (0.1  $\mu$ F) should be placed as close as possible to each positive power pin (<0.2"). If these bypass capacitors are not close to the pins their high-frequency filtering characteristic will be cancelled by the lead inductance of the traces

**Function Table**

| Inputs |         |         |         |         | Outputs                |                        |        |        | PLL          |
|--------|---------|---------|---------|---------|------------------------|------------------------|--------|--------|--------------|
| AVDD   | CLKINT  |         | CLKINC  |         | YT(0:9) <sup>[3]</sup> | YC(0:9) <sup>[3]</sup> | FBOUTT | FBOUTC |              |
| GND    | L       |         | H       |         | L                      | H                      | L      | H      | BYPASSED/OFF |
| GND    | H       |         | L       |         | H                      | L                      | H      | L      | BYPASSED/OFF |
| 2.5V   | L       |         | H       |         | L                      | H                      | L      | H      | On           |
| 2.5V   | H       |         | L       |         | H                      | L                      | H      | L      | On           |
|        | Nom     | Design  | Nom     | Design  |                        |                        |        |        |              |
| 2.5V   | <20 MHz | <30 MHz | <20 MHz | <30 MHz | Hi-Z                   | Hi-Z                   | Hi-Z   | Hi-Z   | Off          |

**Power Management**

The individual output enable/disable control of the CY2SSTV850 allows the user to implement unique power management schemes into the design. Outputs are three-stated when disabled through the two-line interface as individual bits are set low in Byte 0 and Byte 1 registers. The feedback output pair (FBOUTT, FBOUTC) cannot be disabled via two-line serial bus. The enabling and disabling of individual outputs is done in such a manner as to eliminate the possibility of partial “runt” clocks.

**Zero-delay Buffer**

When used as a zero-delay buffer the CY2SSTV850 will likely be in a nested clock tree application. For these applications the CY2SSTV850 offers a differential clock input pair as a PLL reference. The CY2SSTV850 then can lock onto the reference and translate with near zero delay to low-skew outputs. For normal operation, the external feedback input, FBINT, is connected to the feedback output, FBOUTT. By connecting the feedback output to the feedback input the propagation delay through the device is eliminated. The PLL works to align the output edge with the input reference edge thus producing a near zero delay. The reference frequency affects the static phase offset of the PLL and thus the relative delay between the inputs and outputs.

When AVDD is strapped low, the PLL is turned off and bypassed for test purposes.

**Serial Control Registers**

Following the acknowledge of the Address Byte, two additional bytes must be sent:

“Command Code” byte, and “Byte Count” byte.

**2 Line Serial Interface**
**2-Line Serial Interface Slave Address**

| A7 | A6 | A5 | A4 | A3 | A2 | A1 | R/W |
|----|----|----|----|----|----|----|-----|
| 1  | 1  | 0  | 1  | 0  | 0  | 1  | 0   |

Writing to the device is accomplished by sequentially sending the device address D2H, the dummy bytes (command code and the number of bytes), and the data bytes. This sequence is illustrated in the following tables.

**Note:**

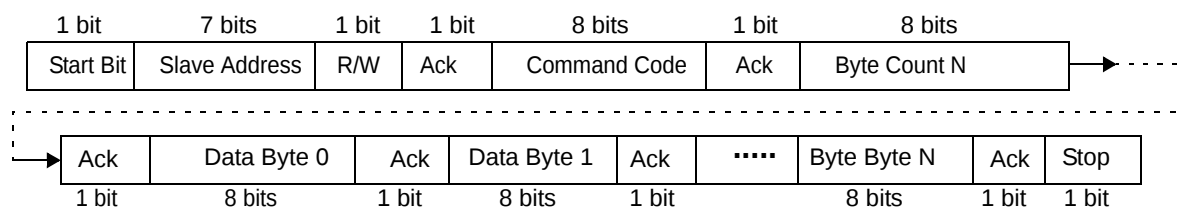
3. Each output pair can be three-stated via the two-line serial interface.

**Byte0: Output Register (1 = Enable, 0 = Disable)**

| Bit | @Pup | Pin#   | Description |
|-----|------|--------|-------------|
| 7   | 1    | 3, 2   | YT0, YC0    |
| 6   | 1    | 5, 6   | YT1, YC1    |
| 5   | 1    | 10, 9  | YT2, YC2    |
| 4   | 1    | 20, 19 | YT3, YC3    |
| 3   | 1    | 22, 23 | YT4, YC4    |
| 2   | 1    | 46, 47 | YT5, YC5    |
| 1   | 1    | 44, 43 | YT6, YC6    |
| 0   | 1    | 39, 40 | YT7, YC7    |

**Byte1: Output Register (1 = Enable, 0 = Disable)**

| Bit | @Pup | Pin#   | Description |
|-----|------|--------|-------------|
| 7   | 1    | 29, 30 | YT8, YC8    |
| 6   | 1    | 27, 26 | YT9, YC9    |
| 5   | 0    |        | Reserved    |
| 4   | 0    |        | Reserved    |
| 3   | 0    |        | Reserved    |
| 2   | 0    |        | Reserved    |
| 1   | 0    |        | Reserved    |
| 0   | 0    |        | Reserved    |



**Table 1. Timing Requirements for the 2-line Serial Interface over Recommended Ranges of Operating Free-air Temperature and VDDI from 3.3V to 3.5V**

| Parameter                     | Description              | Min. | Max. | Unit          |
|-------------------------------|--------------------------|------|------|---------------|
| $f_{\text{SCLK}}$             | SCLK frequency           |      | 100  | kHz           |
| $t_{\text{BUS}}$              | Bus free time            | 4.7  |      | $\mu\text{s}$ |
| $t_{\text{SU}}(\text{START})$ | START set-up time        | 4.7  |      | $\mu\text{s}$ |
| $t_{\text{H}}(\text{START})$  | START hold time          | 4.0  |      | $\mu\text{s}$ |
| $t_{\text{W}}(\text{SCLL})$   | SCLK low pulse duration  | 4.7  |      | $\mu\text{s}$ |
| $t_{\text{W}}(\text{SCLH})$   | SCLK high pulse duration | 4.0  |      | $\mu\text{s}$ |
| $t_{\text{R}}(\text{SDATA})$  | SDATA input rise time    |      | 1000 | ns            |
| $t_{\text{F}}(\text{SDATA})$  | SDATA input fall time    |      | 300  | ns            |
| $t_{\text{SU}}(\text{SDATA})$ | SDATA set-up time        | 250  |      | ns            |
| $t_{\text{H}}(\text{SDATA})$  | SDATA hold time          | 0    |      | ns            |
| $t_{\text{SU}}(\text{STOP})$  | STOP set-up time         | 4    |      | $\mu\text{s}$ |

**Maximum Ratings<sup>[4]</sup>**

Input Voltage Relative to  $V_{SS}$ : .....  $V_{SS} - 0.3V$   
 Input Voltage Relative to  $V_{DDQ}$  or  $AV_{DD}$ : .....  $V_{DD} + 0.3V$   
 Storage Temperature: .....  $-65^{\circ}C$  to  $+150^{\circ}C$   
 Operating Temperature: .....  $0^{\circ}C$  to  $+70^{\circ}C$   
 Maximum Power Supply: .....  $3.5V$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range:

$$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{SS}$  or  $V_{DD}$ ).

**DC Parameters<sup>[5]</sup>** ( $AV_{DD} = V_{DDQ} = 2.5V \pm 5\%$ ,  $V_{DDI} = 3.3V \pm 5\%$ ,  $T_A = 0^{\circ}C$  to  $+70^{\circ}C$ )

| Parameter | Description                                        | Conditions                                           | Min.                | Typ.        | Max.                | Unit    |
|-----------|----------------------------------------------------|------------------------------------------------------|---------------------|-------------|---------------------|---------|
| $V_{IL}$  | Input Low Voltage                                  | SDATA, SCLK                                          |                     |             | 1.0                 | V       |
| $V_{IH}$  | Input High Voltage                                 |                                                      | 2.2                 |             |                     | V       |
| $V_{ID}$  | Differential Input Voltage <sup>[6]</sup>          | CLKINT, FBINT                                        | 0.35                |             | $V_{DDQ} + 0.6$     | V       |
| $V_{IX}$  | Differential Input Crossing Voltage <sup>[7]</sup> | CLKTIN, FBINT                                        | $(V_{DDQ}/2) - 0.2$ | $V_{DDQ}/2$ | $(V_{DDQ}/2) + 0.2$ | V       |
| $I_{IN}$  | Input Current                                      | $V_{IN} = 0V$ or $V_{IN} = V_{DDQ}$ , CLKINT, FBINT  | -10                 |             | 10                  | $\mu A$ |
| $I_{OL}$  | Output Low Current                                 | $V_{DDQ} = 2.375V$ , $V_{OUT} = 1.2V$                | 26                  | 35          |                     | mA      |
| $I_{OH}$  | Output High Current                                | $V_{DDQ} = 2.375V$ , $V_{OUT} = 1V$                  | -18                 | -32         |                     | mA      |
| $V_{OL}$  | Output Low Voltage                                 | $V_{DDQ} = 2.375V$ , $I_{OL} = 12\text{ mA}$         |                     |             | 0.6                 | V       |
| $V_{OH}$  | Output High Voltage                                | $V_{DDQ} = 2.375V$ , $I_{OH} = -12\text{ mA}$        | 1.7                 |             |                     | V       |
| $V_{OUT}$ | Output Voltage Swing <sup>[8]</sup>                |                                                      | 1.1                 |             | $V_{DDQ} - 0.4$     | V       |
| $V_{OC}$  | Output Crossing Voltage <sup>[9]</sup>             |                                                      | $(V_{DDQ}/2) - 0.2$ | $V_{DDQ}/2$ | $(V_{DDQ}/2) + 0.2$ | V       |
| $I_{OZ}$  | High-Impedance Output Current                      | $V_O = GND$ or $V_O = V_{DDQ}$                       | -10                 |             | 10                  | $\mu A$ |
| $I_{DDQ}$ | Dynamic Supply Current <sup>[10]</sup>             | All $V_{DDQ}$ and $V_{DDI}$ , $F_O = 170\text{ MHz}$ |                     | 235         | 300                 | mA      |
| $I_{DD}$  | PLL Supply Current                                 | $AV_{DD}$ only                                       |                     | 9           | 12                  | mA      |
| $C_{in}$  | Input Pin Capacitance                              |                                                      | 2.5                 | 3           | 3.5                 | pF      |

**Notes:**

4. **Multiple Supplies:** The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
5. Unused inputs must be held HIGH or LOW to prevent them from floating.
6. Differential input signal voltage specifies the differential voltage  $|V_{TR} - V_{CP}|$  required for switching, where  $V_{TR}$  is the true input level and  $V_{CP}$  is the complementary input level.
7. Differential cross-point input voltage is expected to track  $V_{DDQ}$  and is the voltage at which the differential signals must be crossing.
8. For load conditions see Figure 6.
9. The value of  $V_{OC}$  is expected to be  $|V_{TR} + V_{CP}|/2$ . In case of each clock directly terminated by a 120 $\Omega$  resistor. See Figure 6.
10. All outputs switching loaded with 16 pF in 60 $\Omega$  environment. See Figure 6.

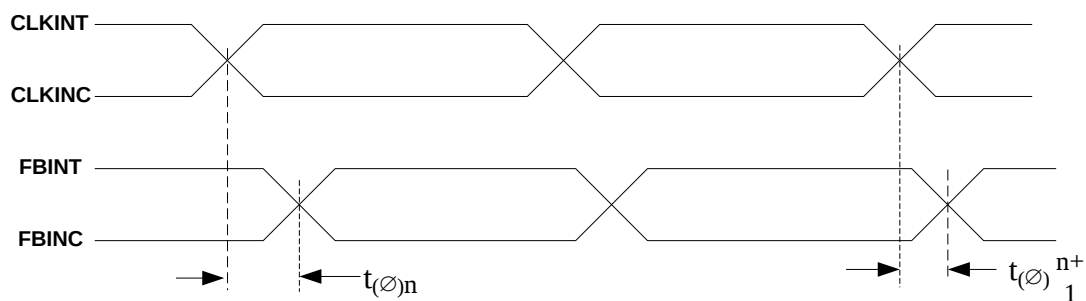
**AC Parameters**<sup>[11, 12]</sup> ( $V_{DD} = V_{DDQ} = 2.5V \pm 5\%$ ,  $V_{DDI} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$ )

| Parameter             | Description                                          | Conditions                                         | Min. | Typ. | Max. | Unit    |
|-----------------------|------------------------------------------------------|----------------------------------------------------|------|------|------|---------|
| $f_{CLK}$             | Operating Clock Frequency                            | $A_{VDD}$ , $V_{DD} = 2.5V \pm 0.2V$               | 60   |      | 170  | MHz     |
| $t_{DC}$              | Input Clock Duty Cycle <sup>[13]</sup>               |                                                    | 40   |      | 60   | %       |
| $t_{lock}$            | Maximum PLL lock Time                                |                                                    |      |      | 100  | $\mu s$ |
| $t_R/t_F$             | Output Clocks Slew Rate                              | 20% to 80% of VOD                                  | 1    |      | 2    | V/ns    |
| $t_{pZL}$ , $t_{pZH}$ | Output Enable Time <sup>[14]</sup><br>(all outputs)  |                                                    |      | 3    |      | ns      |
| $t_{pLZ}$ , $t_{pHZ}$ | Output Disable Time <sup>[14]</sup><br>(all outputs) |                                                    |      | 3    |      | ns      |
| $t_{CCJ}$             | Cycle to Cycle Jitter                                | $f > 66$ MHz                                       | -100 |      | 100  | ps      |
| $t_{jit(h-per)}$      | Half-period jitter <sup>[15]</sup>                   | $f > 66$ MHz                                       | -100 |      | 100  | ps      |
| $t_{PLH}$             | Low-to-High Propagation Delay,<br>CLKINT to YT[0:9]  |                                                    | 1.5  | 3.5  | 6    | ns      |
| $t_{PHL}$             | High-to-Low Propagation Delay,<br>CLKINT to YT[0:9]  |                                                    | 1.5  | 3.5  | 6    | ns      |
| $t_{SK(0)}$           | Any Output to Any Output Skew <sup>[16]</sup>        |                                                    |      |      | 100  | ps      |
| $t_{PHASE}$           | Phase Error <sup>[16]</sup>                          |                                                    | -150 |      | 150  | ps      |
| $t_{JITT(PHASE)}$     | Phase Error Jitter                                   | $f > 66$ MHz                                       | -50  |      | 50   | ps      |
| $t_{d(0)}$            | Dynamic Phase Offset                                 | CLKIN pins to FBIN pins at the DUT <sup>[17]</sup> | 30   |      | 140  | ps      |

**Note:**

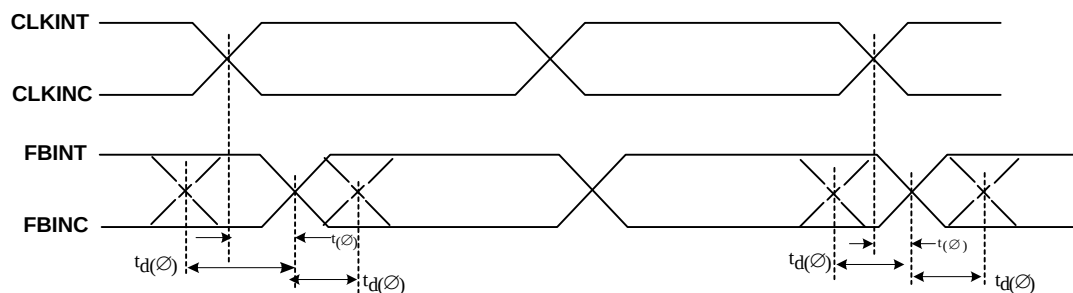
11. Parameters are guaranteed by design and characterization. Not 100% tested in production.
12. PLL is capable of meeting the specified parameters while supporting SSC synthesizers with modulation frequency between 30 kHz and 33.3 kHz with a down spread of -0.5%.
13. While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: duty cycle =  $t_{WH}/t_C$ , where the cycle time ( $t_C$ ) decreases as the frequency goes up.
14. Refers to transition of non-inverting output.
15. Period Jitter and Half-Period Jitter specifications are separate specifications that must be met independently of each other.
16. All differential input and output terminals are terminated with 120 $\Omega$ /16 pF as shown in *Figure 6*.
17. DUT refers to Device Under Test.

# Differential Parameter Measurement Information

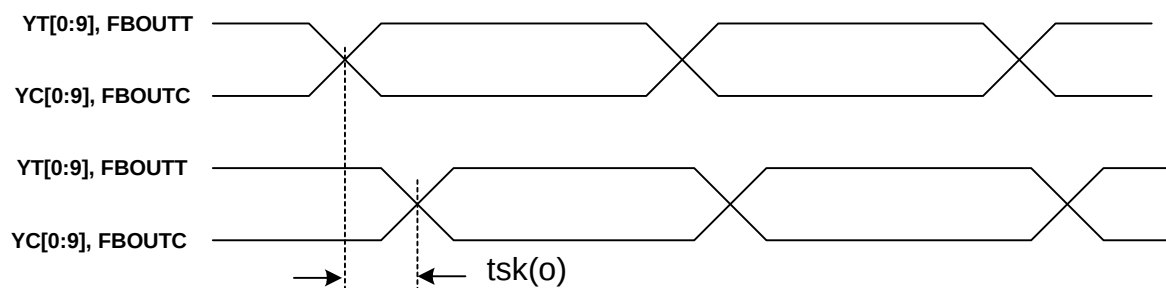


$$t(\phi)_n = \frac{\sum_{1}^{n=N} t(\phi)_n}{N} \quad N(\text{is large number of samples})$$

**Figure 1. Static Phase Offset**



**Figure 2. Dynamic Phase Offset**



**Figure 3. Output Skew**

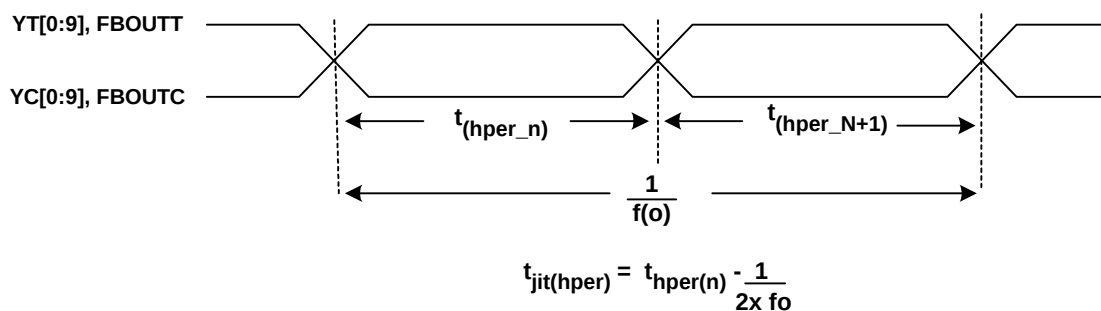


Figure 4. Half-Period Jitter

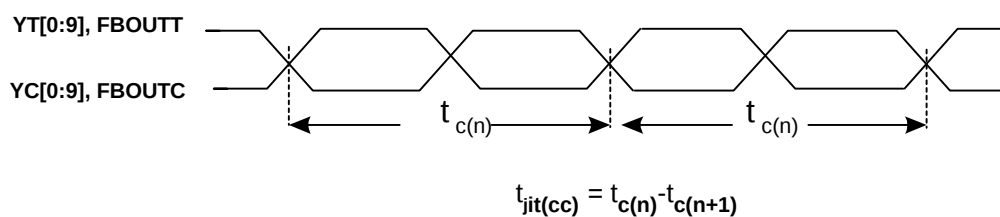


Figure 5. Cycle-to-Cycle Jitter

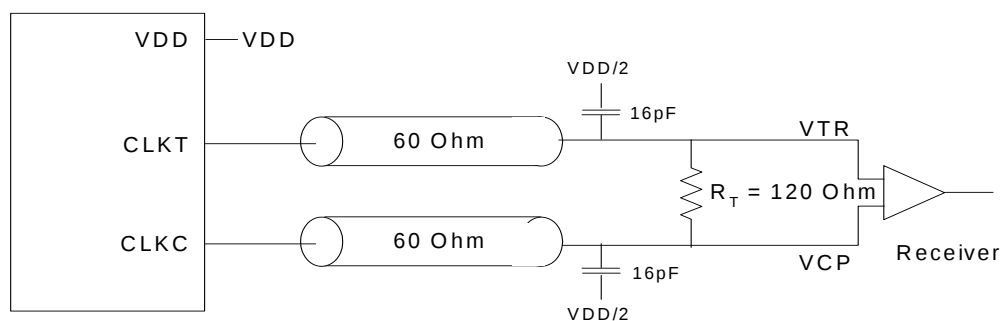


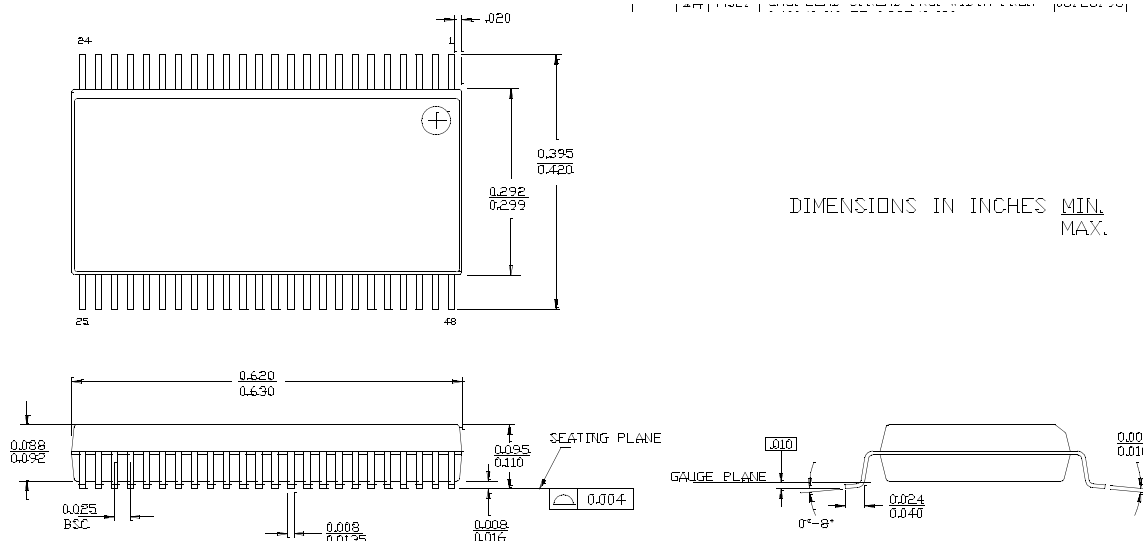
Figure 6. Differential Signal Using Direct Termination Resistor

## Ordering Information

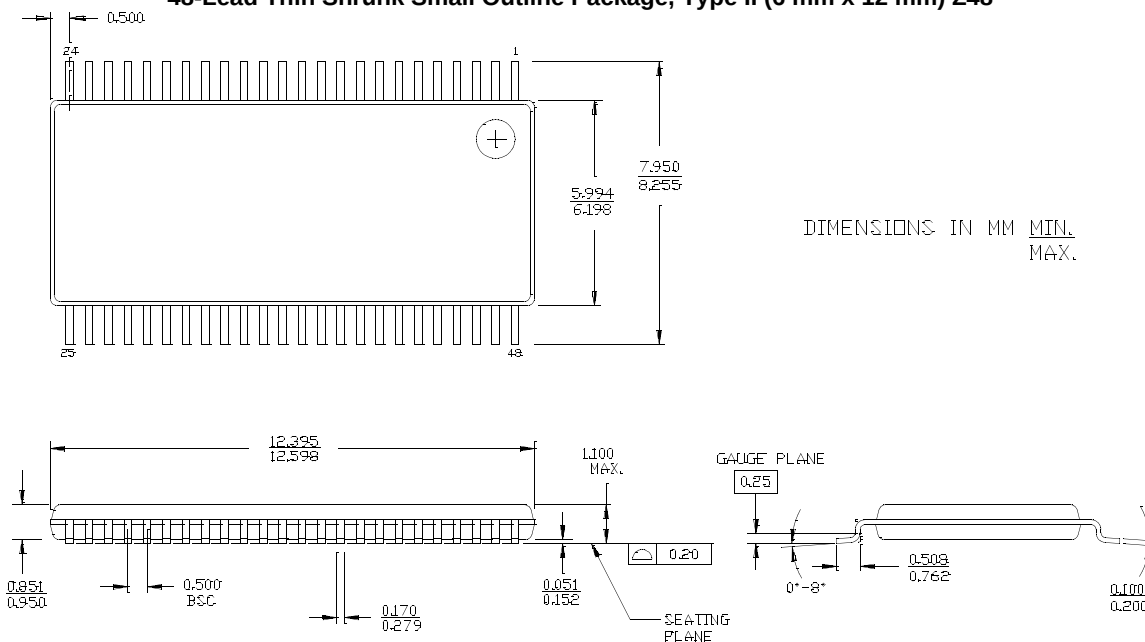
| Part Number   | Package Type                 | Product Flow           |
|---------------|------------------------------|------------------------|
| CY2SSTV850OC  | 48-pin SSOP                  | Commercial, 0° to 70°C |
| CY2SSTV850OCT | 48-pin SSOP - Tape and Reel  | Commercial, 0° to 70°C |
| CY2SSTV850ZC  | 48-pin TSSOP                 | Commercial, 0° to 70°C |
| CY2SSTV850ZCT | 48-pin TSSOP - Tape and Reel | Commercial, 0° to 70°C |

## Package Drawing and Dimensions

### 48-Lead Shrink Small Outline



### 48-Lead Thin Shrink Small Outline Package, Type II (6 mm x 12 mm) Z48



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