



1 MSPS, 8-Channel, Software-Selectable, True Bipolar Input, 12-Bit Plus Sign ADC

AD7329

Power-down modes

TABLE OF CONTENTS

Features	1	Addressing Registers	25
Functional Block Diagram	1	Control Register	26
General Description	1	Sequence Register	28
Product Highlights	1	Range Registers	28
Revision History	2	Sequencer Operation	29
Specifications	3	Reference	31
Timing Specifications	7	V_{DRIVE}	31
Absolute Maximum Ratings	8	Temperature Indicator	31
ESD Caution	8	Modes of Operation	32
Pin Configuration and Function Descriptions	9	Normal Mode (PM1 = PM0 = 0)	32
Typical Performance Characteristics	11	Full Shutdown Mode (PM1 = PM0 = 1)	32
Terminology	15	Autoshutdown Mode (PM1 = 1, PM0 = 0)	33
Theory of Operation	17	Autostandby Mode (PM1 = 0, PM0 = 1)	33
Circuit Information	17	Power vs. Throughput Rate	34
Converter Operation	17	Serial Interface	35
Output Coding	18	Microprocessor Interfacing	36
Transfer Functions	18	AD7329 to ADSP-21xx	36
Analog Input Structure	18	AD7329 to ADSP-BF53x	36
Track-and-Hold Section	19	Applications Information	37
Typical Connection Diagram	20	Layout and Grounding	37
Analog Input	20	Power Supply Configuration	37
Driver Amplifier Choice	23	Outline Dimensions	38
Registers	25	Ordering Guide	38

REVISION HISTORY

12/14—Rev. B to Rev. C

Change to Specifications Section	3
Change to Timing Specifications Section	7
Changes to Table 5	10
Changes to Pseudo Differential Inputs Section	22

1/14—Rev. A to Rev. B

Changes to Circuit Information Section and Table 6	17
Changes to Addressing Registers Section	25
Changes to Power Supply Configuration Section	37
Changes to Ordering Guide	38

2/10—Rev. 0 to Rev. A

Changes to DC Accuracy Parameter, Test Conditions/ Comments, Table 2	4
Change to Normal Mode (Operational) I_{CC} and I_{DRIVE} Parameter and to Power Dissipation Normal Mode Parameter, Table 2	6
Changes to Table 16 and Table 17	36
Added Applications Information Section, Figure 60, and Table 18	37
Changes to Ordering Guide	38

4/06—Revision 0: Initial Version

SPECIFICATIONS

$V_{DD} = 12\text{ V to }16.5\text{ V}$, $V_{SS} = -12\text{ V to }-16.5\text{ V}$, $V_{CC} = 4.75\text{ V to }5.25\text{ V}$, $V_{DRIVE} = 2.7\text{ V to }5.25\text{ V}$, $V_{REF} = 2.5\text{ V internal/external}$, $f_{SCLK} = 20\text{ MHz}$, $f_S = 1\text{ MSPS}$, $T_A = T_{MAX}$ to T_{MIN} , unless otherwise noted. MUX_{OUT+} is connected directly to ADC_{IN+} and MUX_{OUT-} is connected directly to ADC_{IN-} , which is connected to AGND for single-ended mode.

Table 2.

Parameter ¹	Min	B Version Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					$f_{IN} = 50\text{ kHz sine wave}$
Signal-to-Noise Ratio (SNR)	76	77		dB	Differential mode
	72.5	74		dB	Single-ended/pseudo differential mode
Signal-to-Noise and Distortion (SINAD) ²	75	76.5		dB	Differential mode; $\pm 2.5\text{ V}$ and $\pm 5\text{ V}$ ranges
		76.5		dB	Differential mode; $0\text{ V to }+10\text{ V}$ and $\pm 10\text{ V}$ ranges
	72	73.5		dB	Single-ended/pseudo differential mode; $\pm 2.5\text{ V}$ and $\pm 5\text{ V}$ ranges
		73.5		dB	Single-ended/pseudo differential mode; $0\text{ V to }+10\text{ V}$ and $\pm 10\text{ V}$ ranges
Total Harmonic Distortion (THD) ²		-87	-80	dB	Differential mode; $\pm 2.5\text{ V}$ and $\pm 5\text{ V}$ ranges
		-85		dB	Differential mode; $0\text{ V to }+10\text{ V}$ and $\pm 10\text{ V}$ ranges
		-82	-77	dB	Single-ended/pseudo differential mode; $\pm 2.5\text{ V}$ and $\pm 5\text{ V}$ ranges
		-80		dB	Single-ended/pseudo differential mode; $0\text{ V to }+10\text{ V}$ and $\pm 10\text{ V}$ ranges
Peak Harmonic or Spurious Noise (SFDR) ²		-88	-80	dB	Differential mode; $\pm 2.5\text{ V}$ and $\pm 5\text{ V}$ ranges
		-86		dB	Differential mode; $0\text{ V to }+10\text{ V}$ and $\pm 10\text{ V}$ ranges
		-84	-78	dB	Single-ended/pseudo differential mode; $\pm 2.5\text{ V}$ and $\pm 5\text{ V}$ ranges
		-82		dB	Single-ended/pseudo differential mode; $0\text{ V to }+10\text{ V}$ and $\pm 10\text{ V}$ ranges
Intermodulation Distortion (IMD) ²					$f_a = 50\text{ kHz}$, $f_b = 30\text{ kHz}$
Second-Order Terms		-88		dB	
Third-Order Terms		-90		dB	
Aperture Delay ³		7		ns	
Aperture Jitter ³		50		ps	
Common-Mode Rejection (CMRR) ²		-79		dB	Up to 100 kHz ripple frequency; see Figure 17
Channel-to-Channel Isolation ²		-75		dB	f_{IN} on unselected channels up to 100 kHz ; see Figure 14
Full Power Bandwidth		20		MHz	At 3 dB
		1.5		MHz	At 0.1 dB

Parameter ¹	B Version			Unit	Test Conditions/Comments
	Min	Typ	Max		
DC ACCURACY ⁴					All dc accuracy specifications are typical for 0 V to 10 V mode Single-ended/pseudo differential mode 1 LSB = FSR/4096, unless otherwise noted Differential mode 1 LSB = FSR/8192, unless otherwise noted
Resolution	13			Bits	
No Missing Codes	12-bit plus sign (13 bits) 11-bit plus sign (12 bits)			Bits	Differential mode
Integral Nonlinearity ²			±1.1	LSB	Differential mode
			±1	LSB	Single-ended/pseudo differential mode
		−0.7/+1.2		LSB	Single-ended/pseudo differential mode (LSB = FSR/8192)
Differential Nonlinearity ²			−0.9/+1.5	LSB	Differential mode; guaranteed no missing codes to 13 bits
			±0.9	LSB	Single-ended mode; guaranteed no missing codes to 12 bits
		−0.7/+1		LSB	Single-ended/pseudo differential mode (LSB = FSR/8192)
Offset Error ^{2, 5}			−4/+9	LSB	Single-ended/pseudo differential mode
			−7/+10	LSB	Differential mode
Offset Error Match ^{2, 5}			±0.6	LSB	Single-ended/pseudo differential mode
			±0.5	LSB	Differential mode
Gain Error ^{2, 5}			±8.0	LSB	Single-ended/pseudo differential mode
			±14	LSB	Differential mode
Gain Error Match ^{2, 5}			±0.5	LSB	Single-ended/pseudo differential mode
			±0.5	LSB	Differential mode
Positive Full-Scale Error ^{2, 6}			±4	LSB	Single-ended/pseudo differential mode
			±7	LSB	Differential mode
Positive Full-Scale Error Match ^{2, 6}			±0.5	LSB	Single-ended/pseudo differential mode
			±0.5	LSB	Differential mode
Bipolar Zero Code Error ^{2, 6}			±8.5	LSB	Single-ended/pseudo differential mode
			±7.5	LSB	Differential mode
Bipolar Zero Code Error Match ^{2, 6}			±0.5	LSB	Single-ended/pseudo differential mode
			±0.5	LSB	Differential mode
Negative Full-Scale Error ^{2, 6}			±4	LSB	Single-ended/pseudo differential mode
			±6	LSB	Differential mode
Negative Full-Scale Error Match ^{2, 6}			±0.5	LSB	Single-ended/pseudo differential mode
			±0.5	LSB	Differential mode

Parameter ¹	Min	B Version Typ	Max	Unit	Test Conditions/Comments
ANALOG INPUT					
Input Voltage Ranges (Programmed via Range Register)		±10		V	Reference = 2.5 V; see Table 6 $V_{DD} = 10\text{ V min}$, $V_{SS} = -10\text{ V min}$, $V_{CC} = 2.7\text{ V to }5.25\text{ V}$
		±5		V	$V_{DD} = 5\text{ V min}$, $V_{SS} = -5\text{ V min}$, $V_{CC} = 2.7\text{ V to }5.25\text{ V}$
		±2.5		V	$V_{DD} = 5\text{ V min}$, $V_{SS} = -5\text{ V min}$, $V_{CC} = 2.7\text{ V to }5.25\text{ V}$
		0 to 10		V	$V_{DD} = 10\text{ V min}$, $V_{SS} = \text{AGND min}$, $V_{CC} = 2.7\text{ V to }5.25\text{ V}$
Pseudo Differential V_{IN-} Input Range					$V_{DD} = 16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$, $V_{CC} = 5\text{ V}$; see Figure 43 and Figure 44
		±3.5		V	Reference = 2.5 V; range = ±10 V
		±6		V	Reference = 2.5 V; range = ±5 V
		±5		V	Reference = 2.5 V; range = ±2.5 V
		+3/-5		V	Reference = 2.5 V; range = 0 V to +10 V
DC Leakage Current			±100	nA	$V_{IN} = V_{DD}$ or V_{SS}
		3		nA	Per channel, $V_{IN} = V_{DD}$ or V_{SS}
Input Capacitance ³		16		pF	When in track, all ranges, single ended
$ADC_{IN\pm}$ Capacitance ³		7		pF	When in track, ±10 V range, single ended
		10		pF	When in track, ±5 V range, single ended
		14.5		pF	When in track, ±2.5 V range, single ended
		10.5		pF	When in track, 0 V to +10 V range, single ended
		4.0		pF	When in hold, all ranges, single ended
MUX_{OUT-} Capacitance ³		7.5		pF	All ranges, single ended
MUX_{OUT+} Capacitance ³		13		pF	All ranges, single ended
REFERENCE INPUT/OUTPUT					
Input Voltage Range	2.5		3	V	
Input DC Leakage Current			±1	μA	
Input Capacitance		10		pF	
Reference Output Voltage		2.5		V	
Reference Output Voltage Error at 25°C			±5	mV	
Reference Output Voltage T_{MIN} to T_{MAX}			±10	mV	
Reference Temperature Coefficient			25	ppm/°C	
		3		ppm/°C	
Reference Output Impedance		7		Ω	
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4			V	
Input Low Voltage, V_{INL}			0.8	V	$V_{CC} = 4.75\text{ V to }5.25\text{ V}$
			0.4	V	$V_{CC} = 2.7\text{ to }3.6\text{ V}$
Input Current, I_{IN}			±1	μA	$V_{IN} = 0\text{ V or }V_{DRIVE}$
Input Capacitance, C_{IN}^3		10		pF	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	$V_{DRIVE} - 0.2\text{ V}$			V	$I_{SOURCE} = 200\text{ μA}$
Output Low Voltage, V_{OL}			0.4	V	$I_{SINK} = 200\text{ μA}$
Floating-State Leakage Current			±1	μA	
Floating-State Output Capacitance ³		5		pF	
Output Coding		Straight natural binary Twos complement			Coding bit set to 1 in control register Coding bit set to 0 in control register

Parameter ¹	B Version			Unit	Test Conditions/Comments
	Min	Typ	Max		
CONVERSION RATE					
Conversion Time			800	ns	16 SCLK cycles with SCLK = 20 MHz
Track-and-Hold Acquisition Time ^{2,3}			300	ns	Full-scale step input; see the Terminology section
Throughput Rate			1 770	MSPS kSPS	V _{CC} = 4.75 V to 5.25 V; see the Serial Interface section V _{CC} < 4.75 V
POWER REQUIREMENTS					Digital inputs = 0 V or V _{DRIVE}
V _{DD}	12		16.5	V	See Table 6
V _{SS}	−12		−16.5	V	See Table 6
V _{CC}	2.7		5.25	V	See Table 6; typical specifications for V _{CC} < 4.75 V
V _{DRIVE}	2.7		5.25	V	
Normal Mode (Static)		0.9		mA	V _{DD} = 16.5, V _{SS} = −16.5 V, V _{CC} = V _{DRIVE} = 5.25 V
Normal Mode (Operational)					f _S = 1 MSPS
I _{DD}			360	μA	V _{DD} = 16.5 V
I _{SS}			410	μA	V _{SS} = −16.5 V
I _{CC} and I _{DRIVE}			3.4	mA	V _{CC} = V _{DRIVE} = 5.25 V
Autostandby Mode (Dynamic)					f _S = 250 kSPS
I _{DD}			200	μA	V _{DD} = 16.5 V
I _{SS}			210	μA	V _{SS} = −16.5 V
I _{CC} and I _{DRIVE}			1.3	mA	V _{CC} = V _{DRIVE} = 5.25 V
Autoshutdown Mode (Static)					SCLK on or off
I _{DD}			1	μA	V _{DD} = 16.5 V
I _{SS}			1	μA	V _{SS} = −16.5 V
I _{CC} and I _{DRIVE}			1	μA	V _{CC} = V _{DRIVE} = 5.25 V
Full Shutdown Mode					SCLK on or off
I _{DD}			1	μA	V _{DD} = 16.5 V
I _{SS}			1	μA	V _{SS} = −16.5 V
I _{CC} and I _{DRIVE}			1	μA	V _{CC} = V _{DRIVE} = 5.25 V
POWER DISSIPATION					
Normal Mode (Operational)			31	mW	V _{DD} = 16.5 V, V _{SS} = −16.5 V, V _{CC} = 5.25 V
		21		mW	V _{DD} = 12 V, V _{SS} = −12 V, V _{CC} = 5 V
Full Shutdown Mode			38.25	μW	V _{DD} = 16.5 V, V _{SS} = −16.5 V, V _{CC} = 5.25 V

¹ Temperature range is −40°C to +85°C.² See the Terminology section.³ Sample tested during initial release to ensure compliance.⁴ For dc accuracy specifications, the LSB size for differential mode is FSR/8192. For single-ended mode/pseudo differential mode, the LSB size is FSR/4096, unless otherwise noted.⁵ Unipolar 0 V to 10 V range with straight binary output coding.⁶ Bipolar range with twos complement output coding.

TIMING SPECIFICATIONS

$V_{DD} = 12\text{ V to }16.5\text{ V}$, $V_{SS} = -12\text{ V to }-16.5\text{ V}$, $V_{CC} = 4.75\text{ V to }5.25\text{ V}$, $V_{DRIVE} = 2.7\text{ V to }5.25\text{ V}$, $V_{REF} = 2.5\text{ V}$ internal/external, $T_A = T_{MAX}$ to T_{MIN} . Timing specifications apply with a 32 pF load, unless otherwise noted. MUX_{OUT+} is connected directly to ADC_{IN+} and MUX_{OUT-} is connected directly to ADC_{IN-} , which is connected to AGND for single-ended mode.

Table 3.

Parameter	Limit at T_{MIN} , T_{MAX}		Unit	Description $V_{DRIVE} \leq V_{CC}$
	$V_{CC} < 4.75\text{ V}$	$V_{CC} = 4.75\text{ V to }5.25\text{ V}$		
f_{SCLK}	50	50	kHz min	
	14	20	MHz max	
$t_{CONVERT}$	$16 \times t_{SCLK}$	$16 \times t_{SCLK}$	ns max	$t_{SCLK} = 1/f_{SCLK}$
t_{QUIET}	75	60	ns min	Minimum time between end of serial read and next falling edge of $\overline{CS}$
t_1	12	5	ns min	Minimum $\overline{CS}$ pulse width
t_2^1	25	20	ns min	$\overline{CS}$ to SCLK setup time; bipolar input ranges ($\pm 10\text{ V}$, $\pm 5\text{ V}$, $\pm 2.5\text{ V}$)
	45	35	ns min	Unipolar input range (0 V to 10 V)
t_3	26	14	ns max	Delay from $\overline{CS}$ until DOUT three-state disabled
t_4	57	43	ns max	Data access time after SCLK falling edge
t_5	$0.4 \times t_{SCLK}$	$0.4 \times t_{SCLK}$	ns min	SCLK low pulse width
t_6	$0.4 \times t_{SCLK}$	$0.4 \times t_{SCLK}$	ns min	SCLK high pulse width
t_7	13	8	ns min	SCLK to data valid hold time
t_8	40	22	ns max	SCLK falling edge to DOUT high impedance
	10	9	ns min	SCLK falling edge to DOUT high impedance
t_9	4	4	ns min	DIN setup time prior to SCLK falling edge
t_{10}	2	2	ns min	DIN hold time after SCLK falling edge
$t_{POWER-UP}$	750	750	ns max	Power-up from autostandby
	500	500	μs max	Power-up from full shutdown/autoshtutdown mode, internal reference
	25	25	μs typ	Power-up from full shutdown/autoshtutdown mode, external reference

¹ When using $V_{CC} = 4.75\text{ V to }5.25\text{ V}$ and the 0 V to 10 V unipolar range, running at 1 MSPS throughput rate with t_2 at 20 ns, the mark-space ratio must be limited to 50:50.

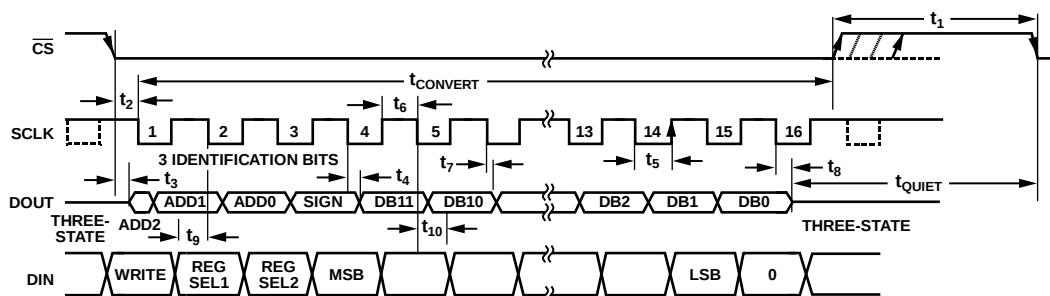


Figure 2. Serial Interface Timing Diagram

05-402-002

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to AGND, DGND	$-0.3\text{ V to }+16.5\text{ V}$
V_{SS} to AGND, DGND	$+0.3\text{ V to }-16.5\text{ V}$
V_{DD} to V_{CC}	$V_{CC} - 0.3\text{ V to }+16.5\text{ V}$
V_{CC} to AGND, DGND	$-0.3\text{ V to }+7\text{ V}$
V_{DRIVE} to AGND, DGND	$-0.3\text{ V to }+7\text{ V}$
AGND to DGND	$-0.3\text{ V to }+0.3\text{ V}$
Analog Input Voltage to AGND ¹	$V_{SS} - 0.3\text{ V to }V_{DD} + 0.3\text{ V}$
Digital Input Voltage to DGND	$-0.3\text{ V to }+7\text{ V}$
Digital Output Voltage to GND	$-0.3\text{ V to }V_{DRIVE} + 0.3\text{ V}$
REF_{IN} to AGND	$-0.3\text{ V to }V_{CC} + 0.3\text{ V}$
Input Current to Any Pin Except Supplies ²	$\pm 10\text{ mA}$
Operating Temperature Range	$-40^\circ\text{C to }+85^\circ\text{C}$
Storage Temperature Range	$-65^\circ\text{C to }+150^\circ\text{C}$
Junction Temperature	150°C
TSSOP Package	
θ_{JA} Thermal Impedance	128°C/W
θ_{JC} Thermal Impedance	42°C/W
Pb-Free Temperature, Soldering	
Reflow	$260(0)^\circ\text{C}$
ESD	2.5 kV

¹ If the analog inputs are driven from alternative V_{DD} and V_{SS} supply circuitry, Schottky diodes should be placed in series with the V_{DD} and V_{SS} supplies of the AD7329 (see the Power Supply Configuration section).

² Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

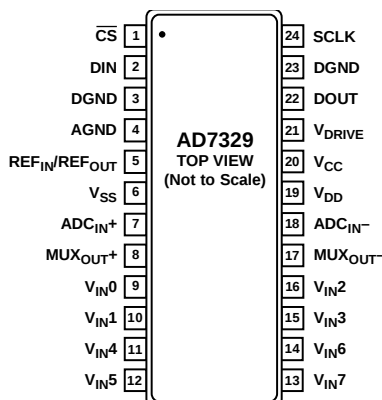


Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Descriptions
1	CS	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7329 and frames the serial data transfer.
2	DIN	Data In. Data to be written to the on-chip registers is provided on this input and is clocked into the register on the falling edge of SCLK (see the Registers section).
3, 23	DGND	Digital Ground. Ground reference point for all digital circuitry on the AD7329. Ideally, the DGND and AGND voltages are at the same potential and must not be more than 0.3 V apart, even on a transient basis.
4	AGND	Analog Ground. Ground reference point for all analog circuitry on the AD7329. All analog input signals and any external reference signal must be referred to this AGND voltage. Ideally, the AGND and DGND voltages are at the same potential and must not be more than 0.3 V apart, even on a transient basis.
5	REF _{IN} /REF _{OUT}	Reference Input/Reference Output. The on-chip reference is available on this pin for use external to the AD7329. The nominal internal reference voltage is 2.5 V, which appears at the pin. A 680 nF capacitor must be placed on the reference pin. Alternatively, the internal reference can be disabled and an external reference can be applied to this input. On power-up, the external reference mode is the default condition (see the Reference section).
6	V _{SS}	Negative Power Supply Voltage. This is the negative supply voltage for the analog input section.
7	ADC _{IN} +	Positive ADC Input. This pin allows access to the on-chip track-and-hold. The voltage applied to this pin is still a high voltage signal (± 10 V, ± 5 V, ± 2.5 V, or 0 V to +10 V).
8	MUX _{OUT} +	Positive Multiplexer Output. The output of the multiplexer appears at this pin. The voltage at this pin is still a high voltage signal equivalent to the voltage applied to the V _{IN} + input channel, as selected in the control register or sequence register. If no external filtering or buffering is required, tie this pin to the ADC _{IN} + pin.
9, 10, 16, 15, 11, 12, 14, 13	V _{IN} 0 to V _{IN} 7	Analog Input 0 Through Analog Input 7. The analog inputs are multiplexed into the on-chip track-and-hold. The analog input channel for conversion is selected by programming the channel address bits, ADD2 through ADD0, in the control register. The inputs can be configured as eight single-ended inputs, four true differential input pairs, four pseudo differential inputs, or seven pseudo differential inputs. The configuration of the analog inputs is selected by programming the mode bits, Mode 1 and Mode 0, in the control register. The input range on each input channel is controlled by programming the range registers. Input ranges of ± 10 V, ± 5 V, ± 2.5 V, or 0 V to +10 V can be selected on each analog input channel (see the Range Registers section). On power-up, V _{IN} 0 is automatically selected and the voltage on this pin appears on MUX _{OUT} +
17	MUX _{OUT} -	Negative Multiplexer Output. This pin allows access to the on-chip track-and-hold. The voltage applied to this pin is still a high voltage signal when the AD7329 is in differential mode. In single-ended mode, this pin can either be left floating or tied to AGND. When the AD7329 is in pseudo differential mode, a small dc voltage appears at this pin, and this pin is tied to the ADC _{IN} - pin.
18	ADC _{IN} -	Negative ADC Input. This pin allows access to the track-and-hold. When the AD7329 is in single-ended mode, tie this pin to AGND. When the AD7329 is in pseudo differential mode, connect this pin to MUX _{OUT} -. When the AD7329 is in true differential mode, the voltage applied to this pin is a high voltage signal (± 10 V, ± 5 V, ± 2.5 V, or 0 V to +10 V).
19	V _{DD}	Positive Power Supply Voltage. This is the positive supply voltage for the analog input section.
20	V _{CC}	Analog Supply Voltage, 2.7 V to 5.25 V. This is the supply voltage for the ADC core on the AD7329. Decouple this supply to AGND.

Pin No.	Mnemonic	Descriptions
21	V _{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the interface operates. Decouple this pin to DGND. The voltage at this pin can be different than that at V _{CC} but must not exceed V _{CC} by more than 0.3 V.
22	DOUT	Serial Data Output. The conversion output data is supplied to this pin as a serial data stream. The bits are clocked out on the falling edge of the SCLK input, and 16 SCLKs are required to access the data. The data stream consists of three channel identification bits, the sign bit, and 12 bits of conversion data. The data is provided MSB first (see the Serial Interface section).
24	SCLK	Serial Clock, Logic Input. A serial clock input provides the SCLK used for accessing the data from the AD7329 . This clock is also used as the clock source for the conversion process.

TYPICAL PERFORMANCE CHARACTERISTICS

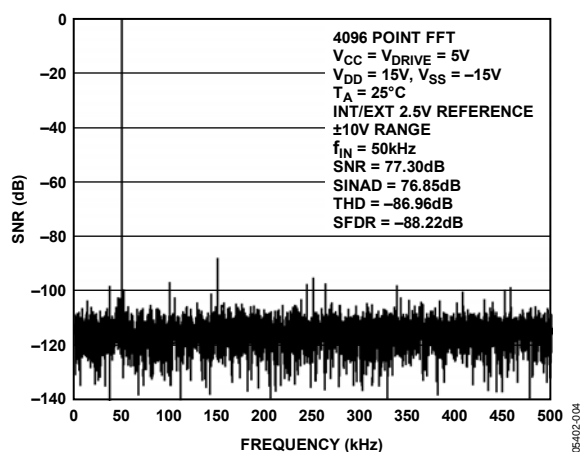


Figure 4. FFT for True Differential Mode

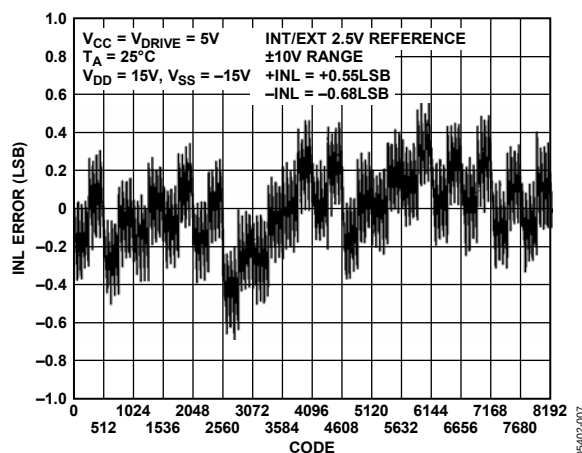


Figure 7. Typical INL for True Differential Mode

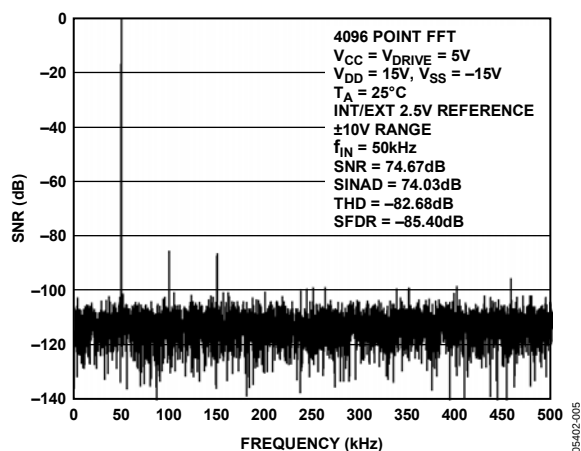


Figure 5. FFT for Single-Ended Mode

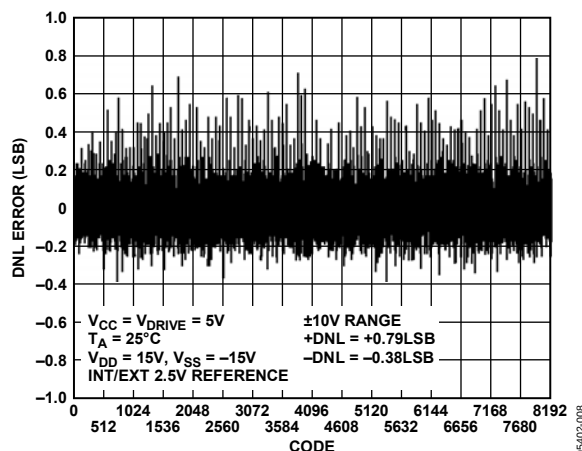


Figure 8. Typical DNL for Single-Ended Mode

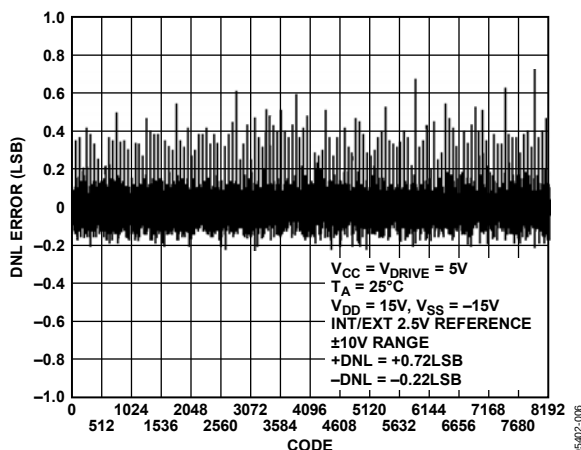


Figure 6. Typical DNL for True Differential Mode

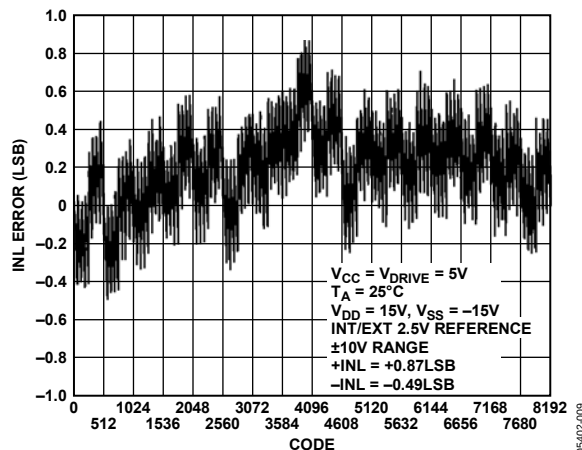


Figure 9. Typical INL for Single-Ended Mode

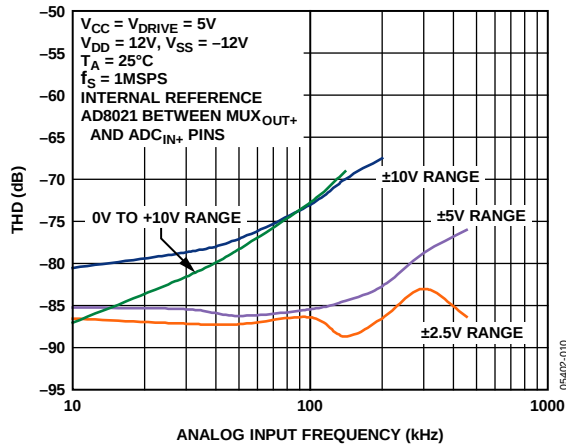
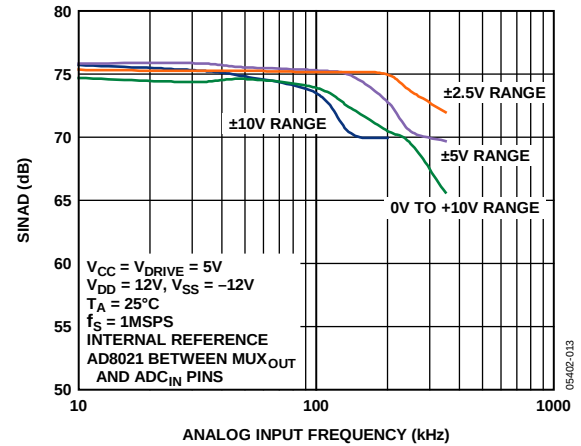
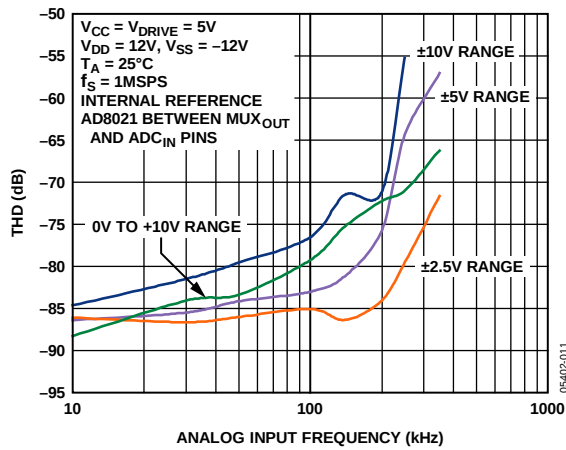
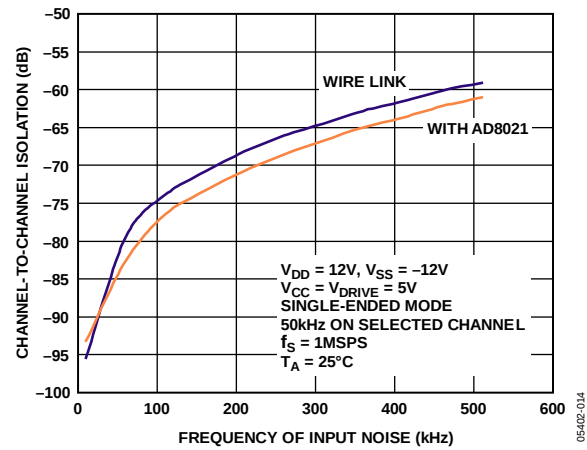
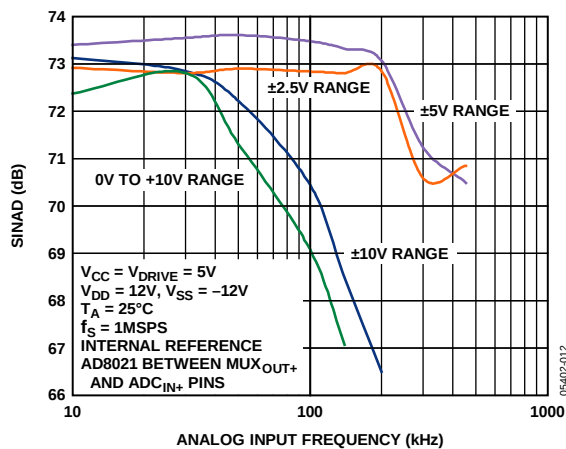
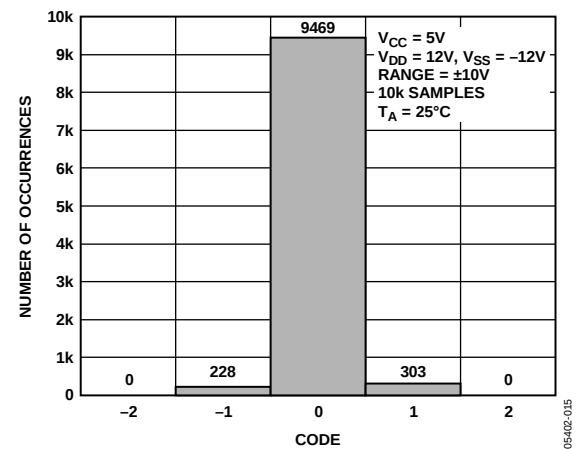
Figure 10. THD vs. Analog Input Frequency for Single-Ended Mode at 5 V V_{CC} Figure 13. SINAD vs. Analog Input Frequency for True Differential Mode at 5 V V_{CC} Figure 11. THD vs. Analog Input Frequency for True Differential Mode at 5 V V_{CC} Figure 14. Channel-to-Channel Isolation with and Without AD8021 Between the MUX_{OUT+} and ADC_{IN+} PinsFigure 12. SINAD vs. Analog Input Frequency for Single-Ended Mode at 5 V V_{CC} 

Figure 15. Histogram of Codes, True Differential Mode

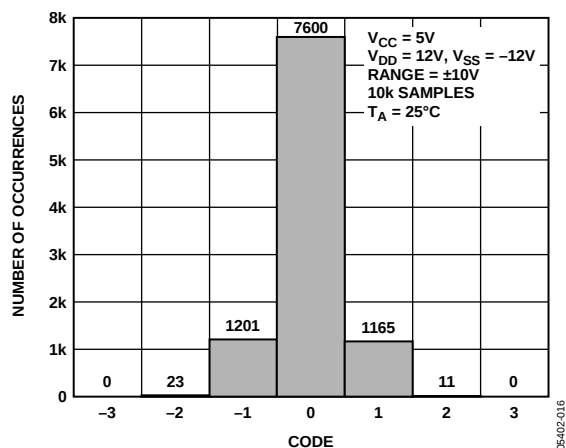


Figure 16. Histogram of Codes, Single-Ended Mode

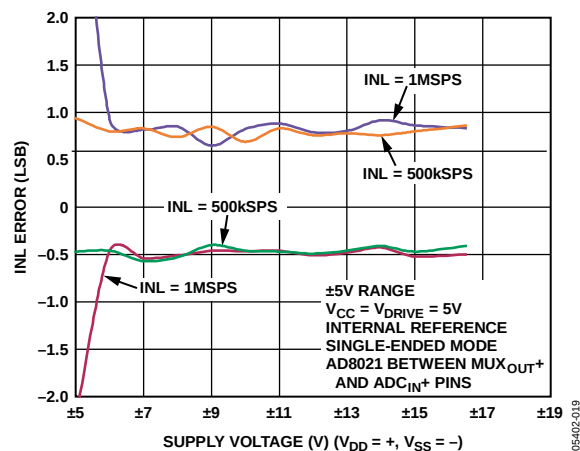


Figure 19. INL Error vs. Supply Voltage at 500 kSPS and 1 MSPS

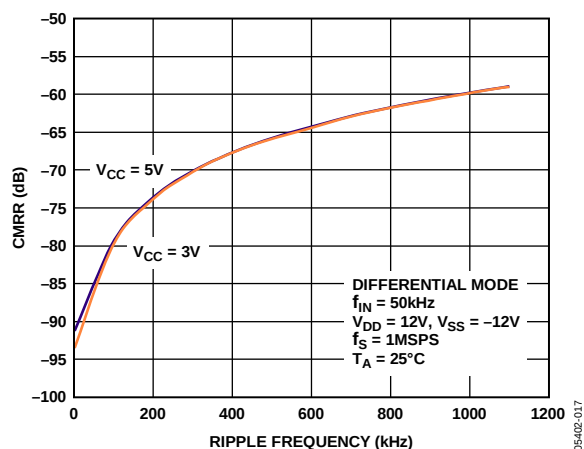


Figure 17. CMRR vs. Common-Mode Ripple Frequency

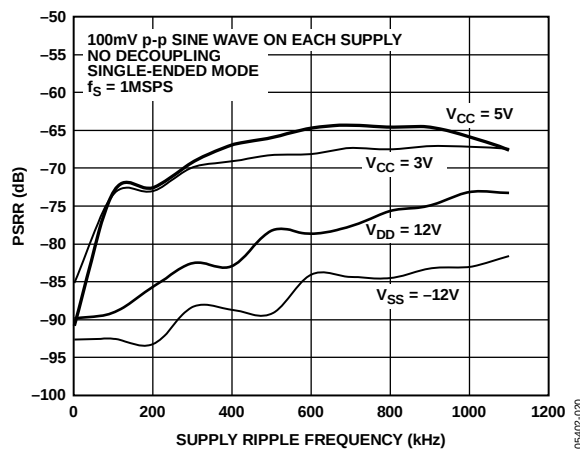


Figure 20. PSRR vs. Supply Ripple Frequency Without Supply Decoupling

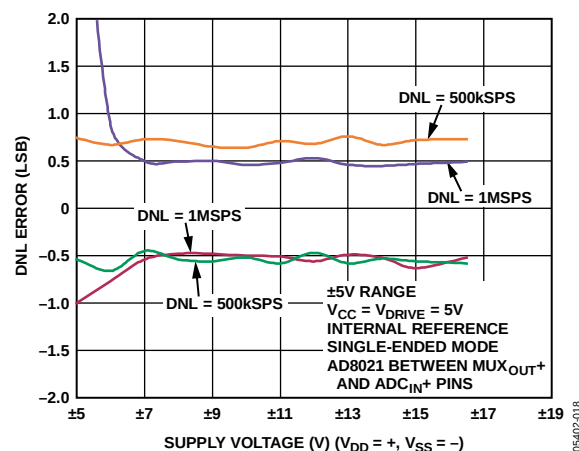


Figure 18. DNL Error vs. Supply Voltage at 500 kSPS and 1 MSPS

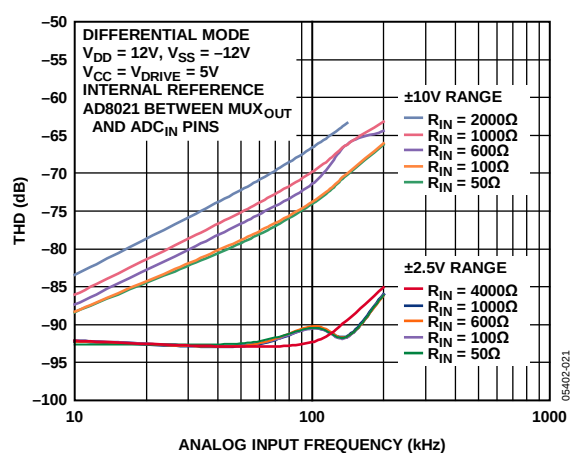


Figure 21. THD vs. Analog Input Frequency for Various Source Impedances, True Differential Mode

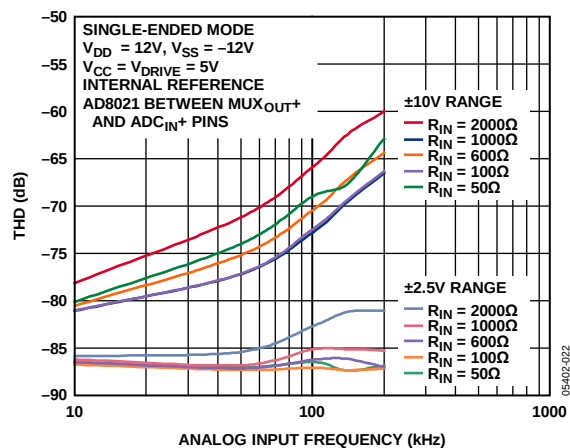


Figure 22. THD vs. Analog Input Frequency for Various Source Impedances, Single-Ended Mode

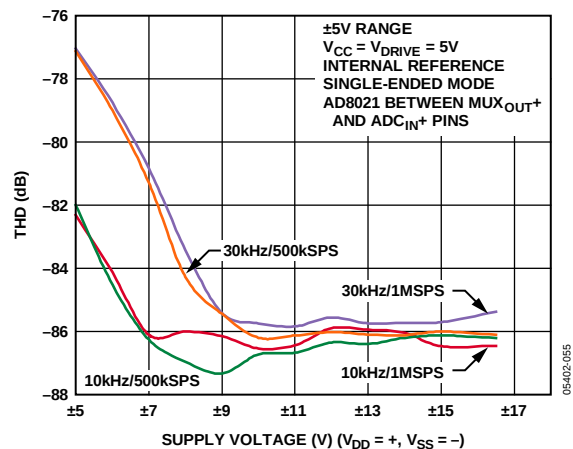


Figure 23. THD vs. Supply Voltage at 500 kSPS and 1 MSPS with 10 kHz and 30 kHz Input Tone

TERMINOLOGY

Differential Nonlinearity

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Integral Nonlinearity

This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale (a point 1 LSB below the first code transition) and full scale (a point 1 LSB above the last code transition).

Offset Error

This applies to straight binary output coding. It is the deviation of the first code transition (00 ... 000) to (00 ... 001) from the ideal, that is, AGND + 1 LSB.

Offset Error Match

This is the difference in offset error between any two input channels.

Gain Error

This applies to straight binary output coding. It is the deviation of the last code transition (111 ... 110) to (111 ... 111) from the ideal (that is, $4 \times V_{REF} - 1$ LSB, $2 \times V_{REF} - 1$ LSB, $V_{REF} - 1$ LSB) after adjusting for the offset error.

Gain Error Match

This is the difference in gain error between any two input channels.

Bipolar Zero Code Error

This applies when using twos complement output coding and a bipolar analog input. It is the deviation of the midscale transition (all 1s to all 0s) from the ideal input voltage, that is, AGND – 1 LSB.

Bipolar Zero Code Error Match

This refers to the difference in bipolar zero code error between any two input channels.

Positive Full-Scale Error

This applies when using twos complement output coding and any of the bipolar analog input ranges. It is the deviation of the last code transition (011 ... 110) to (011 ... 111) from the ideal (that is, $4 \times V_{REF} - 1$ LSB, $2 \times V_{REF} - 1$ LSB, $V_{REF} - 1$ LSB) after adjusting for the bipolar zero code error.

Positive Full-Scale Error Match

This is the difference in positive full-scale error between any two input channels.

Negative Full-Scale Error

This applies when using twos complement output coding and any of the bipolar analog input ranges. This is the deviation of the first code transition (10 ... 000) to (10 ... 001) from the ideal (that is, $-4 \times V_{REF} + 1$ LSB, $-2 \times V_{REF} + 1$ LSB, $-V_{REF} + 1$ LSB) after adjusting for the bipolar zero code error.

Negative Full-Scale Error Match

This is the difference in negative full-scale error between any two input channels.

Track-and-Hold Acquisition Time

The track-and-hold amplifier returns to track mode after the 14th SCLK rising edge. Track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within $\pm \frac{1}{2}$ LSB, after the end of a conversion.

Signal-to-Noise-and-Distortion Ratio

This is the measured ratio of signal to (noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_s/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process. The more levels, the smaller the quantization noise. Theoretically, the signal-to-noise-and-distortion ratio for an ideal N-bit converter with a sine wave input is given by

$$\text{Signal to (Noise + Distortion)} = (6.02 N + 1.76) \text{ dB}$$

For a 13-bit converter, this is 80.02 dB.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the [AD7329](#), it is defined as

$$\text{THD (dB)} = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental, and V_2 , V_3 , V_4 , V_5 , and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_s/2$, excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, the largest harmonic could be a noise peak.

Channel-to-Channel Isolation

Channel-to-channel isolation is a measure of the level of crosstalk between any two channels. It is measured by applying a full-scale, 100 kHz sine wave signal to all unselected input channels and determining the degree to which the signal attenuates in the selected channel with a 50 kHz signal. Figure 14 shows the worst case across all eight channels for the AD7329. The analog input range is programmed to be ± 2.5 V on the selected channel and ± 10 V on all other channels.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, f_a and f_b , any active device with nonlinearities creates distortion products at sum and difference frequencies of $m f_a \pm n f_b$, where $m, n = 0, 1, 2, 3$, and so on. Intermodulation distortion terms are those for which neither m nor n are equal to 0. For example, the second-order terms include $(f_a + f_b)$ and $(f_a - f_b)$, whereas the third-order terms include $(2f_a + f_b)$, $(2f_a - f_b)$, $(f_a + 2f_b)$, and $(f_a - 2f_b)$.

The AD7329 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves, whereas the third-order

terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in decibels.

Power Supply Rejection (PSR)

Variations in power supply affect the full-scale transition but not the linearity of the converter. Power supply rejection is the maximum change in the full-scale transition point due to a change in power supply voltage from the nominal value (see the Typical Performance Characteristics section).

Common-Mode Rejection Ratio (CMRR)

CMRR is defined as the ratio of the power in the ADC output at full-scale frequency, f , to the power of a 100 mV sine wave applied to the common-mode voltage of the V_{IN+} and V_{IN-} frequency, f_s , as

$$CMRR \text{ (dB)} = 10 \log (P_f / P_{f_s})$$

where P_f is the power at frequency f in the ADC output, and P_{f_s} is the power at frequency f_s in the ADC output (see Figure 17).

THEORY OF OPERATION

CIRCUIT INFORMATION

The AD7329 is a fast, 8-channel, 12-bit plus sign, bipolar input, serial ADC. The AD7329 can accept bipolar input ranges that include ± 10 V, ± 5 V, and ± 2.5 V; it can also accept a 0 V to $+10$ V unipolar input range. A different analog input range can be programmed on each analog input channel via the on-chip registers. The AD7329 has a high speed serial interface that can operate at throughput rates up to 1 MSPS.

The AD7329 requires V_{DD} and V_{SS} dual supplies for the high voltage analog input structures. These supplies must be equal to or greater than the analog input range. See Table 6 for the requirements of these supplies for each analog input range. The AD7329 requires a low voltage 2.7 V to 5.25 V V_{CC} supply to power the ADC core.

Table 6. Reference and Supply Requirements for Each Analog Input Range

Selected Analog Input Range (V)	Reference Voltage (V)	Full-Scale Input Range (V)	V_{CC} (V)	Minimum V_{DD}/V_{SS} (V) ¹
± 10	2.5	± 10	3/5	± 10
	3.0	± 12	3/5	± 12
± 5	2.5	± 5	3/5	± 5
	3.0	± 6	3/5	± 6
± 2.5	2.5	± 2.5	3/5	± 5
	3.0	± 3	3/5	± 5
0 to $+10$	2.5	0 to $+10$	3/5	$+10/\text{AGND}$
	3.0	0 to $+12$	3/5	$+12/\text{AGND}$

¹ Guaranteed performance for $V_{DD} = 12$ V to 16.5 V and $V_{SS} = -12$ V to -16.5 V.

The performance specifications are guaranteed for $V_{DD} = 12$ V to 16.5 V and $V_{SS} = -12$ V to -16.5 V. With V_{DD} and V_{SS} supplies outside this range, the AD7329 is fully functional but performance is not guaranteed. When the AD7329 is configured with the minimum V_{DD} and V_{SS} supplies for a chosen analog input range, the throughput rate should be decreased from the maximum throughput range (see the Typical Performance Characteristics section). Figure 18 and Figure 19 show the change in INL and DNL as the V_{DD} and V_{SS} voltages are varied. When operating at the maximum throughput rate, as the V_{DD} and V_{SS} supply voltages are reduced, the INL and DNL error increases. However, as the throughput rate is reduced with the minimum V_{DD} and V_{SS} supplies, the INL and DNL error is reduced.

Figure 23 shows the change in THD as the V_{DD} and V_{SS} supplies are reduced. At the maximum throughput rate, the THD degrades significantly as V_{DD} and V_{SS} are reduced. It is therefore necessary to reduce the throughput rate when using minimum V_{DD} and V_{SS} supplies so that there is less degradation of THD and the specified performance can be maintained. The degradation is due to an increase in the on resistance of the input multiplexer when the V_{DD} and V_{SS} supplies are reduced.

The analog inputs can be configured as eight single-ended inputs, four true differential input pairs, four pseudo differential inputs, or seven pseudo differential inputs. Selection can be made by programming the mode bits, Mode 0 and Mode 1, in the control register.

The serial clock input accesses data from the part and provides the clock source for the successive approximation ADC. The AD7329 has an on-chip 2.5 V reference. However, the AD7329 can also work with an external reference. On power-up, the external reference operation is the default option. If the internal reference is the preferred option, the user must write to the reference bit in the control register to select the internal reference operation.

The AD7329 also features power-down options to allow power savings between conversions. The power-down modes are selected by programming the on-chip control register as described in the Modes of Operation section.

CONVERTER OPERATION

The AD7329 is a successive approximation analog-to-digital converter built around two capacitive DACs. Figure 24 and Figure 25 show simplified schematics of the ADC in single-ended mode during the acquisition and conversion phases, respectively. Figure 26 and Figure 27 show simplified schematics of the ADC in differential mode during acquisition and conversion phases, respectively. In both examples, the $\text{MUX}_{\text{OUT}+}$ pin is connected to the $\text{ADC}_{\text{IN}+}$ pin, and the $\text{MUX}_{\text{OUT}-}$ pin is connected to the $\text{ADC}_{\text{IN}-}$ pin. The ADC is composed of control logic, a SAR, and capacitive DACs. In Figure 24 (the acquisition phase), SW2 is closed and SW1 is in Position A, the comparator is held in a balanced condition, and the sampling capacitor array acquires the signal on the input.

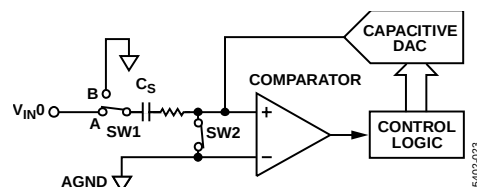


Figure 24. ADC Configuration During Acquisition Phase, Single-Ended Mode

When the ADC starts a conversion (Figure 25), SW2 opens and SW1 moves to Position B, causing the comparator to become unbalanced. The control logic and the charge redistribution DAC are used to add and subtract fixed amounts of charge from the capacitive DAC to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code.

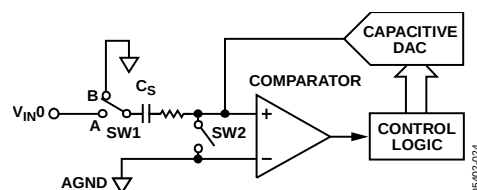
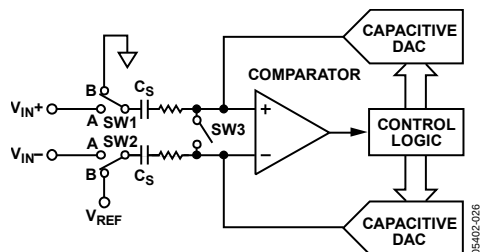


Figure 25. ADC Configuration During Conversion Phase, Single-Ended Mode

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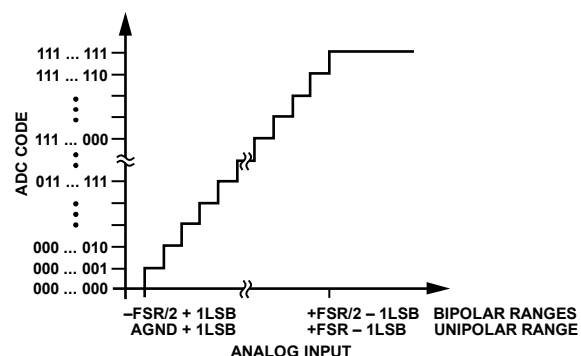
05402-026

The [AD7329](#) default output coding is set to two's complement. The output coding is controlled by the coding bit in the control register. To change the output coding to straight binary coding, the coding bit in the control register must be set. When operating in sequence mode, the output coding for each channel in the sequence is the value written to the coding bit during the last write to the control register.

The designed code transitions occur at successive integer LSB values (that is, 1 LSB, 2 LSB, and so on). The LSB size is dependent on the analog input range selected.

Input Range	Full-Scale Range/8192 Codes	LSB Size
±10 V	20 V	2.441 mV
±5 V	10 V	1.22 mV
±2.5 V	5 V	0.61 mV
0 V to +10 V	10 V	1.22 mV

CS



Summary

The analog inputs of the [AD7329](#) can be configured as single-ended, true differential, or pseudo differential via the control register mode bits, as shown in Table 12. The [AD7329](#) can accept true bipolar input signals. On power-up, the analog inputs operate as eight single-ended analog input channels. If true differential or pseudo differential is required, a write to the control register is necessary after power-up to change this configuration.

The schematic diagram illustrates the input circuit of the proposed ADC. It features an input signal V_{IN0} connected to a node D via a capacitor $C1$. Node D is also connected to V_{DD} and V_{SS} through two diodes. A switch labeled MUX_{OUT+} connects node D to another node, ADC_{IN+} . This second node is connected to ground through a capacitor $C3$ and to a switch labeled ADC_{IN+} through a capacitor $C4$. The output of the ADC_{IN+} switch is connected to a resistor $R1$ and a capacitor $C2$ to ground.

TYPICAL CONNECTION DIAGRAM

Figure 34 shows a typical connection diagram for the AD7329. In this configuration, the AGND pin is connected to the analog ground plane of the system, and the DGND pin is connected to the digital ground plane of the system. The analog inputs on the AD7329 can be configured to operate in single-ended, true differential, or pseudo differential mode. The AD7329 can operate with either an internal or external reference. In Figure 34, the AD7329 is configured to operate with the internal 2.5 V reference. A 680 nF decoupling capacitor is required when operating with the internal reference.

The V_{CC} pin can be connected to either a 3 V or a 5 V supply voltage. The V_{DD} and V_{SS} are the dual supplies for the high voltage analog input structures. The voltage on these pins must be equal to or greater than the highest analog input range selected on the analog input channels (see Table 6 for more information). The V_{DRIVE} pin is connected to the supply voltage of the microprocessor. The voltage applied to the V_{DRIVE} input controls the voltage of the serial interface.

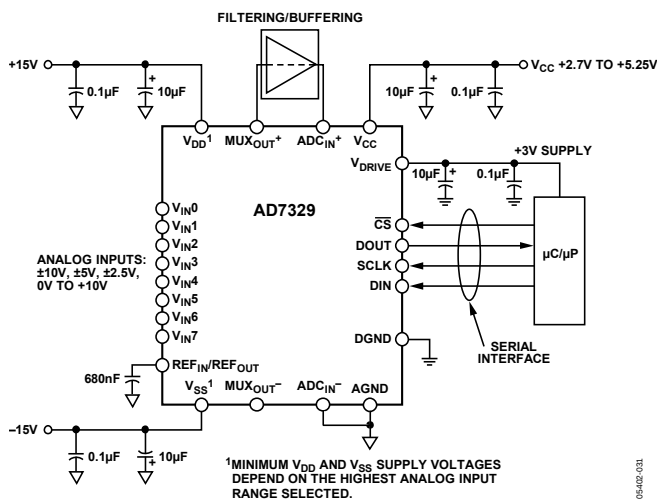


Figure 34. Typical Connection Diagram, Single-Ended Mode

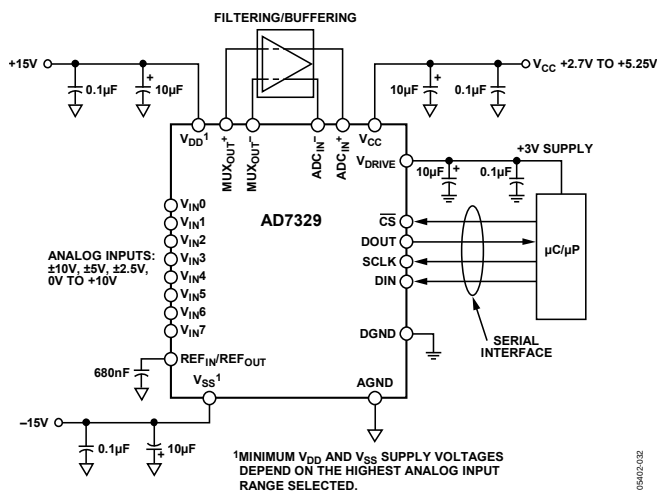
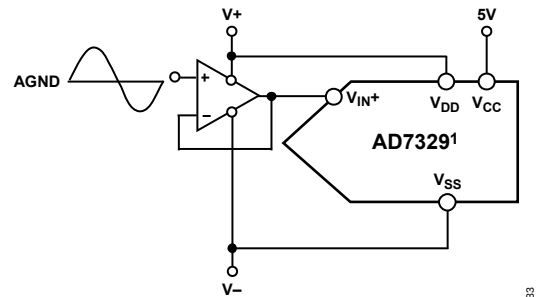


Figure 35. Typical Connection Diagram, Differential Mode

ANALOG INPUT

Single-Ended Inputs

The AD7329 has a total of eight analog inputs when operating in single-ended mode. Each analog input can be independently programmed to one of the four analog input ranges. In applications where the signal source is high impedance, it is recommended to buffer the signal before applying it to the ADC analog inputs. Figure 36 shows the configuration of the AD7329 in single-ended mode.

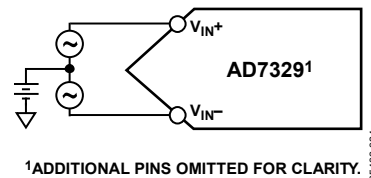


¹ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 36. Single-Ended Mode Typical Connection Diagram

True Differential Mode

The AD7329 can have four true differential analog input pairs. Differential signals have some benefits over single-ended signals, including better noise immunity based on the device's common-mode rejection and improvements in distortion performance. Figure 37 defines the configuration of the true differential analog inputs of the AD7329.



¹ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 37. True Differential Inputs

The amplitude of the differential signal is the difference between the signals applied to the V_{IN+} and V_{IN-} pins in each differential pair (V_{IN+} - V_{IN-}). V_{IN+} and V_{IN-} should be simultaneously driven by two signals of equal amplitude, dependent on the input range selected, that are 180° out of phase. Assuming the $\pm 4 \times V_{REF}$ mode, the amplitude of the differential signal is -20 V to +20 V p-p ($2 \times 4 \times V_{REF}$), regardless of the common mode.

The common mode is the average of the two signals

$$(V_{IN+} + V_{IN-})/2$$

and is therefore the voltage on which the two input signals are centered.

This voltage is set up externally, and its range varies with reference voltage. As the reference voltage increases, the common-mode range decreases. When the differential inputs are driven with an amplifier, the actual common-mode range is determined by the amplifier's output swing. If the differential inputs are not driven from an amplifier, the common-mode range is determined by the supply voltage on the V_{DD} supply pin and the V_{SS} supply pin.

When a conversion takes place, the common mode is rejected, resulting in a noise-free signal of amplitude $-2 \times (4 \times V_{REF})$ to $+2 \times (4 \times V_{REF})$, corresponding to Digital Codes -4096 to $+4095$.

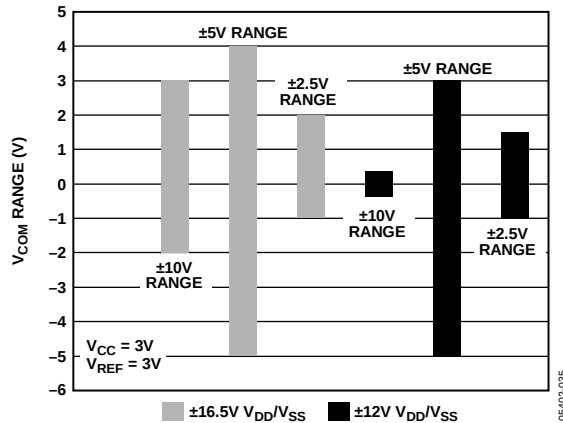


Figure 38. Common-Mode Range for $V_{CC} = 3V$ and $REF_{IN}/REF_{OUT} = 3V$

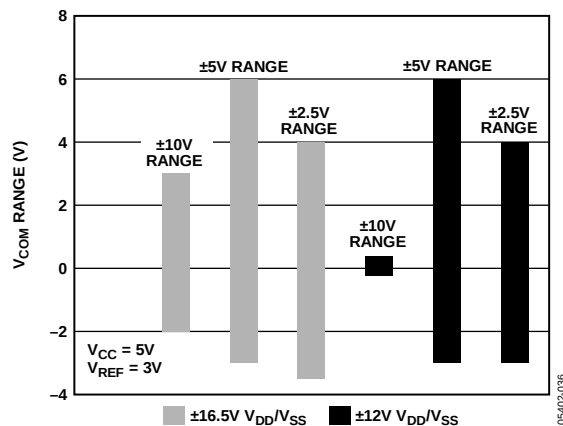


Figure 39. Common-Mode Range for $V_{CC} = 5V$ and $REF_{IN}/REF_{OUT} = 3V$

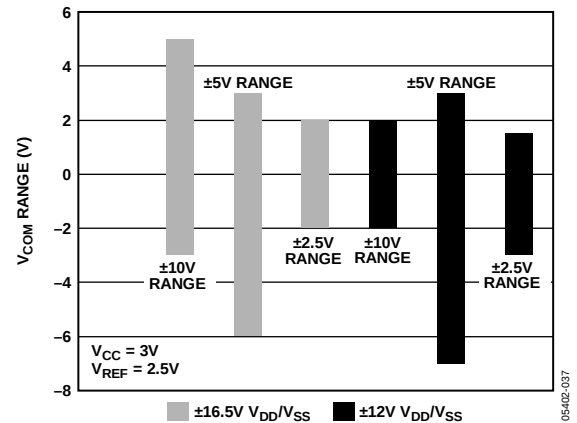


Figure 40. Common-Mode Range for $V_{CC} = 3V$ and $REF_{IN}/REF_{OUT} = 2.5V$

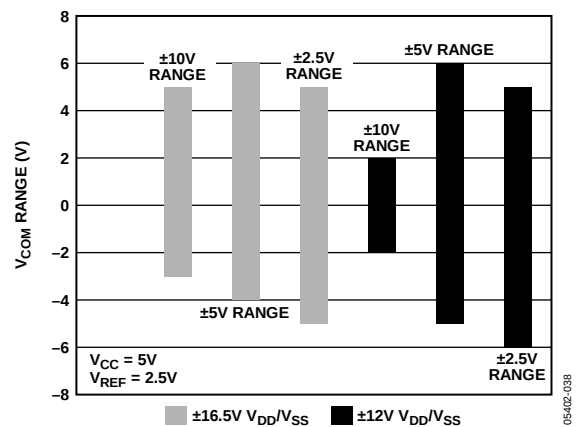


Figure 41. Common-Mode Range for $V_{CC} = 5V$ and $REF_{IN}/REF_{OUT} = 2.5V$

Pseudo Differential Inputs

The AD7329 can have four pseudo differential pairs or seven pseudo differential inputs referenced to a common V_{IN-} pin. The V_{IN+} inputs are coupled to the signal source and must have an amplitude within the selected range for that channel, as programmed in the range register. A dc input is applied to the V_{IN-} pin. The voltage applied to this input provides an offset for the V_{IN+} input from ground or pseudo ground. Pseudo differential inputs separate the analog input signal ground from the ADC ground, allowing cancellation of dc common-mode voltages. Figure 42 shows the configuration of the AD7329 in pseudo differential mode.

See Figure 28 and Figure 29 for the output transfer characteristic when a conversion takes place.

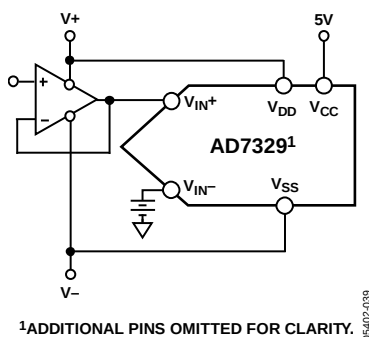


Figure 42. Pseudo Differential Inputs

Figure 43 and Figure 44 show the typical voltage range on the V_{IN-} pin for various analog input ranges when configured in the pseudo differential mode.

For example, when the AD7329 is configured to operate in pseudo differential mode and the ± 5 V range is selected with 16.5 V V_{DD} , -16.5 V V_{SS} , and 5 V V_{CC} , the voltage on the V_{IN-} pin can vary from -6.5 V to +6.5 V.

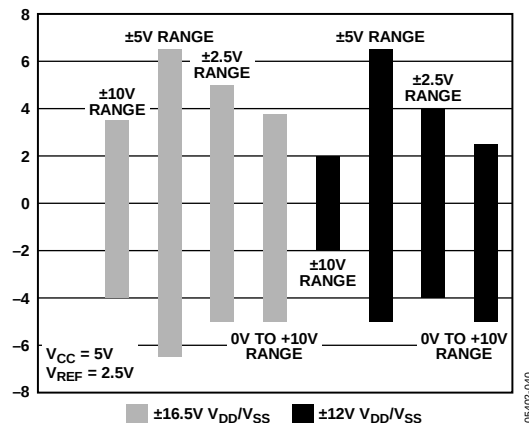


Figure 43. Pseudo Differential Input Range with $V_{CC} = 5$ V

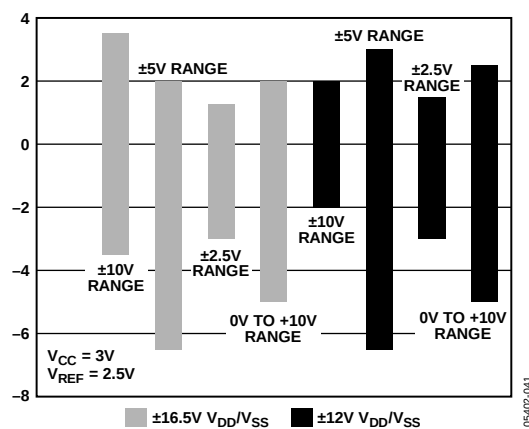


Figure 44. Pseudo Differential Input Range with $V_{CC} = 3$ V

DRIVER AMPLIFIER CHOICE

In applications where the harmonic distortion and signal-to-noise ratio are critical specifications, the analog input of the AD7329 should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC and can necessitate the use of an input buffer amplifier.

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance depends on the amount of THD that can be tolerated in the application. The THD increases as the source impedance increases and performance degrades. Figure 21 and Figure 22 show graphs of the THD vs. the analog input frequency for various source impedances. Depending on the input range and analog input configuration selected, the AD7329 can handle source impedances of up to 4 k Ω before the THD starts to degrade.

Due to the programmable nature of the analog inputs on the AD7329, the choice of op amp used to drive the inputs is a function of the particular application and depends on the input configuration and the analog input voltage ranges selected.

The driver amplifier must be able to settle for a full-scale step to a 13-bit level, within 0.0122%, in less than the specified acquisition time of the AD7329. An op amp such as the AD8021 meets this requirement when operating in single-ended mode. The AD8021 needs an external compensating NPO type of capacitor. The AD8022 can also be used in high frequency applications where a dual version is required. For lower frequency applications, op amps such as the AD797, AD845, and AD8610 can be used with the AD7329 in single-ended mode configuration.

Table 8. Typical AC Performance Using Different Op Amps in Single-Ended Mode, ± 10 V Input Range

Parameter	No Buffer	AD845	AD8021	AD8610
SNR (dB)	74.24	74.03	73.78	73.88
SNRD (dB)	72.42	74.88	72.11	71.98
THD (dB)	-77.05	-75.95	-77.04	-76.47

Table 9. Typical AC Performance Using Different Op Amps in Differential Mode, ± 10 V Input Range

Parameter	No Buffer	AD845	AD8021	AD8610
SNR (dB)	77.16	76.81	76.95	76.76
SNRD (dB)	76.50	76.02	76.78	75.89
THD (dB)	-84.91	-83.74	-90.55	-83.24

Differential operation requires that V_{IN+} and V_{IN-} be simultaneously driven with two signals of equal amplitude that are 180° out of phase. The common mode must be set up externally to the AD7329. The common-mode range is determined by the REF_{IN}/REF_{OUT} voltage, the V_{CC} supply voltage, and the particular amplifier used to drive the analog inputs. Differential mode with either an ac input or a dc input provides the best THD performance over a wide frequency range. Because not all applications have a signal preconditioned for differential operation, there is often a need to perform a single-ended-to-differential conversion.

This single-ended-to-differential conversion can be performed using an op amp pair. Typical connection diagrams for an op amp pair are shown in Figure 45 and Figure 46. In Figure 45, the common-mode signal is applied to the noninverting input of the second amplifier.

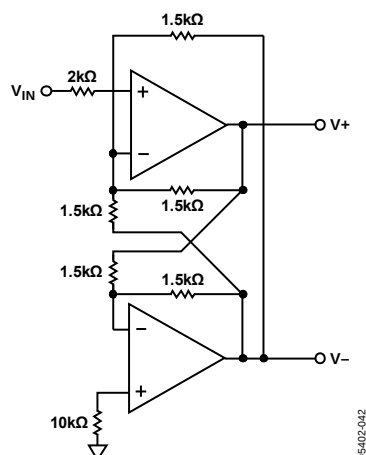


Figure 45. Single-Ended-to-Differential Configuration with the AD845 for Bipolar Operation

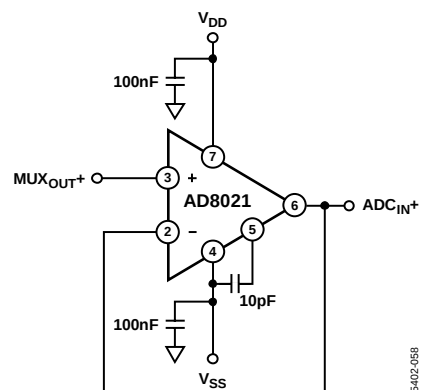


Figure 47. AD8021 Configuration Used Between MUX_OUT and ADC_IN Pins

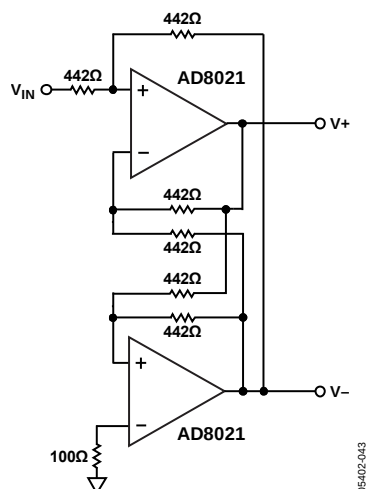


Figure 46. Single-Ended-to-Differential Configuration with the AD8021

REGISTERS

The AD7329 has four programmable registers: the control register, sequence register, Range Register 1, and Range Register 2. These registers are write-only registers.

ADDRESSING REGISTERS

A serial transfer on the AD7329 consists of 16 SCLK cycles. The three MSBs on the DIN line during the 16 SCLK transfer are decoded to determine which register is addressed. The three MSBs consist of the write bit, the Register Select 1 bit, and the Register Select 2 bit. The register select bits are used to determine which of the four on-board registers is selected. The write bit determines if the data on the DIN line following the register select bits loads into the addressed register. If the write bit is 1, the bits load into the register addressed by the register select bits. If the write bit is 0, the data on the DIN line does not load into any register.

Combinations of the write bit, the Register Select 1 bit, and the Register Select 2 bit other than those specified in Table 10 access registers that are for Analog Devices internal use only. Do not access these registers, as doing so may lead to unspecified operation of the device.

Table 10. Decoding Register Select Bits and Write Bit

Write	Register Select 1	Register Select 2	Description
0	0	0	Data on the DIN line during this serial transfer is ignored.
1	0	0	This combination selects the control register. The subsequent 12 bits are loaded into the control register.
1	0	1	This combination selects Range Register 1. The subsequent 8 bits are loaded into Range Register 1.
1	1	0	This combination selects Range Register 2. The subsequent 8 bits are loaded into Range Register 2.
1	1	1	This combination selects the sequence register. The subsequent 8 bits are loaded into the sequence register.

CONTROL REGISTER

The control register is used to select the analog input channel, analog input configuration, reference, coding, and power mode. The control register is a write-only, 12-bit register. Data loaded on the DIN line corresponds to the [AD7329](#) configuration for the next conversion. If the sequence register is being used, data should be loaded into the control register after the range registers and the sequence register have been initialized. The bit functions of the control register are described in Table 11 (the power-up status of all bits is 0).

MSB														LSB	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Register Select 1	Register Select 2	ADD2	ADD1	ADD0	Mode 1	Mode 0	PM1	PM0	Coding	REF	SEQ1	SEQ2	Weak/ Three-State	0

Table 11. Control Register Details

Bit	Mnemonic	Description
12, 11, 10	ADD2, ADD1, ADD0	These three channel address bits are used to select the analog input channel for the next conversion if the sequencer is not being used. If the sequencer is being used, the three channel address bits are used to select the final channel in a consecutive sequence.
9, 8	Mode 1, Mode 0	These two mode bits are used to select the configuration of the eight analog input pins, V_{IN0} to V_{IN7} . These pins are used in conjunction with the channel address bits. On the AD7329 , the analog inputs can be configured as eight single-ended inputs, four fully differential input pairs, four pseudo differential inputs, or seven pseudo differential inputs (see Table 12).
7, 6	PM1, PM0	The power management bits are used to select different power mode options on the AD7329 (see Table 13).
5	Coding	This bit is used to select the type of output coding that the AD7329 uses for the next conversion result. If coding = 0, the output coding is twos complement. If coding = 1, the output coding is straight binary. When operating in sequence mode, the output coding for each channel is the value written to the coding bit during the last write to the control register.
4	REF	The reference bit is used to enable or disable the internal reference. If REF = 0, the external reference is enabled and used for the next conversion and the internal reference is disabled. If REF = 1, the internal reference is used for the next conversion. When operating in sequence mode, the reference used for each channel is the value written to the REF bit during the last write to the control register.
3, 2	SEQ1/SEQ2	The Sequence 1 and Sequence 2 bits are used to control the operation of the sequencer (see Table 14).
1	Weak/Three-State	This bit selects the state of the DOUT line at the end of the current serial transfer. If the bit is set to 1, the DOUT line is weakly driven to Channel Address Bit ADD2 of the following conversion. If this bit is set to 0, DOUT returns to three-state at the end of the serial transfer (see the Serial Interface section).

The eight analog input channels can be configured as seven pseudo differential analog inputs, four pseudo differential inputs, four true differential input pairs, or eight single-ended analog inputs.

Table 12. Analog Input Configuration Selection

Channel Address Bits			7 Pseudo Differential I/Ps (Mode 1 = 1, Mode 0 = 1)		4 Fully Differential I/Ps (Mode 1 = 1, Mode 0 = 0)		4 Pseudo Differential I/Ps (Mode 1 = 0, Mode 0 = 1)		8 Single-Ended I/Ps (Mode 1 = 0, Mode 0 = 0)	
ADD2	ADD1	ADD0	V_{IN+}	V_{IN-}	V_{IN+}	V_{IN-}	V_{IN+}	V_{IN-}	V_{IN+}	V_{IN-}
0	0	0	V_{IN0}	V_{IN7}	V_{IN0}	V_{IN1}	V_{IN0}	V_{IN1}	V_{IN0}	AGND
0	0	1	V_{IN1}	V_{IN7}	V_{IN0}	V_{IN1}	V_{IN0}	V_{IN1}	V_{IN1}	AGND
0	1	0	V_{IN2}	V_{IN7}	V_{IN2}	V_{IN3}	V_{IN2}	V_{IN3}	V_{IN2}	AGND
0	1	1	V_{IN3}	V_{IN7}	V_{IN2}	V_{IN3}	V_{IN2}	V_{IN3}	V_{IN3}	AGND
1	0	0	V_{IN4}	V_{IN7}	V_{IN4}	V_{IN5}	V_{IN4}	V_{IN5}	V_{IN4}	AGND
1	0	1	V_{IN5}	V_{IN7}	V_{IN4}	V_{IN5}	V_{IN4}	V_{IN5}	V_{IN5}	AGND
1	1	0	V_{IN6}	V_{IN7}	V_{IN6}	V_{IN7}	V_{IN6}	V_{IN7}	V_{IN6}	AGND
1	1	1	Temperature indicator		V_{IN6}	V_{IN7}	V_{IN6}	V_{IN7}	V_{IN7}	AGND

Table 13. Power Mode Selection

PM1	PM0	Description
1	1	Full shutdown mode. In this mode, all internal circuitry on the AD7329 is powered down. Information in the control register is retained when the AD7329 is in full shutdown mode.
1	0	Autoshutdown mode. The AD7329 enters autoshutdown on the 15 th SCLK rising edge when the control register is updated. All internal circuitry is powered down in autoshutdown.
0	1	Autostandby mode. In this mode, all internal circuitry is powered down, excluding the internal reference. The AD7329 enters autostandby mode on the 15 th SCLK rising edge after the control register is updated.
0	0	Normal mode. All internal circuitry is powered up at all times.

Table 14. Sequencer Selection

SEQ1	SEQ2	Description
0	0	The channel sequencer is not used. The analog channel, selected by programming the ADD2 to ADD0 bits in the control register, selects the next channel for conversion.
0	1	Uses the sequence of channels that were previously programmed in the sequence register for conversion. The AD7329 starts converting on the lowest channel in the sequence. The channels are converted in ascending order. If uninterrupted, the AD7329 keeps converting the sequence. The range for each channel defaults to the range previously written into the corresponding range register.
1	0	This configuration is used in conjunction with the channel address bits in the control register. This allows continuous conversions on a consecutive sequence of channels, from Channel 0 through a final channel selected by the channel address bits in the control register. The range for each channel defaults to the range previously written into the corresponding range register.
1	1	The channel sequencer is not used. The analog channel, selected by programming the ADD2 bit to ADD0 bit in the control register, selects the next channel for conversion.

SEQUENCE REGISTER

The sequence register on the [AD7329](#) is an 8-bit, write-only register. Each of the eight analog input channels has one corresponding bit in the sequence register. To select a channel for inclusion in the sequence, set the corresponding channel bit to 1 in the sequence register.

MSB											LSB				
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Write	Register Select 1	Register Select 2	V _{IN0}	V _{IN1}	V _{IN2}	V _{IN3}	V _{IN4}	V _{IN5}	V _{IN6}	V _{IN7}	0	0	0	0	0

RANGE REGISTERS

The range registers are used to select one analog input range per analog input channel. Range Register 1 is used to set the ranges for Channel 0 to Channel 3. It is an 8-bit, write-only register with two dedicated range bits for each of the analog input channels from Channel 0 to Channel 3. There are four analog input ranges, ± 10 V, ± 5 V, ± 2.5 V, and 0 V to +10 V. A write to Range Register 1 is selected by setting the write bit to 1 and the range select bits to 0 and 1, respectively. After the initial write to Range Register 1 occurs, each time an analog input is selected, the [AD7329](#) automatically configures the analog input to the appropriate range, as indicated by Range Register 1. The ± 10 V input range is selected by default on each analog input channel (see Table 15).

MSB											LSB				
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Write	Register Select 1	Register Select 2	V _{IN0A}	V _{IN0B}	V _{IN1A}	V _{IN1B}	V _{IN2A}	V _{IN2B}	V _{IN3A}	V _{IN3B}	0	0	0	0	0

Range Register 2 is used to set the ranges for Channel 4 to Channel 7. It is an 8-bit, write-only register with two dedicated range bits for each of the analog input channels from Channel 4 to Channel 7. There are four analog input ranges, ± 10 V, ± 5 V, ± 2.5 V, and 0 V to +10 V. After the initial write to Range Register 2 occurs, each time an analog input is selected, the [AD7329](#) automatically configures the analog input to the appropriate range, as indicated by Range Register 2. The ± 10 V input range is selected by default on each analog input channel (see Table 15).

MSB											LSB				
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Write	Register Select 1	Register Select 2	V _{IN4A}	V _{IN4B}	V _{IN5A}	V _{IN5B}	V _{IN6A}	V _{IN6B}	V _{IN7A}	V _{IN7B}	0	0	0	0	0

Table 15. Range Selection

V _{INxA}	V _{INxB}	Description
0	0	This combination selects the ± 10 V input range on V _{INx} .
0	1	This combination selects the ± 5 V input range on V _{INx} .
1	0	This combination selects the ± 2.5 V input range on V _{INx} .
1	1	This combination selects the 0 V to +10 V input range on V _{INx} .

```

graph TD
    Start([POWER ON.]) --> CS1[CS]
    CS1 --> Box1[DIN: WRITE TO RANGE REGISTER 1 TO SELECT THE RANGE FOR EACH ANALOG INPUT CHANNEL.  
DOUT: CONVERSION RESULT FROM CHANNEL 0, ±10V RANGE, SINGLE-ENDED MODE.]
    Box1 --> CS2[CS]
    CS2 --> Box2[DIN: WRITE TO RANGE REGISTER 2 TO SELECT THE RANGE FOR EACH ANALOG INPUT CHANNEL.  
DOUT: CONVERSION RESULT FROM CHANNEL 0, SINGLE-ENDED MODE, RANGE SELECTED IN RANGE REGISTER 1.]
    Box2 --> CS3[CS]
    CS3 --> Box3[DIN: WRITE TO SEQUENCE REGISTER TO SELECT THE ANALOG INPUT CHANNELS TO BE INCLUDED IN THE SEQUENCE.  
DOUT: CONVERSION RESULT FROM CHANNEL 0, SINGLE-ENDED MODE, RANGE SELECTED IN RANGE REGISTER 1.]
    Box3 --> CS4[CS]
    CS4 --> Box4[DIN: WRITE TO CONTROL REGISTER TO START THE SEQUENCE, SEQ1 = 0, SEQ2 = 1.  
DOUT: CONVERSION RESULT FROM CHANNEL 0, SINGLE-ENDED MODE, RANGE SELECTED IN RANGE REGISTER 1.]
    Box4 --> CS5[CS]
    CS5 --> Box5[DIN: TIE DIN LOW/WRITE BIT = 0 TO CONTINUE TO CONVERT THROUGH THE SEQUENCE OF CHANNELS.  
DOUT: CONVERSION RESULT FROM FIRST CHANNEL IN THE SEQUENCE.]
    Box5 --> CS6[CS]
    CS6 --> Box6[DIN: WRITE TO CONTROL REGISTER TO STOP THE SEQUENCE, SEQ1 = 0, SEQ2 = 0.  
DOUT: CONVERSION RESULT FROM CHANNEL IN SEQUENCE.]
    Box6 --> CS7[CS]
    CS7 --> Box7[DIN: WRITE TO SEQUENCE REGISTER TO SELECT THE NEW SEQUENCE.  
DOUT: CONVERSION RESULT FROM CHANNEL X IN THE FIRST SEQUENCE.]
    Box5 --> CS6
    Box5 --> CS7
    Box5 --> CS8[CS]
    CS8 --> Box5
    Box5 --> CS9[CS]
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These two initial serial transfers are required only if input ranges other than the default ranges are required. After the analog input ranges are configured, a write to the sequence register is necessary to select the channels to be included in the sequence. After the channels for the sequence have been selected, the sequence can be initiated by writing to the control register and setting SEQ1 to 0 and SEQ2 to 1. The [AD7329](#) continues to convert the selected sequence without interruption if the sequence register remains unchanged and SEQ1 = 0 and SEQ2 = 1 in the control register.

If a change to one of the range registers is required during a sequence, it is necessary to first stop the sequence by writing to the control register and setting SEQ1 to 0 and SEQ2 to 0. Next, write to the range register to change the required range. The previously selected sequence should then be initiated again by writing to the control register and setting SEQ1 to 0 and SEQ2 to 1. The ADC converts the first channel in the sequence.

The AD7329 can be configured to convert a sequence of consecutive channels (see Figure 49). This sequence begins by converting on Channel 0 and ends with a final channel as selected by Bit ADD2 to Bit ADD0 in the control register. In this configuration, there is no need for a write to the sequence register. To operate the AD7329 in this mode, set SEQ1 to 1 and

SEQ2 to 0 in the control register, and then select the final channel in the sequence by programming Bit ADD2 to Bit ADD0 in the control register.

After the control register is configured to operate the AD7329 in this mode, the DIN line can be held low or the write bit can be set to 0. To return to traditional multichannel operation, a write to the control register to set SEQ1 to 0 and SEQ2 to 0 is necessary.

When SEQ1 and SEQ2 are both set to 0 or to 1, the AD7329 is configured to operate in traditional multichannel mode, where a write to Channel Address Bit ADD2 to Bit ADD0 in the control register selects the next channel for conversion.

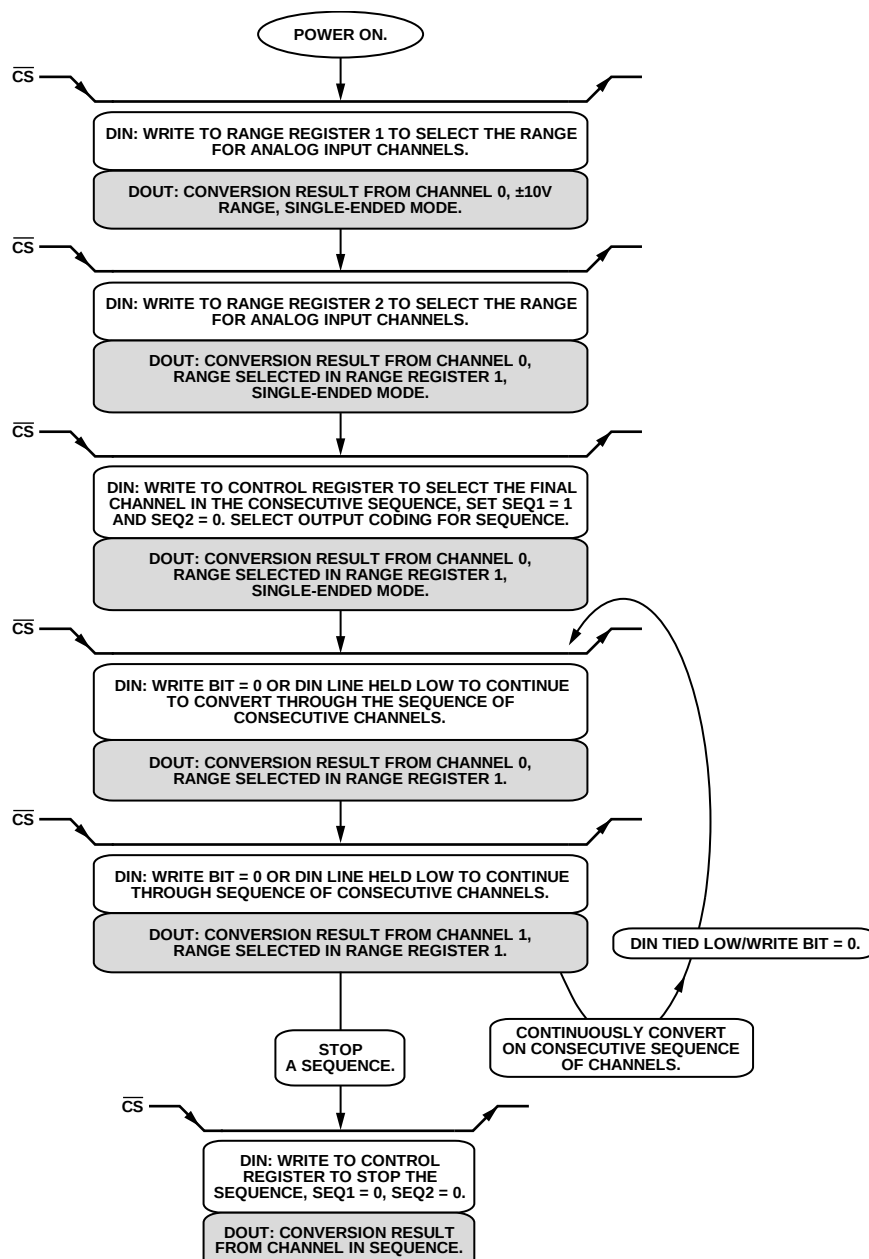


Figure 49. Flowchart for Consecutive Sequence of Channels

REFERENCE

The AD7329 can operate with either the internal 2.5 V on-chip reference or an externally applied reference. The internal reference is selected by setting the REF bit in the control register to 1. On power-up, the REF bit is 0, which selects the external reference for the AD7329 conversion. Suitable reference sources for the AD7329 include AD780, AD1582, ADR431, REF193, and ADR391.

The internal reference circuitry consists of a 2.5 V band gap reference and a reference buffer. When operating the AD7329 in internal reference mode, the 2.5 V internal reference is available at the REF_{IN}/REF_{OUT} pin, which should be decoupled to AGND using a 680 nF capacitor. It is recommended that the internal reference be buffered before applying it elsewhere in the system. The internal reference is capable of sourcing up to 90 μ A.

On power-up, if the internal reference operation is required for the ADC conversion, a write to the control register is necessary to set the REF bit to 1. During the control register write, the conversion result from the first initial conversion is invalid. The reference buffer requires 500 μ s to power up and charge the 680 nF decoupling capacitor during the power-up time.

The AD7329 is specified for a 2.5 V to 3 V reference range. When a 3 V reference is selected, the ranges are ± 12 V, ± 6 V, ± 3 V, and 0 V to +12 V. For these ranges, the V_{DD} and V_{SS} supply must be equal to or greater than the maximum analog input range selected.

V_{DRIVE}

The AD7329 has a V_{DRIVE} feature to control the voltage at which the serial interface operates. V_{DRIVE} allows the ADC to easily interface to both 3 V and 5 V processors. For example, if the AD7329 is operated with a V_{CC} of 5 V, the V_{DRIVE} pin can be powered from a 3 V supply. This allows the AD7329 to accept large bipolar input signals with low voltage digital processing.

TEMPERATURE INDICATOR

The AD7329 has an on-chip temperature indicator. The temperature indicator can be used to provide local temperature measurements on the AD7329. To access the temperature indicator, the ADC should be configured in pseudo differential mode, Mode 1 = Mode 0 = 1, which sets Channel Bits ADD2, ADD1, and ADD0 to 1. V_{IN7} must be tied to AGND or to a small dc voltage within the specified pseudo differential input range for the selected analog input range. When a conversion is initiated in this configuration, the output code represents the temperature (see Figure 50 and Figure 51). When using the temperature indicator on the AD7329, the part should be operated at low throughput rates, such as approximately 30 kSPS for the ± 2.5 V range. The throughput rate is reduced for the temperature indicator mode because the AD7329 requires more acquisition time for this mode.

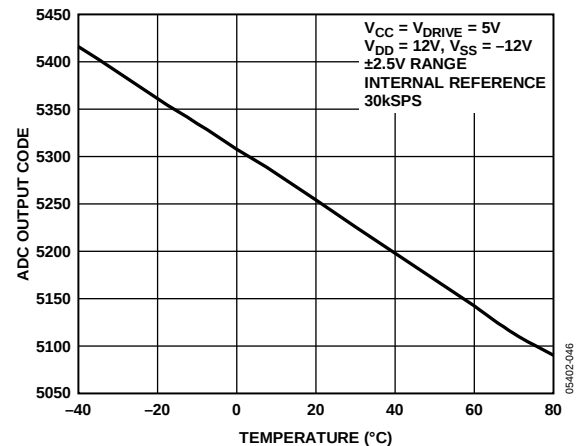


Figure 50. ADC Output Code vs. Temperature for ± 2.5 V Range

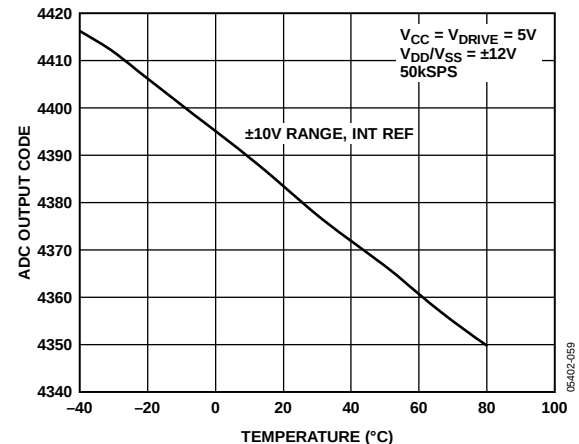


Figure 51. ADC Output Code vs. Temperature for ± 10 V Range

MODES OF OPERATION

The AD7329 has several modes of operation that are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for different application requirements. The mode of operation of the AD7329 is controlled by the power management bits, Bit PM1 and Bit PM0, in the control register as shown in Table 13. The default mode is normal mode, where all internal circuitry is fully powered up.

NORMAL MODE (PM1 = PM0 = 0)

This mode is intended for the fastest throughput rate performance with the AD7329 being fully powered up at all times. Figure 52 shows the general operation of the AD7329 in normal mode.

The conversion is initiated on the falling edge of $\overline{\text{CS}}$, and the track-and-hold section enters hold mode, as described in the Serial Interface section. The data on the DIN line during the 16 SCLK transfer is loaded into one of the on-chip registers if the write bit is set. The register is selected by programming the register select bits (see Table 10).

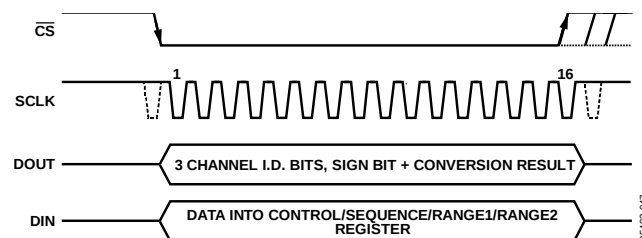


Figure 52. Normal Mode

The AD7329 remains fully powered up at the end of the conversion if both PM1 and PM0 contain 0 in the control register.

To complete the conversion and access the conversion result, 16 serial clock cycles are required. At the end of the conversion, $\overline{\text{CS}}$ can idle either high or low until the next conversion.

After the data transfer is complete, another conversion can be initiated after the quiet time, t_{QUIET} , has elapsed.

FULL SHUTDOWN MODE (PM1 = PM0 = 1)

In this mode, all internal circuitry on the AD7329 is powered down. The part retains information in the registers during full shutdown. The AD7329 remains in full shutdown mode until the power management bits, Bit PM1 and Bit PM0, in the control register are changed.

A write to the control register with PM1 = PM0 = 1 places the part into full shutdown mode. The AD7329 enters full shutdown mode on the 15th SCLK rising edge when the control register is updated.

If a write to the control register occurs while the part is in full shutdown mode with the power management bits, Bit PM1 and Bit PM0, set to 0 (normal mode), the part begins to power up on the 15th SCLK rising edge when the control register is updated. Figure 53 shows how the AD7329 is configured to exit full shutdown mode. To ensure that the AD7329 is fully powered up, $t_{\text{POWER-UP}}$ should elapse before the next $\overline{\text{CS}}$ falling edge.

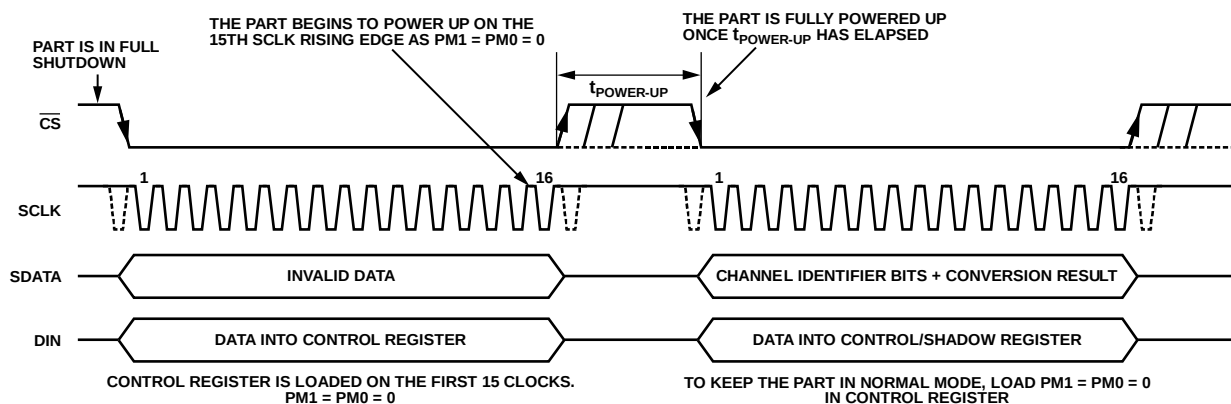


Figure 53. Exiting Full Shutdown Mode

AUTOSHUTDOWN MODE**(PM1 = 1, PM0 = 0)**

When the autoshutdown mode is selected, the AD7329 automatically enters shutdown on the 15th SCLK rising edge. In autoshutdown mode, all internal circuitry is powered down. The AD7329 retains information in the registers during autoshutdown. The track-and-hold section is in hold mode during autoshutdown. On the rising $\overline{CS}$ edge, the track-and-hold section, which was in hold during shutdown, returns to track as the AD7329 begins to power up. The time to power up from autoshutdown is 500 μ s.

When the control register is programmed to transition to autoshutdown mode, it does so on the 15th SCLK rising edge. Figure 54 shows the part entering autoshutdown mode. The AD7329 automatically begins to power up on the $\overline{CS}$ rising edge. The $t_{POWER-UP}$ is required before a valid conversion, initiated by bringing the $\overline{CS}$ signal low, can take place. After this valid conversion is complete, the AD7329 powers down again on the 15th SCLK rising edge. The $\overline{CS}$ signal must remain low again to keep the part in autoshutdown mode.

AUTOSTANDBY MODE**(PM1 = 0, PM0 = 1)**

In autostandby mode, portions of the AD7329 are powered down, but the on-chip reference remains powered up. The reference bit in the control register should be 1 to ensure that the on-chip reference is enabled. This mode is similar to autoshutdown but allows the AD7329 to power up much faster, which allows faster throughput rates.

As is the case with autoshutdown mode, the AD7329 enters standby on the 15th SCLK rising edge when the control register is updated (see Figure 54). The part retains information in the registers during standby. The AD7329 remains in standby until it receives a $\overline{CS}$ rising edge. The ADC begins to power up on the $\overline{CS}$ rising edge. On the $\overline{CS}$ rising edge, the track-and-hold, which was in hold mode while the part was in standby, returns to track.

The power-up time from standby is 750 ns. The user should ensure that 750 ns have elapsed before bringing $\overline{CS}$ low to attempt a valid conversion. After this valid conversion is complete, the AD7329 again returns to standby on the 15th SCLK rising edge. The $\overline{CS}$ signal must remain low to keep the part in standby mode.

Figure 54 shows the part entering autoshutdown mode. The sequence of events is the same when entering autostandby mode. In Figure 54, the power management bits are configured for autoshutdown. For autostandby mode, the power management bits, PM1 and PM0, should be set to 0 and 1, respectively.

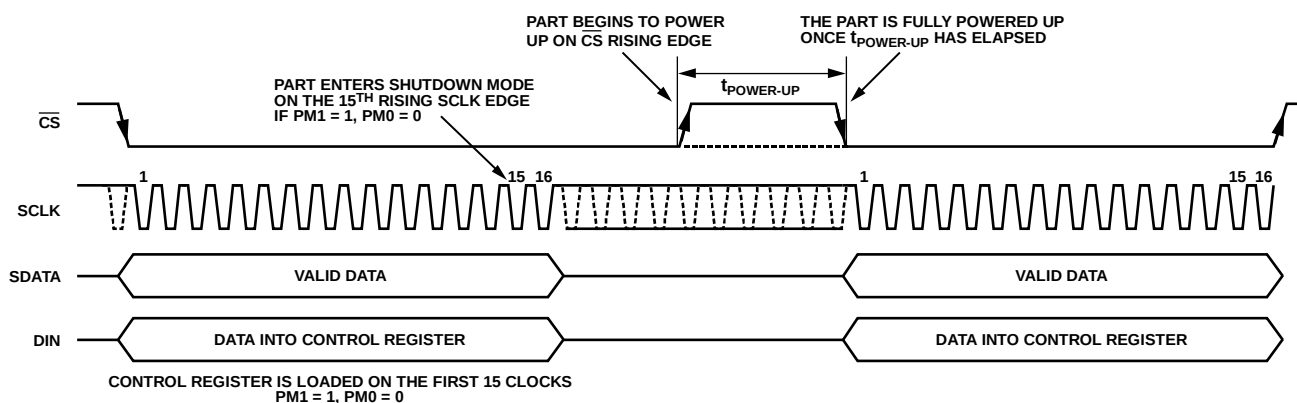


Figure 54. Entering Autosutdown/Autostandby Mode

08402-010

POWER VS. THROUGHPUT RATE

The power consumption of the AD7329 varies with throughput rate. The static power consumed by the AD7329 is very low, and significant power savings can be achieved as the throughput rate is reduced. Figure 55 and Figure 56 show the power vs. throughput rate for the AD7329 at a V_{CC} of 3 V and 5 V, respectively. Both plots clearly show that the average power consumed by the AD7329 is greatly reduced as the sample frequency is reduced. This is true whether a fixed SCLK value is used or if the SCLK value is scaled with the sampling frequency. Figure 55 and Figure 56 show the power consumption when operating the device in normal mode for a fixed 20 MHz SCLK and a variable SCLK that scales with the sampling frequency.

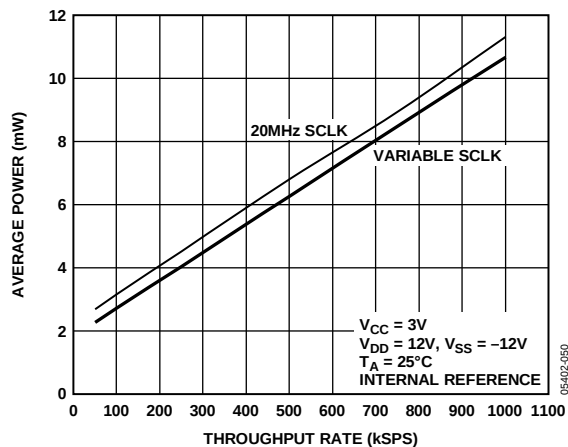


Figure 55. Power vs. Throughput Rate with 3 V V_{CC}

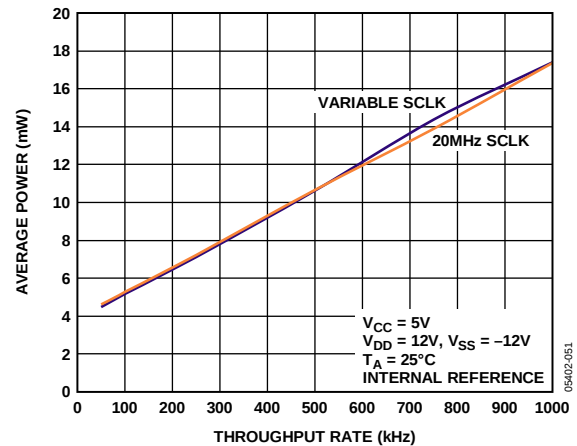


Figure 56. Power vs. Throughput Rate with 5 V V_{CC}

SERIAL INTERFACE

Figure 57 shows the timing diagram for the serial interface of the AD7329. The serial clock applied to the SCLK pin provides the conversion clock and controls the transfer of information to and from the AD7329 during a conversion.

The $\overline{\text{CS}}$ signal initiates the data transfer and the conversion process. The falling edge of $\overline{\text{CS}}$ puts the track-and-hold section into hold mode and takes the bus out of three-state. The analog input signal is then sampled. Once the conversion is initiated, 16 SCLK cycles are required for the conversion to complete.

The track-and-hold section goes back into track mode on the 14th SCLK rising edge. On the 16th SCLK falling edge, the DOUT line returns to three-state. If the rising edge of $\overline{\text{CS}}$ occurs before 16 SCLK cycles have elapsed, the conversion is terminated and the DOUT line returns to three-state. Depending on where the $\overline{\text{CS}}$ signal is brought high, the addressed register may update.

Data is clocked into the AD7329 on the SCLK falling edge. The three MSBs on the DIN line are decoded to select which register is addressed. The control register is a 12-bit register. If the control register is addressed by the three MSBs, the data on the DIN line is loaded into the control on the 15th SCLK rising edge. If the sequence register or either of the range registers is addressed, the data on the DIN line is loaded into the addressed register on the 11th SCLK falling edge.

Conversion data is clocked out of the AD7329 on each SCLK falling edge. Data on the DOUT line consists of three channel identifier bits, a sign bit, and a 12-bit conversion result. The channel identifier bits are used to indicate which channel corresponds to the conversion result.

If the Weak/Three-State bit is set in the control register, rather than returning to true three-state upon the 16th SCLK falling edge, the DOUT line is pulled weakly to the logic level corresponding to ADD3 of the next serial transfer. This is done to ensure that the MSB of the next serial transfer is set up in time for the first SCLK falling edge after the $\overline{\text{CS}}$ falling edge. If the Weak/Three-State bit is set to 0 and the DOUT line returns to true three-state between conversions, then depending on the particular processor interfacing to the AD7329, the ADD3 bit may be valid in time for the processor to clock it in successfully. If the Weak/Three-State bit is set to 1, then although the DOUT line has been driven to ADD3 since the previous conversion, it is nevertheless so weakly driven that another device could take control of the bus. This will not lead to a bus contention issue because, for example, a 10 k Ω pull-up or pull-down resistor is sufficient to overdrive the logic level of ADD3. When the Weak/Three-State bit is set to 1, the ADD3 is typically valid 9 ns after the $\overline{\text{CS}}$ falling edge, compared with 14 ns when the DOUT line returns to three-state at the end of the conversion.

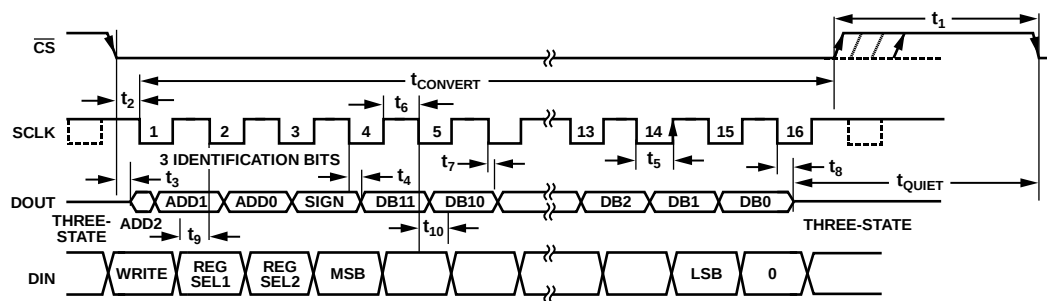


Figure 57. Serial Interface Timing Diagram (Control Register Write)

05402-052

MICROPROCESSOR INTERFACING

The serial interface on the [AD7329](#) allows the part to be directly connected to a range of different microprocessors. This section explains how to interface the [AD7329](#) with some of the most common microcontroller and DSP serial interface protocols.

AD7329 TO ADSP-21xx

The [ADSP-21xx](#) family of DSPs interfaces directly to the [AD7329](#) without requiring glue logic. The V_{DRIVE} pin of the [AD7329](#) takes the same supply voltage as that of the [ADSP-21xx](#). This allows the ADC to operate at a higher supply voltage than its serial interface. The SPORT0 on the [ADSP-21xx](#) should be configured as shown in Table 16.

Table 16. SPORT0 Control Register Setup

Setting	Description
TFSW = RFSW = 1	Alternative framing
INVRFS = INVTF = 1	Active low frame signal
DTYPE = 00	Right justify data
SLEN = 1111	16-bit data-word
ISCLK = 1	Internal serial clock
TFSR = RFSR = 1	Frame every word
IRFS = 0	Internal receive frame sync
ITFS = 1	Internal transmit frame sync

The connection diagram is shown in Figure 58. The [ADSP-21xx](#) has TFS0 and RFS0 tied together. TFS0 is set as an output, and RFS0 is set as an input. The DSP operates in alternative framing mode, and the SPORT0 control register is set up as described in Table 16. The frame synchronization signal generated on TFS is tied to $\overline{\text{CS}}$ and, as with all signal processing applications, requires equidistant sampling. However, as in this example, the timer interrupt is used to control the sampling rate of the ADC, and under certain conditions equidistant sampling cannot be achieved.

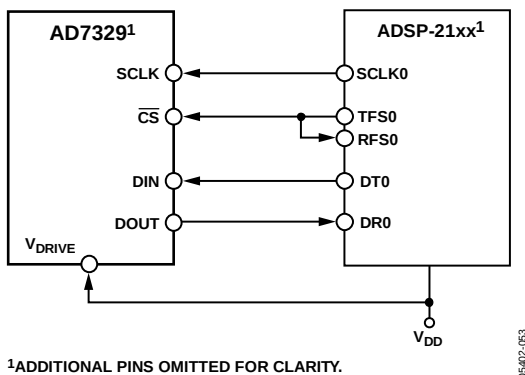


Figure 58. Interfacing the [AD7329](#) to the [ADSP-21xx](#)

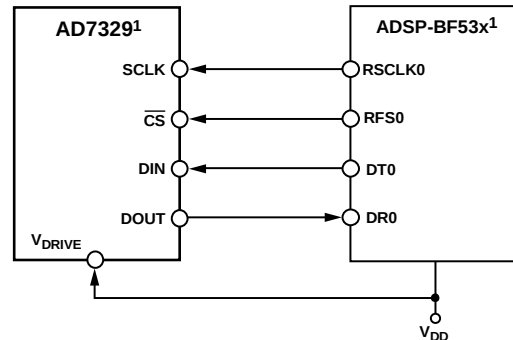
The timer registers are loaded with a value that provides an interrupt at the required sampling interval. When an interrupt is received, a value is transmitted with TFS/DT (ADC control word). The TFS is used to control the RFS and, hence, the reading of data.

The frequency of the serial clock is set in the SCLKDIV register. When the instruction to transmit with TFS is given ($\text{AX0} = \text{TX0}$), the state of the serial clock is checked. The DSP waits until the SCLK has gone high, low, and high again before starting the transmission. If the timer and SCLK are chosen so that the instruction to transmit occurs on or near the rising edge of SCLK, data can be transmitted immediately or at the next clock edge.

For example, if the [ADSP-21xx](#) has a master clock frequency of 16 MHz and the SCLKDIV register is loaded with the value 3, an SCLK of 2 MHz is obtained, and eight master clock periods elapse for every one SCLK period. If the timer registers are loaded with the value 803, 100.5 SCLKs occur between interrupts and, subsequently, between transmit instructions. This situation leads to nonequidistant sampling because the transmit instruction occurs on an SCLK edge. If the number of SCLKs between interrupts is an integer of N, equidistant sampling is implemented by the DSP.

AD7329 TO ADSP-BF53x

The [ADSP-BF53x](#) family of DSPs interfaces directly to the [AD7329](#) without requiring glue logic, as shown in Figure 59. The SPORT0 Receive Configuration 1 register should be set up as outlined in Table 17.



¹ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 59. Interfacing the [AD7329](#) to the [ADSP-BF53x](#)

Table 17. SPORT0 Receive Configuration 1 Register

Setting	Description
RCKFE = 1	Sample data with falling edge of RSCLK
LRFS = 1	Active low frame signal
RFSR = 1	Frame every word
IRFS = 1	Internal RFS used
RLSBIT = 0	Receive MSB first
RDTYPE = 00	Zero fill
IRCLK = 1	Internal receive clock
RSPEN = 1	Receive enable
SLEN = 1111	16-bit data-word
TFSR = RFSR = 1	Transmit and receive frame sync

APPLICATIONS INFORMATION

LAYOUT AND GROUNDING

The printed circuit board that houses the AD7329 should be designed so that the analog and digital sections are confined to certain areas of the board. This design facilitates the use of ground planes that can be easily separated.

To provide optimum shielding for ground planes, a minimum etch technique is generally best. All AGND pins on the AD7329 should be connected to the AGND plane. Digital and analog ground pins should be joined in only one place. If the AD7329 is in a system where multiple devices require an AGND and DGND connection, the connection should still be made at only one point. A star point should be established as close as possible to the ground pins on the AD7329.

Good connections should be made to the power and ground planes. This can be done with a single via or multiple vias for each supply and ground pin.

Avoid running digital lines under the AD7329 device because this couples noise onto the die. However, the analog ground plane should be allowed to run under the AD7329 to avoid noise coupling. The power supply lines to the AD7329 device should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line.

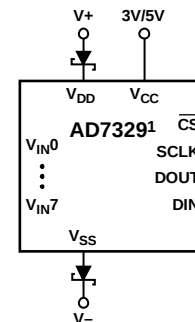
To avoid radiating noise to other sections of the board, components, such as clocks, with fast switching signals should be shielded with digital ground and never run near the analog inputs. Avoid crossover of digital and analog signals. To reduce the effects of feedthrough within the board, traces should be run at right angles to each other. A microstrip technique is the best method, but its use may not be possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, and signals are placed on the other side.

Good decoupling is also important. All analog supplies should be decoupled with 10 μF tantalum capacitors in parallel with 0.1 μF capacitors to AGND. To achieve the best results from these decoupling components, they must be placed as close as possible to the device, ideally right up against the device. The 0.1 μF capacitors should have a low effective series resistance (ESR) and low effective series inductance (ESI), such as is typical of common ceramic and surface-mount types of capacitors.

These low ESR, low ESI capacitors provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

POWER SUPPLY CONFIGURATION

It is recommended that Schottky diodes be placed in series with the AD7329 V_{DD} and V_{SS} supply signals. Figure 60 shows this Schottky diode configuration. BAT43 Schottky diodes are used.



¹ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 60. Schottky Diode Connection

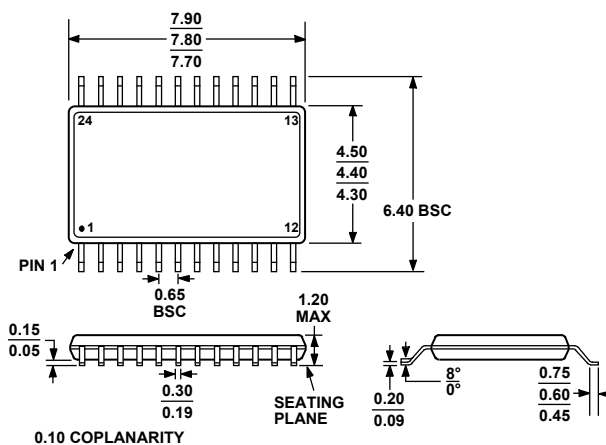
In an application where nonsymmetrical V_{DD} and V_{SS} supplies are used, adhere to the guidelines provided in Table 18, which outlines the V_{SS} supply range that can be used for various V_{DD} voltages when nonsymmetrical supplies are required. When operating the AD7329 with low V_{DD} and V_{SS} voltages, it is recommended that these supplies be symmetrical.

Table 18. Nonsymmetrical V_{DD} and V_{SS} Requirements

V_{DD}	Typical V_{SS} Range
5 V	–5 V to –5.5 V
6 V	–5 V to –8.5 V
7 V	–5 V to –11.5 V
8 V	–5 V to –15 V
9 V	–5 V to –16.5 V
10 V to 16.5 V	–5 V to –16.5 V

For the 0 V to $4 \times V_{\text{REF}}$ range, V_{SS} can be tied to AGND as per the minimum supply recommendations outlined in Table 6.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AD

Figure 61. 24-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-24)

Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
AD7329BRUZ	–40°C to +85°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
AD7329BRUZ-REEL	–40°C to +85°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
AD7329BRUZ-REEL7	–40°C to +85°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
EVAL-AD7329SDZ		Evaluation Board	
EVAL-SDP-CBZ1		Controller Board	

¹ Z = RoHS Compliant Part.