RoHS Compliant

1GB DDR2 SDRAM SO-DIMM Industrial

Product Specifications

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Version 1.1

Apacer Technology Inc.
1F., No.32, Zhongcheng Rd., Tucheng Dist., New Taipei City 236, Taiwan
Tel: +886-2-2267-8000 Fax: +886-2-2267-2261
www.apacer.com

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General Description

Apacer **75.073AR.G070C** is a 128M x 64 Double Data Rate SDRAM high density memory modules based on first generation of 1GB DDR2 SDRAM respectively.

It consists of 8 pieces 128M x 8 bit with 8banks Double Data Rate SDRAMs in 60Ball FBGA packages mounted on a 200pin glass-epoxy substrate. Decoupling capacitors are mounted on the printed circuit board in parallel for each DDR2 SDRAM.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Ordering Information

Part Number	Bandwidth	Speed Grade	Max Frequency	CAS Latency
75.073AR.G070C	5.3 GB/sec	667 Mbps	333 MHz	CL5

Density	Organization	Component	Rank
1GB	128M x 64	128M x8*8	1

Key Parameters

MT/s	DDR2-667	DDR2-800	DDR2-800	Unit
Grade	-CL5	-CL5	-CL6	
tCK (min)	3	2.5	2.5	ns
CAS latency	5	5	6	tCK
tRCD (min)	15	12.5	15	ns
tRP (min)	15	12.5	15	ns
tRAS (min)	45	45	45	ns
tRC (min)	60	57.5	60	ns
CL-tRCD-tRP	5-5-5	5-5-5	6-6-6	tCK

Specifications:

- JEDEC standard 1.8V ± 0.1V
- Power Supply VDDQ = 1.8V± 0.1V
- Interface: SSTL_18
- Posted CAS
- Programmable CAS Latency: 3, 4, 5
- Programmable Additive Latency: 0, 1 , 2 , 3 and 4
- Write Latency(WL) = Read Latency(RL) -1
- Burst Length: 4 , 8(Interleave/nibble sequential)
- Programmable Sequential / Interleave Burst Mode
- On Die Termination
- Refresh and Self Refresh
- Average Refresh Period 7.8us
- Serial presence detect with EEPROM
- Compliance with RoHS
- Compliance with CE
- Supports auto-refresh/self-refresh
- Operating Temperature Range:
  Industrial -40˚C ≦ TC ≦ 95˚C
  -40˚C ≦ TA ≦ 85˚C
- Average refresh period
  7.8us at 0°C ≦ TC ≦ 85°C
  3.9us at 85°C ≦ TC ≦ 95°C
- PCB: 30µ gold finger

Pin Assignments

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	VREF	51	DQS2	101	A1	151	DQ42
3	VSS	53	VSS	103	VDD	153	DQ43
5	DQ0	55	DQ18	105	A10	155	VSS
7	DQ1	57	DQ19	107	BA0	157	DQ48
9	VSS	59	VSS	109	$\overline{\text{WE}}$	159	DQ49
11	$\overline{\text{DQS0}}$	61	DQ24	111	VDD	161	VSS
13	DQS0	63	DQ25	113	CAS#	163	NC
15	VSS	65	VSS	115	S1#	165	VSS
17	DQ2	67	DM3	117	VDD	167	$\overline{\text{DQS6}}$
19	DQ3	69	NC	119	ODT1	169	DQS6
21	VSS	71	VSS	121	VSS	171	VSS
23	DQ8	73	DQ26	123	DQ32	173	DQ50
25	DQ9	75	DQ27	125	DQ33	175	DQ51
27	VSS	77	VSS	127	VSS	177	VSS
29	$\overline{\text{DQS1}}$	79	CKE0	129	$\overline{\text{DQS4}}$	179	DQ56
31	DQS1	81	VDD	131	DQS4	181	DQ57
33	VSS	83	NC	133	VSS	183	VSS
35	DQ10	85	NC/BA2	135	DQ34	185	DM7
37	DQ11	87	VDD	137	DQ35	187	VSS
39	VSS	89	A12	139	VSS	189	DQ58
41	VSS	91	A9	141	DQ40	191	DQ59
43	DQ16	93	A8	143	DQ41	193	VSS
45	DQ17	95	VDD	145	VSS	195	SDA
47	VSS	97	A5	147	DM5	197	SCL
49	$\overline{\text{DQS2}}$	99	A3	149	VSS	199	VDDSPD

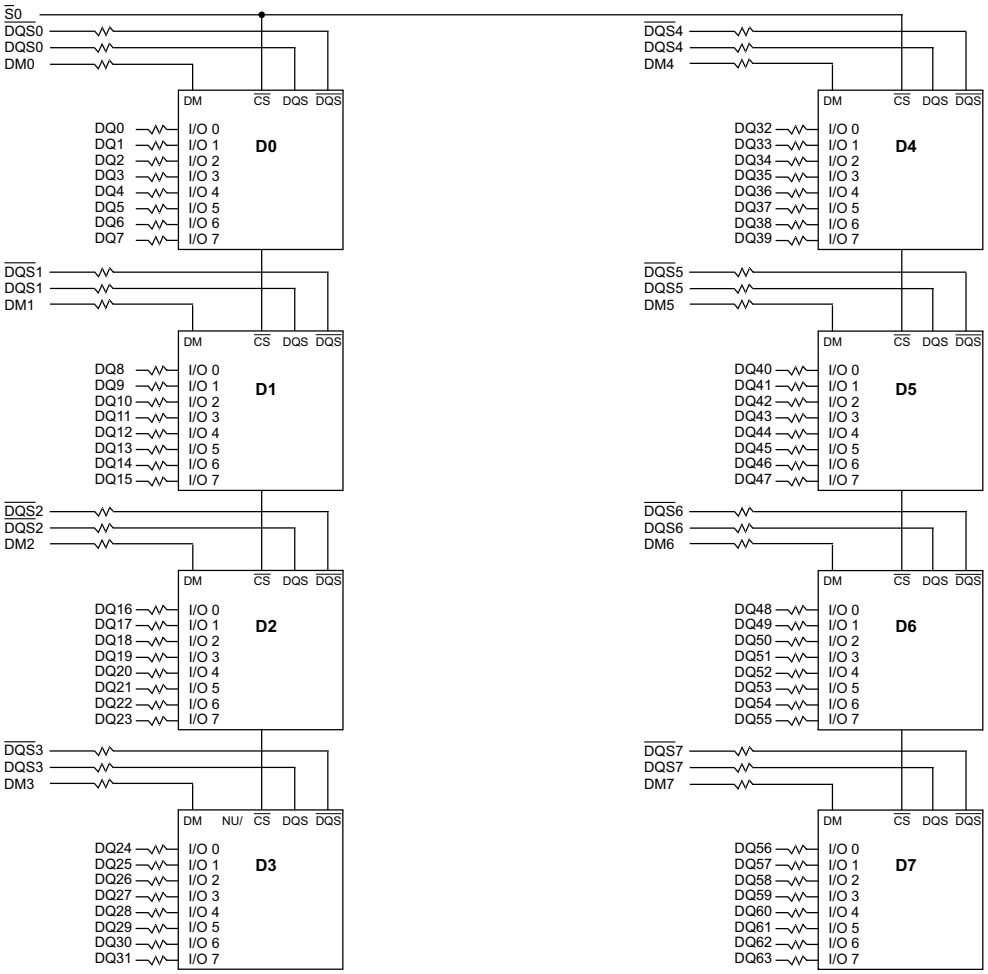
Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
2	VSS	52	DM2	102	A0	152	DQ46
4	DQ4	54	VSS	104	VDD	154	DQ47
6	DQ5	56	DQ22	106	BA1	156	VSS
8	VSS	58	DQ23	108	$\overline{RAS}$	158	DQ52
10	DM0	60	VSS	110	$\overline{S0}$	160	DQ53
12	VSS	62	DQ28	112	VDD	162	VSS
14	DQ6	64	DQ29	114	ODT0	164	CK1
16	DQ7	66	VSS	116	NC	166	$\overline{CK1}$
18	VSS	68	$\overline{DQS3}$	118	VDD	168	VSS
20	DQ12	70	DQS3	120	NC	170	DM6
22	DQ13	72	VSS	122	VSS	172	VSS
24	VSS	74	DQ30	124	DQ36	174	DQ54
26	DM1	76	DQ31	126	DQ37	176	DQ55
28	VSS	78	VSS	128	VSS	178	VSS
30	CK0	80	NC/CKE1	130	DM4	180	DQ60
32	$\overline{CK0}$	82	VDD	132	VSS	182	DQ61
34	VSS	84	NC	134	DQ38	184	VSS
36	DQ14	86	NC	136	DQ39	186	$\overline{DQS7}$
38	DQ15	88	VDD	138	VSS	188	DQS7
40	VSS	90	A11	140	DQ44	190	VSS
42	VSS	92	A7	142	DQ45	192	DQ62
44	DQ20	94	A6	144	VSS	194	DQ63
46	DQ21	96	VDD	146	$\overline{DQS5}$	196	VSS
48	VSS	98	A4	148	DQS5	198	SA0
50	NC	100	A2	150	VSS	200	SA1

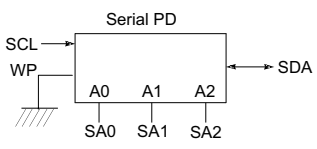
*Pin 85 is NC for 512MB and BA2 for 1GB

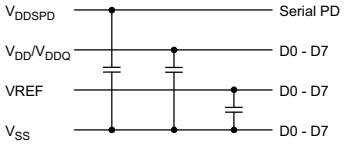
Pin Descriptions

Pin Name	Description
Ax	SDRAM address bus
BAx	SDRAM bank select
$\overline{RAS}$	SDRAM row address strobe
$\overline{CAS}$	SDRAM column address strobe
$\overline{WE}$	SDRAM write enable
$\overline{Sx}$	DIMM Rank Select Lines
CKEx	SDRAM clock enable lines
ODTx	On-die termination control lines
DQx	DIMM memory data bus
DQSx	SDRAM data strobes(positive line of differential pair)
$\overline{DQSx}$	SDRAM data strobes(negative line of differential pair)
DMx	SDRAM data masks high data strobes(x8-based X72 DIMMs)
CKx	SDRAM clocks(positive line of differential pair)
$\overline{CKx}$	SDRAM clocks(negative line of differential pair)
SCL	I2C serial bus clock for EEPROM
SDA	I2C serial bus data line for EEPROM
SAx	I2C slave address select for EEPROM
VDD	SDRAM core power supply
V_{DDQ}	SDRAM I/0 Driver power supply
V_{REF}	SDRAM I/O reference supply
V_{SS}	Power supply return(ground)
V_{DD}SPD	Serial EEPROM positive power supply
NC	Spare pins(no connect)

Functional Block Diagram







* Clock Wiring	
Clock Input	DDR2 SDRAMs
*CK0/CK0	2 DDR2 SDRAMs
*CK1/CK1	3 DDR2 SDRAMs
*CK2/CK2	3 DDR2 SDRAMs

*Wire per Clock Loading Table/Wiring Diagrams

BA0 - BA2 → BA0-BA2 : DDR2 SDRAMs D0 - D7
A0 - A13 → A0-A13 : DDR2 SDRAMs D0 - D7
RAS → RAS : DDR2 SDRAMs D0 - D7
CAS → CAS : DDR2 SDRAMs D0 - D7
CKE0 → CKE : DDR2 SDRAMs D0 - D7
WE → WE : DDR2 SDRAMs D0 - D7
ODT0 → ODT : DDR2 SDRAMs D0 - D7

Notes :
1. DQ,DM, DQS/DQS resistors : 22 Ohms ± 5%.
2. BAx, Ax, RAS, CAS, WE resistors : 10 Ohms ± 5%.

Absolute Maximum Ratings

Parameter	Symbol	Description	Units
Voltage on VDD pin relative to Vss	V_{DD}	- 0.5 V ~ 2.3 V	V
Voltage on VDDQ pin relative to Vss	V_{DDQ}	- 0.5 V ~ 2.3 V	V
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	- 0.5 V ~ 2.3 V	V
Storage Temperature	TSTG	-55 to +100	℃

Notes:

1. Stress greater than those listed may cause permanent damage to the device. This is a stress rating only and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Units	Notes
T_{OPER}	Operating case Temperature (TC)	-40 to 95	℃	1,2,3
	Operating ambient temperature (TA)	-40 to 85	℃	3,4

Notes:

1. Operating case temperature TC is measured in the center/top side of the DRAM.
2. Device functionality is not guaranteed if the device exceeds maximum TC during operation.
3. Both temperature TA and TC specifications must be satisfied.
4. Operating ambient temperature surrounding the package.

Industrial Temperature

The industrial temperature (IT) option, if offered, has two simultaneous requirements: ambient temperature(TA) surrounding the device cannot be less than –40°C or greater than+85°C, and the case temperature(TC) cannot be less than –40°C or greater than +95°C.

Operating Conditions

Recommended DC Operating Conditions – DDR2 (1.8V) operation

Symbol	Parameter	Rating			Units
		Min.	Typ.	Max.	
VDD	Supply Voltage	1.7	1.8	1.9	V
VDDQ	Supply Voltage for Output	1.7	1.8	1.9	V

Notes:

1. Under all conditions VDDQ must be less than or equal to VDD..
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

IDD Specifications

Conditions	Symbol	MICRON-M	Unit
Operating one bank active-precharge current: tCK = tCK (IDD); tRC = tRC (IDD); tRAS = tRAS MIN (IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0*	480	mA
Operating one bank active-read-precharge current: IOUT = 0 mA; BL = 8; CL = CL (IDD);, AL = 0;, tCK = tCK (IDD); tRC = tRC (IDD); tRAS = tRAS MIN (IDD); tRCD = tRCD (IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD1*	560	mA
Precharge power-down current: All device banks idle; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P	80	mA
Precharge standby current; All device banks idle: tCK = tCK (IDD); CKE is HIGH; CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD2N**	192	mA
Precharge quiet standby current: All device banks idle; tCK = tCK (IDD); CKE is HIGH; CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q**	192	mA
Active power-down current: All device banks open; tCK = tCK (IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD3P-F	224	mA
	IDD3P-S	160	
Active standby current: All device banks open; tCK = tCK (IDD); tRP = tRP (IDD); tRAS = tRAS MAX (IDD); CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD3N**	240	mA

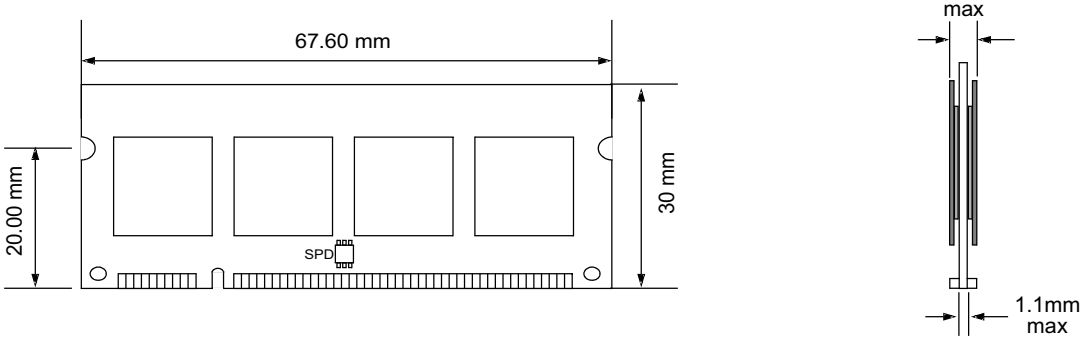
Operating burst read current: All device banks open; Continuous burst reads; IOUT = 0 mA; BL = 8; CL = CL (IDD); AL = 0; tCK = tCK (IDD); tRAS = tRAS MAX (IDD); tRP = tRP (IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data patter is same as IDD4W	IDD4R*	880	mA
Operating burst write current: All device banks open; Continuous burst writes; BL = 8; CL = CL(IDD);AL = 0; tCK= tCK(IDD); tRAS= tRAS MAX(IDD); tRP= tRP(IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD4W*	920	mA
Burst refresh current: tCK=tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH; CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD5**	1200	mA
Self refresh current: CK and CK# at 0V; CKE < 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.	IDD6**	56	mA
Operating bank interleave read current: All bank interleaving reads; IOUT = 0mA; BL = 8; CL = CL(IDD); AL = tRCD(IDD) - 1*tCK(IDD); tCK= tCK(IDD); tRC= tRC(IDD); tRRD = tRRD(IDD); tRCD = 1*tCK(IDD) ; CKE is HIGH; CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R.	IDD7*	1480	mA

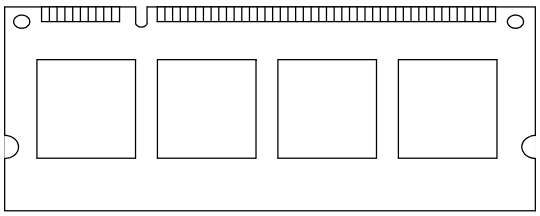
Notes:

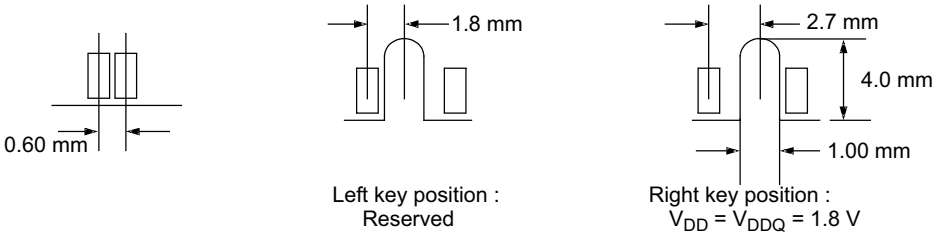
*Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.

**Value calculated reflects all module ranks in this operating condition.

Mechanical Drawing







30µ gold finger

Unit: mm

Tolerances:+-0.15mm unless otherwise specified

Revision History

Revision	Date	Description	Remark
0.9	08/28/2012	Official release	
1.0	08/29/2012	release	
1.1	07/23/2013	Changed headquarters address	

Global Presence

Taiwan (Headquarters)

Apacer Technology Inc.
1F., No.32, Zhongcheng Rd., Tucheng Dist.,
New Taipei City 236, Taiwan R.O.C.
Tel: +886-2-2267-8000
Fax: +886-2-2267-2261
amtsales@apacer.com

U.S.A.

Apacer Memory America, Inc.
46732 Lakeview Blvd., Fremont, CA 94538
Tel: 1-408-518-8699
Fax: 1-510-249-9568
sa@apacerus.com

Japan

Apacer Technology Corp.
5F, Matsura Bldg., Shiba, Minato-Ku
Tokyo, 105-0014, Japan
Tel: 81-3-5419-2668
Fax: 81-3-5419-0018
jpservices@apacer.com

Europe

Apacer Technology B.V.
Science Park Eindhoven 5051 5692 EB Son,
The Netherlands
Tel: 31-40-267-0000
Fax: 31-40-290-0686
sales@apacer.nl

China

Apacer Electronic (Shanghai) Co., Ltd.
Room D, 22/FL, No.2, Lane 600, JieyunPlaza,
Tianshan RD , Shanghai , 200051, China
Tel: 86-21-6228-9939
Fax:86-21-6228-9936
sales@apacer.com.cn

India

Apacer Technologies Pvt Ltd.
Unit No.201, "Brigade Corner", 7th Block Jayanagar, Yediyur
Circle, Bangalore – 560082, India
Tel: 91-80-4152-9061
Fax: 91-80-4170-0215
sales_india@apacer.com