

# 74LVT245B

## 3.3 V octal transceiver with direction pin (3-state)

Rev. 02 — 8 May 2008

Product data sheet

### 1. General description

The 74LVT245B is a high-performance BiCMOS product designed for  $V_{CC}$  operation at 3.3 V.

This device is an octal transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an output enable ( $\overline{OE}$ ) input for easy cascading and a direction (DIR) input for direction control.

### 2. Features

- 3-state buffers
- Octal bidirectional bus interface
- Input and output interface capability to systems at 5 V supply
- TTL input and output switching levels
- Output capability: +64 mA/–32 mA
- Latch-up protection exceeds 500 mA per JEDEC Std 17
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
- Bus-hold data inputs eliminate the need for external pull-up resistors for unused inputs
- Live insertion/extraction permitted
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVT245BD	–40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LVT245BDB	–40 °C to +85 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74LVT245BPW	–40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74LVT245BBQ	–40 °C to +85 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

### 4. Functional diagram

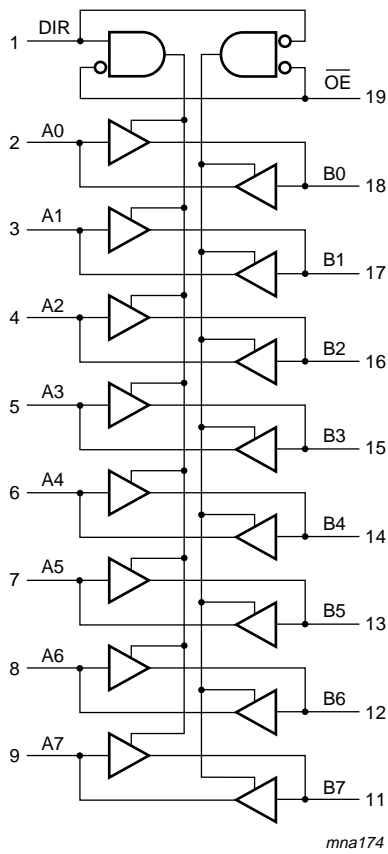


Fig 1. Logic diagram

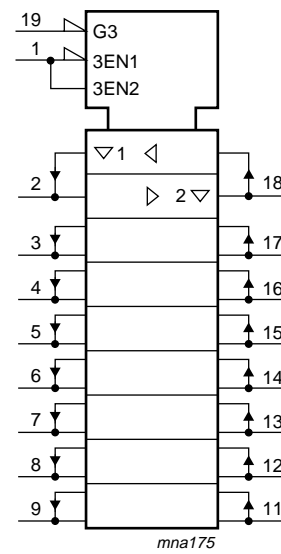
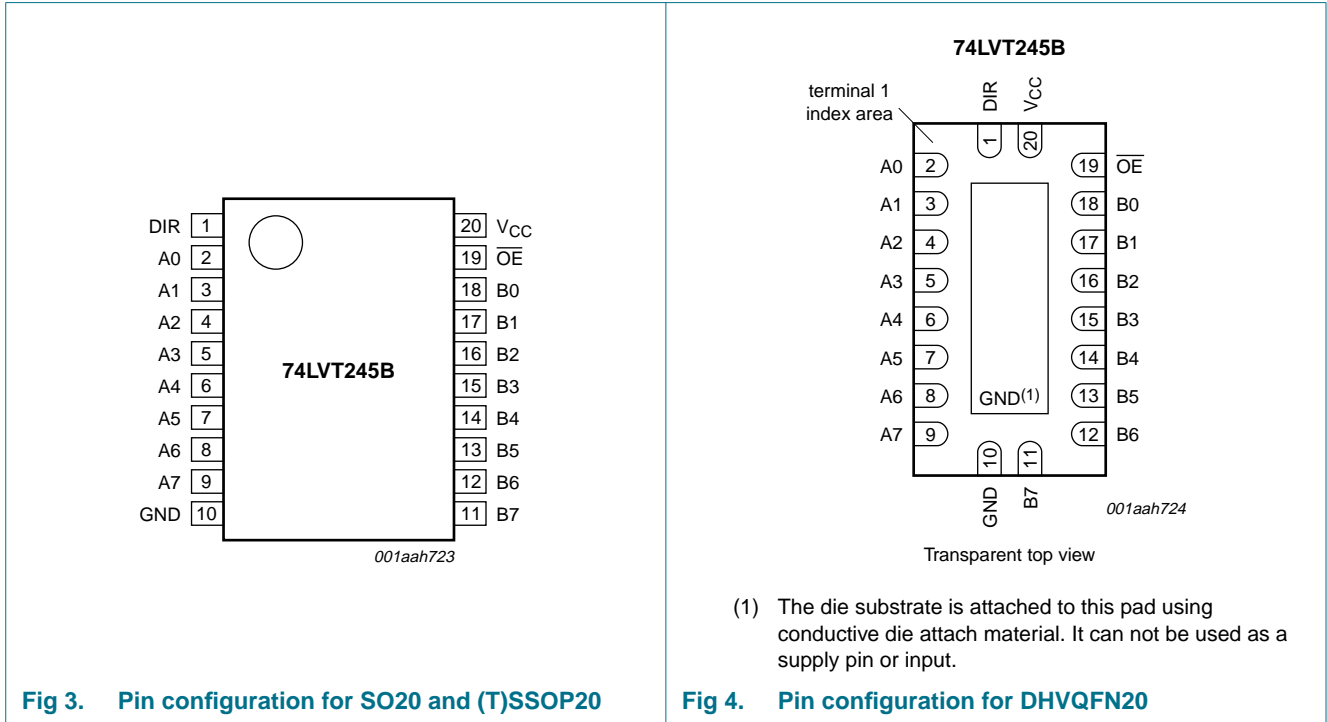


Fig 2. IEC logic symbol

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
DIR	1	direction control
A0 to A7	2, 3, 4, 5, 6, 7, 8, 9	data input/output
GND	10	ground (0 V)
B0 to B7	18, 17, 16, 15, 14, 13, 12, 11	data input/output
OE	19	output enable input (active LOW)
V <sub>CC</sub>	20	supply voltage

## 6. Functional description

**Table 3. Function selection**

Inputs		Inputs/outputs		
$\overline{\text{OE}}$	DIR	An	Bn	
L	L	An = Bn	inputs	
L	H	inputs	Bn = An	
H	X	Z	Z	

- [1] H = HIGH voltage level;  
 L = LOW voltage level;  
 X = don't care;  
 Z = high impedance OFF-state.

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).<sup>[1][2]</sup>

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+4.6	V
$V_I$	input voltage		<sup>[3]</sup> -0.5	+7.0	V
$V_O$	output voltage	output in OFF or HIGH state	<sup>[3]</sup> -0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < 0$	-50	-	mA
$I_{OK}$	output clamping current	$V_O < 0$	-50	-	mA
$I_O$	output current	output in LOW state	-	128	mA
		output in HIGH state	-64	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature		<sup>[2]</sup> -	150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C to }+85\text{ °C}$	<sup>[4]</sup> -	500	mW

- [1] Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- [2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
- [3] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
- [4] For SO20 packages: above 70 °C derate linearly with 8 mW/K.  
 For SSOP20 and TSSOP20 packages: above 60 °C derate linearly with 5.5 mW/K.  
 For DHVQFN20 packages: above 60 °C derate linearly with 4.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		2.7	3.6	V
$V_I$	input voltage		0	5.5	V
$I_{OH}$	HIGH-level output current		-	-32	mA
$I_{OL}$	LOW-level output current		-	32	mA
		current duty cycle $\leq 50\%$ ; $f_i \geq 1$ kHz	-	64	mA
$T_{amb}$	ambient temperature	in free air	-40	+85	$^{\circ}\text{C}$
$\Delta t/\Delta V$	input transition rise and fall rate	output enabled	0	10	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$			Unit
			Min	Typ <sup>[1]</sup>	Max	
$V_{IK}$	input clamping voltage	$V_{CC} = 2.7$ V; $I_{IK} = -18$ mA	-1.2	-0.9	-	V
$V_{IH}$	HIGH-level input voltage		2.0	-	-	V
$V_{IL}$	LOW-level input voltage		-	-	0.8	
$V_{OH}$	HIGH-level output voltage	$V_{CC} = 2.7$ V to 3.6 V; $I_{OH} = -100$ $\mu\text{A}$	$V_{CC} - 0.2$	$V_{CC} - 0.1$	-	V
		$V_{CC} = 2.7$ V; $I_{OH} = -8$ mA	2.4	2.5	-	
		$V_{CC} = 3.0$ V; $I_{OH} = -32$ mA	2.0	2.2	-	V
$V_{OL}$	LOW-level output voltage	$V_{CC} = 2.7$ V; $I_{OL} = 100$ $\mu\text{A}$		0.1	0.2	V
		$V_{CC} = 2.7$ V; $I_{OL} = 24$ mA	-	0.3	0.5	V
		$V_{CC} = 3.0$ V; $I_{OL} = 16$ mA	-	0.25	0.4	V
		$V_{CC} = 3.0$ V; $I_{OL} = 32$ mA	-	0.3	0.5	V
		$V_{CC} = 3.0$ V; $I_{OL} = 64$ mA	-	0.4	0.55	V
$I_I$	input leakage current	control pins				
		$V_{CC} = 0$ V or 3.6 V; $V_I = 5.5$ V	-	1	10	$\mu\text{A}$
		$V_{CC} = 3.6$ V; $V_I = V_{CC}$ or GND	-	$\pm 0.1$	$\pm 1$	$\mu\text{A}$
		I/O data pins <sup>[2]</sup>				
		$V_{CC} = 3.6$ V; $V_I = 5.5$ V	-	1	20	$\mu\text{A}$
		$V_{CC} = 3.6$ V; $V_I = V_{CC}$	-	0.1	1	$\mu\text{A}$
		$V_{CC} = 3.6$ V; $V_I = 0$ V	-5	-1	-	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	$V_{CC} = 0$ V; $V_I$ or $V_O = 0$ V to 4.5 V	-	1	$\pm 100$	$\mu\text{A}$
$I_{LO}$	output leakage current	$V_O = 5.5$ V; $V_{CC} = 3.6$ V; output HIGH	-	60	125	$\mu\text{A}$
$I_{O(pu/pd)}$	power-up/power-down output current	$V_{CC} \leq 1.2$ V $V_O = 0.5$ V to $V_{CC}$ ; $V_I = \text{GND}$ or $V_{CC}$ ; $\overline{OE} = \text{don't care}$	<sup>[3]</sup> -	15	$\pm 100$	$\mu\text{A}$
$I_{BHL}$	bus hold LOW current	$V_{CC} = 3.0$ V; $V_I = 0.8$ V	<sup>[4]</sup> 75	150	-	$\mu\text{A}$
$I_{BHH}$	bus hold HIGH current	$V_{CC} = 3.0$ V; $V_I = 2.0$ V	-150	-75	-	$\mu\text{A}$
$I_{BHLO}$	bus hold LOW overdrive current	$V_{CC} = 0$ V to 3.0 V; $V_I = 3.6$ V	500	-	-	$\mu\text{A}$

**Table 6.** Static characteristics ...continued

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ <sup>[1]</sup>	Max	
$I_{BHHO}$	bus hold HIGH overdrive current	$V_{CC} = 0 \text{ V to } 3.0 \text{ V}; V_I = 3.6 \text{ V}$	-	-	-500	$\mu\text{A}$
$I_{CC}$	supply current	$V_{CC} = 3.6 \text{ V}; V_I = V_{CC} \text{ or } \text{GND}; I_O = 0 \text{ A}$				
		outputs HIGH	-	0.13	0.19	mA
		outputs LOW	-	3	12	mA
		outputs disabled	-	0.13	0.19	mA
$\Delta I_{CC}$	additional supply current	per input pin; $V_{CC} = 3.0 \text{ V to } 3.6 \text{ V};$ one input = $V_{CC} - 0.6 \text{ V}$ others = $V_{CC}$ or GND <sup>[5]</sup>	-	0.1	0.2	mA
$C_I$	input capacitance	DIR and $\overline{OE}$ inputs; $V_I = 0 \text{ V or } 3.0 \text{ V}$	-	4	-	pF
$C_{I/O}$	input/output capacitance	at input/output data pins, outputs disabled; $V_{I/O} = 0 \text{ V or } 3.0 \text{ V}$	-	10	-	pF

[1] All typical values are measured at  $V_{CC} = 3.3 \text{ V}$  (unless stated otherwise) and  $T_{amb} = 25 \text{ }^\circ\text{C}$ .[2] Unused pins at  $V_{CC}$  or GND.[3] This parameter is valid for any  $V_{CC}$  between 0 V and 1.2 V with a transition time of up to 10 ms. From  $V_{CC} = 1.2 \text{ V}$  to  $V_{CC} = 3.6 \text{ V}$  a transition time of 100 ms is permitted. This parameter is valid for  $T_{amb} = +25 \text{ }^\circ\text{C}$  only.

[4] This is the bus hold overdrive current required to force the input to the opposite logic state.

[5] This is the increase in supply current for each input at the specified voltage level other than  $V_{CC}$  or GND.

## 10. Dynamic characteristics

**Table 7.** Dynamic characteristicsVoltages are referenced to GND (ground = 0 V). For test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ <sup>[1]</sup>	Max	
$t_{PLH}$	LOW to HIGH propagation delay	An to Bn or Bn to An				
		$V_{CC} = 2.7 \text{ V}$	-	-	4.0	ns
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1.2	2.4	3.5	ns
$t_{PHL}$	HIGH to LOW propagation delay	An to Bn or Bn to An				
		$V_{CC} = 2.7 \text{ V}$	-	-	4.0	ns
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1.2	2.4	3.5	ns
$t_{PZH}$	OFF-state to HIGH propagation delay	see <a href="#">Figure 6</a>				
		$V_{CC} = 2.7 \text{ V}$	-	-	7.1	ns
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1.3	3.3	5.5	ns
$t_{PZL}$	OFF-state to LOW propagation delay	see <a href="#">Figure 6</a>				
		$V_{CC} = 2.7 \text{ V}$	-	-	6.5	ns
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1.7	3.2	5.5	ns
$t_{PHZ}$	HIGH to OFF-state propagation delay	see <a href="#">Figure 6</a>				
		$V_{CC} = 2.7 \text{ V}$	-	-	6.5	ns
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	2.2	3.6	5.9	ns

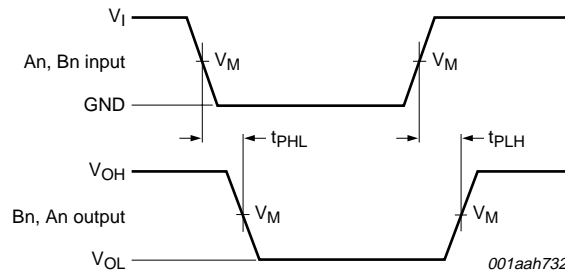
**Table 7. Dynamic characteristics ...continued**

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ <sup>[1]</sup>	Max	
t <sub>PLZ</sub>	LOW to OFF-state propagation delay	see <a href="#">Figure 6</a>				
		V <sub>CC</sub> = 2.7 V	-	-	5.1	ns
		V <sub>CC</sub> = 3.3 V ± 0.3 V	2.2	3.4	5.0	ns

[1] Typical values are measured at T<sub>amb</sub> = 25 °C and V<sub>CC</sub> = 3.3 V

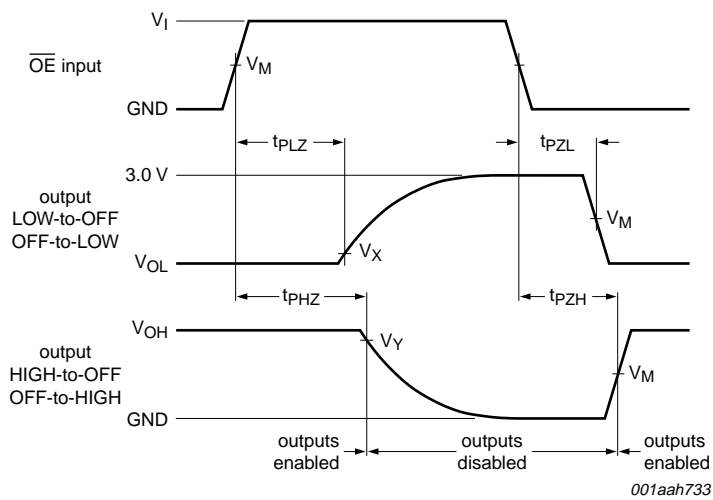
## 11. Waveforms



See [Table 8](#) for measurement points.

V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage levels that occur with the output load.

**Fig 5. Input (An, Bn) to output (Bn, An) propagation delays and output transition times**



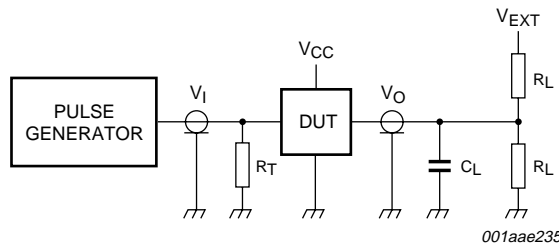
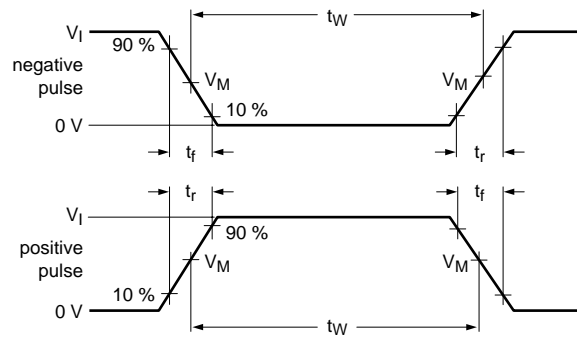
See [Table 8](#) for measurement points.

V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage levels that occur with the output load.

**Fig 6. 3-state output enable and disable times**

Table 8. Measurement points

V <sub>CC</sub>	Input		Output		
	V <sub>IN</sub>	V <sub>M</sub>	V <sub>M</sub>	V <sub>x</sub>	V <sub>y</sub>
2.7 V to 3.6 V	GND to 2.7 V	1.5 V	1.5 V	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> - 0.3 V



Test data is given in [Table 9](#).

Definitions test circuit:

R<sub>L</sub> = Load resistance;

C<sub>L</sub> = Load capacitance including jig and probe capacitance;

R<sub>T</sub> = Termination resistance should be equal to output impedance Z<sub>o</sub> of the pulse generator;

V<sub>EXT</sub> = External voltage for measuring switching times.

Fig 7. Test circuit for switching times

Table 9. Test data

Input				Load		V <sub>EXT</sub>		
V <sub>I</sub>	f <sub>i</sub>	t <sub>w</sub>	t <sub>r</sub> , t <sub>f</sub>	R <sub>L</sub>	C <sub>L</sub>	t <sub>PHZ</sub> , t <sub>PZH</sub>	t <sub>PLZ</sub> , t <sub>PZL</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	500 Ω	50 pF	GND	6 V	open



12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

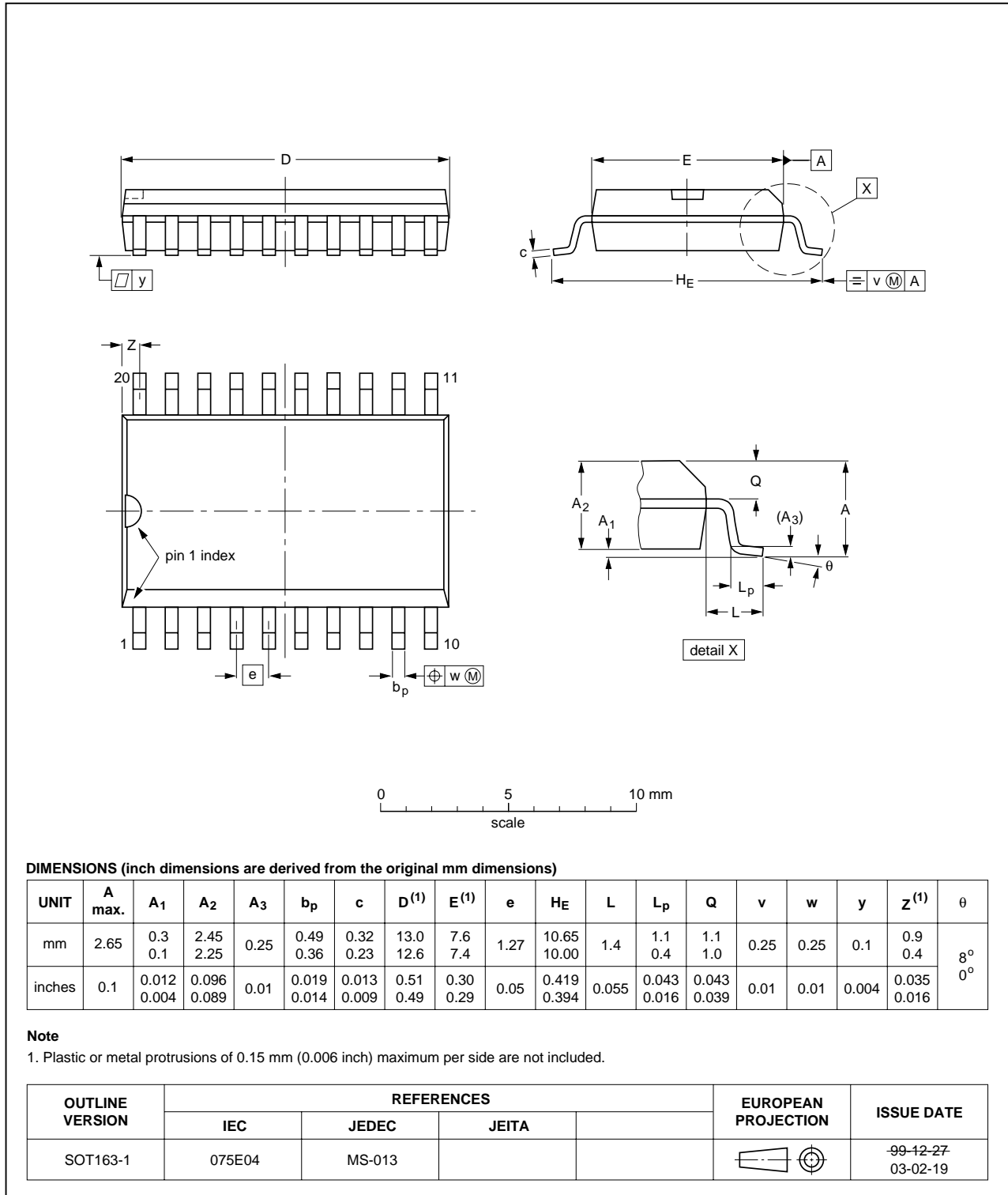


Fig 8. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

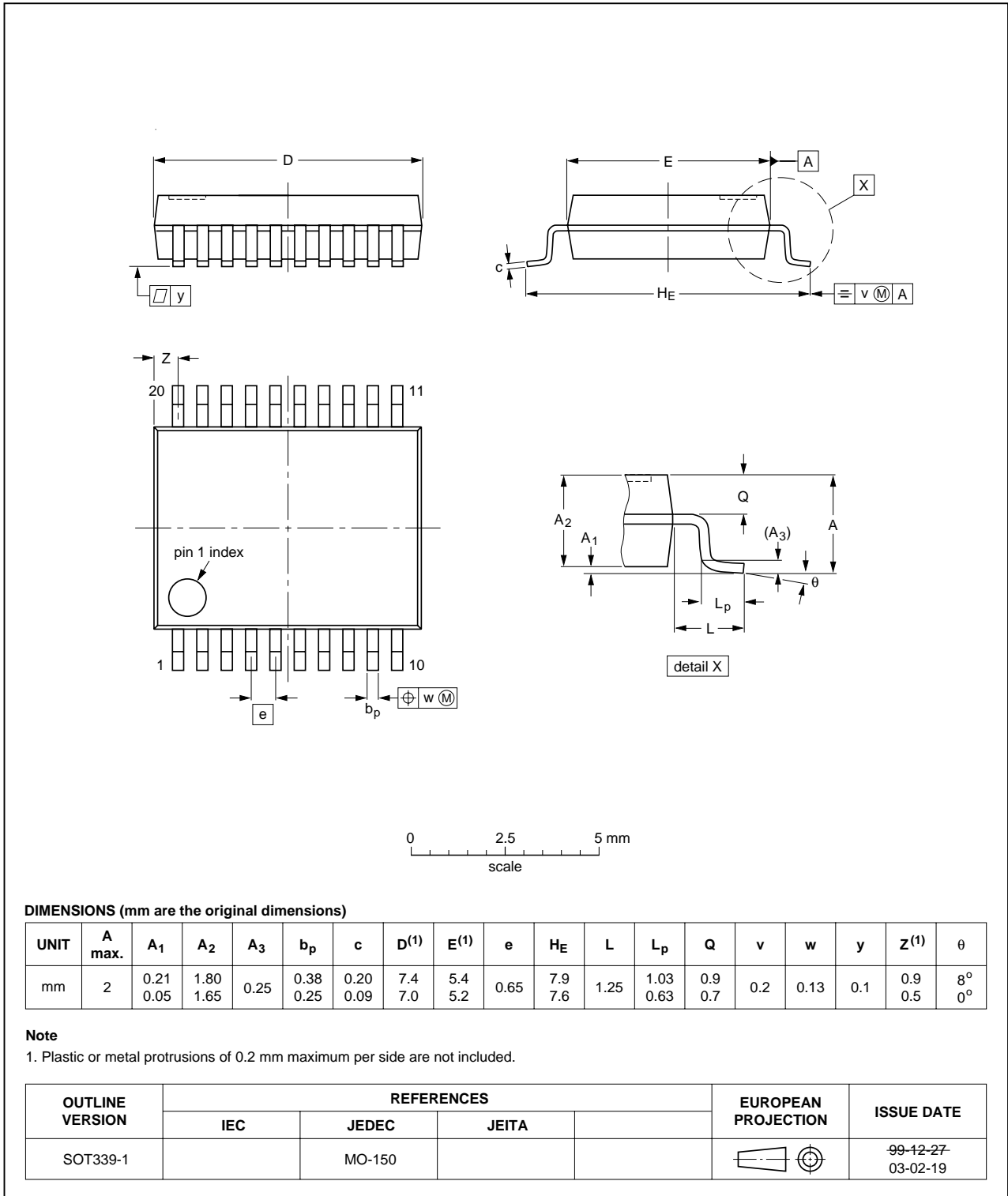


Fig 9. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

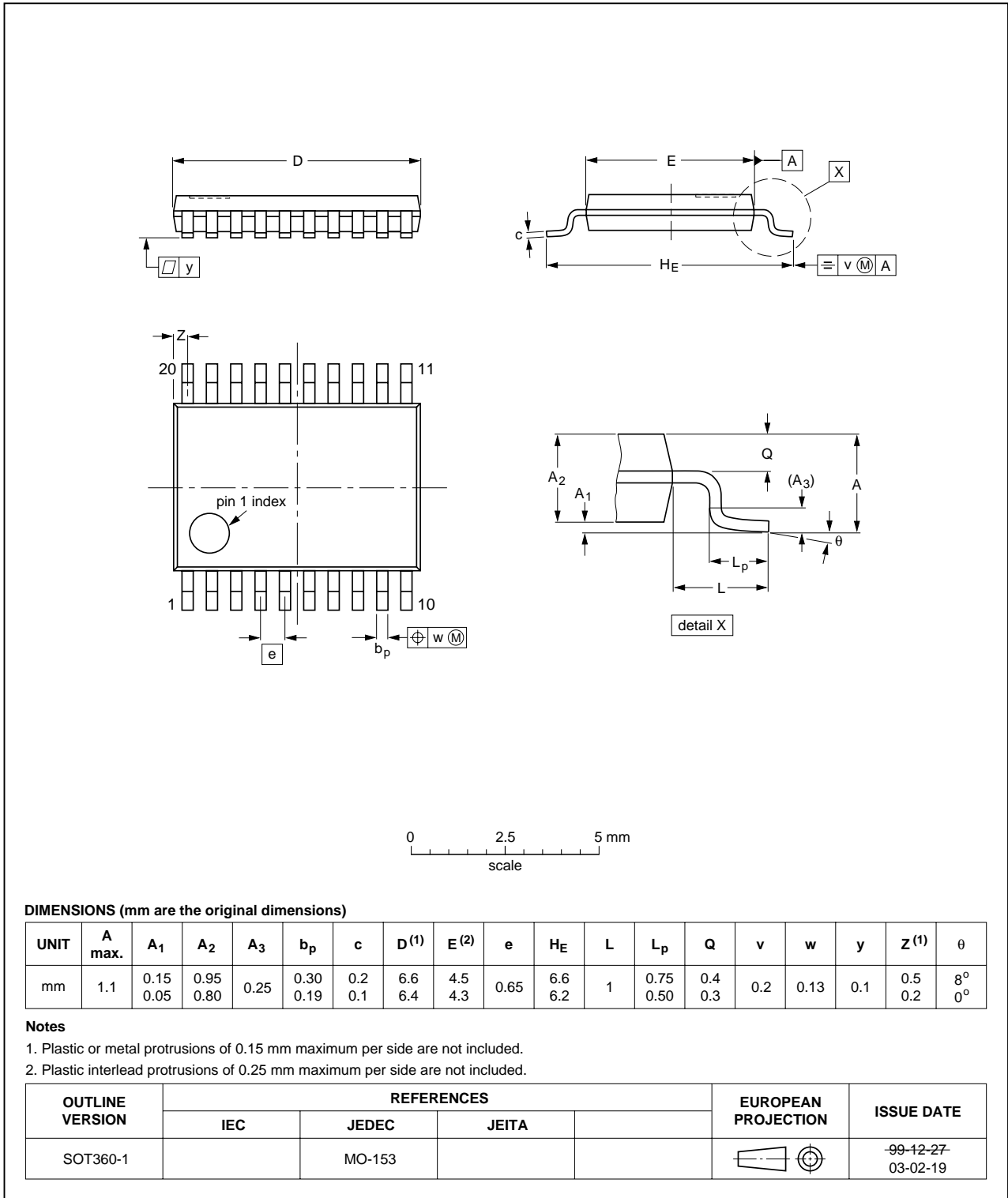


Fig 10. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

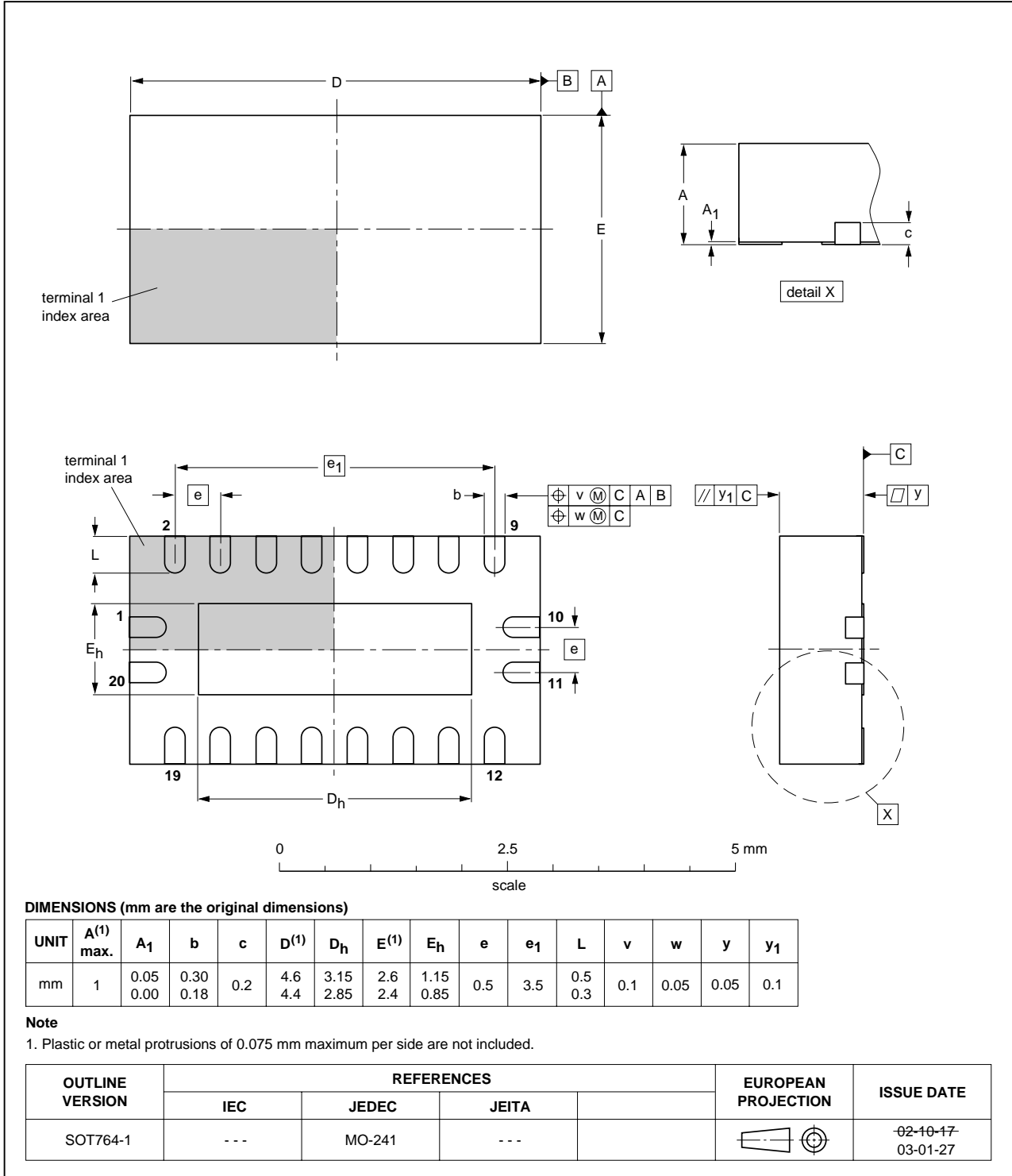


Fig 11. Package outline SOT764-1 (DHVQFN20)

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT245B_2	20080508	Product data sheet	ECN07_046	74LVT245B_1
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>DHVQFN20 package added to <a href="#">Section 3 “Ordering information”</a> and <a href="#">Section 12 “Package outline”</a></li> </ul>			
74LVT245B_1	19990319	Product specification	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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