



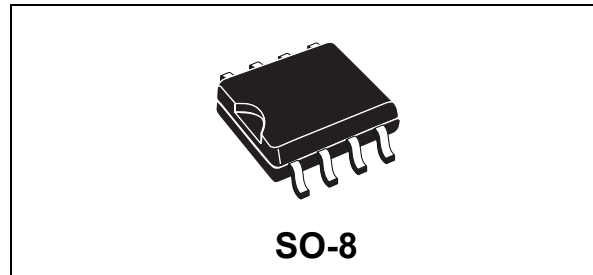
VNS3NV04DP-E

OMNIFET II fully autoprotected Power MOSFET

Features

| | | |
|-----------------------------------|-------------|----------------|
| Max on-state resistance (per ch.) | R_{ON} | 120 m Ω |
| Current limitation (typ) | I_{LIMH} | 3.5 A |
| Drain-source clamp voltage | V_{CLAMP} | 40 V |

- ECOPACK®: lead free and RoHS compliant
- Automotive Grade: compliance with AEC guidelines
- Linear current limitation
- Thermal shutdown
- Short circuit protection
- Integrated clamp
- Low current drawn from input pin
- Diagnostic feedback through input pin
- ESD protection
- Direct access to the gate of the Power MOSFET (analog driving)
- Compatible with standard Power MOSFET



Description

The VNS3NV04DP-E device is made up of two monolithic chips (OMNIFET II) housed in a standard SO-8 package. The OMNIFET II is designed using STMicroelectronics™ VIPower™ M0-3 technology and is intended for replacement of standard Power MOSFETs in up to 50 kHz DC applications.

Built-in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments.

Fault feedback can be detected by monitoring voltage at the input pin

Table 1. Device summary

| Package | Order codes | |
|---------|--------------|----------------|
| | Tube | Tape and reel |
| SO-8 | VNS3NV04DP-E | VNS3NV04DPTR-E |

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1 Block diagram and pin description

Figure 1. Block diagram

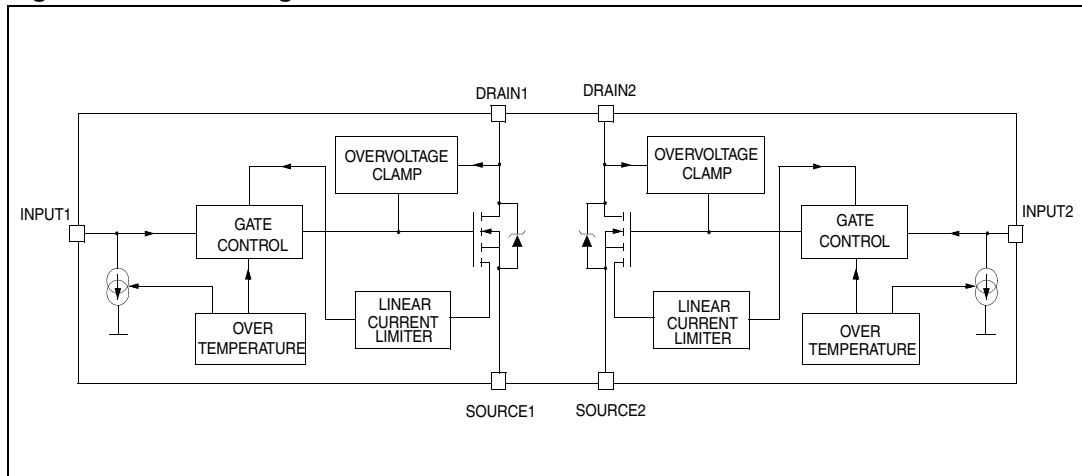
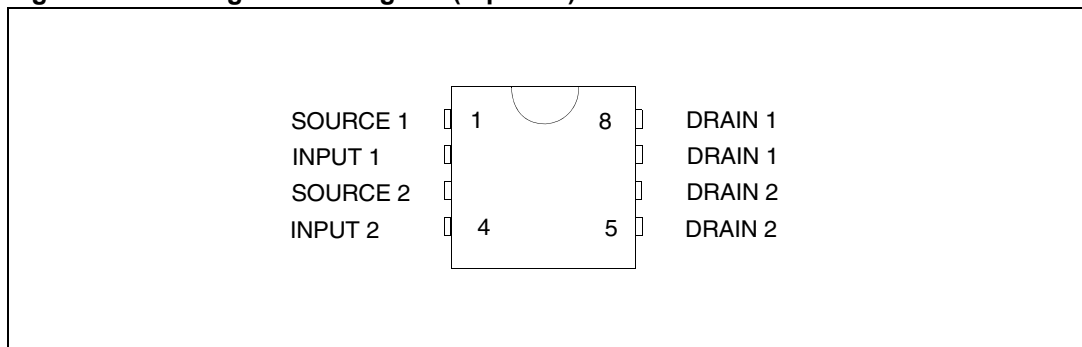
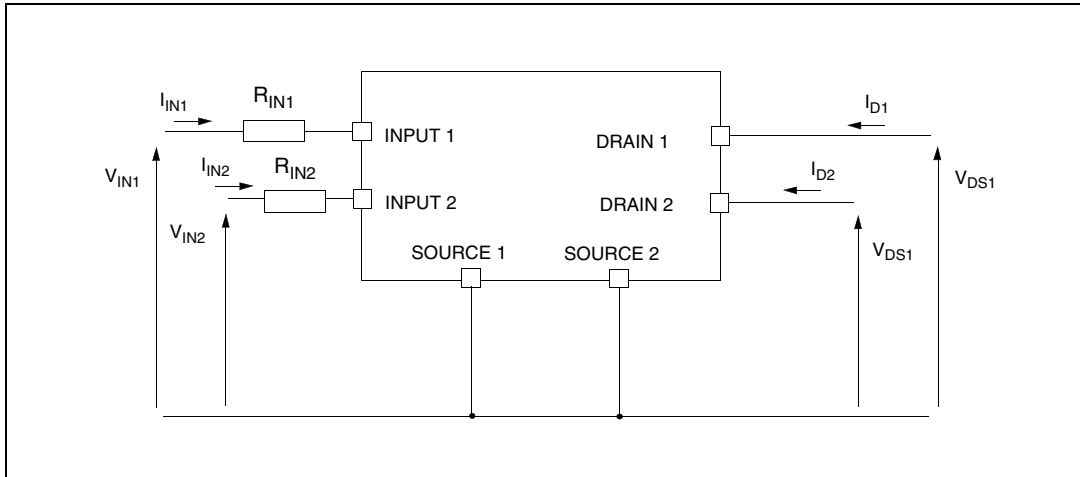


Figure 2. Configuration diagram (top view)



2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to Absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality document.

Table 2. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|----------------|---|--------------------|------------------|
| V_{DSn} | Drain-Source Voltage ($V_{INn} = 0\text{ V}$) | Internally clamped | V |
| V_{INn} | Input voltage | Internally clamped | V |
| I_{INn} | Input current | +/- 20 | mA |
| $R_{IN\ MINn}$ | Minimum input series impedance | 220 | Ω |
| I_{Dn} | Drain current | Internally limited | A |
| I_{Rn} | Reverse DC output current | -5.5 | A |
| V_{ESD1} | Electrostatic discharge ($R = 1.5\text{ K}\Omega$, $C = 100\text{ pF}$) | 4000 | V |
| V_{ESD2} | Electrostatic discharge on output pins only ($R = 330\ \Omega$, $C = 150\text{ pF}$) | 16500 | V |
| P_{tot} | Total dissipation at $T_c = 25\text{ }^\circ\text{C}$ | 4 | Ω |
| T_j | Operating junction temperature | Internally limited | $^\circ\text{C}$ |
| T_c | Case operating temperature | Internally limited | $^\circ\text{C}$ |
| T_{stg} | Storage temperature | -55 to 150 | $^\circ\text{C}$ |

2.2 Thermal data

Table 3. Thermal data

| Symbol | Parameter | Max value | Unit |
|----------------|--|-------------------|------|
| $R_{thj-lead}$ | Thermal resistance junction-lead (per channel) | 30 | °C/W |
| $R_{thj-amb}$ | Thermal resistance junction-ambient | 80 ⁽¹⁾ | °C/W |

1. When mounted on a standard single-sided FR4 board with 50mm² of Cu (at least 35 μm thick) connected to all DRAIN pins of the relative channel

2.3 Electrical characteristics

Values specified in this section are for $-40\text{ °C} < T_j < 150\text{ °C}$, unless otherwise stated.

Table 4. Off

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|-------------|--|---|-----|-----|------|------|
| V_{CLAMP} | Drain-source clamp voltage | $V_{IN} = 0\text{ V}; I_D = 1.5\text{ A}$ | 40 | 45 | 55 | V |
| V_{CLTH} | Drain-source clamp threshold voltage | $V_{IN} = 0\text{ V}; I_D = 2\text{ mA}$ | 36 | | | V |
| V_{INTH} | Input threshold voltage | $V_{DS} = V_{IN}; I_D = 1\text{ mA}$ | 0.5 | | 2.5 | V |
| I_{ISS} | Supply current from input pin | $V_{DS} = 0\text{ V}; V_{IN} = 5\text{ V}$ | | 100 | 150 | μA |
| V_{INCL} | Input-source clamp voltage | $I_{IN} = 1\text{ mA}$ | 6 | 6.8 | 8 | V |
| | | $I_{IN} = -1\text{ mA}$ | -1 | | -0.3 | V |
| I_{DSS} | Zero input voltage drain current ($V_{IN} = 0\text{ V}$) | $V_{DS} = 13\text{ V}; V_{IN} = 0\text{ V}; T_j = 25\text{ °C}$ | | | 30 | μA |
| | | $V_{DS} = 25\text{ V}; V_{IN} = 0\text{ V}$ | | | 75 | μA |

Table 5. On

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|--------------|-----------------------------------|---|-----|-----|-----|------|
| $R_{DS(on)}$ | Static drain-source on resistance | $V_{IN} = 5\text{ V}; I_D = 1.5\text{ A}; T_j = 25\text{ °C}$ | — | — | 120 | mΩ |
| | | $V_{IN} = 5\text{ V}; I_D = 1.5\text{ A}$ | — | — | 240 | mΩ |

$T_j = 25\text{ °C}$, unless otherwise specified

Table 6. Dynamic

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|----------------|--------------------------|---|-----|-----|-----|------|
| $g_{fs}^{(1)}$ | Forward transconductance | $V_{DD} = 13\text{ V}; I_D = 1.5\text{ A}$ | — | 5.0 | — | S |
| C_{OSS} | Output capacitance | $V_{DS} = 13\text{ V}; f = 1\text{ MHz}; V_{IN} = 0\text{ V}$ | — | 150 | — | pF |

Table 7. Switching

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|----------------|-----------------------|--|-----|------|------|------------------------|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = 15\text{ V}; I_D = 1.5\text{ A};$ $V_{gen} = 5\text{ V}; R_{gen} = R_{IN}$ $MIN = 220\ \Omega$ (see Figure 4) | | 90 | 300 | ns |
| t_r | Rise time | | | 250 | 750 | ns |
| $t_{d(off)}$ | Turn-off delay time | | | 450 | 1350 | ns |
| t_f | Fall time | | | 250 | 750 | ns |
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = 15\text{ V}; I_D = 1.5\text{ A};$ $V_{gen} = 5\text{ V}; R_{gen} = 2.2\text{ K}\Omega$ (see Figure 4) | | 0.45 | 1.35 | μs |
| t_r | Rise time | | | 2.5 | 7.5 | μs |
| $t_{d(off)}$ | Turn-off delay time | | | 3.3 | 10.0 | μs |
| t_f | Fall time | | | 2.0 | 6.0 | μs |
| $(di/dt)_{on}$ | Turn-on current slope | $V_{DD} = 15\text{ V}; I_D = 1.5\text{ A};$ $V_{gen} = 5\text{ V};$ $R_{gen} = R_{IN\ MIN} = 220\ \Omega$ | | 4.7 | | $\text{A}/\mu\text{s}$ |
| Q_i | Total input charge | $V_{DD} = 12\text{ V}; I_D = 1.5\text{ A}; V_{IN} = 5\text{ V};$ $I_{gen} = 2.13\text{ mA}$ (see Figure 7) | | 8.5 | | nC |

Table 8. Source drain diode

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit | |
|----------------|--------------------------|--|-----|-----|-----|------|---------------|
| $V_{SD}^{(1)}$ | Forward on voltage | $I_{SD} = 1.5\text{ A}; V_{IN} = 0\text{ V}$ | | 0.8 | | V | |
| t_{rr} | Reverse recovery time | $I_{SD} = 1.5\text{ A}; di/dt = 12\text{ A}/\mu\text{s};$ $V_{DD} = 30\text{ V}; L = 200\ \mu\text{H}$ (see Figure 5) | | 107 | | ns | |
| Q_{rr} | Reverse recovery charge | | | | 37 | | μC |
| I_{RRM} | Reverse recovery current | | | | 0.7 | | A |

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

-40 °C < T_j < 150 °C, unless otherwise specified

Table 9. Protections

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|------------|-------------------------------|---|-----|-----|-----|---------------|
| I_{lim} | Drain current limit | $V_{IN} = 5\text{ V}; V_{DS} = 13\text{ V}$ | 3.5 | 5 | 7 | A |
| t_{dlim} | Step response current limit | $V_{IN} = 5\text{ V}; V_{DS} = 13\text{ V}$ | | 10 | | μs |
| T_{jsh} | Overtemperature shutdown | | 150 | 175 | 200 | °C |
| T_{jrs} | Overtemperature reset | | 135 | | | °C |
| I_{gf} | Fault sink current | $V_{IN} = 5\text{ V}; V_{DS} = 13\text{ V}; T_j = T_{jsh}$ | 10 | 15 | 20 | mA |
| E_{as} | Single pulse avalanche energy | Starting $T_j = 25\text{ °C}; V_{DD} = 24\text{ V};$ $V_{IN} = 5\text{ V}; R_{gen} = R_{IN\ MIN} = 220\ \Omega;$ $L = 24\text{ mH}$ (see Figure 6 and Figure 8) | 100 | | | mJ |

Figure 4. Switching time test circuit for resistive load

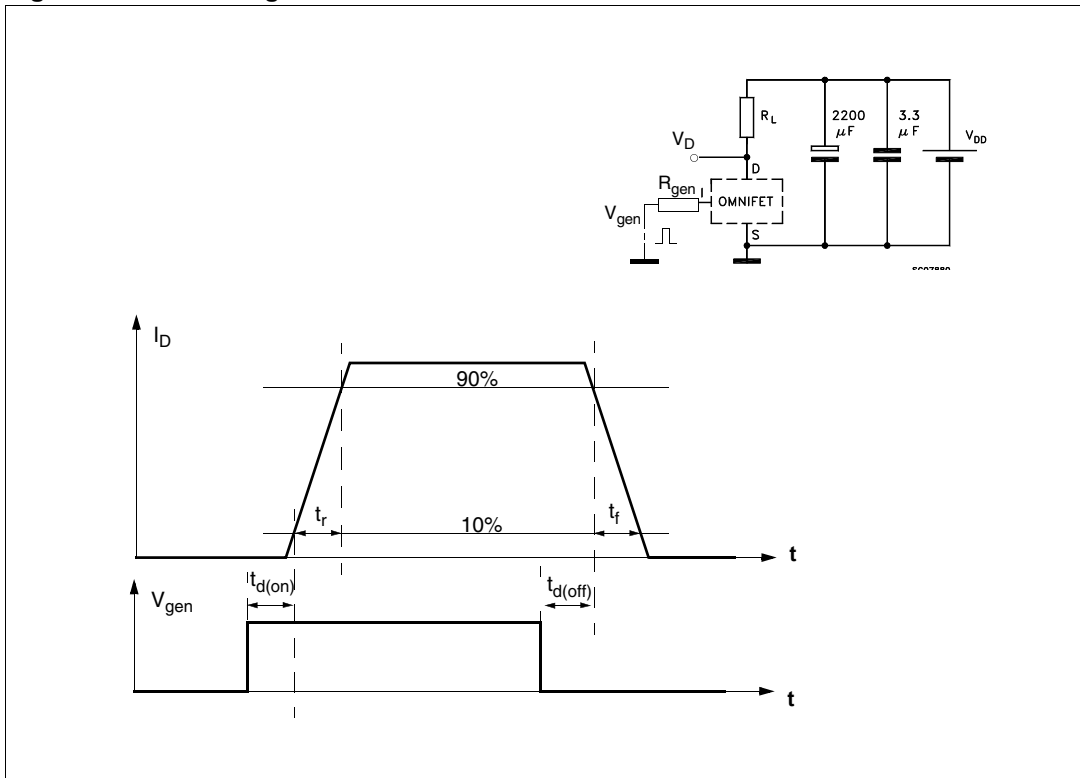


Figure 5. Test circuit for diode recovery times

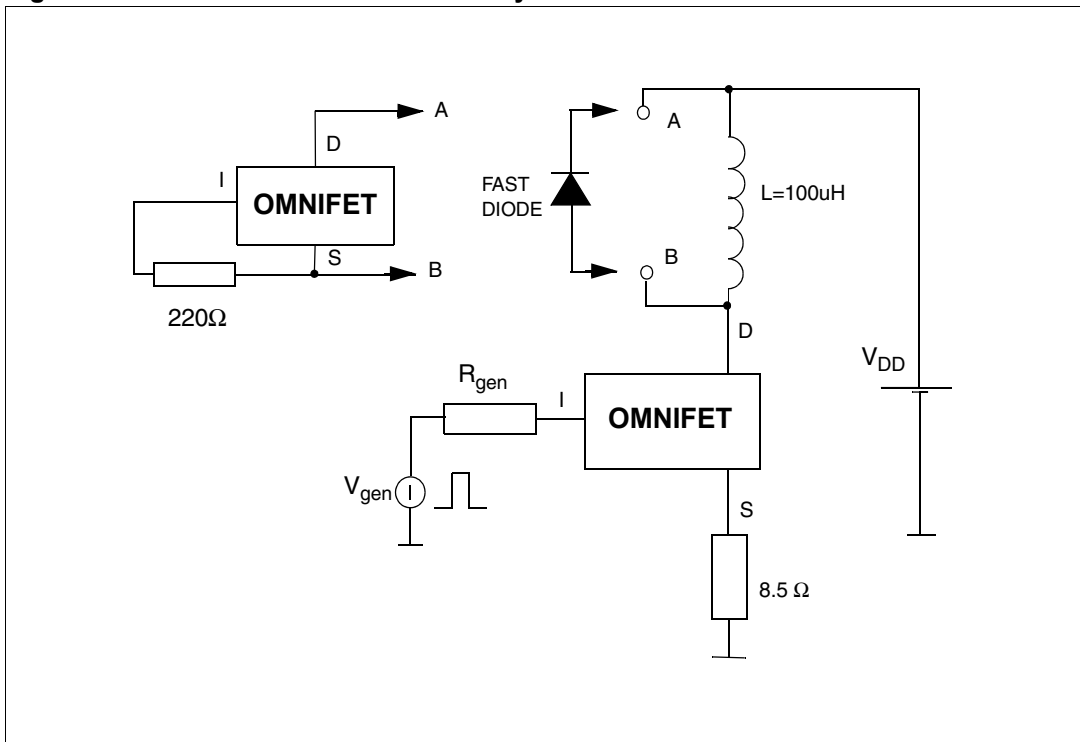


Figure 6. Unclamped inductive load test circuits

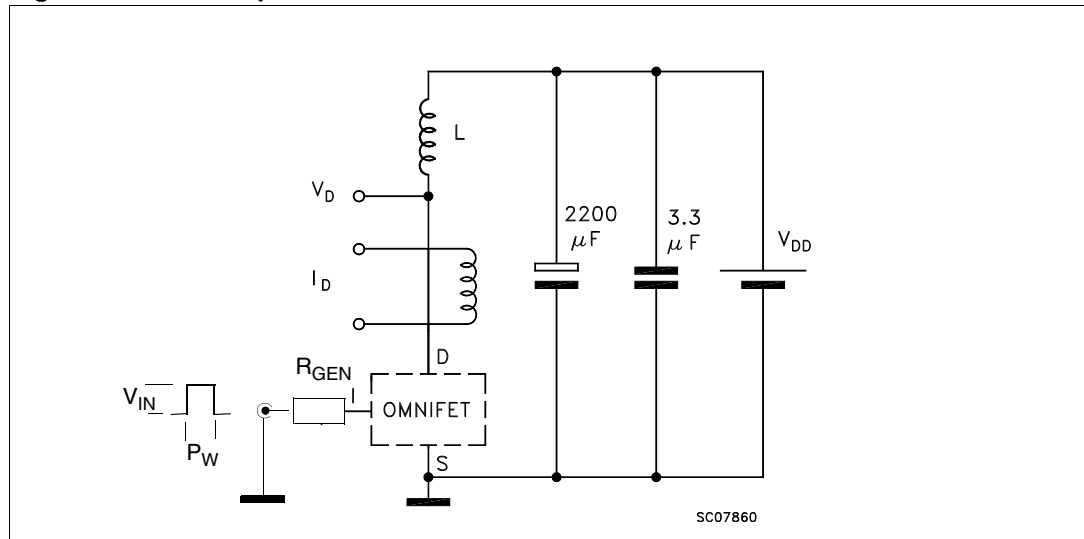


Figure 7. Input charge test circuit

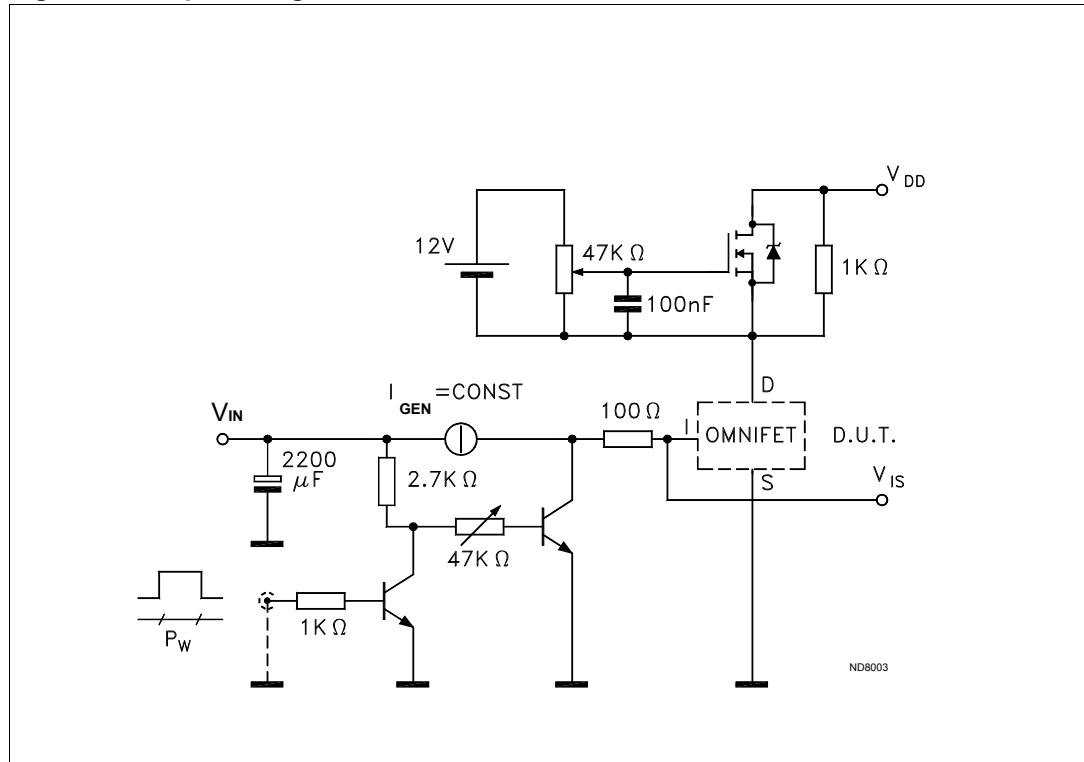
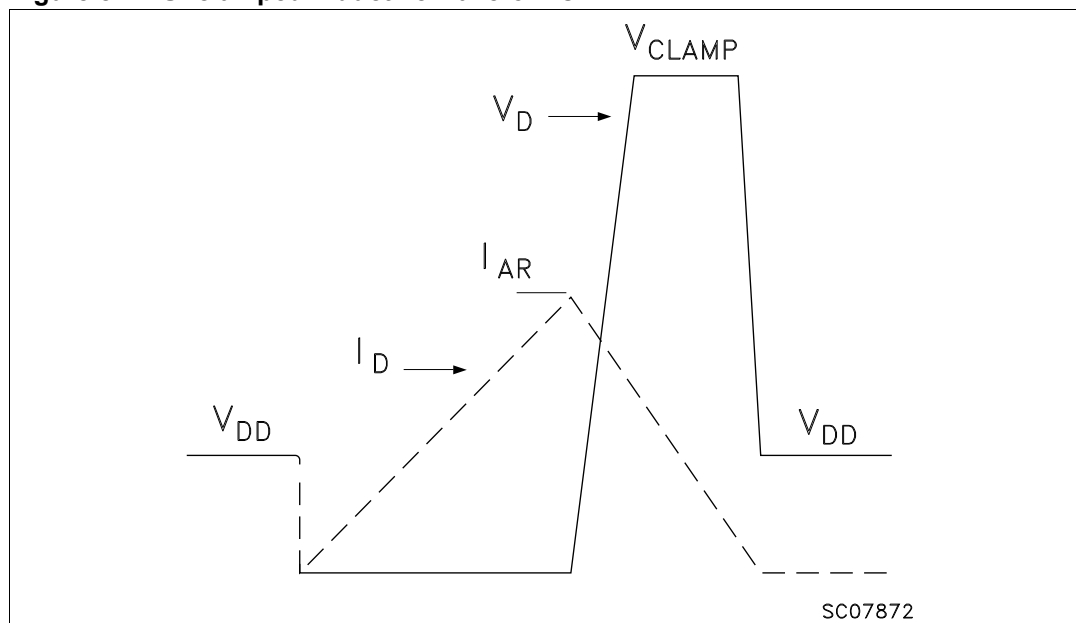


Figure 8. Unclamped inductive waveforms



2.4 Electrical characteristics curves

Figure 9. Source-drain diode forward characteristics

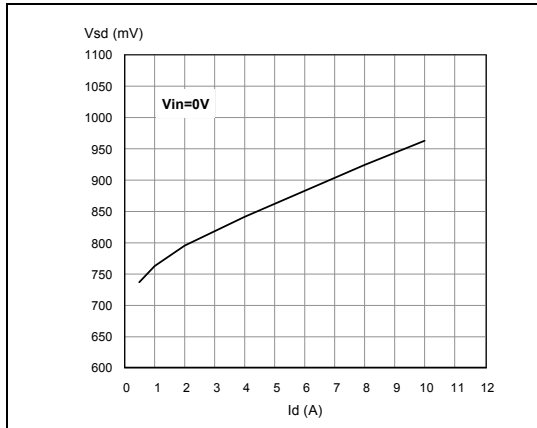


Figure 10. Static drain-source on resistance

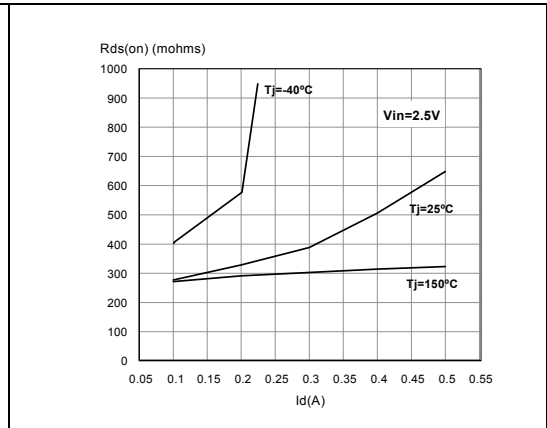


Figure 11. Derating curve

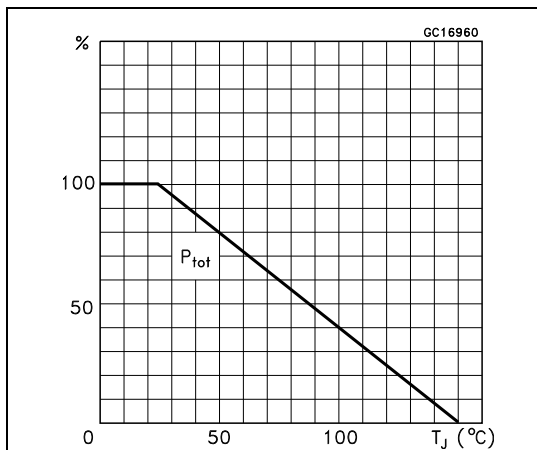


Figure 12. Static drain-source on resistance vs input voltage (part 1)

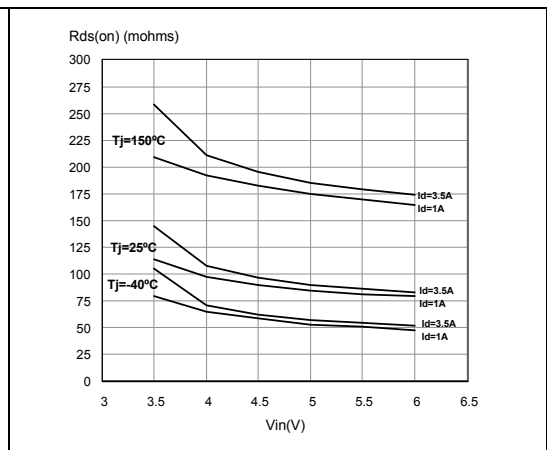


Figure 13. Static drain-source on resistance vs input voltage (part 2)

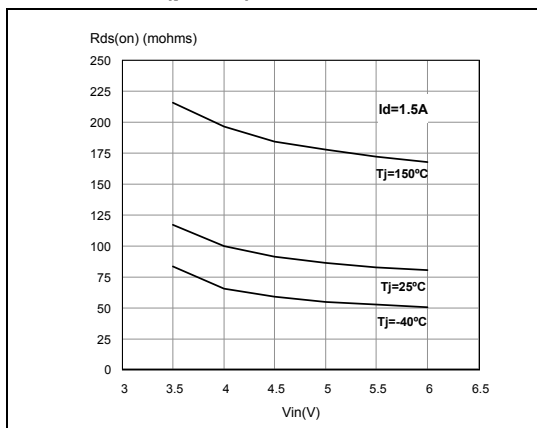


Figure 14. Transconductance

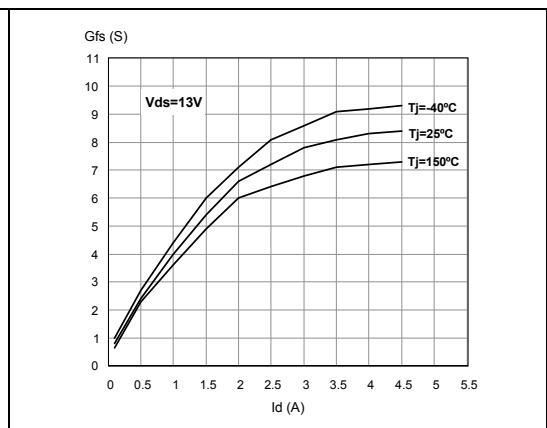


Figure 15. Static drain-source on resistance vs Id

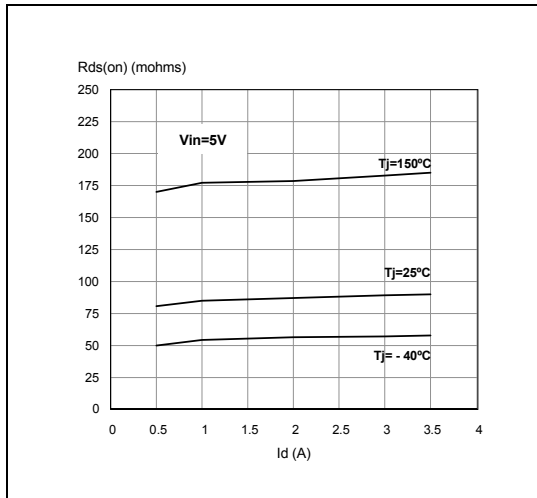


Figure 16. Transfer characteristics

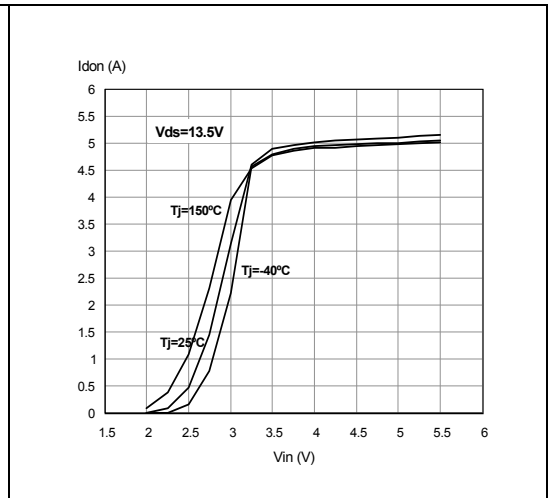


Figure 17. Turn-on current slope (part 1) Figure 18. Turn-on current slope (part 2)

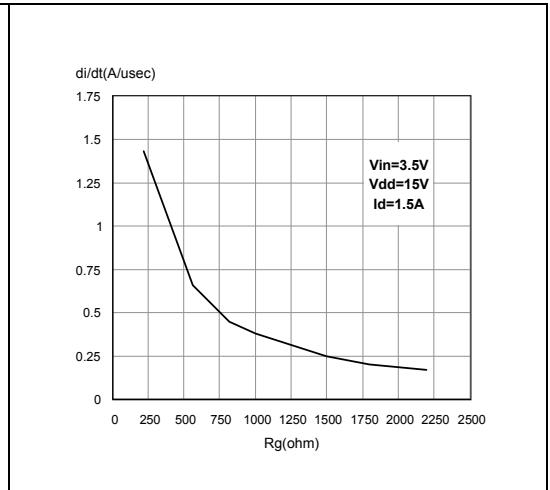
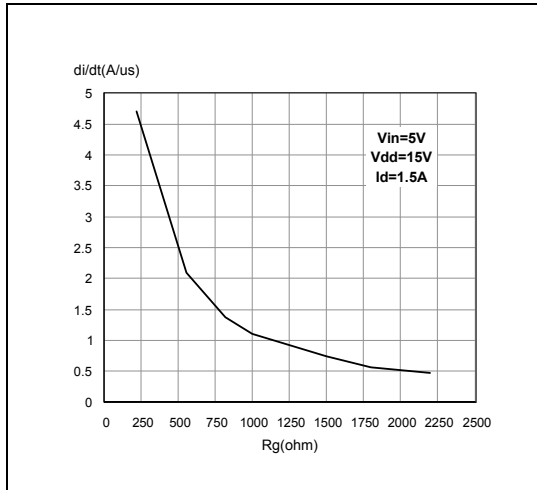


Figure 19. Input voltage vs input charge Figure 20. Turn-off drain source voltage slope (part 1)

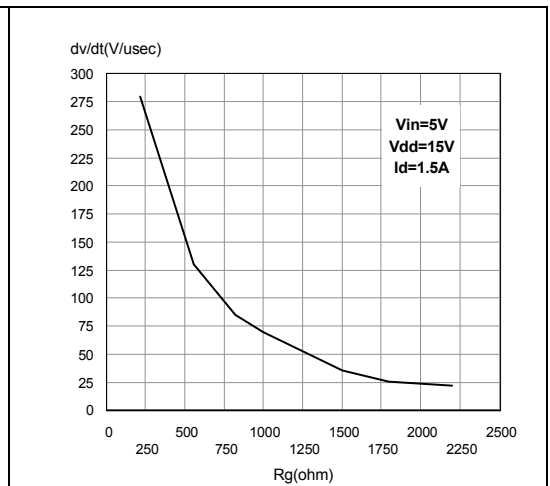
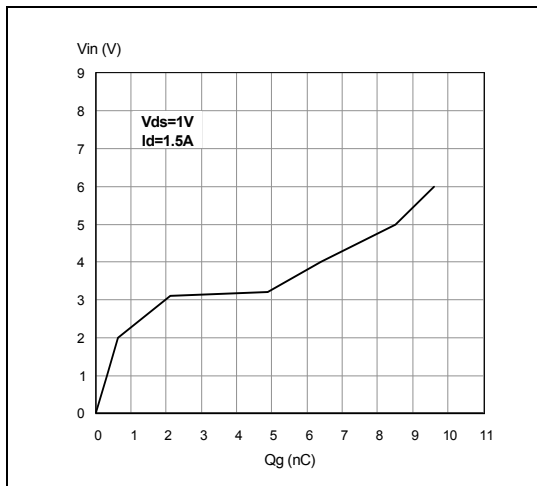


Figure 21. Turn-off drain-source voltage slope (part 2) **Figure 22. Capacitance variations**

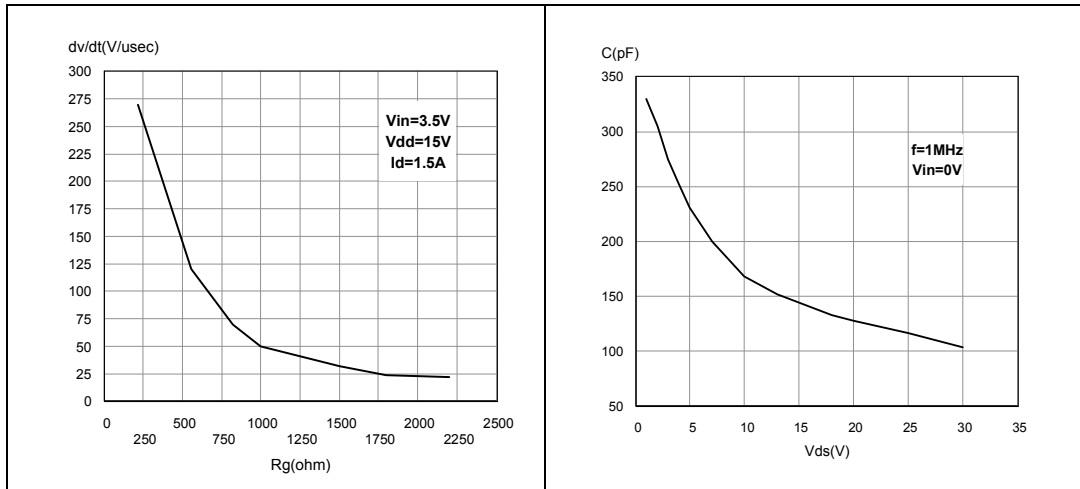


Figure 23. Switching time resistive load (part 1) **Figure 24. Switching time resistive load (part 1)**

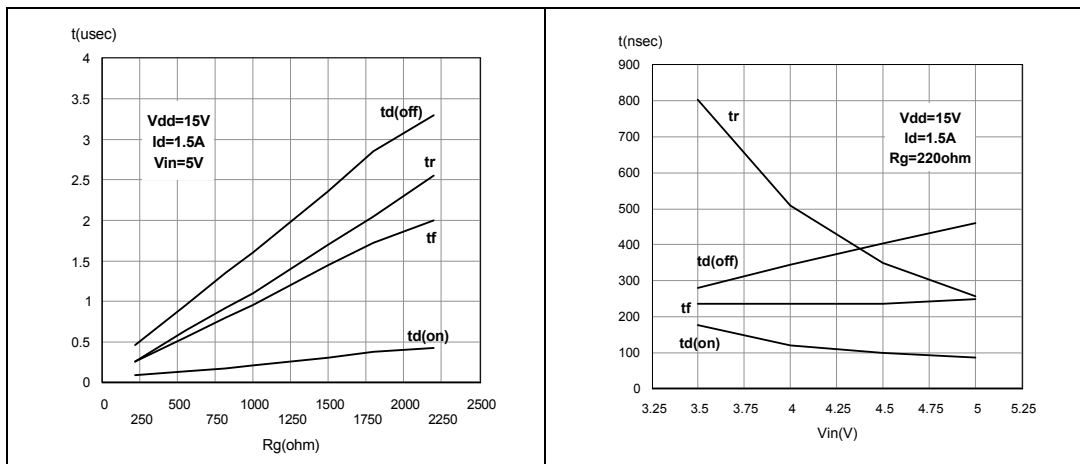


Figure 25. Output characteristics **Figure 26. Normalized on resistance vs temperature**

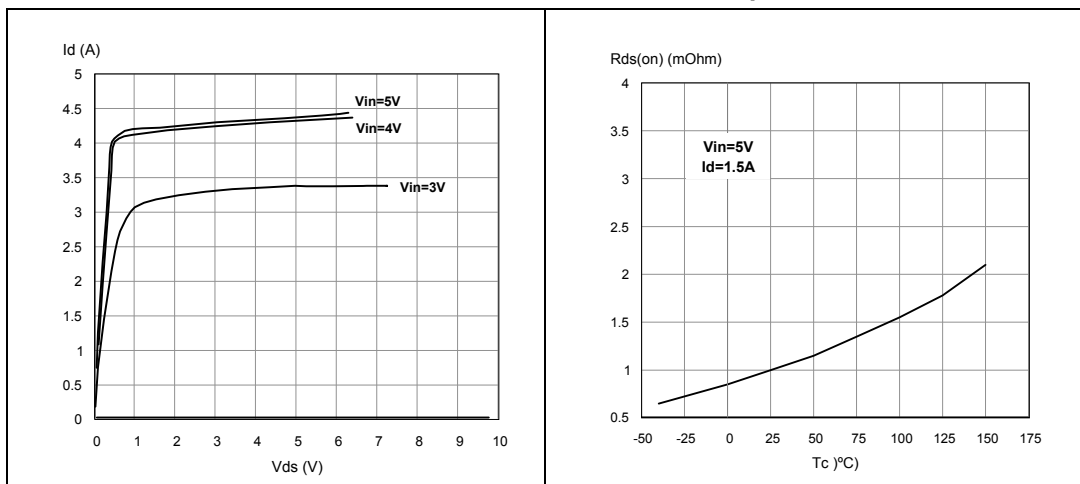


Figure 27. Normalized input threshold voltage vs temperature

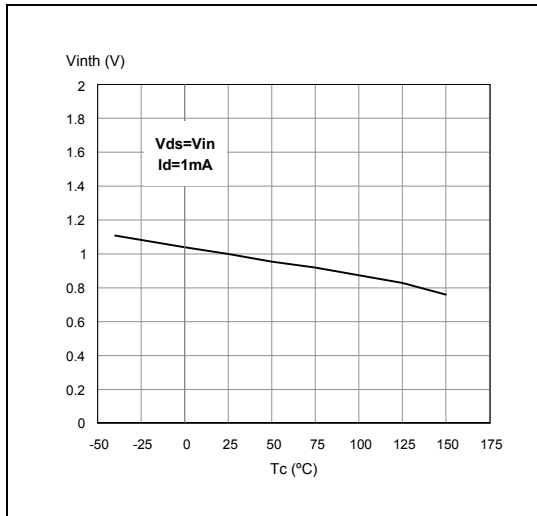


Figure 28. Normalized current limit vs junction temperature

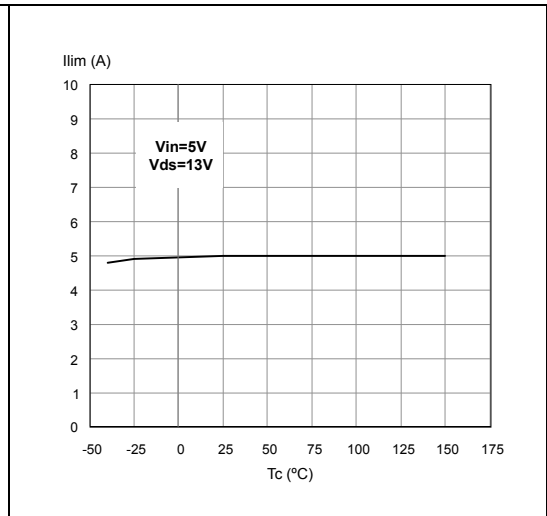
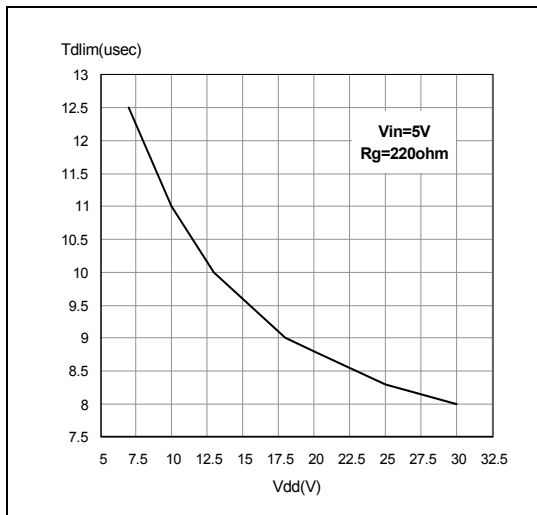


Figure 29. Step response current limit



3 Protection features

During normal operation, the INPUT pin is electrically connected to the gate of the internal power MOSFET through a low impedance path.

The device then behaves like a standard power MOSFET and can be used as a switch from DC up to 50 KHz. The only difference from the user's standpoint is that a small DC current I_{ISS} (typ. 100 μ A) flows into the INPUT pin in order to supply the internal circuitry.

The following sections describe the device features.

3.1 Overvoltage clamp protection

Internally set at 45 V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.

3.2 Linear current limiter circuit

Limits the drain current I_D to I_{lim} whatever the INPUT pin voltages. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the overtemperature threshold T_{jsh} .

3.3 Overtemperature and short circuit protection

These are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Overtemperature cutout occurs in the range 150 to 190 °C, a typical value being 170 °C. The device is automatically restarted when the chip temperature falls of about 15 °C below shutdown temperature.

3.4 Status feedback

In the case of an overtemperature fault condition ($T_j > T_{jsh}$), the device tries to sink a diagnostic current I_{gf} through the INPUT pin in order to indicate fault condition. If driven from a low impedance source, this current may be used in order to warn the control circuit of a device shutdown. If the drive impedance is high enough so that the INPUT pin driver is not able to supply the current I_{gf} , the INPUT pin falls to 0 V. This however not affects the device operation: no requirement is put on the current capability of the INPUT pin driver except to be able to supply the normal operation drive current I_{ISS} .

Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL Logic circuit.

4 Package and packing information

4.1 ECOPACK[®] packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

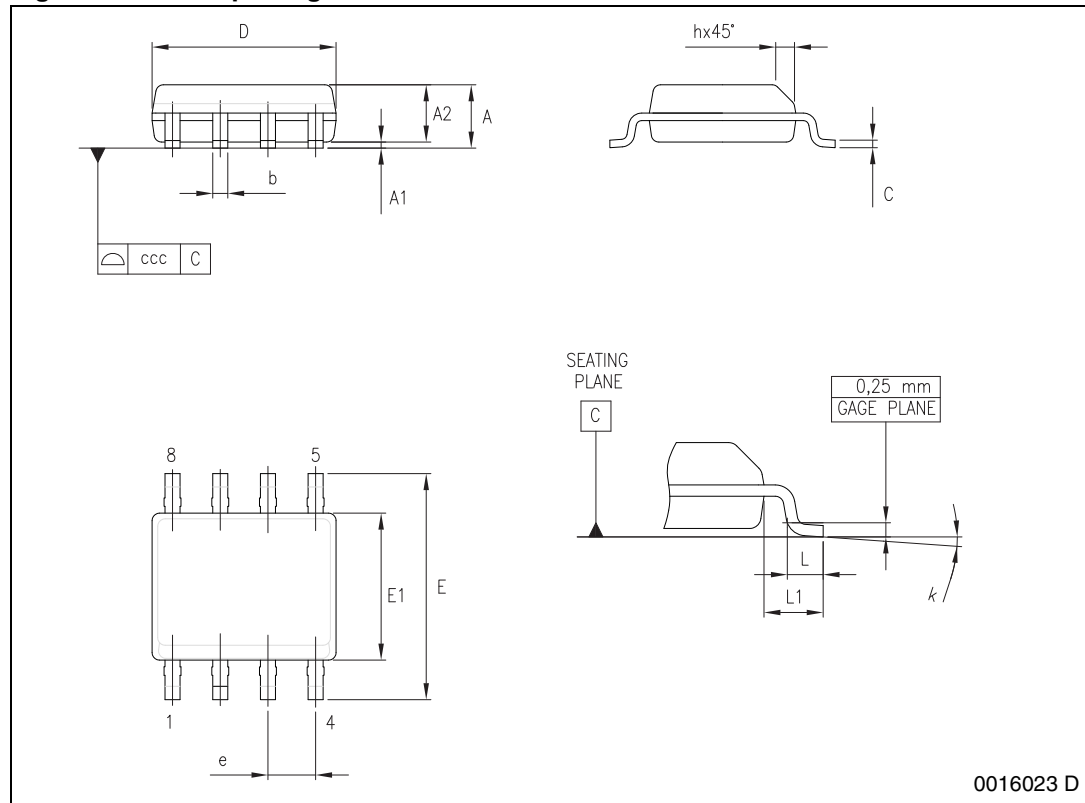
4.2 SO-8 mechanical data

Table 10. SO-8 mechanical data

| Dim. | mm | | |
|-------------------|------|------|------|
| | Min. | Typ. | Max. |
| A | | | 1.75 |
| A1 | 0.10 | | 0.25 |
| A2 | 1.25 | | |
| b | 0.28 | | 0.48 |
| c | 0.17 | | 0.23 |
| D ⁽¹⁾ | 4.80 | 4.90 | 5.00 |
| E | 5.80 | 6.00 | 6.20 |
| E1 ⁽²⁾ | 3.80 | 3.90 | 4.00 |
| e | | 1.27 | |
| h | 0.25 | | 0.50 |
| L | 0.40 | | 1.27 |
| L1 | | 1.04 | |
| k | 0° | | 8° |
| ccc | | | 0.10 |

1. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm in total (both side).
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.

Figure 30. SO-8 package dimension



4.3 SO-8 packing information

Figure 31. SO-8 tube shipment (no suffix)

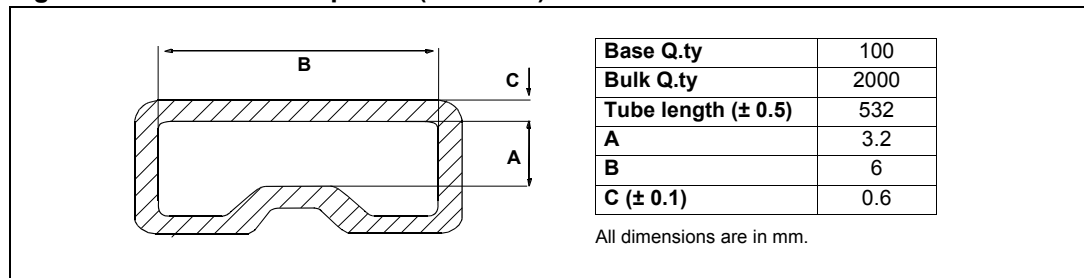
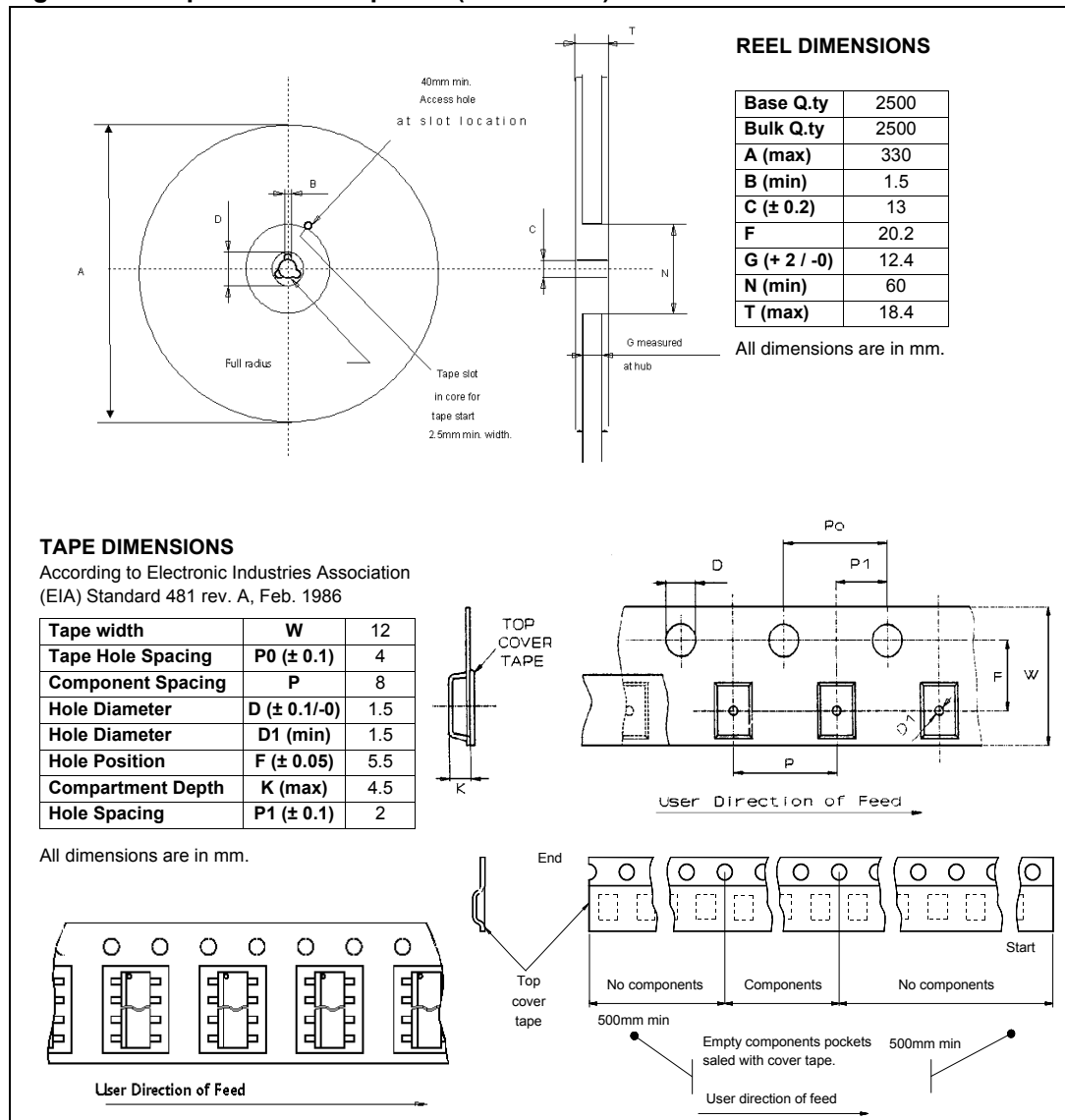


Figure 32. Tape and reel shipment (suffix "TR")



5 Revision history

Table 11. Document revision history

| Date | Revision | Changes |
|-------------|----------|--------------------|
| 09-Mar-2011 | 1 | Initial release. |
| 18-Sep-2013 | 2 | Updated Disclaimer |

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