A 7-Bit Current DAC with SPI Interface

FEATURES

- **±0.8% I_{DAC} Positive Output Current Accuracy (Over Temp)**
- **±1.5% I_{DAC} Negative Output Current Accuracy (Over Temp)**
- **Input Voltage Range: 2.5V to 5.5V**
- **High Impedance at IDAC Output When Disabled**
- **Wide IDAC Operation Voltage (0.4V to 2.0V)**
- 7-Bit Programmable DAC Output Current for DC/DC V_{OUT} Control
- Wide Range IDAC Output Current: ±16µA to ±256µA
- Programmable Slew Rate: 500ns ~ 3ms per Bit
- Available in a 10-Lead (3mm × 2mm) DFN Package

APPLICATIONS

- General Purpose Power Systems
- Telecom Systems
- Industrial Applications

DESCRIPTION

The LTC®7106-1 is a precision, SPI controlled, bidirectional current digital-to-analog converter that adjusts the output voltage of any conventional V_{FB} referenced regulator. The LTC7106-1 can work with the vast majority of power management controllers or regulators to enable digital control of the output voltage. Internal power-on reset circuitry keeps the DAC output current at zero (high impedance IDAC) until a valid write takes place.

Features include a range bit for easy interfacing to almost any impedance resistor divider, and an open-drain GPO output for controlling the Run or Enable pin of the DC/DC regulator. For most applications, the current DAC error is significantly attenuated with proper design. See more detail about V_{OUT} accuracy in the Applications Information section of this data sheet. The LTC7106 shares the same current DAC, but is controlled by an I^2C PMBus interface.

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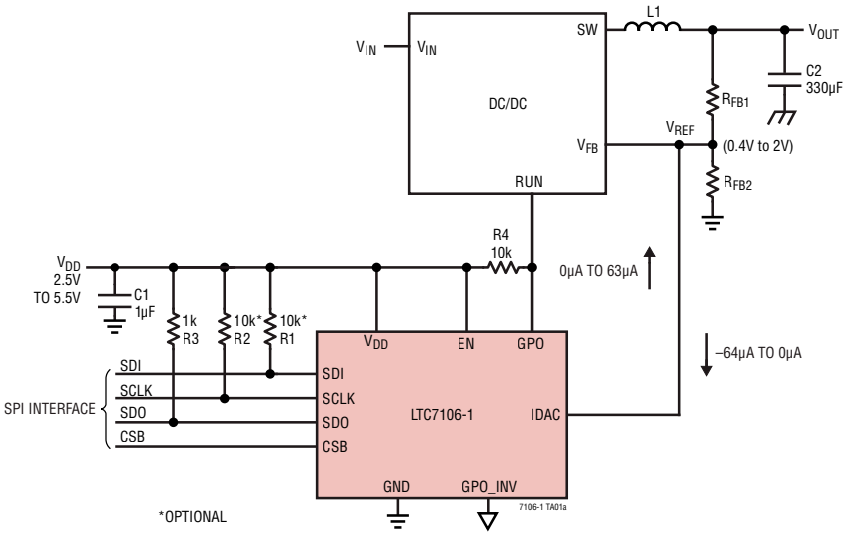
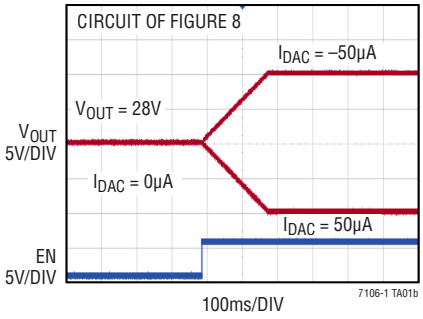
TYPICAL APPLICATION

Using LTC7106-1 to Vary V_{OUT} of DC/DC Converter



Margin High and Margin Low

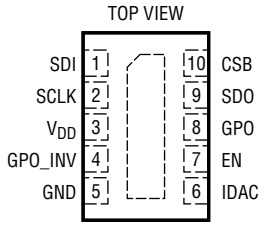


ABSOLUTE MAXIMUM RATINGS

(Note 1)

All Pins Except GND ..... –0.3V to 6.0V
Operating Junction Temperature Range... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



DDB PACKAGE
10-LEAD (3mm × 2mm) PLASTIC DFN
θ_{JA} = 55°C/W, θ_{JC} = 16.8°C/W
NOTE: THE EXPOSED PAD IS FLOATING INTERNALLY

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC7106EDDB-1#PBF	LTC7106EDDB-1#TRPBF	LHCH	10-Lead (3mm × 2mm) Plastic DFN	–40°C to 125°C
LTC7106IDDB-1#PBF	LTC7106IDDB-1#TRPBF	LHCH	10-Lead (3mm × 2mm) Plastic DFN	–40°C to 125°C

Consult ADI Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2), V_{DD} = 3.3V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{DD}	Power Supply				2.5		5.5	V
I_Q	Supply Quiescent Current	EN High				1.3	1.5	mA
V_{UVLO_R}	Undervoltage Rising Threshold	V_{DD} Rising				2.35		V
V_{UVLO_F}	Undervoltage Falling Threshold	V_{DD} Falling				2.15		V
V_{EN_R}	Enable Rising Threshold	V_{EN} Rising					1.35	V
V_{EN_F}	Enable Falling Threshold	V_{EN} Falling			0.8			V
IDAC_OUT								
I_{DAC}	Accuracy	Full Scale Positive 0.4 ≤ V_{IDAC} ≤ 2V (Note 3)	Range = Normal	●	62.5	63.0	63.5	µA
			Range = Low	●	15.50	15.75	16.00	µA
			Range = High	●	246.7	252.0	255.3	µA
		Full Scale Negative 0.4 ≤ V_{IDAC} ≤ 2V (Note 3)	Range = Normal (0°C to 85°C)		–64.6	–64.0	–63.0	µA
			Range = Normal	●	–65	–64.0	–63	µA
			Range = Low	●	–16.4	–16.0	–15.6	µA
			Range = High	●	–263.5	–256.0	–249.5	µA
LSB		0.4 ≤ V_{IDAC} ≤ 2V	Range = Normal			1.0		µA
			Range = Low			0.25		µA
			Range = High			4.0		µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2), V_{DD} = 3.3V, unless otherwise specified.

INL		0.4 ≤ V_{IDAC} ≤ 2V	Range = Normal		–1.0	1.0	LSB
			Range = Low		–1.5	1.5	LSB
			Range = High		–1.6	1.6	LSB
DNL		0.4 ≤ V_{IDAC} ≤ 2V	Range = Normal		–0.3	0.3	LSB
			Range = Low		–0.5	0.5	LSB
			Range = High		–0.8	0.8	LSB
IHZ	High-Z Current	0.4 ≤ V_{IDAC} ≤ 2V	V_{EN} = 0	●		20	nA
Digital Input: SDI, SCLK, CSB, GPO_INV							
V_{IH}						1.4	V
V_{IL}					0.8		V
C_{PIN}	Input Capacitance					10	pF
Open-Drain Outputs: GPO, SDO							
SDO V_{OL}	Output Low Voltage (Note 4)	I_{SINK} = 3mA				0.2	0.4	V
GPO V_{OL}	Output Low Voltage	I_{SINK} = 2mA				0.1	0.3	V

SPI INTERFACE TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2), V_{DD} = 3.3V, unless otherwise specified.

SYMBOL	PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{CKH}	SCLK High Time			95	100	105	ns
t_{CKL}	SCLK Low Time			95	100	105	ns
t_{CSS}	CSB Setup Time			15			ns
t_{CSH}	CSB High Time			15			ns
t_{CS}	SDI to SCLK Setup Time			15			ns
t_{CH}	SDI to SCLK Hold Time			20			ns
t_{DO}	SCLK to SDO Time			90			ns
	SCLK Duty Cycle					±5	%
f	Frequency					5	MHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC7106-1 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC7106-1E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC7106-1I is guaranteed over the –40°C to 125°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$$T_J = T_A + (P_D \bullet 55°C/W).$$

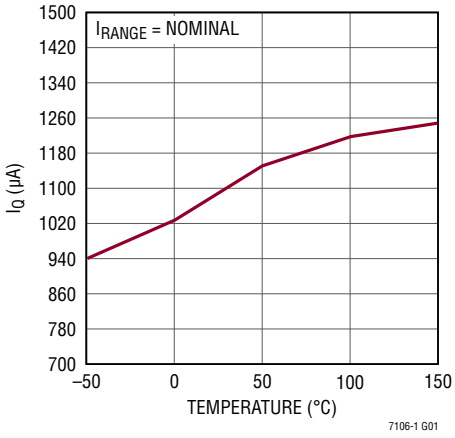
Note 3: IDAC is a bidirectional current DAC, controlled by 2's complementary logic. Under the setting of Range = Normal, I_{DAC} = 63µA for Code = 0111111 provides the maximum source current and I_{DAC} = –64µA for Code = 1000000 provides the maximum sink current. Max sink current generates the Highest V_{OUT}, while Max source current generates the lowest V_{OUT}. See the Operation section for more details.

Note 4: $R_{DS(ON)}$ MAX is 125Ω

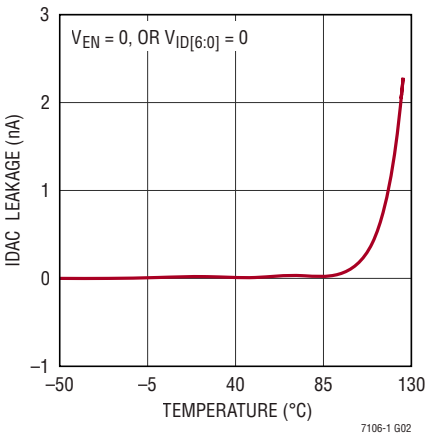
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 3.3V, V_{IDAC} = 1.0V, Range = Normal unless otherwise noted.

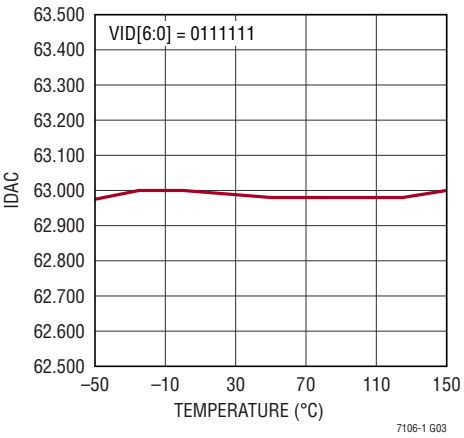
Quiescent Current vs Temperature



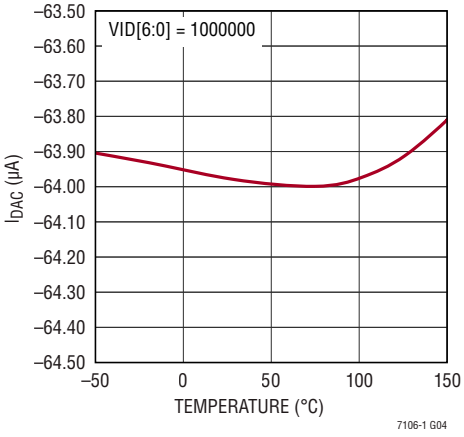
IDAC Leakage Current vs Temperature



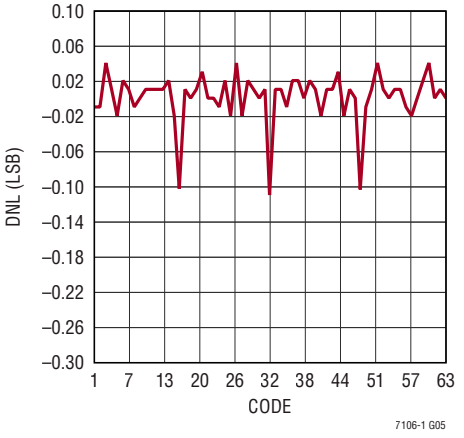
PIDAC Full-Scale vs Temperature



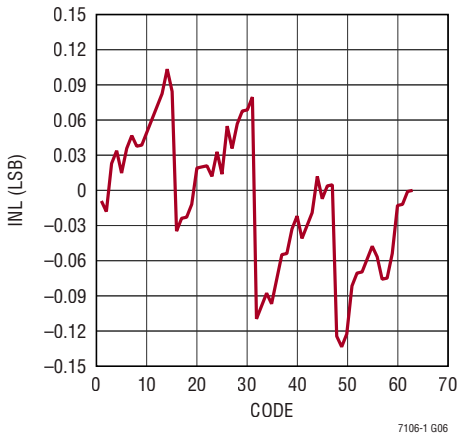
NIDAC vs Temperature



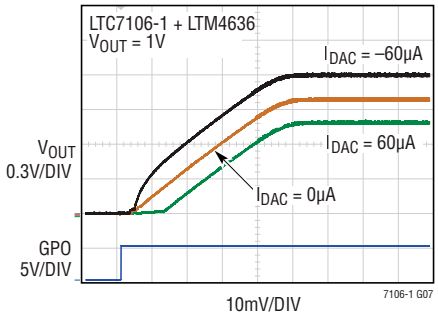
Differential Nonlinearity



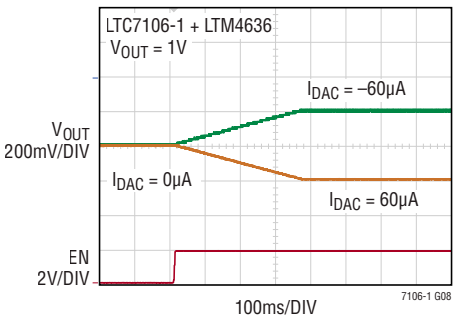
Integral Nonlinearity



Buck Start-Up with IDAC



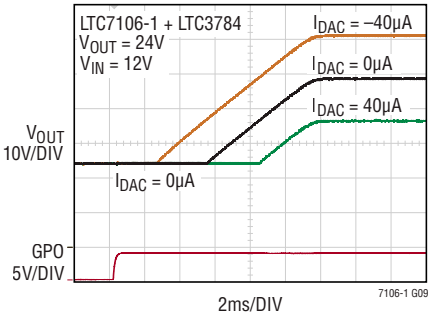
Margin High and Margin Low



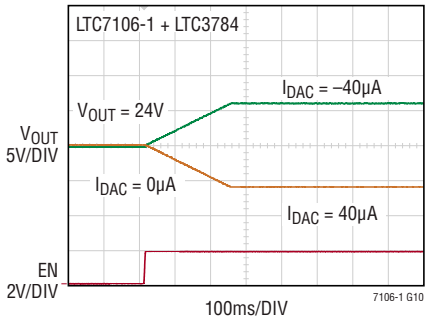
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 3.3V, Range = Normal unless otherwise noted.

Boost Start-Up with IDAC



Margin High and Margin Low



PIN FUNCTIONS

V_{DD} (Pin 3): Input Supply. Bypass this pin to GND with a capacitor (0.1µF to 1µF).

IDAC (Pin 6): Bidirectional Current DAC Output.

EN (Pin 7): DAC output current Enable. Current DAC output is in high impedance state when EN is Grounded. Do not leave EN floating.

SDI (Pin 1): Serial Bus Data Input.

SCLK (Pin 2): Serial Bus Clock Input.

GPO (Pin 8): Open-Drain Digital Output. A pull-up resistor to V_{DD} is required.

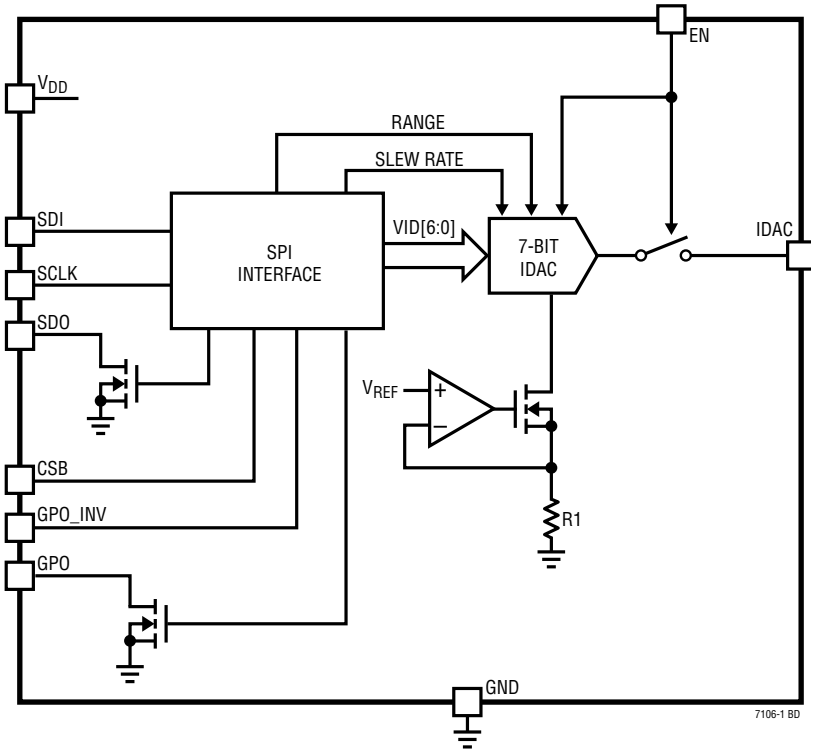
GPO_INV (Pin 4): Set to V_{DD} to invert the GPO output pin. Otherwise set to GND.

GND (Pin 5): Ground.

SDO (Pin 9): Open-Drain Serial Bus Data Output. A pull-up resistor to V_{DD} is required in the application.

CSB (Pin 10): Chip Select Active Low.

BLOCK DIAGRAM



OPERATION

The LTC7106-1 is an SPI controlled 7-bit D/A converter current source. Through its SPI interface, the LTC7106-1 receives a 7-bit DAC code and converts this value to a bidirectional analog output current through the pin IDAC. By connecting IDAC to the feedback node of a voltage regulator, I_{DAC} can change the output voltage of the regulator with the equation:

$$V_{OUT} = V_{REF} \bullet (1 + R_{FB1}/R_{FB2}) – I_{DAC} \bullet R_{FB1}$$

where V_{REF} is the reference voltage of the voltage regulator. R_{FB1} and R_{FB2} are the resistor divider for the voltage regulator. I_{DAC} is the programmed bidirectional current shown in Table 2.

A typical application diagram is shown on the front page. Therefore, the traditional pure analog designed oriented PWM controller can be controlled by a digital interface.

This illustrates the flexibility of the LTC7106-1 providing a SPI interface to conventional analog DC/DC converters.

(EN PIN)

The LTC7106-1's output is activated by the EN pin. It turns on/off the output device with threshold of 1.2V. When EN is low (<1.2V), IDAC is in high impedance (Hi-Z).

However, SPI interface as well as all the control circuits are still active when EN is low which means users can program the device and readback the internal register's value. The device will execute the commands of MFR_IOUT_COMMAND, MFR_IOUT_MARGIN_HIGH, MFR_IOUT_MARGIN_LOW after EN goes high.

SLEW RATE CONTROL

To prevent abrupt changes in the D/A output current and subsequently the output voltage of the DC/DC regulator, an internal digital programmable slew rate control is included. The slew rate range can be programmed with a 6-bit register from 0.5µs/step to 3.58ms/step with a default value of 3.58ms/step.

CURRENT RANGE SETTING AND D/A PROGRAMMING

The LTC7106-1 is a 7-bit bidirectional current DAC with a 1µA LSB as its default setting. The MSB determines the current direction. When MSB is 0, I_{DAC} is sourcing current (reducing V_{OUT}), which is positive current flowing out of the pin, and when MSB is 1, I_{DAC} is sinking current (increasing V_{OUT}), which is negative current flowing into the pin. The LTC7106-1 also provides range high and range low options through its digital interface to change the LSB value to 4µA expanding the output current range and subsequently widening the programmable output voltage range. Alternately for higher resolution, the low range is provided with a LSB of 0.25µA. Users have additional flexibility of choosing the resistor divider ratio and resistor values to meet the output specification target. However, the design is most accurate using the nominal range which is the recommended setting. Table 1 lists the output current range and Table 2 lists the detailed DAC codes vs I_{DAC} current.

Table 1. Output Current Range

Range	LSB (µA)	I_{MIN} (µA)	I_{MAX} (µA)
Nominal	1	–64	63
Range High	4	–256	252
Range Low	0.25	–16	15.75

OPERATION

Table 2. IDAC Current and Corresponding DAC Codes

DAC CODE							I_{DAC} (µA)		
[6]	[5]	[4]	[3]	[2]	[1]	[0]	NOMINAL	RANGE HIGH	RANGE LOW
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1	4	0.25
0	0	0	0	0	1	0	2	8	0.5
0	0	0	0	0	1	1	3	12	0.75
0	0	0	0	1	0	0	4	16	1
0	0	0	0	1	0	1	5	20	1.25
0	0	0	0	1	1	0	6	24	1.5
0	0	0	0	1	1	1	7	28	1.75
0	0	0	1	0	0	0	8	32	2
0	0	0	1	0	0	1	9	36	2.25
0	0	0	1	0	1	0	10	40	2.5
0	0	0	1	0	1	1	11	44	2.75
0	0	0	1	1	0	0	12	48	3
0	0	0	1	1	0	1	13	52	3.25
0	0	0	1	1	1	0	14	56	3.5
0	0	0	1	1	1	1	15	60	3.75
0	0	1	0	0	0	0	16	64	4
0	0	1	0	0	0	1	17	68	4.25
0	0	1	0	0	1	0	18	72	4.5
0	0	1	0	0	1	1	19	76	4.75
0	0	1	0	1	0	0	20	80	5
0	0	1	0	1	0	1	21	84	5.25
0	0	1	0	1	1	0	22	88	5.5
0	0	1	0	1	1	1	23	92	5.75
0	0	1	1	0	0	0	24	96	6
0	0	1	1	0	0	1	25	100	6.25
0	0	1	1	0	1	0	26	104	6.5
0	0	1	1	0	1	1	27	108	6.75
0	0	1	1	1	0	0	28	112	7
0	0	1	1	1	0	1	29	116	7.25
0	0	1	1	1	1	0	30	120	7.5
0	0	1	1	1	1	1	31	124	7.75
0	1	0	0	0	0	0	32	128	8
0	1	0	0	0	0	1	33	132	8.25
0	1	0	0	0	1	0	34	136	8.5
0	1	0	0	0	1	1	35	140	8.75
0	1	0	0	1	0	0	36	144	9
0	1	0	0	1	0	1	37	148	9.25
0	1	0	0	1	1	0	38	152	9.5
0	1	0	0	1	1	1	39	156	9.75
0	1	0	1	0	0	0	40	160	10
0	1	0	1	0	0	1	41	164	10.25
0	1	0	1	0	1	0	42	168	10.5
0	1	0	1	0	1	1	43	172	10.75
0	1	0	1	1	0	0	44	176	11
0	1	0	1	1	0	1	45	180	11.25
0	1	0	1	1	1	0	46	184	11.5
0	1	0	1	1	1	1	47	188	11.75
0	1	1	0	0	0	0	48	192	12
0	1	1	0	0	0	1	49	196	12.25
0	1	1	0	0	1	0	50	200	12.5
0	1	1	0	0	1	1	51	204	12.75
0	1	1	0	1	0	0	52	208	13
0	1	1	0	1	0	1	53	212	13.25
0	1	1	0	1	1	0	54	216	13.5
0	1	1	0	1	1	1	55	220	13.75
0	1	1	1	0	0	0	56	224	14
0	1	1	1	0	0	1	57	228	14.25
0	1	1	1	0	1	0	58	232	14.5
0	1	1	1	0	1	1	59	236	14.75
0	1	1	1	1	0	0	60	240	15
0	1	1	1	1	0	1	61	244	15.25
0	1	1	1	1	1	0	62	248	15.5
0	1	1	1	1	1	1	63	252	15.75
1	0	0	0	0	0	0	–64	–256	–16
1	0	0	0	0	0	1	–63	–252	–15.75
1	0	0	0	0	1	0	–62	–248	–15.5
1	0	0	0	0	1	1	–61	–244	–15.25
1	0	0	0	1	0	0	–60	–240	–15
1	0	0	0	1	0	1	–59	–236	–14.75
1	0	0	0	1	1	0	–58	–232	–14.5
1	0	0	0	1	1	1	–57	–228	–14.25
1	0	0	1	0	0	0	–56	–224	–14
1	0	0	1	0	0	1	–55	–220	–13.75
1	0	0	1	0	1	0	–54	–216	–13.5
1	0	0	1	0	1	1	–53	–212	–13.25

OPERATION

Table 2. IDAC Current and Corresponding DAC Codes (Continued)

DAC CODE							I_{DAC} (µA)		
[6]	[5]	[4]	[3]	[2]	[1]	[0]	NOMINAL	RANGE HIGH	RANGE LOW
1	0	0	1	1	0	0	–52	–208	–13
1	0	0	1	1	0	1	–51	–204	–12.75
1	0	0	1	1	1	0	–50	–200	–12.5
1	0	0	1	1	1	1	–49	–196	–12.25
1	0	1	0	0	0	0	–48	–192	–12
1	0	1	0	0	0	1	–47	–188	–11.75
1	0	1	0	0	1	0	–46	–184	–11.5
1	0	1	0	0	1	1	–45	–180	–11.25
1	0	1	0	1	0	0	–44	–176	–11
1	0	1	0	1	0	1	–43	–172	–10.75
1	0	1	0	1	1	0	–42	–168	–10.5
1	0	1	0	1	1	1	–41	–164	–10.25
1	0	1	1	0	0	0	–40	–160	–10
1	0	1	1	0	0	1	–39	–156	–9.75
1	0	1	1	0	1	0	–38	–152	–9.5
1	0	1	1	0	1	1	–37	–148	–9.25
1	0	1	1	1	0	0	–36	–144	–9
1	0	1	1	1	0	1	–35	–140	–8.75
1	0	1	1	1	1	0	–34	–136	–8.5
1	0	1	1	1	1	1	–33	–132	–8.25
1	1	0	0	0	0	0	–32	–128	–8
1	1	0	0	0	0	1	–31	–124	–7.75
1	1	0	0	0	1	0	–30	–120	–7.5
1	1	0	0	0	1	1	–29	–116	–7.25
1	1	0	0	1	0	0	–28	–112	–7
1	1	0	0	1	0	1	–27	–108	–6.75
1	1	0	0	1	1	0	–26	–104	–6.5
1	1	0	0	1	1	1	–25	–100	–6.25
1	1	0	1	0	0	0	–24	–96	–6
1	1	0	1	0	0	1	–23	–92	–5.75
1	1	0	1	0	1	0	–22	–88	–5.5
1	1	0	1	0	1	1	–21	–84	–5.25
1	1	0	1	1	0	0	–20	–80	–5
1	1	0	1	1	0	1	–19	–76	–4.75
1	1	0	1	1	1	0	–18	–72	–4.5
1	1	0	1	1	1	1	–17	–68	–4.25
1	1	1	0	0	0	0	–16	–64	–4
1	1	1	0	0	0	1	–15	–60	–3.75
1	1	1	0	0	1	0	–14	–56	–3.5
1	1	1	0	0	1	1	–13	–52	–3.25
1	1	1	0	1	0	0	–12	–48	–3
1	1	1	0	1	0	1	–11	–44	–2.75
1	1	1	0	1	1	0	–10	–40	–2.5
1	1	1	0	1	1	1	–9	–36	–2.25
1	1	1	1	0	0	0	–8	–32	–2
1	1	1	1	0	0	1	–7	–28	–1.75
1	1	1	1	0	1	0	–6	–24	–1.5
1	1	1	1	0	1	1	–5	–20	–1.25
1	1	1	1	1	0	0	–4	–16	–1
1	1	1	1	1	0	1	–3	–12	–0.75
1	1	1	1	1	1	0	–2	–8	–0.5
1	1	1	1	1	1	1	–1	–4	–0.25

OPERATION

GPO

GPO is a general purpose open-drain output pin, which can be set by SPI command. It is designed to turn on/off the DC/DC regulator by connecting GPO to the RUN pin of the regulator. Once GPO is set high, it stays high even if the EN pin goes low as long as the device is not power cycled.

SPI SERIAL PORT

The LTC7106-1 SPI-compatible serial port provides chip control.

Communication Sequence

The serial bus is comprised of chip select active low (CSB), serial clock (SCLK), serial data input (SDI), serial data output (SDO) signals. Data transfers to the LTC7106-1 are accomplished by the serial bus master device first taking CSB LOW, which enables the LTC7106-1's serial port. Input data applied on SDI is clocked on the rising edge of SCLK, with most significant bits transferred first. The communication burst is terminated by the serial bus master device returning CSB HIGH. See Figure 1 for details.

Data is read from the part during a communication burst using SDO. Read back may be multidrop (more than one LTC7106-1 connected in parallel on the serial bus), as SDO is set to a high impedance (Hi-Z) when CSB is HIGH or when data is not being read from the part.

SINGLE BYTE TRANSFERS

All data bursts are comprised of at least two bytes. The seven most significant bits (MSB) of the first byte are the register address, with a least significant bit (LSB) of 1 indicating a read from the part, and an LSB of 0 indicating

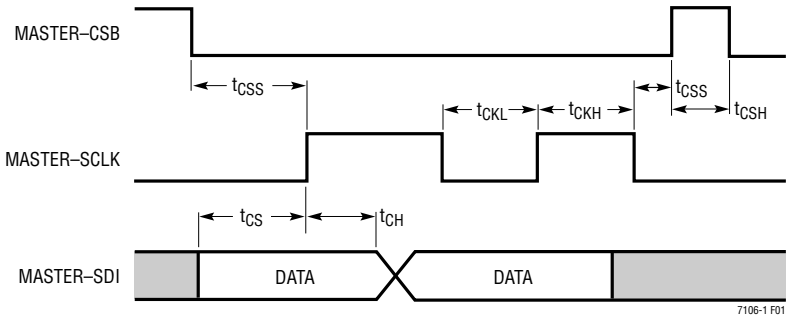


Figure 1. Serial Port Write Timing Diagram

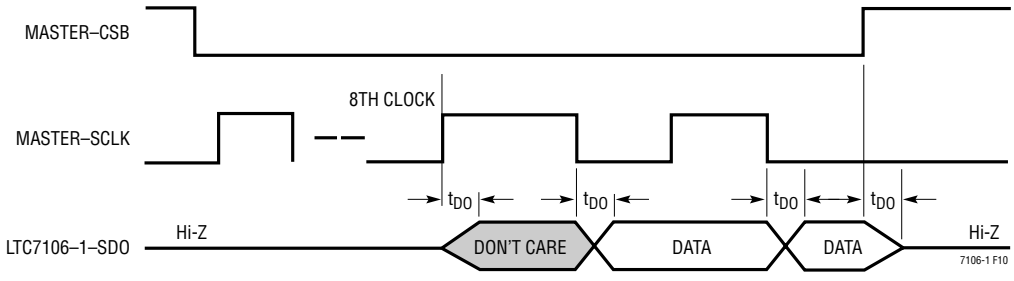


Figure 2. Serial Port Read Timing Diagram

OPERATION

a write to the part. The subsequent byte, or bytes, is data from/to the specified register address. See Figure 3 for an example of a detailed write sequence, and Figure 4 for a read sequence.

To terminate the first communication burst, CSB is taken HIGH.

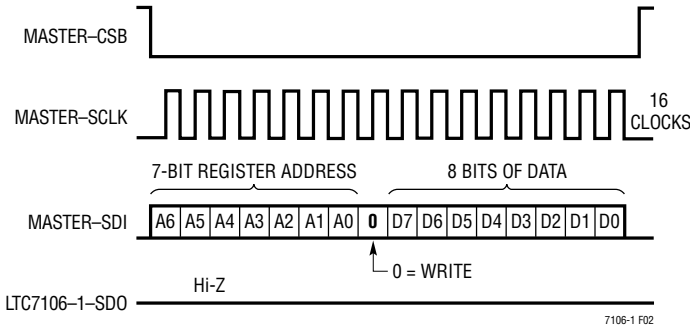


Figure 3. Serial Port Write Sequence

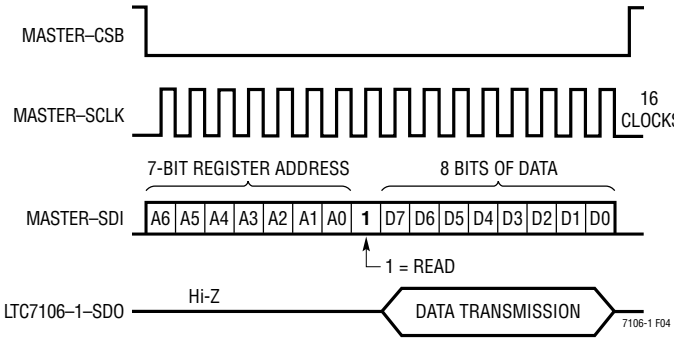


Figure 4. Serial Port Read Sequence

REGISTER COMMAND DETAILS

Table 3. Supported SPI Commands

SPI CMD CODE (7 BITS)	COMMAND NAME	R/W TYPE	DATA BYTES	DESCRIPTION
0x01	OPERATION	R/W	1	Default is On: [7:0] = 0x80
0x38	STATUS_BYTE	R/W	1	Read Fault Status: CML, write 1 to reset
0x62	MFR_CHIP_CTRL	R/W	1	[7:1] – Reserved, [0] = GPO enable
0x64	MFR_DAC_CTRL	R/W	1	[7:6] = Current Range: 0.25µA, 1µA, 4µA [5:0] = DAC Slew Rate Control: 0.5µs to 3580µs
0x65	MFR_IOUT_MARGIN_HIGH	R/W	1	Same format as MFR_IOUT_COMMAND
0x66	MFR_IOUT_MAX	R/W	1	Clamped value that IDAC value cannot exceed Default 7-bit value of 0x00 = cannot sink current
0x68	MFR_IOUT_COMMAND	R/W	1	I_{OUT} Margining Command (2's comp) [5:0] IDAC value, source: [6] = 0, sink: [6] = 1
0x6D	MFR_IOUT_MARGIN_LOW	R/W	1	Same format as MFR_IOUT_COMMAND
0x7D	MFR_RESET	Write	1	Reset to Power-On State (except for MFR_DAC_CTRL) Write data is ignored

MFR_IOUT_COMMAND

DAC output current command that is formatted as a 7-bit 2's complement value. When the operation register is set to 0x80, DAC takes the value stored in this register. Setting bit[6] to 0 sources the current from the IC and bit[6] to 1 sinks the current into the IC. Default value for this register is 0x00. The valid range of values are from 0x40 to 0x3F.

Do not attempt to write values outside of this range or undesired behavior may result.

MFR_IOUT_MARGIN_HIGH

DAC margining register with the same format and rules as MFR_IOUT_COMMAND. The DAC value will take the value stored in this register when the operation register is set to margin high, 0xA8.

MFR_IOUT_MARGIN_LOW

DAC margining register with the same format and rules as MFR_IOUT_COMMAND. The DAC value will take the value stored in this register when the operation register is set to margin low, 0x98.

MFR_IOUT_MAX

Clamping value that DAC cannot exceed. The format is a 7-bit 2's complement value, the same as the margin registers. Therefore, the DAC value cannot be a smaller 2's complement value than what is stored in this register.

The 7-bit default value is 0x00 = cannot sink current. I_{OUT} cannot be set to a higher value unless this value is changed to a negative number, bit [7] = 1.

Setting this register to 0x40 allows the LTC7106-1 to sink the maximum current with no clamping.

REGISTER COMMAND DETAILS

MFR_CHIP_CTRL

This register is for general chip control and status. Please refer to Table 6 for each bit description.

Bits Description

[7:1] Reserved

[0] GPO, General Purpose Output

0 = GPO Pulls Open Drain to GND

1 = Hi-Z on GPO

MFR_DAC_CTRL

8-bit register to control the IDAC LSB current value and the timer count for the slew rate control. Default value = 0x40.

Bits Description

[7:6] Selector Range for IDAC Step:

b'00 = 0.25µA/Step, Range Low

b'01 = 1.0µA/Step, Nominal

b'10 = 4.0µA/Step, Range High

b'11 = Reserved

[5:0] Selector for Time in µs/Step

Default Value 0x00 = Max = 3584µs/Step

See Table 4 for Allowable Values

Only a power cycle, POR, will reset this register to prevent unwanted immediate current changes in IDAC. MFR_RESET will not reset this register.

In addition, IDAC must be at 0x00 to change the current range selector to prevent unwanted large swings in IDAC current. The time step selector, bits [5:0], can be changed at any time.

Table 4. Programmable Delay Per Current Step

Slew Rate Timer Clock (µs/Step)					
[5:0]		[5:0]		[5:0]	
0 0 0 0 0 0	= 3584	0 1 0 0 0 0	= 16	1 0 0 0 0 0	= 256
0 0 0 0 0 1	= 0.5	0 1 0 0 0 1	= 20	1 0 0 0 0 1	= 320
0 0 0 0 1 0	= 1.0	0 1 0 0 1 0	= 24	1 0 0 0 1 0	= 384
0 0 0 0 1 1	= 1.5	0 1 0 0 1 1	= 28	1 0 0 0 1 1	= 448
0 0 0 1 0 0	= 2.0	0 1 0 1 0 0	= 32	1 0 0 1 0 0	= 512
0 0 0 1 0 1	= 2.5	0 1 0 1 0 1	= 40	1 0 0 1 0 1	= 640
0 0 0 1 1 0	= 3.0	0 1 0 1 1 0	= 48	1 0 0 1 1 0	= 768
0 0 0 1 1 1	= 3.5	0 1 0 1 1 1	= 56	1 0 0 1 1 1	= 896
0 0 1 0 0 0	= 4.0	0 1 1 0 0 0	= 64	1 0 1 0 0 0	= 1280*
0 0 1 0 0 1	= 5.0	0 1 1 0 0 1	= 80	1 0 1 0 0 1	= 1280
0 0 1 0 1 0	= 6.0	0 1 1 0 1 0	= 96	1 0 1 0 1 0	= 1536
0 0 1 0 1 1	= 7.0	0 1 1 0 1 1	= 112	1 0 1 0 1 1	= 1792
0 0 1 1 0 0	= 8.0	0 1 1 1 0 0	= 128	1 0 1 1 0 0	= 2560*
0 0 1 1 0 1	= 10	0 1 1 1 0 1	= 160	1 0 1 1 0 1	= 2560
0 0 1 1 1 0	= 12	0 1 1 1 1 0	= 192	1 0 1 1 1 0	= 3584*
0 0 1 1 1 1	= 14	0 1 1 1 1 1	= 224	1 0 1 1 1 1	= 3584

* Duplicate Encoding

REGISTER COMMAND DETAILS

MFR_RESET

This command provides a means by which the user can perform a reset of the LTC7106-1. All latched faults and register contents will be reset to a power-on condition by this command. V_{OUT} will remain in regulation but may change due to the reset of the margin registers.

This is a write-only command. The data byte is ignored.

OPERATION

The OPERATION command is used to turn the unit on/off and for margining the output voltage.

The ON bit is automatically reset to ON after a master shutdown (EN), power cycle, or MFR_RESET command.

The MARGIN_LOW/HIGH bits command the I_{OUT} reference to the offset value stored in either the MFR_IOUT_MARGIN_HIGH or MFR_IOUT_MARGIN_LOW.

This command has one data byte. It will accept one or two but ignores the second byte.

Table 5. Supported OPERATION Command Register Values

ACTION	VALUE
Turn Off Immediately	0x00
Turn On	0x80
Margin Low	0x98
Margin High	0xA8

STATUS_BYTE

The STATUS_BYTE command returns a byte of information with a summary of the unit's fault condition.

See Table 6 for a list of the status bits that are supported and the conditions in which each bit is set.

Writing a "1" to a particular bit in the status byte will attempt to reset that fault in the status byte. If the fault is still present, the status byte bit will rmain asserted.

Table 6. Status Byte Bit Descriptions and Conditions

BIT	DESCRIPTION	CONDITION	CLEARABLE BY WRITING '1' TO BIT?
0 (LSB)	None of the Above	MFR_VOUT_MAX Register Exceeded	Yes
1	Communication Failure	Not Implemented	
2	Temperature Fault	Not Implemented	
3	V_{IN} Undervoltage Fault	Not Implemented	
4	Output Overcurrent Fault	Not Implemented	
5	Output Overvoltage Fault	Not Implemented	
6	OFF	Not Implemented	
7	Busy	Not Implemented	

APPLICATIONS INFORMATION

I_{DAC} ACCURACY

The LTC7106-1 provides three ranges of I_{DAC} output current. However, only nominal range (LSB = ±1µA) is optimized with the highest accuracy. It is recommended that users design the resistor divider using the nominal range of the IDAC setting.

TWO'S COMPLEMENTARY CODE

VID [6:0] of the LTC7106-1 is in the format of two's complementary. From Table 2, it is easy to program the register once the desired output current is known. For example, if output current is 20µA, then set VID [6:0] = 0010100. If the output current is –20µA, then set VID [6:0] = 1101100 for the nominal I_{DAC} setting.

V_{OUT} ACCURACY

When I_{DAC} = 0, define:

$$V_{OUT0} = V_{REF}\left[1+\frac{R_{FB1}}{R_{FB2}}\right] \quad (1)$$

Referring to Figure 5, the output voltage is set according to:

$$V_{OUT} = V_{REF}\left[1+\frac{R_{FB1}}{R_{FB2}}\right] - I_{DAC} \bullet R_{FB1} \quad (2)$$

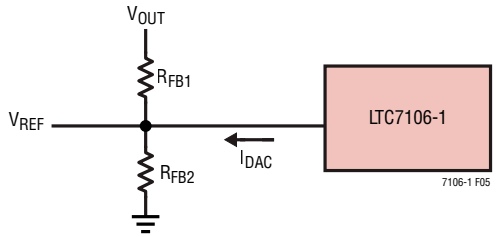


Figure 5. Setting the Output Voltage Using the LTC7106-1

Define ΔV_{OUT} as the V_{OUT} error caused by the I_{DAC} error ΔI_{DAC}, then we can derive the following equation from equation (1) and (2):

$$\frac{\Delta V_{OUT}}{V_{OUT}} = \left(\frac{\Delta I_{DAC} / I_{DAC}}{Ratio - 1}\right) \quad (3)$$

Where:

$$Ratio = \frac{V_{OUT0}}{I_{DAC} \bullet R_{FB1}} \quad (4)$$

It is clear that when Ratio < 0 or Ratio ≥ 2, the V_{OUT} error can be attenuated from the I_{DAC} error:

$$\left|\frac{\Delta V_{OUT}}{V_{OUT}}\right| \le \left|\frac{\Delta I_{DAC}}{I_{DAC}}\right| \quad (5)$$

In the case of margin high, I_{DAC} < 0 so Ratio < 0. Therefore, the V_{OUT} error is always smaller than the I_{DAC} error by a factor of:

$$\frac{V_{OUT0}}{I_{DAC} \bullet R_{FB1}} - 1 \quad (6)$$

In the case of margin low, I_{DAC} > 0. So the V_{OUT} error will only be attenuated when:

$$Ratio = \frac{V_{OUT0}}{I_{DAC} \bullet R_{FB1}} > 2$$

$$\text{or} \quad I_{DAC} \bullet R_{FB1} < \frac{V_{OUT0}}{2} \quad (7)$$

In other words, as long as V_{OUT} is margining low within 50% of the V_{OUT} default value, V_{OUT0}, the V_{OUT} error won't be larger than the I_{DAC} error.

DESIGN EXAMPLES

The LTC7106-1 can work with almost all the power management controllers or regulators. Figure 6, Figure 7 and Figure 8 show three design examples using the LTC7106-1 to control the output voltage with a monolithic buck regulator, an µModule® and a boost controller.

APPLICATIONS INFORMATION

Case One

Assume that the LTC7150S, a monolithic buck regulator, provides a 1.5V output and requires to margin low V_{OUT} from 1.5V to 1.0V (see Figure 6). The V_{FB} is 0.6V and the voltage dividers are external. In order to achieve the best accuracy of the LTC7106-1, it is recommended to design I_{DAC} in nominal range. Also within certain current range (nominal, high or low), the larger the absolute I_{DAC} current amplitude is, the better accuracy the LTC7106-1 can achieve. So it is easy to choose R_{TOP} = 10kΩ and R_{BOT} = 6.65kΩ. Then I_{DAC} = (1.5V – 1.0V)/10kΩ = + 50µA. Choose MFR_CONTROL [6:5] = 00 (Range = Nominal) to set I_{DAC} LSB =1µA.

By looking in Table 2, choose DAC [6:0] = 0110010 to set the I_{DAC} = +50µA, which will margin V_{OUT} from 1.5V to 1.0V.

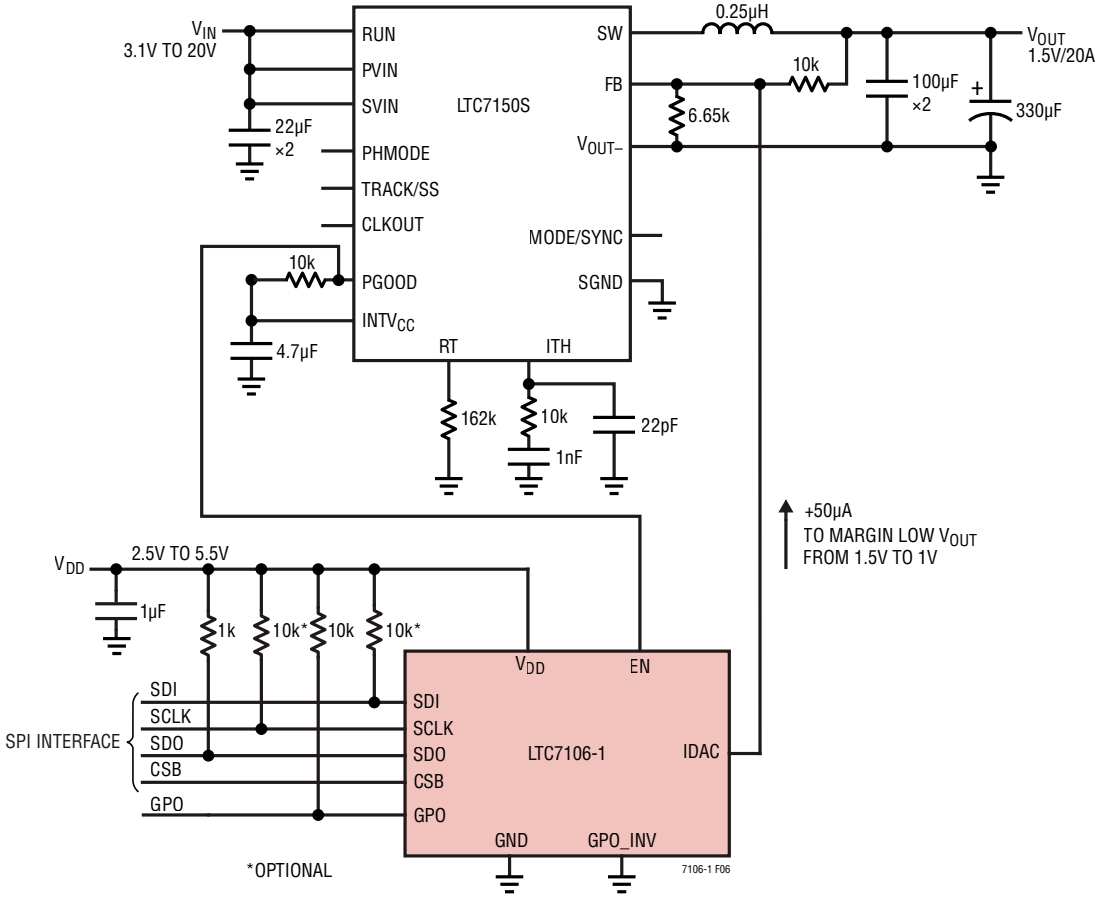


Figure 6. Using the LTC7106-1 to Margin Low Monolithic Buck Regulator LTC7150S Providing 1.5V to 1.0V at 20A

APPLICATIONS INFORMATION

Case Two

In this case, the µModule LTM4636 provides a 1.2V output and requires to margin high V_{OUT} from 1.2V to 2.0V (see Figure 7). The V_{FB} of the LTM4636 is again 0.6V. However, the top voltage divider is internal (R_{TOP} = 4.99kΩ), so the R_{BOT} is also fixed at 4.99kΩ. Then I_{DAC} = (1.2V – 2.0V)/ 4.99kΩ = –160µA.

So we have to choose MFR_CONTROL [6:5] = 10 (Range = High) to set I_{DAC} LSB = 4µA.

From Table 3, choose DAC[6:0] = 1011000 to set the I_{DAC} = –160µA, which will margin V_{OUT} from 1.2V to 2.0V.

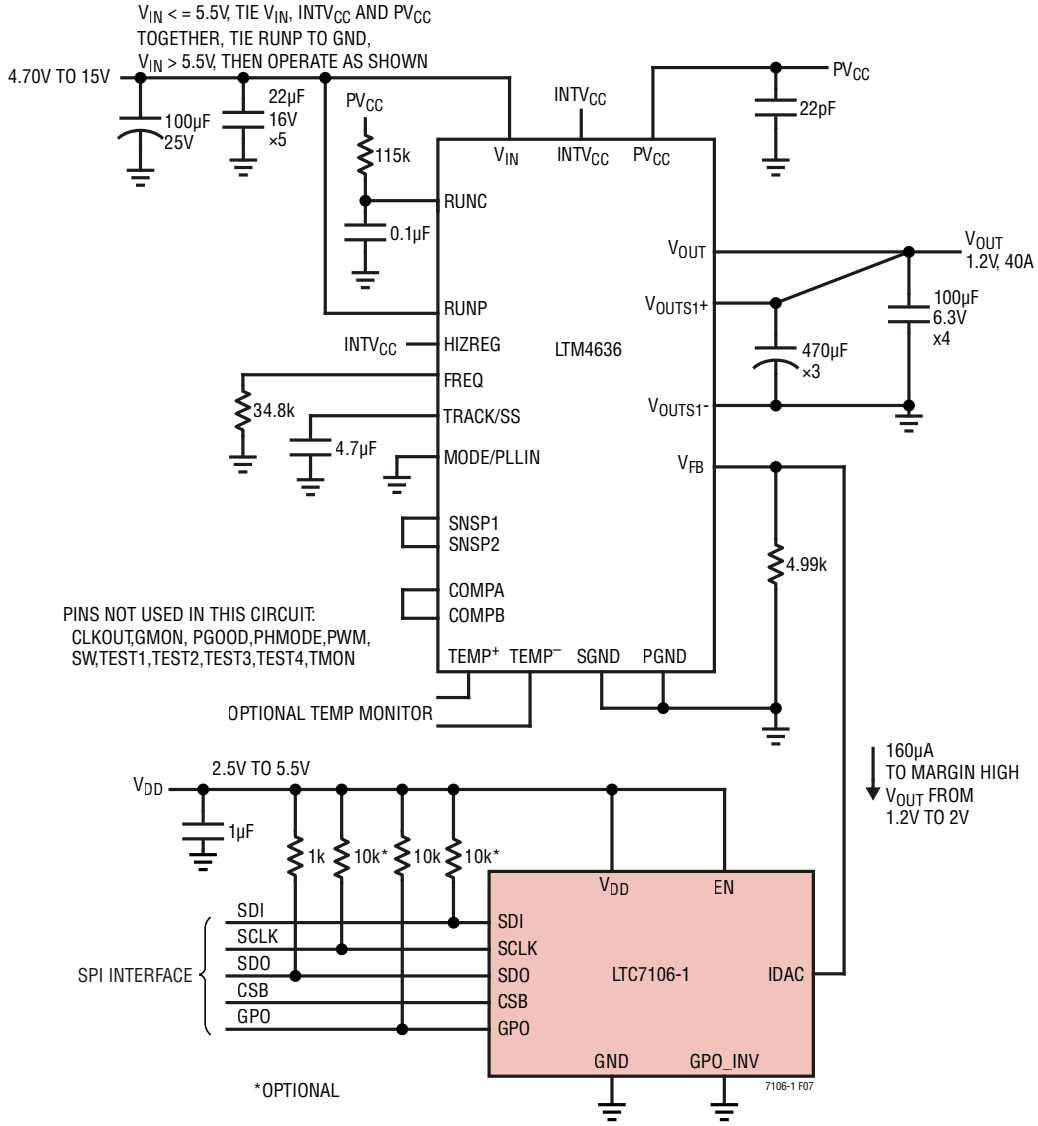


Figure 7. Using the LTC7106-1 to Margin High µModule LTM4636 Providing 1.2V to 2.0V at 40A

APPLICATIONS INFORMATION

Case Three

The LTC7106-1 can also work with boost converters. In this case, the LTC3784, a synchronous boost controller, provides a 2-phase 28V/10A output and requires to control V_{OUT} from 28V to 18V (see Figure 8). The VFB is 1.2V and the voltage dividers are external. Based on the same design criteria in Case One, we can choose R_{TOP} = 200kΩ and R_{BOT} = 8.97kΩ for the best accuracy. Then I_{DAC} = (28V – 18V)/200kΩ = +50µA. Choose MFR_CONTROL [6:5] = 00 (Range Nominal) to set I_{DAC} LSB = 1µA. By looking in Table 2, choose DAC[6:0] = 0001110 to set the I_{DAC} = +50µA, which will margin V_{OUT} from 28V to 18V.

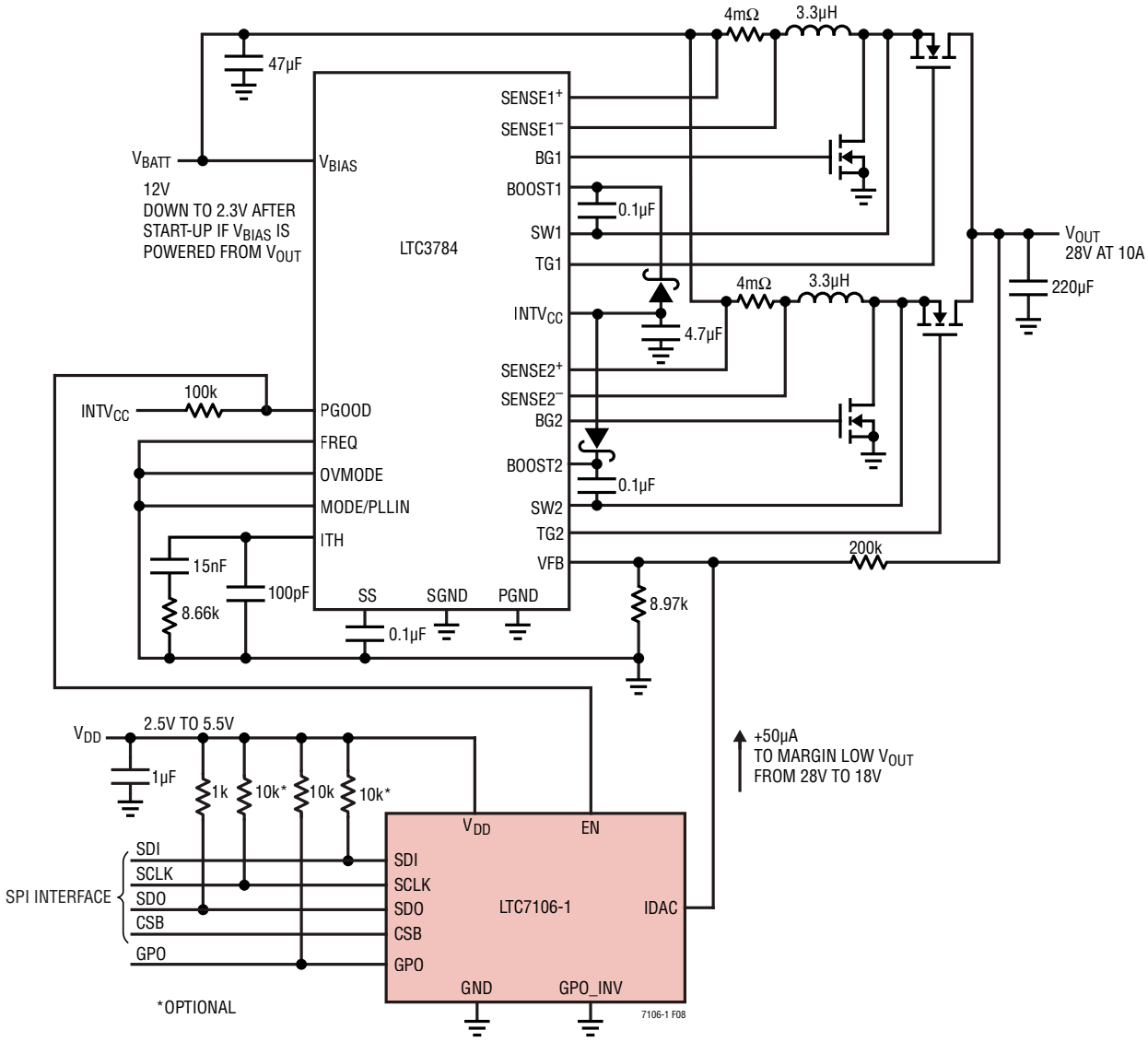
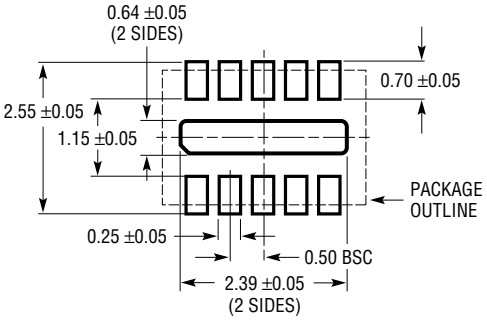


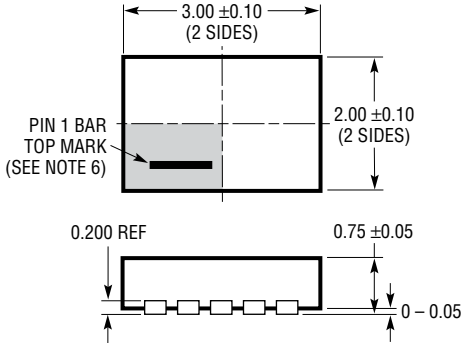
Figure 8. Using the LTC7106-1 with a Boost Controller to Vary V_{OUT} from 28V to 18V

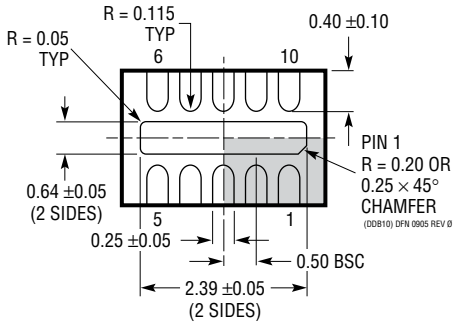
PACKAGE DESCRIPTION

DDB Package
10-Lead Plastic DFN (3mm × 2mm)
(Reference LTC DWG # 05-08-1722 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS





BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

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TYPICAL APPLICATION

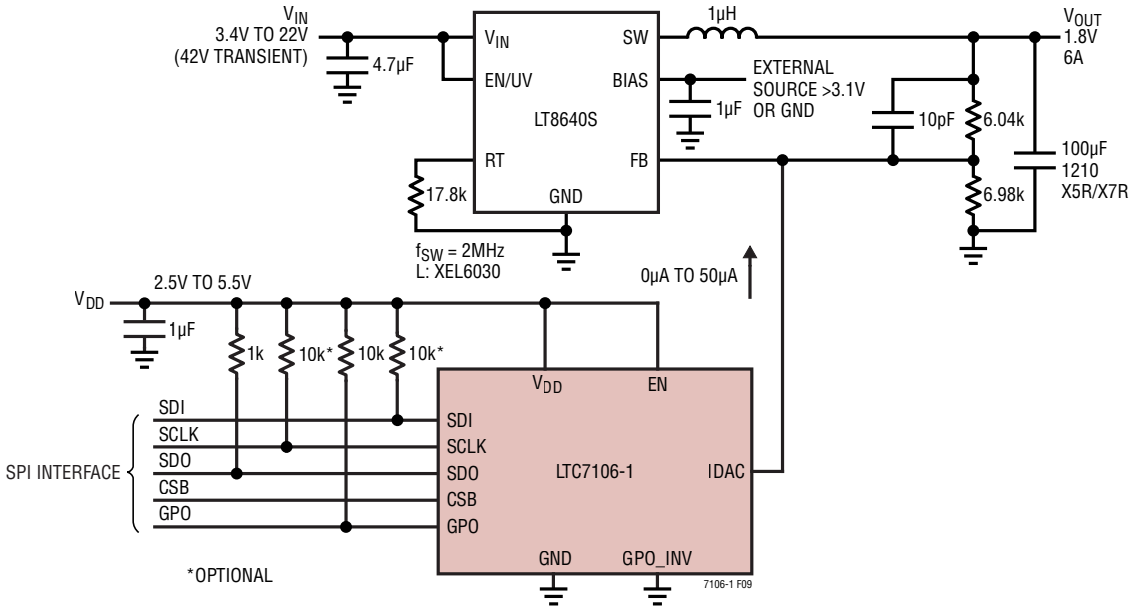

Figure 9. Margining a LT8640S from 1.8V to 1.5V at 6A

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3605/LTC3605A	20V, 5A Synchronous Step-Down Regulator	4V < V_{IN} < 20V, 0.6V < V_{OUT} < 20V, 96% Maximum Efficiency, 4mm × 4mm QFN-24 Package
LTC3626	20V, 2.5A Synchronous Step-Down Regulator with Current and Temperature Monitoring	95% Efficiency, V_{IN}: 3.6V to 20V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 300µA, ISD < 15µA, 3mm × 4mm QFN-20
LTC3636	20V, Dual 6A Synchronous Step-Down Regulator	95% Efficiency, V_{IN}: 3.1V to 17V, $V_{OUT(MIN)}$ = 0.6V, I_Q < 8µA (Both Channels Enabled), ISD < 1µA, 3mm × 5mm QFN-24 Package
LTC3779	150V V_{IN} and V_{OUT} Synchronous 4-Switch Buck-Boost DC/DC Controller	4.5V ≤ V_{IN} ≤ 150V, Input or Output Average Current Loop, PLL, TSSOP-38 Package
LTC3784	Low I_Q, Multiphase, Dual Channel Single Output Synchronous Step-Up DC/DC Controller	4.5V (Down to 2.5V After Start-Up) ≤ V_{IN} ≤ 60V, V_{OUT} Up to 60V, PLL Fixed Frequency 50kHz to 900kHz , I_Q = 28µA
LTC3807	38V, Low I_Q, Synchronous Step-Down Controller with 24V Output Voltage Capability	PLL Fixed Frequency 50kHz to 900kHz, 4V ≤ V_{IN} ≤ 38V, 0.8V ≤ V_{OUT} ≤ 24V, I_Q = 50µA
LTC3871	100V Bidirectional PolyPhase® Buck or Boost Controller	Dynamic Regulation of V_{IN}, V_{OUT} and Current, PLL, Current Monitor, 48-Lead LQPF Package
LTM®4636	40A DC/DC µModule Step-Down Regulator	Complete 40A Switch Mode Power Supply, 4.75V ≤ V_{IN} ≤ 15V, 0.6V ≤ V_{OUT} ≤ 3.3V, 16mm × 16mm × 7.12mm BGA
LTC7150S	20V, 20A Synchronous Step-Down Regulator	93% Efficiency, V_{IN}: 3.1V to 20V, $V_{OUT(MIN)}$ = 0.6V, Output Remote Sense, 42-Lead 6mm × 5mm × 1.3mm BGA Package
LT®8640S	42V, 6A Synchronous Step-Down Silent Switcher®2	I_Q = 2.5µA, $V_{IN(MIN)}$ = 3.4V, $V_{OUT(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0
LTC7106	A 7-bit Current DAC with Digital PMBus Interface	2.5V ≤ V_{DD} ≤ 5.5V, Wide I_{DAC}, ±16µA to ±250µA

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