Polmaddie7 User Manual

Issue – 1.0

Foreword

PLEASE READ THIS ENTIRE MANUAL BEFORE PLUGGING IN OR POWERING UP YOUR POLMADDIE7 BOARD.
PLEASE TAKE SPECIAL NOTE OF THE WARNINGS WITHIN THIS MANUAL.

Trademarks

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Polmaddie7 is a trademark of Enterpoint Ltd.

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Introduction

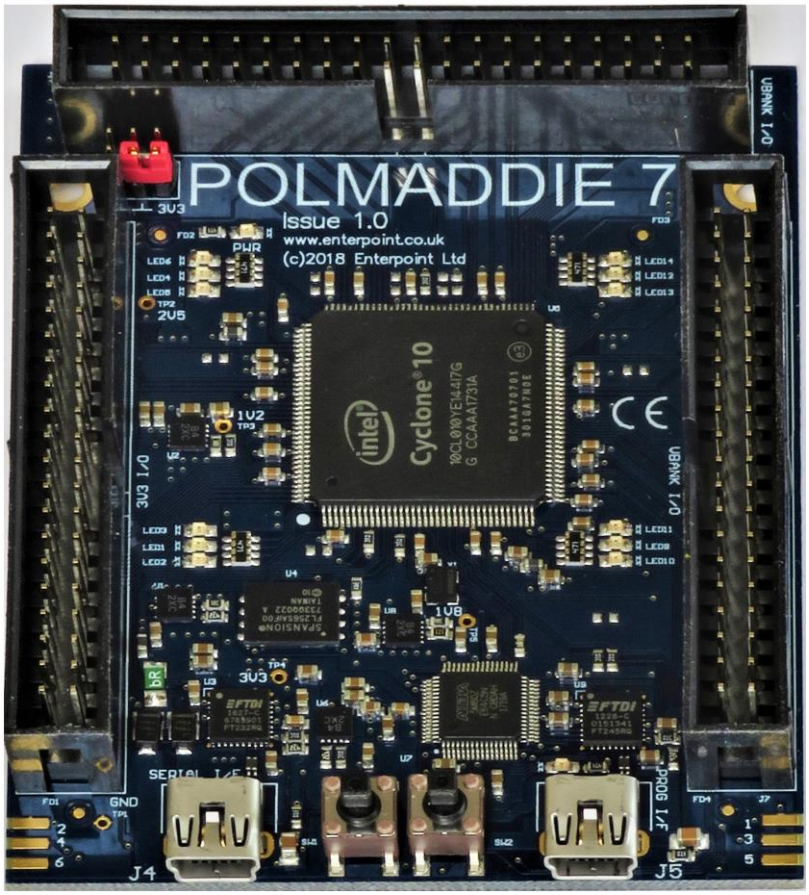

Figure 1 – Polmaddie7 Board

Welcome to your Polmaddie7 board. The Polmaddie series of CPLD/FPGA development boards offer high quality, high user I/O, solutions for training and development purposes. Polmaddie7 is targeted at students and engineers and offered at a competitive price point. The product is also in a production friendly format allowing customers to incorporate this product as working OEM element within their design. As with all Enterpoint board products we expect to offer this product for sale on a long lifetime schedule from launch (2018) with an expected manufacturing lifecycle typically of between 10 and 15 years. For more specific guarantees please contact us.

Enterpoint can offer custom board derivatives and further development assistance services to customers wishing to base their project on a Polmaddie product but needing a more custom solution for production equipment usage. Please contact us if you wish to know more.

Polmaddie7 features an Intel® Cyclone®10-LP FPGA which is highly flexible and facilitates development of general logic or even simple microprocessor systems based on an Intel® NIOS® processor. The standard FPGA fit on Polmaddie7 is a part number 10CL010YE144I7G. Other variants can be offered subject to minimum order value or quantity. Please contact us if this of interest for a quote.

The aim of this manual is to assist in using the main features of Polmaddie7. More extensive support is available through our website www.enterpoint.co.uk or our support email - support@enterpoint.co.uk.

Polmaddie7 features

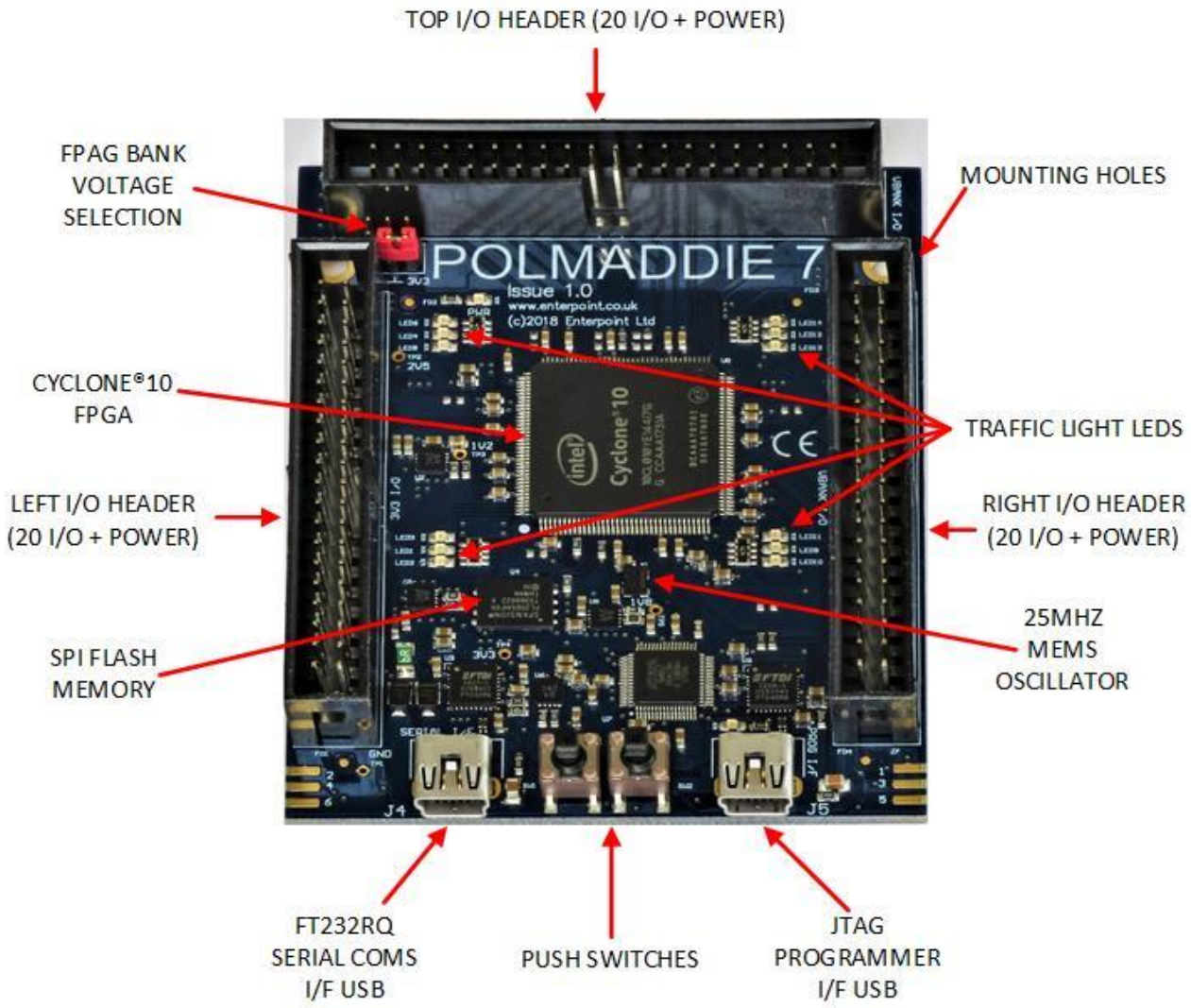

Figure 2 – Polmaddie7 Features

Getting Started

Your Polmaddie7 will be supplied pre-programmed with a ‘traffic lights’ test design. The test design will allow the user to determine that the LEDs and the push button switches of the Polmaddie7 board are working. To use this test you should:

(1) Apply power to the Polmaddie7 board by plugging in one or both of the USB interfaces to a host computer or power supply.

(2) The LEDs should light in a ‘traffic lights’ sequence. There is also Power indicator LED which will light to show that power is present.

(3) Press SW1 (This is the left Push Button switch). The traffic lights sequence will reset to the beginning of the sequence.

(4) Press SW2 (This is the right Push Button switch). The traffic lights sequence will pause until the switch is released.

Power Features

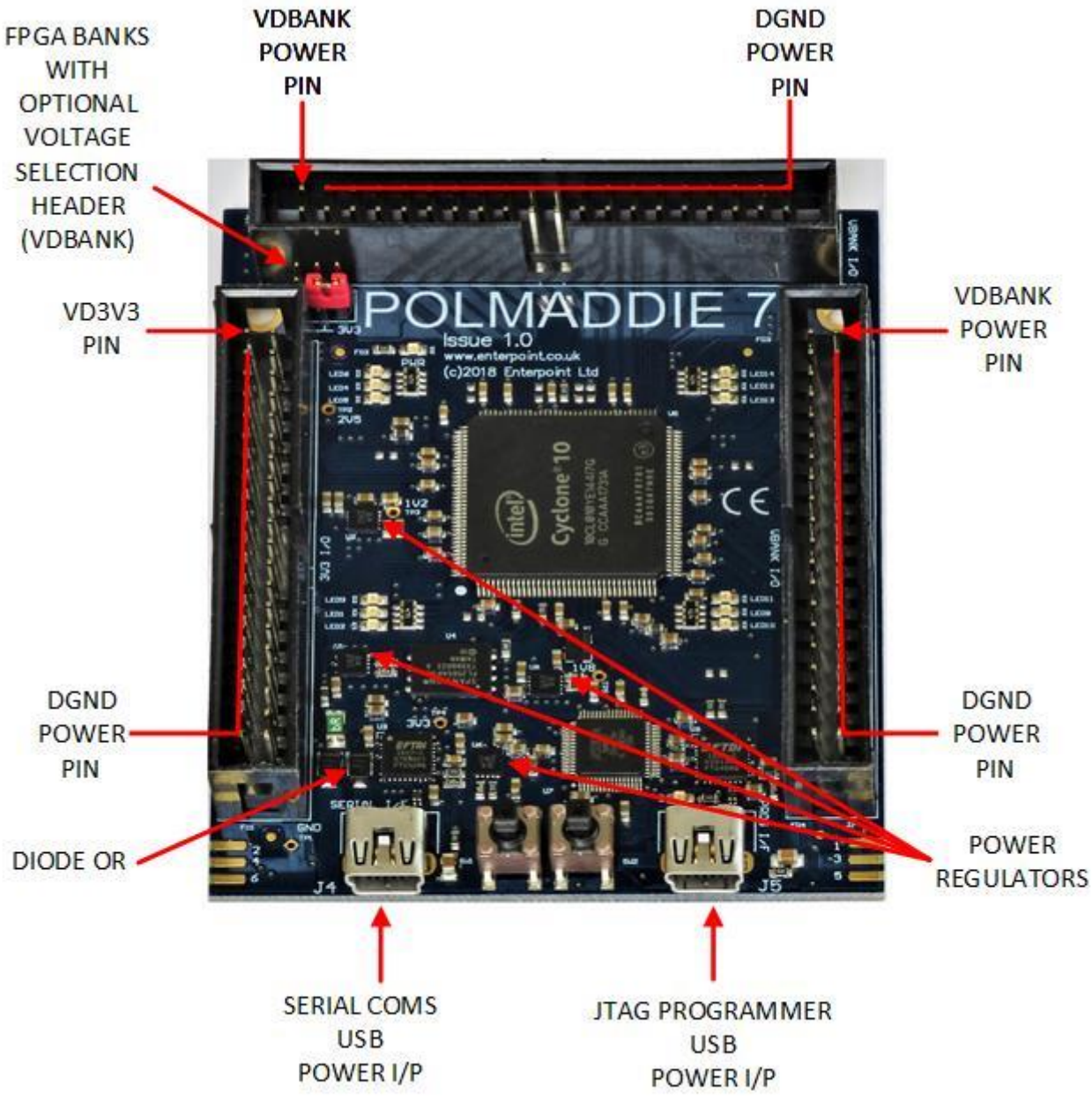

*Figure 3 – Polmaddie7 Power Supply Features***.**

WARNING – THE REGULATORS MAY BECOME HOT IN NORMAL OPERATION ALONG WITH THE BOARDS THERMAL RELIEF. PLEASE DO NOT TOUCH OR PLACE HIGHLY FLAMABLE MATERIALS NEAR THESE DEVICES WHILST THE POLMADDIE7 BOARD IS IN OPERATION.

Polmaddie7 is powered either by connecting either USB interface to host computer or a standard USB (5V) power supply. The board has a diode ORs circuit for the USB power inputs. This can facilitate a crude fall over to backup battery, or secondary, supply if required.

For this battery backup technique to work the battery/secondary input must be less that the main supply or it will continuously supply power instead of your primary. A typical battery approach might be a stack of 3 AA alkaline batteries each with a nominal 1.5V output giving a series voltage of approximately 4.5V.

To ensure all on board regulators operate correctly any input voltage should not be less than 4.3V and not more than 5.5V. Input voltages above 5.5V will potentially damage the circuits contained within this product.

Polmaddie7 provides power to add-on modules through the three 2x20 IDC style headers. These headers are aligned on a 2.54mm (0.1 inch) grid facilitating stripboard add-ons. The top and right headers each have a pin with power supply VDBANK on it. This voltage corresponds to that supplied to FPGA bank I/Os that are available on the top and right I/O headers. The left side header has 3.3V available and that corresponds to FPGA I/Os available on that header. The current limit for any rail (including Polmaddie7 usage) is 1.2A.

Each header has 19 GND/0V (DGND) pins for connection to add-on modules. These also facilitate cross talk minimisation when IDC ribbon cables are used in these headers.

There are test points on board for most power rails. These are marked on the silk screen of the board. If using these test points care must be taken not to short to adjacent pins and components.

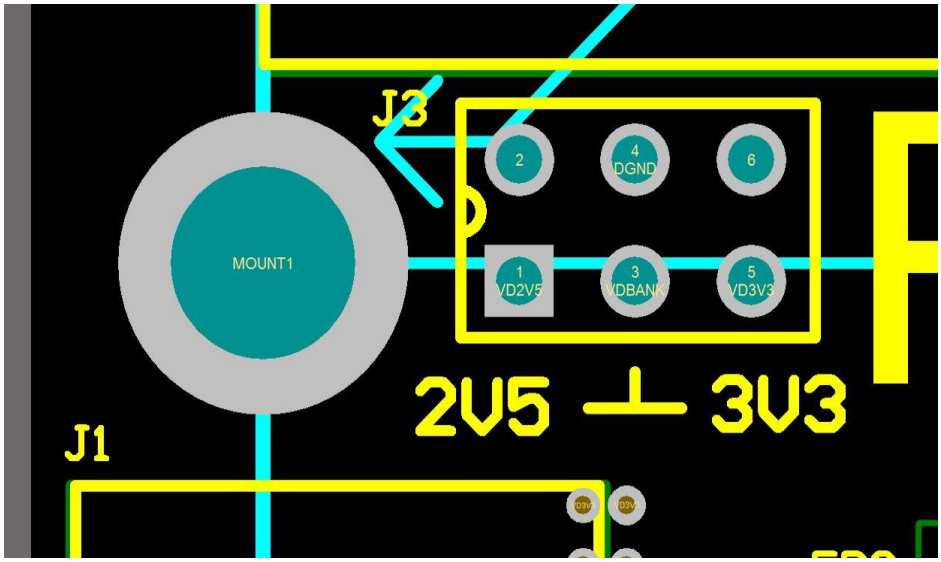

Figure 4 – Polmaddie7 FPGA Bank Voltage Selection.

The VDBANK selection header shown above offers selection between 2.5V and 3.3V as standard using a supplied 2mm jumper. However it also possible to plug in a regulator module to facilitate other voltages e.g. 1.8V. Contact us should you wish to use this feature.

Detail pinouts follow:

IO Headers

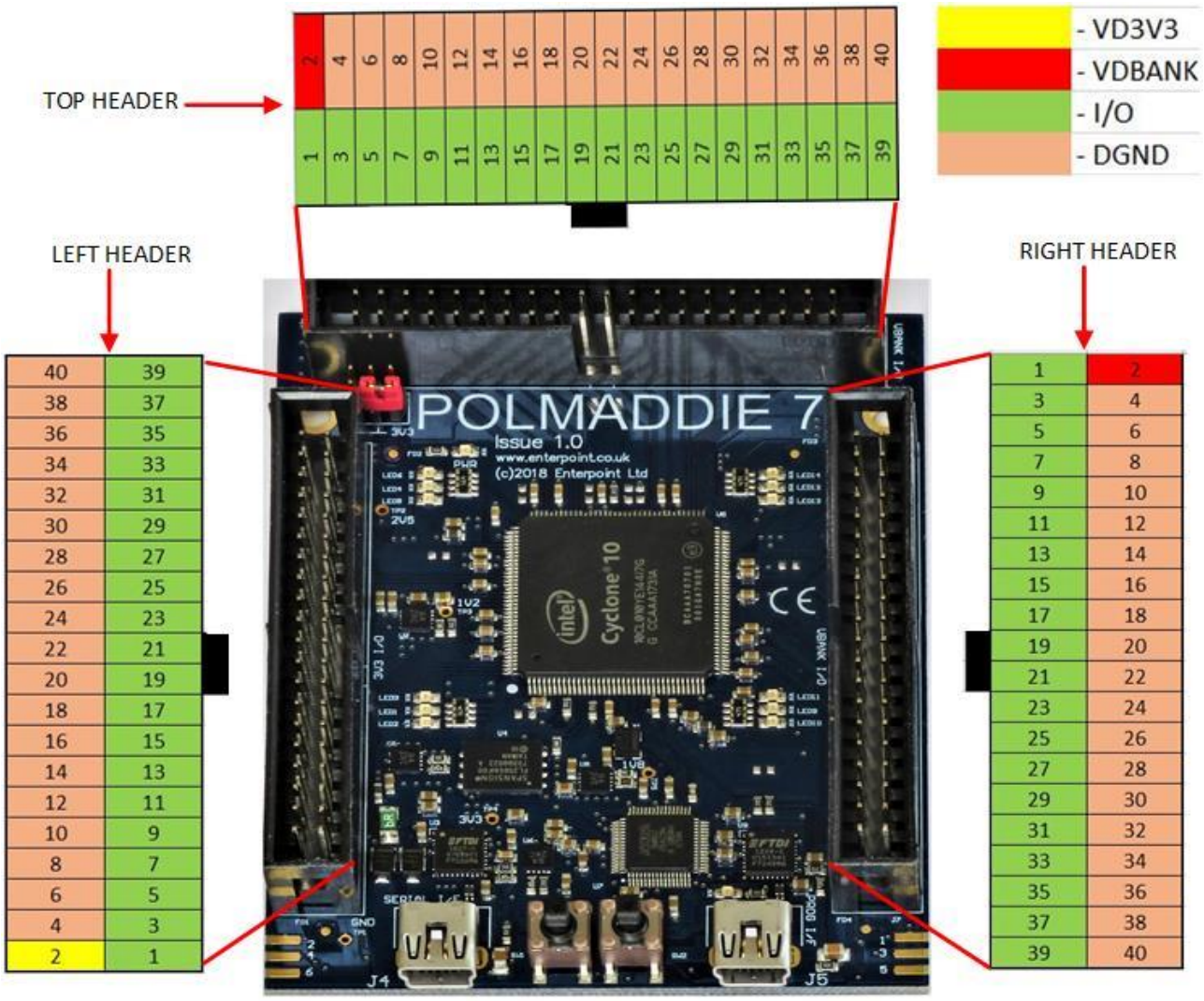

Figure 5 – Polmaddie7 Headers

The three 40-pin IDC Headers provide a simple mechanical and electrical interface for external signal inputs. The connectors on this header are on a 0.1inch (2.54mm), pitch and allow other electronic circuitry or user-designed add-on boards to be connected.

The left header I/O operates at a fixed 3.3V bank voltage and should not have a voltage exceeding 3.465V applied. These connect to Banks7 and 8 of the FPGA.

The top header I/O operates at a variable bank voltage selected by the bank voltage selection header. I/O should not have a voltage exceeding 3.465V(3.3V selected) or 2.625V(2.5V selected) applied. These connect to Banks 4,5 and 6 of the FPGA.

The right header I/O operates at a variable bank voltage selected by the bank voltage selection header. I/O should not have a voltage exceeding 3.465V(3.3V selected) or 2.625V(2.5V selected) applied. These connect to Banks 3 and 4 of the FPGA.

LEFT HEADER				
PIN	USE	FPGA PIN	PIN	USE
1	IO40	144	2	3.3V
3	IO39	143	4	0V
5	IO38	142	6	0V
7	IO37	141	8	0V
9	IO36	137	10	0V
11	IO35	136	12	0V
13	IO34	135	14	0V
15	IO33	133	16	0V
17	IO32	132	18	0V
19	IO31	129	20	0V
21	IO30	128	22	0V
23	IO29	127	24	0V
25	IO28	126	26	0V
27	IO27	125	28	0V
29	IO26	124	30	0V
31	IO25	121	32	0V
33	IO24	120	34	0V
35	IO23	119	36	0V
37	IO22	113	38	0V
39	IO21	112	40	0V

Figure 6

TOP HEADER				
PIN	USE	FPGA PIN	PIN	USE
1	IO20	106	2	VDBANK
3	IO19	105	4	0V
5	IO18	103	6	0V
7	IO17	101	8	0V
9	IO16	100	10	0V
11	IO15	99	12	0V
13	IO14	98	14	0V
15	IO13	87	16	0V
17	IO12	86	18	0V
19	IO11	85	20	0V
21	IO10	84	22	0V
23	IO9	80	24	0V
25	IO8	77	26	0V
27	IO7	76	28	0V
29	IO6	75	30	0V
31	IO5	74	32	0V
33	IO4	73	34	0V
35	IO3	72	36	0V
37	IO2	71	38	0V
39	IO1	70	40	0V

Figure 7

RIGHT HEADER				
PIN	USE	FPGA PIN	PIN	USE
1	IO60	96	2	VDBANK
3	IO59	67	4	0V
5	IO58	66	6	0V
7	IO57	65	8	0V
9	IO56	60	10	0V
11	IO55	59	12	0V
13	IO54	58	14	0V
15	IO53	55	16	0V
17	IO52	54	18	0V
19	IO51	53	20	0V
21	IO50	52	22	0V
23	IO49	51	24	0V
25	IO48	50	26	0V
27	IO47	49	28	0V
29	IO46	46	30	0V
31	IO45	44	32	0V
33	IO44	43	34	0V
35	IO43	42	36	0V
37	IO42	39	38	0V
39	IO41	38	40	0V

Figure 8

More information about the IO specifications and capabilities is available from https://www.altera.com/documentation/egg1487191218630.html#qed1487191199116 .

FPGA

The main device on the Polmaddie7 is the Intel Cyclone10-LP 10CL010YE144I7G FPGA. More information on the Cyclone10-LP family can be found at https://www.altera.com/products/fpga/cyclone-series/cyclone-10/cyclone-10-lp/overview.html .

Oscillator

The oscillator on Polmaddie7 is a 25MHz ASEMB oscillator operating at 3.3V. This clock signal is routed via the programming circuit and connects to the FPGA on pin 22.

LEDs

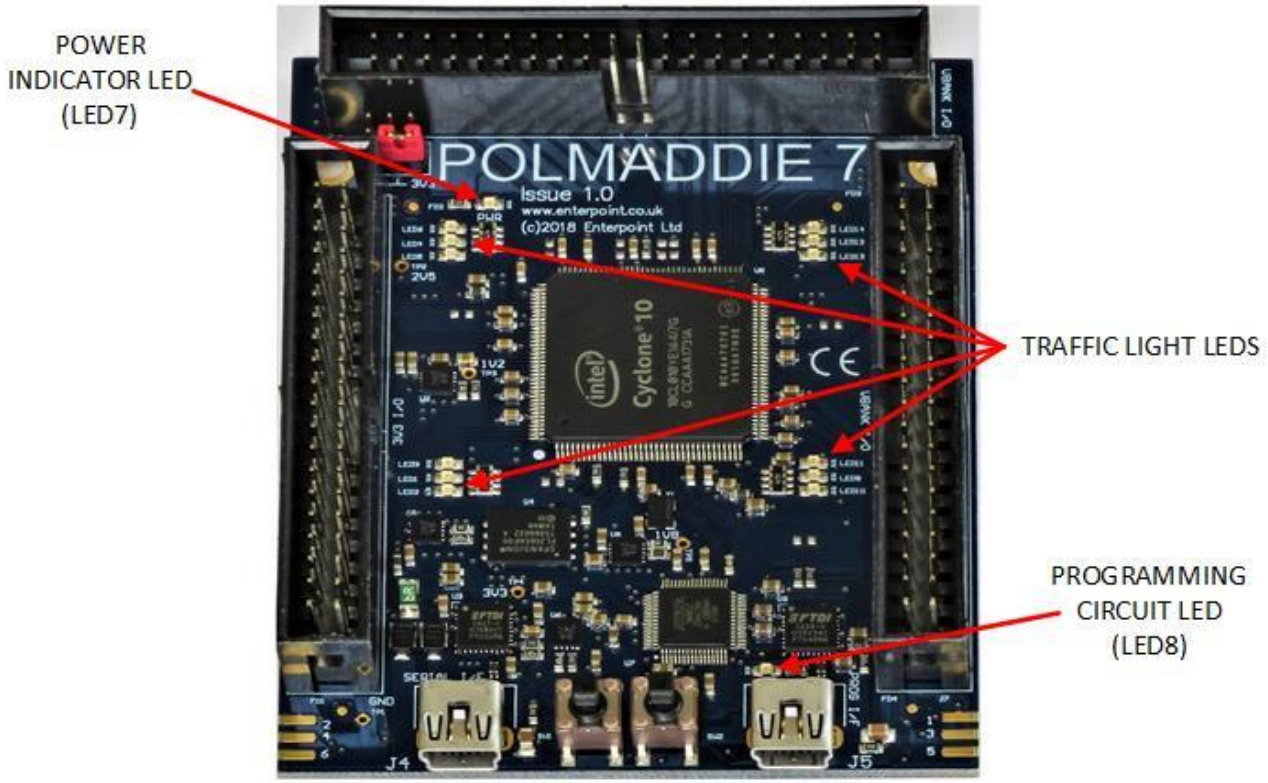

Figure 9 – Position of LEDs

Polmaddie7 has 14 LEDs.

LED7 is a green power indicator LED and indicates the presence of the 3.3V supply. It cannot be controlled by the FPGA.

LED8 is the programming indicator LED and not controlled by the FPGA.

LEDs 1 to 6 and 9 to 14 are arranged in 4 blocks of three, each block having one red, one yellow and one green LED. This means they can be used to simulate traffic lights. They are all controlled by the FPGA. They connect to the FPGA as shown below:

LED	FPGA PIN	COLOUR	LED	FPGA PIN	COLOUR
LED11(RL)	34	RED	LED3(LL)	138	RED
LED9(RL)	33	YELLOW	LED1(LL)	2	YELLOW
LED10(RL)	32	GREEN	LED2(LL)	1	GREEN
LED14(RU)	69	RED	LED6(LU)	115	RED
LED12(RU)	31	YELLOW	LED4(LU)	114	YELLOW
LED13(RU)	28	GREEN	LED5(LU)	111	GREEN

Figure 10 –LED FPGA pins.

LL – Left Lower
LU – Left Upper
RL – Right Lower
RU – Right Upper

Switches

Figure 11 –LED FPGA pins.

Polmaddie7 has two push button switches with individual inputs to the FPGA. When pushed they pull down the input which each of which has a 10Kohm pullup to 3.3V.

The two switches are connected to the following IO pins:

SW1	SW2
24	25

USB Coms Interface

Figure 12 – USB coms interface.

The USB coms interface on the Polmaddie7 is implemented using an FT232RQ USB to serial UART interface IC. The datasheet and drivers for this device are available from http://www.ftdichip.com. When appropriate drivers are installed in the host the Polmaddie7 USB coms port should be detected as a serial port. Polmaddie7 is wired to support TXD, RXD, RTS and CTS signals. Flow control RTS and CTS do not need to be used in an active fashion.

The connections between the USB device and the FPGA are shown below:

FT232RQ PIN	FPGA DIRECTION	FPGA PIN
TXD	INPUT	11
RTS	INPUT	10
RXD	OUTPUT	7
CTS	OUTPUT	3

Figure 13 – USB coms interface pinout.

Programming Polmaddie7

The programming of the FPGA on Polmaddie7 can be achieved using the Intel® tool QuartusII and the Polmaddie in built JTAG programmer. QuartusII Version 17 or later is required to program the Cyclone10-LP device. Connect the USB JTAG Programmer interface to the host PC with the supplied cable and the board will be recognised as a Blaster Cable provided QuartusII is installed with appropriate drivers.

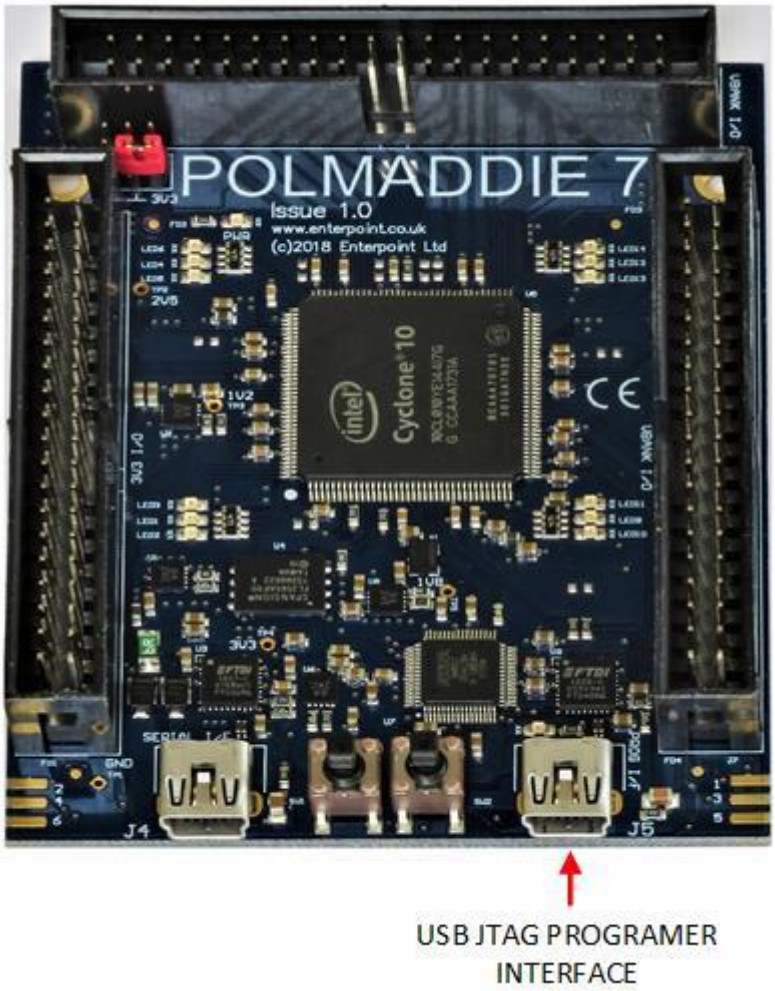

Figure 14 – USB JTAG programmer interface..

To program you will first have to build your source design and then apply a file conversion as described in QuartusII documentation.

Mechanical Arrangement

Dimensions are in millimetres. The three 40-way connectors are arranged on a 0.1 inch grid relative to each other.

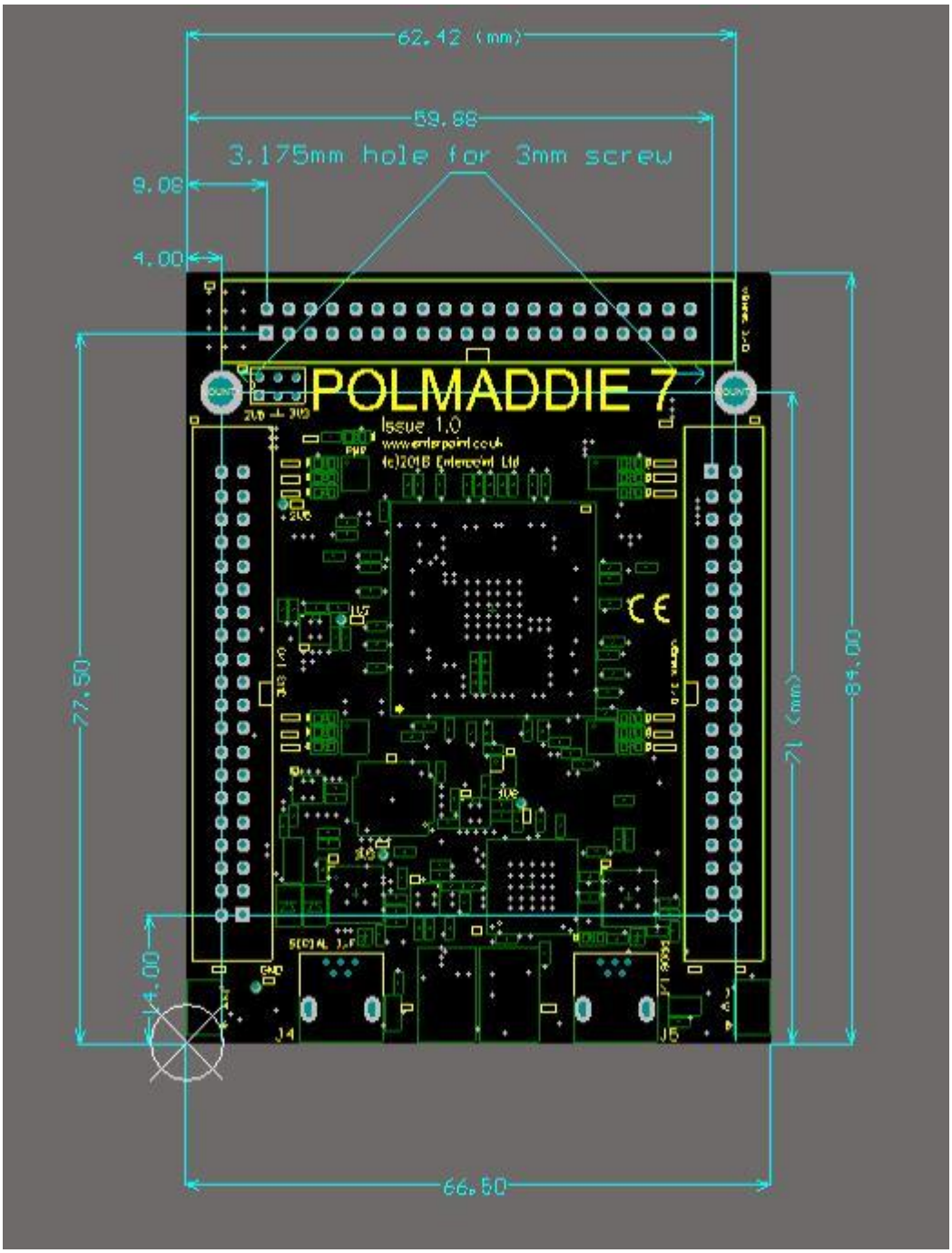

Figure 10– Polmaddie7 Mechanical Arrangement

The PCB is 1.6mm thick and the tallest component are the IDC headers which are approximately 9.1mm high. Dimensions are subject to manufacturing tolerances.

Medical and Safety Critical Use

Polmaddie7 boards are not authorised for the use in, or use in the design of, medical or other safety critical systems without the express written person of the Board of Enterpoint. If such use is allowed the said use will be entirely the responsibility of the user. Enterpoint Ltd will accepts no liability for any failure or defect of the Polmaddie7 board, or its design, when it is used in any medical or safety critical application

Warranty

Polmaddie7 comes with a 90 return to base warranty. Enterpoint reserves the right not honour a warranty if the failure is due to maltreatment of the Polmaddie7 board.

Outside the warranty period Enterpoint offers a fixed price repair or replacement service. We reserve the right not to offer this service where a Polmaddie7 has been maltreated or otherwise deliberately damaged. Please contact support if need to use this service.

Other specialised warranty programs can be offered to users of multiple Enterpoint products. Please contact sales on boardsales@enterpoint.co.uk if you are interested in these types of warranty,

Support

Enterpoint offers support during normal United Kingdom working hours 9.00am to 5.00pm. Please examine our Polmaddie7 FAQ web page and the contents of this manual before raising a support query. We can be contacted as follows:

Telephone - +44 (0) 1684 566499
Email - support@enterpoint.co.uk