

### FEATURES

*isoPower* integrated, isolated dc-to-dc converter

Regulated 3.15 V to 5.25 V output

Up to 150 mW output power

High common-mode transient immunity: >25 kV/μs

*iCoupler* integrated I<sup>2</sup>C digital isolator

Bidirectional I<sup>2</sup>C communication

3.0 V to 5.5 V supply/logic levels

Open-drain interfaces

Suitable for hot swap applications

30 mA current sink capability

1000 kHz maximum frequency

20-lead SSOP package with 5.3 mm creepage

High temperature operation: 105°C

**Safety and regulatory approvals**

UL recognition

2500 V rms for 1 minute per UL 1577

CSA Component Acceptance Notice 5A

VDE Certificate of Conformity (pending)

DIN V VDE V 0884-10 (VDE V 0884-10):2006-12

V<sub>IORM</sub> = 560 V peak

### APPLICATIONS

Isolated I<sup>2</sup>C, SMBus, and PMBus interfaces

Multilevel I<sup>2</sup>C interfaces

Central office switching

Telecommunication and data communication equipment

–48 V distributed power systems

–48 V power supply modules

Networking

### GENERAL DESCRIPTION

Based on the *iCoupler*<sup>®</sup> and *isoPower*<sup>®</sup> chip scale transformer technology, the ADM3260<sup>1</sup> is a hot swappable digital and power isolator with two nonlatching, bidirectional communication channels, supporting a complete isolated I<sup>2</sup>C interface, and an integrated isolated dc-to-dc converter, supporting up to 150 mW of isolated power conversion.

*iCoupler* is a chip scale transformer technology with functional, performance, size, and power consumption advantages as compared to optocouplers. The bidirectional I<sup>2</sup>C channels eliminate the need for splitting I<sup>2</sup>C signals into separate transmit and receive signals for use with standalone optocouplers.

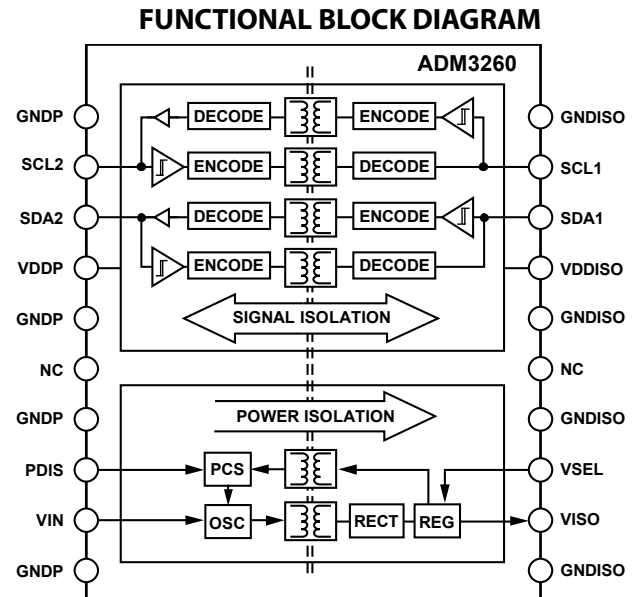


Figure 1.

Table 1. Power Levels for Isolated Converter

| Input Voltage (V) | Output Voltage (V) | Output Power (mW) |
|-------------------|--------------------|-------------------|
| 5.0               | 5.0                | 150               |
| 5.0               | 3.3                | 100               |
| 3.3               | 3.3                | 66                |

Based on the Analog Devices, Inc., *isoPower* technology, the on-chip isolated dc-to-dc converter provides a regulated, isolated voltage of 3.15 V to 5.25 V with up to 150 mW of output power (see Figure 1).

With the ADM3260, the *iCoupler* and *isoPower* channels, along with the I<sup>2</sup>C transceivers, can be integrated with semiconductor circuitry, which enables a complete isolated I<sup>2</sup>C interface and allows the power converter to be implemented in a small form factor. The ADM3260 is available in 20-lead SSOP package and has an operating temperature range of –40°C to +105°C.

*isoPower* uses high frequency switching elements to transfer power through its transformer. Special care must be taken during printed circuit board (PCB) layout to meet emissions standards. See the AN-0971 Application Note for board layout recommendations.

<sup>1</sup> Protected by U.S. Patents 5,952,849; 6,873,065; and 7,075,329. Other patents are pending.

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## REVISION HISTORY

### 11/2017—Rev. C to Rev. D

|                         |   |
|-------------------------|---|
| Change to Table 1 ..... | 1 |
|-------------------------|---|

### 3/2016—Rev. B to Rev. C

|  |    |
|--|----|
| Changed VDDP (V) to VIN (V), Table 15..... | 10 |
|--|----|

### 4/2015—Rev. A to Rev. B

|   |    |
|---|----|
| Changes to Features Section.....                | 1  |
| Changes to Table 9 and Table 10.....            | 7  |
| Changes to Functional Description Section ..... | 15 |

### 6/2014—Rev. 0 to Rev. A

|                                 |    |
|---------------------------------|----|
| Changes to Pin 8, Table 16..... | 11 |
|---------------------------------|----|

### 12/2013—Revision 0: Initial Version

## SPECIFICATIONS

### ELECTRICAL CHARACTERISTICS—5 V PRIMARY INPUT SUPPLY/5 V SECONDARY ISOLATED SUPPLY

All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = V_{ISO} = 5\text{ V}$ , VSEL resistor network  $R_{BOTTOM} = 10\text{ k}\Omega$ ,  $R_{TOP} = 30.9\text{ k}\Omega$ . Minimum/maximum specifications apply over the entire recommended operation range which is  $4.5\text{ V} \leq V_{IN}$ ,  $V_{ISO} \leq 5.5\text{ V}$ , and  $-40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$ , unless otherwise noted. Switching specifications are tested with  $C_L = 15\text{ pF}$  and CMOS signal levels, unless otherwise noted.

Table 2.

| Parameter                        | Symbol           | Min | Typ | Max | Unit                         | Test Conditions/Comments  |
|----------------------------------|------------------|-----|-----|-----|------------------------------|---|
| DC-TO-DC CONVERTER SUPPLY        |                  |     |     |     |                              |   |
| Setpoint                         | $V_{ISO}$        |     | 5   |     | V                            | $I_{ISO} = 15\text{ mA}$ , $R_{BOTTOM} = 10\text{ k}\Omega$ , $R_{TOP} = 30.9\text{ k}\Omega$                     |
| Thermal Coefficient              | $V_{ISO(TC)}$    |     | -44 |     | $\mu\text{V}/^\circ\text{C}$ |   |
| Line Regulation                  | $V_{ISO(LINE)}$  |     | 20  |     | mV/V                         | $I_{ISO} = 15\text{ mA}$ , $V_{IN} = 4.5\text{ V to } 5.5\text{ V}$   |
| Load Regulation                  | $V_{ISO(LOAD)}$  |     | 1.3 | 3   | %                            | $I_{ISO} = 3\text{ mA to } 27\text{ mA}$  |
| Output Ripple                    | $V_{ISO(RIP)}$   |     | 75  |     | mV p-p                       | 20 MHz bandwidth, $C_{OUTPUT\_BYPASS} = 0.1\text{ }\mu\text{F}  10\text{ }\mu\text{F}$ , $I_{ISO} = 27\text{ mA}$ |
| Output Noise                     | $V_{ISO(NOISE)}$ |     | 200 |     | mV p-p                       | $C_{OUTPUT\_BYPASS} = 0.1\text{ }\mu\text{F}  10\text{ }\mu\text{F}$ , $I_{ISO} = 27\text{ mA}$                   |
| Switching Frequency              | $f_{OSC}$        |     | 125 |     | MHz                          |   |
| Pulse-Width Modulation Frequency | $f_{PWM}$        |     | 600 |     | kHz                          |   |
| Output Current                   | $I_{ISO(MAX)}$   | 30  |     |     | mA                           | $V_{ISO} > 4.5\text{ V}$  |
| Efficiency at $I_{ISO(MAX)}$     |                  |     | 29  |     | %                            | $I_{ISO} = 27\text{ mA}$  |
| $I_{VIN}$ , No $V_{ISO}$ Load    | $I_{VIN(Q)}$     |     | 6.8 | 12  | mA                           |   |
| $I_{VIN}$ , Full $V_{ISO}$ Load  | $I_{VIN(MAX)}$   |     | 104 |     | mA                           |   |
| Thermal Shutdown                 |                  |     |     |     |                              |   |
| Shutdown Temperature             | $T_{SHUTDOWN}$   |     | 154 |     | $^\circ\text{C}$             |   |
| Thermal Hysteresis               | $T_{HYST}$       |     | 10  |     | $^\circ\text{C}$             |   |

### ELECTRICAL CHARACTERISTICS—5 V PRIMARY INPUT SUPPLY/3.3 V SECONDARY ISOLATED SUPPLY

All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 5\text{ V}$ ,  $V_{ISO} = 3.3\text{ V}$ , VSEL resistor network  $R_{BOTTOM} = 10\text{ k}\Omega$ ,  $R_{TOP} = 16.9\text{ k}\Omega$ . Minimum/maximum specifications apply over the entire recommended operation range, which is  $4.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}$ ,  $3\text{ V} \leq V_{ISO} \leq 3.6\text{ V}$ , and  $-40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$ , unless otherwise noted. Switching specifications are tested with  $C_L = 15\text{ pF}$  and CMOS signal levels, unless otherwise noted.

Table 3.

| Parameter                        | Symbol           | Min | Typ | Max | Unit                         | Test Conditions/Comments  |
|----------------------------------|------------------|-----|-----|-----|------------------------------|---|
| DC-TO-DC CONVERTER SUPPLY        |                  |     |     |     |                              |   |
| Setpoint                         | $V_{ISO}$        |     | 3.3 |     | V                            | $I_{ISO} = 15\text{ mA}$ , $R_{BOTTOM} = 10\text{ k}\Omega$ , $R_{TOP} = 16.9\text{ k}\Omega$                     |
| Thermal Coefficient              | $V_{ISO(TC)}$    |     | -26 |     | $\mu\text{V}/^\circ\text{C}$ |   |
| Line Regulation                  | $V_{ISO(LINE)}$  |     | 20  |     | mV/V                         | $I_{ISO} = 15\text{ mA}$ , $V_{IN} = 4.5\text{ V to } 5.5\text{ V}$   |
| Load Regulation                  | $V_{ISO(LOAD)}$  |     | 1.3 | 3   | %                            | $I_{ISO} = 3\text{ mA to } 27\text{ mA}$  |
| Output Ripple                    | $V_{ISO(RIP)}$   |     | 50  |     | mV p-p                       | 20 MHz bandwidth, $C_{OUTPUT\_BYPASS} = 0.1\text{ }\mu\text{F}  10\text{ }\mu\text{F}$ , $I_{ISO} = 27\text{ mA}$ |
| Output Noise                     | $V_{ISO(NOISE)}$ |     | 130 |     | mV p-p                       | $C_{OUTPUT\_BYPASS} = 0.1\text{ }\mu\text{F}  10\text{ }\mu\text{F}$ , $I_{ISO} = 27\text{ mA}$                   |
| Switching Frequency              | $f_{OSC}$        |     | 125 |     | MHz                          |   |
| Pulse-Width Modulation Frequency | $f_{PWM}$        |     | 600 |     | kHz                          |   |
| Output Current                   | $I_{ISO(MAX)}$   | 30  |     |     | mA                           | $3\text{ V} < V_{ISO} < 3.6\text{ V}$   |
| Efficiency at $I_{ISO(MAX)}$     |                  |     | 24  |     | %                            | $I_{ISO} = 27\text{ mA}$  |
| $I_{VIN}$ , No $V_{ISO}$ Load    | $I_{VIN(Q)}$     |     | 3.2 | 8   | mA                           |   |
| $I_{VIN}$ , Full $V_{ISO}$ Load  | $I_{VIN(MAX)}$   |     | 85  |     | mA                           |   |
| Thermal Shutdown                 |                  |     |     |     |                              |   |
| Shutdown Temperature             | $T_{SHUTDOWN}$   |     | 154 |     | $^\circ\text{C}$             |   |
| Thermal Hysteresis               | $T_{HYST}$       |     | 10  |     | $^\circ\text{C}$             |   |

**ELECTRICAL CHARACTERISTICS—3.3 V PRIMARY INPUT SUPPLY/3.3 V SECONDARY ISOLATED SUPPLY**

All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = V_{ISO} = 3.3\text{ V}$ , VSEL resistor network  $R_{BOTTOM} = 10\text{ k}\Omega$ ,  $R_{TOP} = 16.9\text{ k}\Omega$ . Minimum/maximum specifications apply over the entire recommended operation range which is  $3.0\text{ V} \leq V_{IN}$ ,  $V_{ISO} \leq 3.6\text{ V}$ , and  $-40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$ , unless otherwise noted. Switching specifications are tested with  $C_L = 15\text{ pF}$  and CMOS signal levels, unless otherwise noted.

Table 4.

| Parameter                        | Symbol           | Min | Typ | Max  | Unit                         | Test Conditions/Comments  |
|----------------------------------|------------------|-----|-----|------|------------------------------|---|
| <b>DC-TO-DC CONVERTER SUPPLY</b> |                  |     |     |      |                              |   |
| Setpoint                         | $V_{ISO}$        |     | 3.3 |      | V                            | $I_{ISO} = 10\text{ mA}$ , $R_{BOTTOM} = 10\text{ k}\Omega$ , $R_{TOP} = 16.9\text{ k}\Omega$                     |
| Thermal Coefficient              | $V_{ISO(TC)}$    |     | -26 |      | $\mu\text{V}/^\circ\text{C}$ | $I_{ISO} = 20\text{ mA}$  |
| Line Regulation                  | $V_{ISO(LINE)}$  |     | 20  |      | mV/V                         | $I_{ISO} = 10\text{ mA}$ , $V_{IN} = 3.0\text{ V to }3.6\text{ V}$  |
| Load Regulation                  | $V_{ISO(LOAD)}$  |     | 1.3 | 3    | %                            | $I_{ISO} = 2\text{ mA to }18\text{ mA}$   |
| Output Ripple                    | $V_{ISO(RIP)}$   |     | 50  |      | mV p-p                       | 20 MHz bandwidth, $C_{OUTPUT\_BYPASS} = 0.1\text{ }\mu\text{F}  10\text{ }\mu\text{F}$ , $I_{ISO} = 18\text{ mA}$ |
| Output Noise                     | $V_{ISO(Noise)}$ |     | 130 |      | mV p-p                       | $C_{OUTPUT\_BYPASS} = 0.1\text{ }\mu\text{F}  10\text{ }\mu\text{F}$ , $I_{ISO} = 18\text{ mA}$                   |
| Switching Frequency              | $f_{OSC}$        |     | 125 |      | MHz                          |   |
| Pulse-Width Modulation Frequency | $f_{PWM}$        |     | 600 |      | kHz                          |   |
| Output Current                   | $I_{ISO(MAX)}$   | 20  |     |      | mA                           | $3.6\text{ V} > V_{ISO} > 3\text{ V}$   |
| Efficiency at $I_{ISO(MAX)}$     |                  |     | 27  |      | %                            | $I_{ISO} = 18\text{ mA}$  |
| $I_{VIN}$ , No $V_{ISO}$ Load    | $I_{VIN(Q)}$     |     | 3.3 | 10.5 | mA                           |   |
| $I_{VIN}$ , Full $V_{ISO}$ Load  | $I_{VIN(MAX)}$   |     | 77  |      | mA                           |   |
| <b>Thermal Shutdown</b>          |                  |     |     |      |                              |   |
| Shutdown Temperature             | $T_{SHUTDOWN}$   |     | 154 |      | $^\circ\text{C}$             |   |
| Thermal Hysteresis               | $T_{HYST}$       |     | 10  |      | $^\circ\text{C}$             |   |

**DC-TO-DC CONVERTER CHARACTERISTICS**

All typical specifications are at  $T_A = 25^\circ\text{C}$ . Minimum/maximum specifications apply over the entire recommended operation range unless otherwise noted. Switching specifications are tested with  $C_L = 15\text{ pF}$  and CMOS signal levels, unless otherwise noted.

Table 5.

| Parameter                   | Symbol     | Min          | Typ   | Max          | Unit          | Test Conditions/Comments               |
|-----------------------------|------------|--------------|-------|--------------|---------------|--|
| <b>UNDERVOLTAGE LOCKOUT</b> |            |              |       |              |               |  |
| Positive Going Threshold    | $V_{UV+}$  |              | 2.7   |              | V             | $V_{IN}$ , $V_{ISO}$ supply            |
| Negative Going Threshold    | $V_{UV-}$  |              | 2.4   |              | V             |  |
| <b>PDIS PIN</b>             |            |              |       |              |               |  |
| Input Threshold             |            |              |       |              |               |  |
| Logic High                  | $V_{IH}$   | 0.7 $V_{IN}$ |       |              | V             |  |
| Logic Low                   | $V_{IL}$   |              |       | 0.3 $V_{IN}$ | V             |  |
| Input Current               | $I_{PDIS}$ | -10          | +0.01 | +10          | $\mu\text{A}$ | $0\text{ V} \leq V_{PDIS} \leq V_{IN}$ |

## DIGITAL ISOLATOR DC SPECIFICATIONS

All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DDISO} = 3.3\text{ V}$  or  $5\text{ V}$ , and  $V_{DDP} = 3.3\text{ V}$  or  $5\text{ V}$ , unless otherwise noted. All voltages are relative to their respective ground.

Table 6.

| Parameter  | Symbol                                   | Min      | Typ  | Max      | Unit          | Test Conditions/Comments   |
|--|--|----------|------|----------|---------------|--|
| <b>I<sup>2</sup>C SIGNAL ISOLATION BLOCK</b>         |  |          |      |          |               |  |
| Input Supply Current                                 |  |          |      |          |               |  |
| Side 1 (5 V)   | $I_{DDISO1}$                             |          | 2.8  | 5.0      | mA            | $V_{DDISO} = 5\text{ V}$   |
| Side 2 (5 V)   | $I_{DDP1}$                               |          | 2.7  | 5.0      | mA            | $V_{DDP} = 5\text{ V}$   |
| Side 1 (3.3 V)                                       | $I_{DDISO2}$                             |          | 1.9  | 3.0      | mA            | $V_{DDISO} = 3.3\text{ V}$   |
| Side 2 (3.3 V)                                       | $I_{DDP2}$                               |          | 1.7  | 3.0      | mA            | $V_{DDP} = 3.3\text{ V}$   |
| LEAKAGE CURRENTS                                     | $I_{SDA1}, I_{SDA2}, I_{SCL1}, I_{SCL2}$ |          | 0.01 | 10       | $\mu\text{A}$ | $V_{SDA1} = V_{DDISO}, V_{SDA2} = V_{DDP}, V_{SCL1} = V_{DDISO}, V_{SCL2} = V_{DDP}$ |
| <b>SIDE 1 LOGIC LEVELS</b>                           |  |          |      |          |               |  |
| Logic Input Threshold <sup>1</sup>                   | $V_{SDA1T}, V_{SCL1T}$                   | 500      |      | 700      | mV            |  |
| Logic Low Output Voltages                            | $V_{SDA1OL}, V_{SCL1OL}$                 | 600      |      | 900      | mV            | $I_{SDA1} = I_{SCL1} = 3.0\text{ mA}$  |
|  |  | 600      |      | 850      | mV            | $I_{SDA1} = I_{SCL1} = 0.5\text{ mA}$  |
| Input/Output Logic Low Level Difference <sup>2</sup> | $\Delta V_{SDA1}, \Delta V_{SCL1}$       | 50       |      |          | mV            |  |
| <b>SIDE 2 LOGIC LEVELS</b>                           |  |          |      |          |               |  |
| Input Voltage  |  |          |      |          |               |  |
| Logic Low  | $V_{SDA2IL}, V_{SCL2IL}$                 |          |      | 0.3 VDDP | V             |  |
| Logic High   | $V_{SDA2IH}, V_{SCL2IH}$                 | 0.7 VDDP |      |          | V             |  |
| Output Voltage                                       |  |          |      |          |               |  |
| Logic Low  | $V_{SDA2OL}, V_{SCL2OL}$                 |          |      | 400      | mV            | $I_{SDA2} = I_{SCL2} = 30\text{ mA}$   |

<sup>1</sup>  $V_{IL} < 0.5\text{ V}$ ,  $V_{IH} > 0.7\text{ V}$ .

<sup>2</sup>  $\Delta V_{SDA1} = V_{SDA1OL} - V_{SDA1T}$ ,  $\Delta V_{SCL1} = V_{SCL1OL} - V_{SCL1T}$ . This is the minimum difference between the output logic low level and the input logic threshold within a given component. This ensures that there is no possibility of the device latching up the bus to which it is connected.

## DIGITAL ISOLATOR AC SPECIFICATIONS

All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DDISO} = 3.3\text{ V}$  or  $5\text{ V}$ , and  $V_{DDP} = 3.3\text{ V}$  or  $5\text{ V}$ , unless otherwise noted. Refer to Figure 17. All voltages are relative to their respective ground.

Table 7.

| Parameter                            | Symbol      | Min  | Typ | Max | Unit | Test Conditions/Comments   |
|--------------------------------------|-------------|------|-----|-----|------|--|
| MAXIMUM FREQUENCY                    |             | 1000 |     |     | kHz  |  |
| <b>OUTPUT FALL TIME</b>              |             |      |     |     |      |  |
| 5 V Operation                        |             |      |     |     |      | $4.5\text{ V} \leq V_{DDISO}, V_{DDP} \leq 5.5\text{ V}, C_{L1} = 40\text{ pF}, R1 = 1.6\text{ k}\Omega, C_{L2} = 400\text{ pF}, R2 = 180\text{ }\Omega$ |
| Side 1 Output (0.9 VDDISO to 0.9 V)  | $t_{f1}$    | 13   | 26  | 120 | ns   |  |
| Side 2 Output (0.9 VDDP to 0.1 VDDP) | $t_{f2}$    | 32   | 52  | 120 | ns   |  |
| 3 V Operation                        |             |      |     |     |      | $3.0\text{ V} \leq V_{DDISO}, V_{DDP} \leq 3.6\text{ V}, C_{L1} = 40\text{ pF}, R1 = 1.0\text{ k}\Omega, C_{L2} = 400\text{ pF}, R2 = 120\text{ }\Omega$ |
| Side 1 Output (0.9 VDDISO to 0.9 V)  | $t_{f1}$    | 13   | 32  | 120 | ns   |  |
| Side 2 Output (0.9 VDDP to 0.1 VDDP) | $t_{f2}$    | 32   | 61  | 120 | ns   |  |
| <b>PROPAGATION DELAY</b>             |             |      |     |     |      |  |
| 5 V Operation                        |             |      |     |     |      | $4.5 \leq V_{DDISO}, V_{DDP} \leq 5.5\text{ V}, C_{L1} = C_{L2} = 0\text{ pF}, R1 = 1.6\text{ k}\Omega, R2 = 180\text{ }\Omega$                          |
| Side 1 to Side 2                     |             |      |     |     |      |  |
| Rising Edge <sup>1</sup>             | $t_{PLH12}$ |      | 95  | 130 | ns   |  |
| Falling Edge <sup>2</sup>            | $t_{PHL12}$ |      | 162 | 275 | ns   |  |

| Parameter   | Symbol                     | Min | Typ       | Max        | Unit        | Test Conditions/Comments   |  |
|---|----------------------------|-----|-----------|------------|-------------|--|--|
| Side 2 to Side 1<br>Rising Edge <sup>3</sup><br>Falling Edge <sup>4</sup><br>3 V Operation                  | $t_{PLH21}$<br>$t_{PHL21}$ |     | 31<br>85  | 70<br>155  | ns<br>ns    | 3.0 V $\leq$ VDDISO, VDDP $\leq$ 3.6 V, $C_{L1} = C_{L2} = 0$ pF,<br>R1 = 1.0 k $\Omega$ , R2 = 120 $\Omega$ |  |
| Side 1 to Side 2<br>Rising Edge <sup>1</sup><br>Falling Edge <sup>2</sup>                                   | $t_{PLH12}$<br>$t_{PHL12}$ |     | 82<br>196 | 125<br>340 | ns<br>ns    |  |  |
| Side 2 to Side 1<br>Rising Edge <sup>3</sup><br>Falling Edge <sup>4</sup>                                   | $t_{PLH21}$<br>$t_{PHL21}$ |     | 32<br>110 | 75<br>210  | ns<br>ns    |  |  |
| PULSE WIDTH DISTORTION<br>5 V Operation   |                            |     |           |            |             |  | 4.5 V $\leq$ VDDISO, VDDP $\leq$ 5.5 V, $C_{L1} = C_{L2} = 0$ pF,<br>R1 = 1.6 k $\Omega$ , R2 = 180 $\Omega$ |
| Side 1 to Side 2, $ t_{PLH12} - t_{PHL12} $<br>Side 2 to Side 1, $ t_{PLH21} - t_{PHL21} $<br>3 V Operation | $PWD_{12}$<br>$PWD_{21}$   |     | 67<br>54  | 145<br>85  | ns<br>ns    |  | 3.0 V $\leq$ VDDISO, VDDP $\leq$ 3.6 V, $C_{L1} = C_{L2} = 0$ pF,<br>R1 = 1.0 k $\Omega$ , R2 = 120 $\Omega$ |
| Side 1 to Side 2, $ t_{PLH12} - t_{PHL12} $<br>Side 2 to Side 1, $ t_{PLH21} - t_{PHL21} $                  | $PWD_{12}$<br>$PWD_{21}$   |     | 114<br>77 | 215<br>135 | ns<br>ns    |  |  |
| COMMON-MODE TRANSIENT IMMUNITY <sup>5</sup>   | $ CM_H $ , $ CM_L $        | 25  | 35        |            | kV/ $\mu$ s |  |  |

<sup>1</sup>  $t_{PLH12}$  propagation delay is measured from the Side 1 input logic threshold to an output value of 0.7 VDDP.

<sup>2</sup>  $t_{PHL12}$  propagation delay is measured from the Side 1 input logic threshold to an output value of 0.4 V.

<sup>3</sup>  $t_{PLH21}$  propagation delay is measured from the Side 2 input logic threshold to an output value of 0.7 VDDISO.

<sup>4</sup>  $t_{PHL21}$  propagation delay is measured from the Side 2 input logic threshold to an output value of 0.9 V.

<sup>5</sup>  $|CM_H|$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_O > 0.8$  VDDP.  $|CM_L|$  is the maximum common-mode voltage slew rate that can be sustained while maintaining  $V_O < 0.8$  V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

## PACKAGE CHARACTERISTICS

Table 8. Thermal and Isolation Characteristics

| Parameter                                  | Symbol        | Min | Typ              | Max | Unit           | Test Conditions/Comments  |
|--|---------------|-----|------------------|-----|----------------|---|
| Resistance (Input to Output) <sup>1</sup>  | $R_{I-O}$     |     | 10 <sup>12</sup> |     | $\Omega$       |   |
| Capacitance (Input to Output) <sup>1</sup> | $C_{I-O}$     |     | 2.2              |     | pF             | f = 1 MHz   |
| Input Capacitance <sup>2</sup>             | $C_I$         |     | 4.0              |     | pF             |   |
| IC Junction-to-Ambient Thermal Resistance  | $\theta_{JA}$ |     | 50               |     | $^{\circ}$ C/W | Thermocouple located at center of package underside,<br>test conducted on 4-layer board with thin traces <sup>3</sup> |

<sup>1</sup> The device is considered a 2-terminal device: Pin 1 through Pin 10 are shorted together; and Pin 11 through Pin 20 are shorted together.

<sup>2</sup> Input capacitance is from any input data pin to ground.

<sup>3</sup> See the Thermal Analysis section for thermal model definitions.

**REGULATORY APPROVALS****Table 9.**

| UL <sup>1</sup>   | CSA   | VDE (Pending) <sup>2</sup>   |
|---|---|--|
| Recognized Under 1577 Component Recognition Program <sup>1</sup><br>Single Protection, 2500 V RMS Isolation Voltage<br>File E214100 | Approved under CSA Component Acceptance Notice 5A<br>Basic insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms (565 V peak) maximum working voltage<br>File 205078 | Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 <sup>2</sup><br>Reinforced insulation, 560 V peak<br>File 2471900-4880-0001 |

<sup>1</sup> In accordance with UL 1577, each ADM3260 is proof tested by applying an insulation test voltage  $\geq 3000$  V rms for 1 second (current leakage detection limit = 10  $\mu$ A).

<sup>2</sup> In accordance with DIN V VDE V 0884-10, ADM3260 is proof tested by applying an insulation test voltage  $\geq 1590$  V peak for 1 second (partial discharge detection limit = 5 pC). The \* marking branded on the component designates DIN V VDE V 0884-10 approval.

**INSULATION AND SAFETY RELATED SPECIFICATIONS****Table 10. Critical Safety Related Dimensions and Material Properties**

| Parameter   | Symbol | Value     | Unit  | Test Conditions/Comments  |
|---|--------|-----------|-------|---|
| Rated Dielectric Insulation Voltage   |        | 2500      | V rms | 1-minute duration   |
| Minimum External Air Gap (Clearance)  | L(I01) | 5.1       | mm    | Measured from input terminals to output terminals, shortest distance through air  |
| Minimum External Tracking (Creepage)  | L(I02) | 5.1       | mm    | Measured from input terminals to output terminals, shortest distance path along body  |
| Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance) | L(PCB) | 5.5       | mm    | Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane (for information only) |
| Minimum Internal Gap (Internal Clearance)                                   |        | 0.017 min | mm    | Distance through insulation   |
| Tracking Resistance (Comparative Tracking Index)                            | CTI    | >400      | V     | DIN IEC 112/VDE 0303, Part 1  |
| Isolation Group   |        | II        |       | Material group (DIN VDE 0110, 1/89, Table 1)  |

**DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS**

This isolator is suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by the protective circuits. The asterisk (\*) marking on packages denotes DIN V VDE V 0884-10 approval.

**Table 11. VDE Characteristics**

| Description   | Test Conditions/Comments  | Symbol             | Characteristic                 | Unit   |
|---|---|--------------------|--------------------------------|--------|
| Installation Classification per DIN VDE 0110<br>For Rated Mains Voltage ≤ 150 V rms<br>For Rated Mains Voltage ≤ 300 V rms<br>For Rated Mains Voltage ≤ 400 V rms |   |                    | I to IV<br>I to III<br>I to II |        |
| Climatic Classification   |   |                    | 40/105/21                      |        |
| Pollution Degree per DIN VDE 0110, Table 1  |   |                    | 2                              |        |
| Maximum Working Insulation Voltage  |   | V <sub>IORM</sub>  | 560                            | V peak |
| Input-to-Output Test Voltage, Method b1   | V <sub>IORM</sub> × 1.875 = V <sub>pd(m)</sub> , 100% production test,<br>t <sub>ini</sub> = t <sub>m</sub> = 1 sec, partial discharge < 5 pC | V <sub>pd(m)</sub> | 1050                           | V peak |
| Input-to-Output Test Voltage, Method a<br>After Environmental Tests Subgroup 1  | V <sub>IORM</sub> × 1.5 = V <sub>pd(m)</sub> , t <sub>ini</sub> = 60 sec, t <sub>m</sub> = 10 sec,<br>partial discharge < 5 pC                | V <sub>pd(m)</sub> | 840                            | V peak |
| After Input and/or Safety Test Subgroup 2<br>and Subgroup 3   | V <sub>IORM</sub> × 1.2 = V <sub>pd(m)</sub> , t <sub>ini</sub> = 60 sec, t <sub>m</sub> = 10 sec,<br>partial discharge < 5 pC                | V <sub>pd(m)</sub> | 672                            | V peak |
| Highest Allowable Overvoltage   |   | V <sub>IOTM</sub>  | 3535                           | V peak |
| Surge Isolation Voltage   |   | V <sub>IOSM</sub>  | 4000                           | V peak |
| Safety Limiting Values  | V <sub>IOSM(TEST)</sub> = 10 kV, 1.2 μs rise time, 50 μs, 50% fall time<br>Maximum value allowed in the event of a failure (see Figure 2)     |                    |                                |        |
| Case Temperature  |   | T <sub>S</sub>     | 150                            | °C     |
| Converter Safety Total Dissipated Power   |   | I <sub>S1</sub>    | 2.5                            | W      |
| VDDP + VDDISO Current   |   | I <sub>TMAX</sub>  | 212                            | mA     |
| Insulation Resistance at T <sub>S</sub> for Isolated Converter  | V <sub>IO</sub> = 500 V   | R <sub>S</sub>     | >10 <sup>9</sup>               | Ω      |

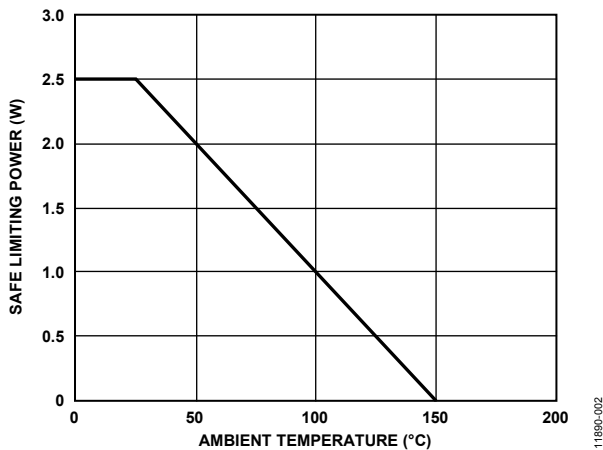


Figure 2. Isolated Converter Thermal Derating Curve, Dependence of Safety Limiting Values on Case Temperature, per DIN V VDE V 0884-10

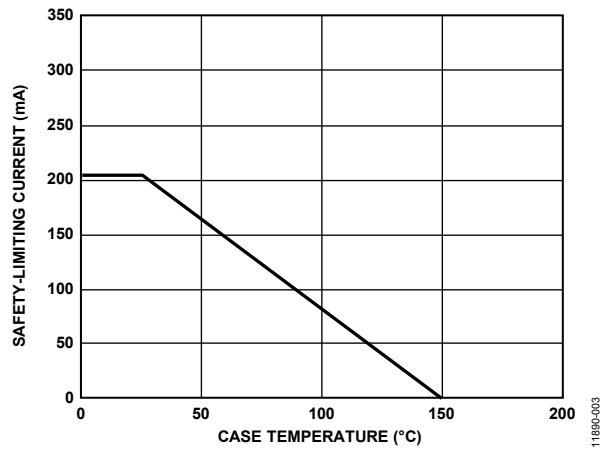


Figure 3. Digital Isolator Thermal Derating Curve, Dependence of Safety-Limiting Values on Case Temperature, per DIN V VDE V 0884-10



**RECOMMENDED OPERATING CONDITIONS**

Table 12.

| Parameter   | Value           |
|---|-----------------|
| OPERATING TEMPERATURE <sup>1</sup>  | -40°C to +105°C |
| ISOLATED CONVERTER  |                 |
| Supply Voltages <sup>2</sup>  |                 |
| VIN at VISO Set to Regulate to 3.3 V  | 3.0 V to 5.5 V  |
| VIN at VISO Set to Regulate to 5 V  | 4.5 V to 5.5 V  |
| DIGITAL ISOLATOR  |                 |
| Supply Voltages (VDDISO, VDDP) <sup>3</sup>                                       | 3.0 V to 5.5 V  |
| Input/Output Signal Voltage ( $V_{SDA1}$ , $V_{SCL1}$ , $V_{SDA2}$ , $V_{SCL2}$ ) | 5.5 V           |
| Capacitive Load   |                 |
| Side 1 ( $C_{L1}$ )   | 40 pF           |
| Side 2 ( $C_{L2}$ )   | 400 pF          |
| STATIC OUTPUT LOADING   |                 |
| Side 1 ( $I_{SDA1}$ , $I_{SCL1}$ )  | 0.5 mA to 3 mA  |
| Side 2 ( $I_{SDA2}$ , $I_{SCL2}$ )  | 0.5 mA to 30 mA |

<sup>1</sup> Operation at 105°C requires reduction of the maximum load current (see Table 13).

<sup>2</sup> Each voltage is relative to its respective ground.

<sup>3</sup> All voltages are relative to their respective ground.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 13.

| Parameter   | Rating   |
|---|--|
| Storage Temperature ( $T_{ST}$ )  | $-55^\circ\text{C}$ to $+150^\circ\text{C}$                  |
| Ambient Operating Temperature ( $T_A$ )   | $-40^\circ\text{C}$ to $+105^\circ\text{C}$                  |
| Supply Voltages ( $V_{IN}$ , $V_{ISO}$ ) <sup>1</sup>                                 | $-0.5\text{ V}$ to $+7.0\text{ V}$                           |
| Supply Voltages ( $V_{DDISO}$ , $V_{DDP}$ ) <sup>1</sup>                              | $-0.5\text{ V}$ to $+7.0\text{ V}$                           |
| VISO Supply Current <sup>2</sup><br>$T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$ | 30 mA  |
| Digital Isolator Average Output Current per Pin <sup>3</sup>                          |  |
| Side 1 ( $I_{O1}$ )   | $\pm 18\text{ mA}$   |
| Side 2 ( $I_{O2}$ )   | $\pm 100\text{ mA}$  |
| Input/Output Voltage  |  |
| Side 1 ( $V_{SDA1}$ , $V_{SCL1}$ ) <sup>3</sup>                                       | $-0.5\text{ V}$ to $V_{DDISO} + 0.5\text{ V}$                |
| Side 2 ( $V_{SDA2}$ , $V_{SCL2}$ ) <sup>3</sup>                                       | $-0.5\text{ V}$ to $V_{DDP} + 0.5\text{ V}$                  |
| Input Voltage ( $PDIS$ , $VSEL$ ) <sup>1, 4</sup>                                     | $-0.5\text{ V}$ to $V_{IN} + 0.5\text{ V}$                   |
| Common-Mode Transients <sup>5</sup>   | $-100\text{ kV}/\mu\text{s}$ to $+100\text{ kV}/\mu\text{s}$ |

<sup>1</sup> All voltages are relative to their respective ground.

<sup>2</sup> VISO provides current for dc and dynamic loads on the VISO input/output channels. This current must be included when determining the total VISO supply current.

<sup>3</sup> See Figure 3 for maximum rated current values for various temperatures.

<sup>4</sup>  $V_{CC}$  can be either  $V_{IN}$  or  $V_{ISO}$  depending on the whether the input is on the primary or secondary side of the device, respectively.

<sup>5</sup> Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 14. Maximum Continuous Working Voltage Supporting 50-Year Minimum Lifetime<sup>1</sup>

| Parameter         | Maximum | Unit   | Applicable Certification              |
|-------------------|---------|--------|---------------------------------------|
| AC Voltage        |         |        |                                       |
| Bipolar Waveform  | 560     | V peak | All certifications, 50-year operation |
| Unipolar Waveform | 560     | V peak |                                       |
| DC Voltage        |         |        |                                       |
| DC Peak Voltage   | 560     | V peak |                                       |

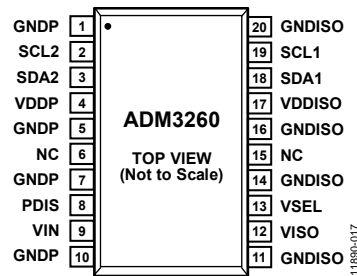
<sup>1</sup> Refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more information.

## VISO VOLTAGE TRUTH TABLE

Table 15. Truth Table (Positive Logic)

| VIN (V) | VSEL Input   | PDIS Input | VISO Output (V) | Notes                         |
|---------|--|------------|-----------------|-------------------------------|
| 5       | $R_{BOTTOM} = 10\text{ k}\Omega$ , $R_{TOP} = 30.9\text{ k}\Omega$ | Low        | 5               |                               |
| 5       | $R_{BOTTOM} = 10\text{ k}\Omega$ , $R_{TOP} = 30.9\text{ k}\Omega$ | High       | 0               |                               |
| 3.3     | $R_{BOTTOM} = 10\text{ k}\Omega$ , $R_{TOP} = 16.9\text{ k}\Omega$ | Low        | 3.3             |                               |
| 3.3     | $R_{BOTTOM} = 10\text{ k}\Omega$ , $R_{TOP} = 16.9\text{ k}\Omega$ | High       | 0               |                               |
| 5       | $R_{BOTTOM} = 10\text{ k}\Omega$ , $R_{TOP} = 16.9\text{ k}\Omega$ | Low        | 3.3             |                               |
| 5       | $R_{BOTTOM} = 10\text{ k}\Omega$ , $R_{TOP} = 16.9\text{ k}\Omega$ | High       | 0               |                               |
| 3.3     | $R_{BOTTOM} = 10\text{ k}\Omega$ , $R_{TOP} = 30.9\text{ k}\Omega$ | Low        | 5               | Configuration not recommended |
| 3.3     | $R_{BOTTOM} = 10\text{ k}\Omega$ , $R_{TOP} = 30.9\text{ k}\Omega$ | High       | 0               |                               |

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



## NOTES

1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN

Figure 4. Pin Configuration

Table 16. Pin Function Descriptions

| Pin No.        | Mnemonic | Description  |
|----------------|----------|--|
| 1, 5, 7, 10    | GNDP     | Ground Reference for Primary Side. Connect all GNDP pins to the primary ground reference.  |
| 2              | SCL2     | Clock Input/Output, Primary Side.  |
| 3              | SDA2     | Data Input/Output, Primary Side.   |
| 4              | VDDP     | Digital Isolator Primary Supply Input, 3.0 V to 5.5 V.   |
| 6, 15          | NC       | No Connect. Do not connect to this pin.  |
| 8              | PDIS     | Power Disable. When PDIS is tied to VIN, the power supply enters low power standby mode. When PDIS is tied to GNDP, the power converter is active.   |
| 9              | VIN      | <i>iso</i> Power Converter Primary Supply Input, 3.0 V to 5.5 V.   |
| 11, 14, 16, 20 | GNDISO   | Ground Reference for Isolated Side. Connect all GNDISO pins to the isolated ground reference.  |
| 12             | VISO     | Secondary Supply Voltage Output for Digital Isolator Isolated Side Power and External Loads. The output voltage is adjustable from 3.15 V to 5.25 V.   |
| 13             | VSEL     | Output Voltage Set. Provide a thermally matched resistor network between VISO and GNDISO to divide the required output voltage to match the 1.25 V reference voltage. The VISO voltage can be programmed up to 20% higher or 75% lower than VIN but must be within the allowed output voltage range. |
| 17             | VDDISO   | Digital Isolator Isolated Side Supply Input, 3.0 V to 5.5 V.   |
| 18             | SDA1     | Data Input/Output, Isolated Side.  |
| 19             | SCL1     | Clock Input/Output, Isolated Side.   |

TYPICAL PERFORMANCE CHARACTERISTICS

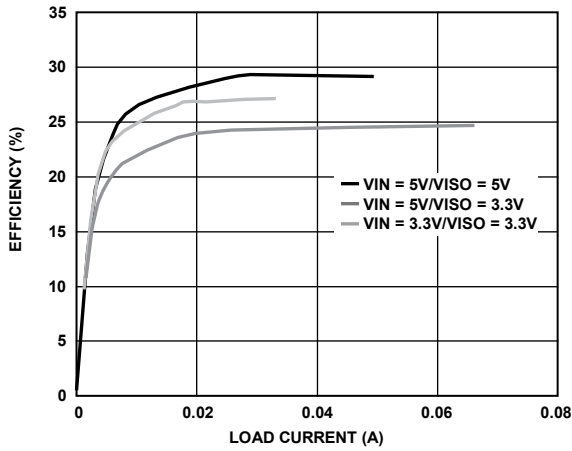


Figure 5. Typical Power Supply Efficiency at 5 V/5 V, 5 V/3.3 V, and 3.3 V/3.3 V

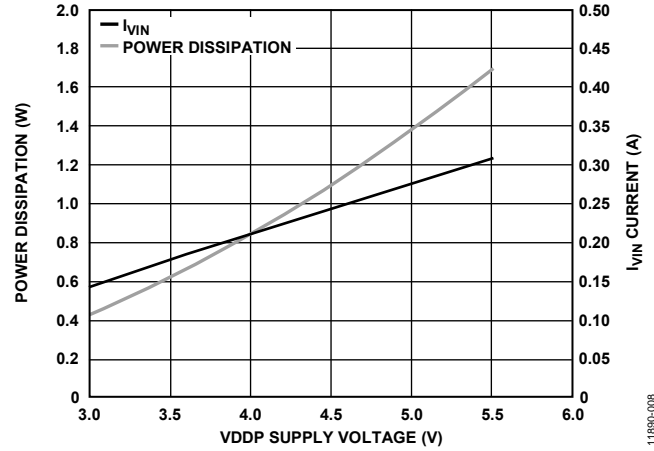


Figure 8. Power Dissipation and  $I_{VIN}$  Current vs. VDDP Supply Voltage

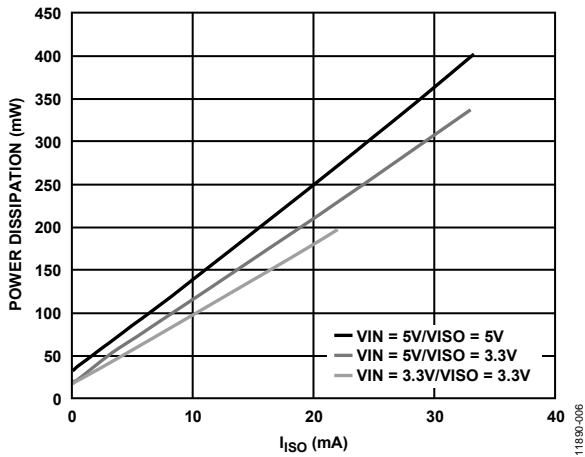


Figure 6. Typical Total Power Dissipation vs.  $I_{ISO}$

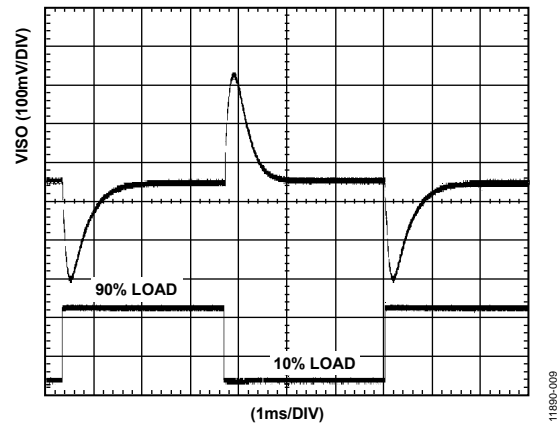


Figure 9. Typical VISO Transient Load Response, 5 V Output, 10% to 90% Load Step

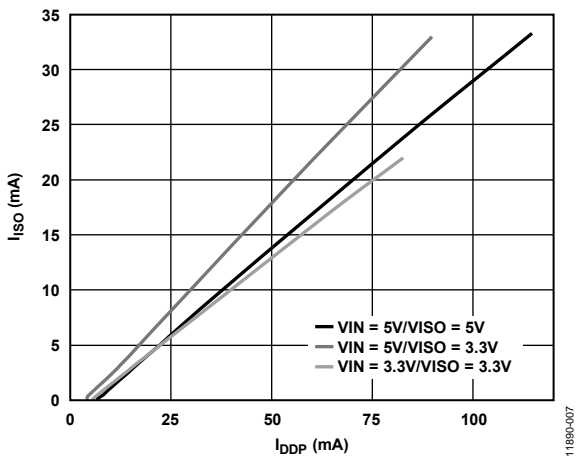


Figure 7. Typical Isolated Output Supply Current ( $I_{ISO}$ ) as a Function of External Load at 5 V/5 V, 5 V/3.3 V, and 3.3 V/3.3 V

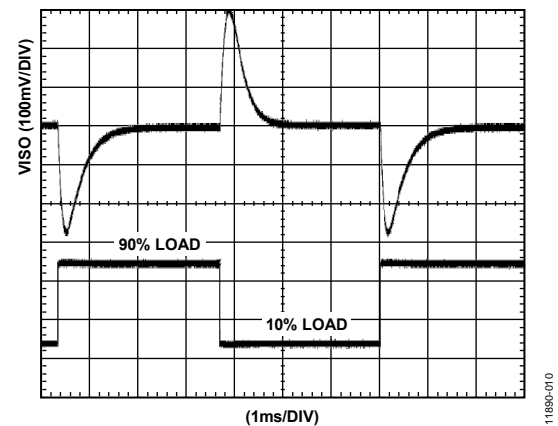


Figure 10. Typical VISO Transient Load Response, 3.3 V Input, 3.3 V Output, 10% to 90% Load Step

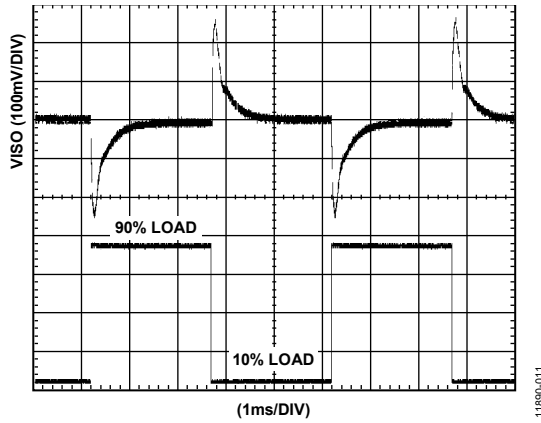


Figure 11. Typical VISO Transient Load Response, 5 V Input, 3.3 V Output, 10% to 90% Load Step

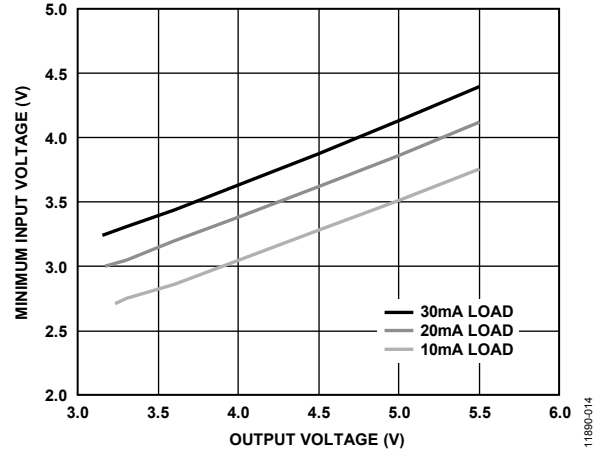


Figure 14. Relationship Between Output Voltage and Required Input Voltage, Under Load to Maintain >80% Duty Factor in the PWM

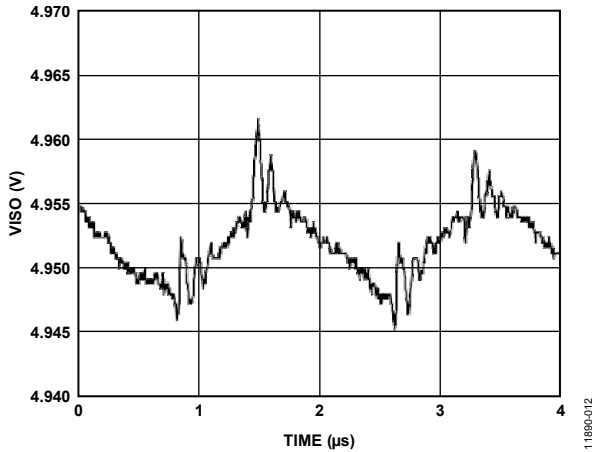


Figure 12. Typical VISO = 5 V Output Voltage Ripple at 90% Load

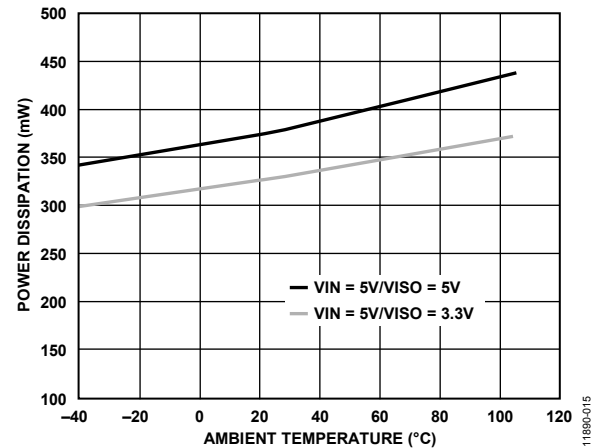


Figure 15. Power Dissipation with a 30 mA Load vs. Ambient Temperature

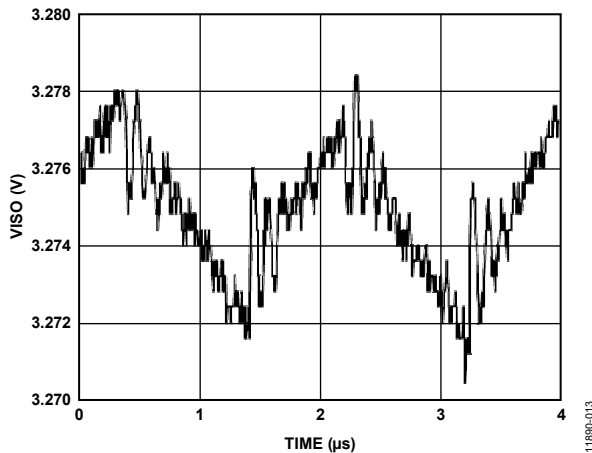


Figure 13. Typical VISO = 3.3 V Output Voltage Ripple at 90% Load

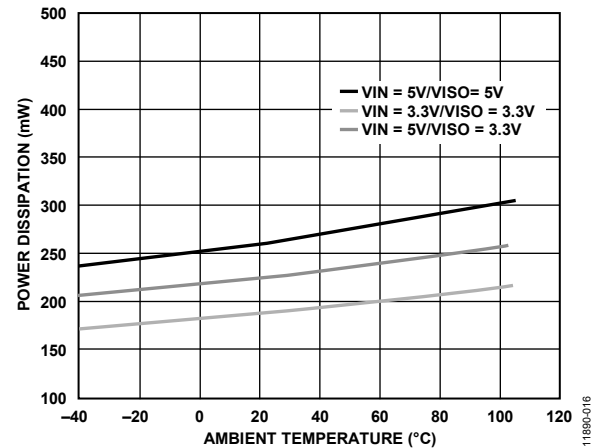


Figure 16. Power Dissipation with a 20 mA Load vs. Ambient Temperature

TEST CONDITION

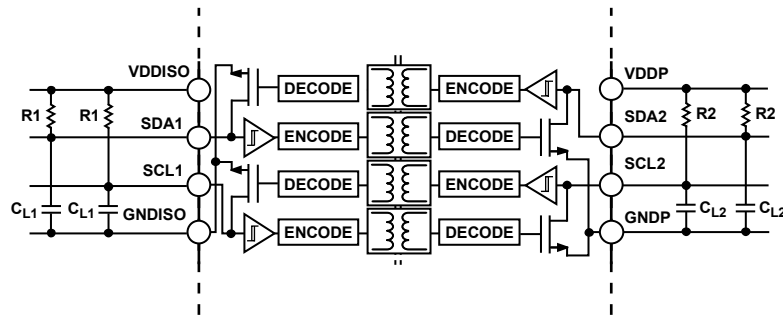


Figure 17. Timing Test Diagram

11890-004

## APPLICATIONS INFORMATION

### FUNCTIONAL DESCRIPTION

The digital isolator block on the [ADM3260](#) interfaces on each side to a bidirectional I<sup>2</sup>C signal. Internally, the I<sup>2</sup>C interface is split into two unidirectional channels communicating in opposing directions via a dedicated *i*Coupler isolation channel for each. One channel (the bottom channel of each channel pair shown in Figure 17) senses the voltage state of the Side 1 I<sup>2</sup>C pin (SCL1 or SDA1) and transmits its state to its respective Side 2 I<sup>2</sup>C pin (SCL2 or SDA2).

Both the Side 1 (isolated side) and the Side 2 (primary side) I<sup>2</sup>C pins interface to an I<sup>2</sup>C bus operating in the 3.0 V to 5.5 V range. A logic low on either pin causes the opposite pin to pull low enough to comply with the logic low threshold requirements of the other I<sup>2</sup>C devices on the bus. To avoid I<sup>2</sup>C bus contention, input a low threshold at SDA1 or SCL1 to guarantee at least 50 mV less than the output low signal at the same pin. This step prevents an output logic low at Side 1 from transmitting back to Side 2 and pulling down the I<sup>2</sup>C bus.

Because the Side 2 logic levels or thresholds are standard I<sup>2</sup>C values, multiple [ADM3260](#) devices connected to a bus by their Side 2 pins communicate with each other and with other I<sup>2</sup>C-compatible devices. I<sup>2</sup>C compatibility refers to situations in which the logic levels of a component do not necessarily meet the requirements of the I<sup>2</sup>C specification but still allow the component to communicate with an I<sup>2</sup>C-compliant device. I<sup>2</sup>C compliance refers to situations in which the logic levels of a component meet the requirements of the I<sup>2</sup>C specification.

However, because the Side 1 pin has a modified output level/ input threshold, this side of the [ADM3260](#) communicates only with devices that conform to the I<sup>2</sup>C standard. In other words, Side 2 of the [ADM3260](#) is I<sup>2</sup>C compliant, whereas Side 1 is only I<sup>2</sup>C compatible.

The output logic low levels are independent of the VDDISO and VDDP voltages. The input logic low threshold at Side 1 is also independent of VDDISO. However, the input logic low threshold at Side 2 is at 0.3 VDDP, consistent with I<sup>2</sup>C requirements. The Side 1 and Side 2 pins have open-collector outputs whose high levels are set via pull-up resistors to their respective supply voltages.

The dc-to-dc converter section of the [ADM3260](#) works on principles that are common to most modern power supplies. It has a split controller architecture with isolated pulse-width modulation (PWM) feedback. VIN power is supplied to an oscillating circuit that switches current into a chip-scale air core transformer. Power transferred to the secondary side is rectified and regulated to a value between 3.15 V and 5.25 V depending on the setpoint supplied by an external voltage divider (see Equation 1). The secondary (VISO) side controller regulates the output by creating a PWM control signal that is sent to the primary (VIN) side by a dedicated *i*Coupler data channel.

The PWM modulates the oscillator circuit to control the power being sent to the secondary side. Feedback allows for significantly higher power and efficiency.

$$VISO = 1.23 \times \frac{R_{TOP} + R_{BOTTOM}}{R_{BOTTOM}} (V) \quad (1)$$

where:

$R_{TOP}$  is a resistor between VSEL and VISO.

$R_{BOTTOM}$  is a resistor between VSEL and GNDISO.

Because the output voltage is adjusted continuously, there are an infinite number of operating conditions. This data sheet addresses three discrete operating conditions in the Specifications section. Many other combinations of input and output voltage are possible; Figure 14 depicts the supported voltage combinations at room temperature. Figure 14 was generated by using a fixed VISO load and decreasing the input voltage until the PWM was at 80% duty cycle. Each of the curves represents the minimum input voltage that is required for operation under this criterion. For example, if the application requires 30 mA of output current at 5 V, the minimum input voltage at VIN is 4.25 V. Figure 14 also illustrates that a configuration with VIN = 3.3 V and VISO = 5 V is not recommended. Even at 10 mA of output current, the PWM cannot maintain less than 80% duty factor, leaving no margin to support load or temperature variations.

Typically, the dc-to-dc converter section of the [ADM3260](#) dissipates about 17% more power between room temperature and maximum temperature; therefore, the 20% PWM margin covers temperature variations.

The isolated converter implements undervoltage lockout (UVLO) with hysteresis on the input/output pins of the primary and secondary sides as well as the VIN power input. This feature ensures that the converter does not go into oscillation due to noisy input power or slow power-on ramp rates.

**DIGITAL ISOLATOR STARTUP**

Both the VDDISO and VDDP supplies of the digital isolator block have an undervoltage lockout feature to prevent the signal channels from operating unless certain criteria are met. This feature prevents input logic low signals from pulling down the I<sup>2</sup>C bus inadvertently during power-up/power-down.

To enable the signal channels, the following two criteria must be met:

- Both supplies must be at least 2.5 V.
- At least 40 μs must elapse after both supplies exceed the internal start-up threshold of 2.0 V.

Until both criteria are met for both supplies, pull the outputs of the digital isolator block of the ADM3260 high, ensuring a startup that avoids any disturbances on the bus.

Figure 18 and Figure 19 illustrate the supply conditions for fast and slow input supply slew rates.

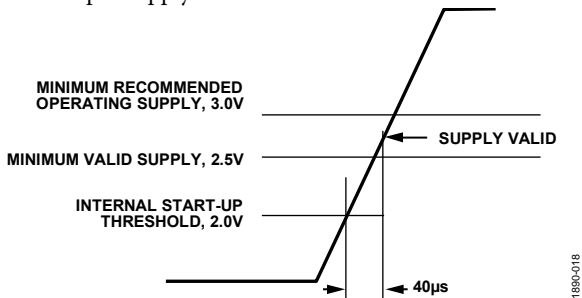


Figure 18. Digital Isolator Start-Up Condition, Supply Slew Rate > 12.5 V/ms

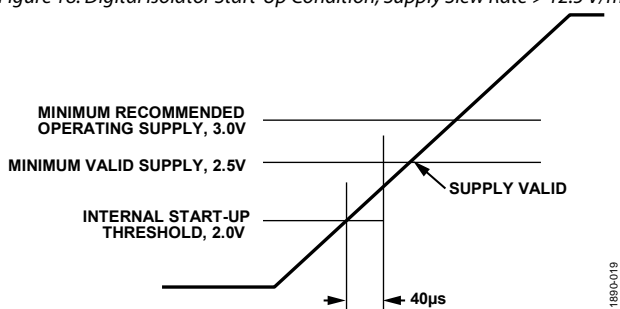


Figure 19. Digital Isolator Start-Up Condition, Supply Slew Rate < 12.5 V/ms

**TYPICAL APPLICATION DIAGRAM**

Figure 20 shows a typical application circuit including the pull-up resistors required for both Side 1 and Side 2 buses. Bypass capacitor with values from 0.01 μF to 0.1 μF are required between VDDP and GNDP and between VDDISO and GNDISO.

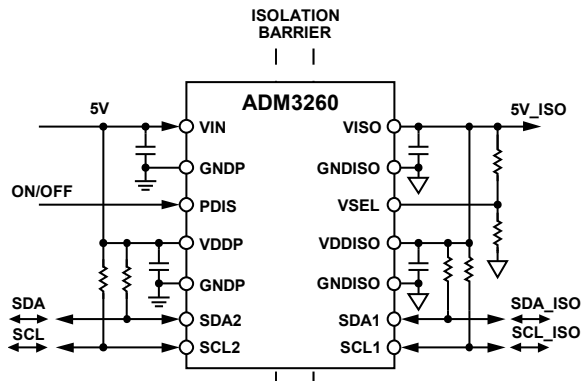


Figure 20. Typical Isolated I<sup>2</sup>C Interface Using the ADM3260

**PCB LAYOUT**

Supply bypassing of the 0.15 W isoPower integrated dc-to-dc converter with a low ESR capacitor is required as near the chip pads as possible. The isoPower inputs require several passive components to bypass the power effectively, as well as to set the output voltage and to bypass the core voltage regulator (see Figure 21 through Figure 23).

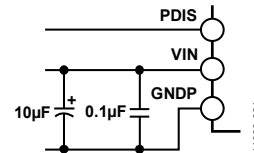


Figure 21. VIN Bias and Bypass Components

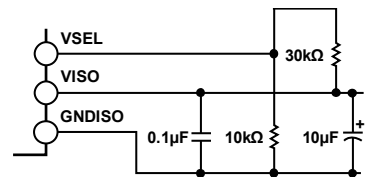


Figure 22. VISO Bias and Bypass Components

The power supply section of the ADM3260 uses a 125 MHz oscillator frequency to efficiently pass power through its chip-scale transformers. Choose bypass capacitors carefully because they must perform more than one function. Noise suppression requires a low inductance, high frequency capacitor; ripple suppression and proper regulation require a large value bulk capacitor. Connect these capacitors most conveniently between Pin VIN and Pin GNDP for VIN and between Pin VISO and Pin GNDISO for VISO. To suppress noise and reduce ripple, a parallel combination of at least two capacitors is required. The recommended capacitor values are 0.1 μF and 10 μF for VIN. The smaller capacitor must have a low ESR; for example, use of an NP0 or X5R ceramic capacitor is advised. Ceramic capacitors are also recommended for the 10 mF bulk capacitance. Add an additional 10 nF capacitor in parallel if further EMI/EMC control is desired.

Do not exceed 2 mm for the total lead length between the ends of the low ESR capacitor and the input power supply.

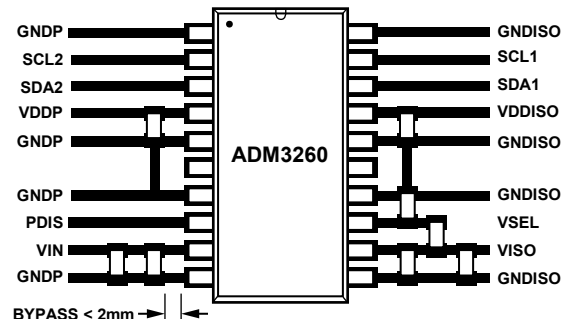


Figure 23. Recommended PCB Layout



In applications involving high common-mode transients, design the board layout such that any coupling that does occur affects all pins on a given component side equally. Failure to ensure this can cause voltage differentials between pins, exceeding the absolute maximum ratings specified in Table 13, and thereby leading to latch-up and/or permanent damage.

### THERMAL ANALYSIS

The ADM3260 consist of four internal die attached to a split lead frame with four die attach paddles. For the purposes of thermal analysis, treat the chip as a thermal unit, with the highest junction temperature reflected in the  $\theta_{JA}$  value from Table 8. The value of  $\theta_{JA}$  is based on measurements taken with the devices mounted on a JEDEC standard, 4-layer board with fine width traces and still air. Under normal operating conditions, the ADM3260 operates at a full load across the full temperature range without derating the output current.

Power dissipation in the device varies with ambient temperature due to the characteristics of the switching and rectification elements. Figure 15 and Figure 16 show the relationship between total power dissipation at two load conditions and ambient temperature. Use this information to determine the junction temperature at various operating conditions to ensure that the device does not go into thermal shutdown unexpectedly.

### EMI CONSIDERATIONS

The dc-to-dc converter section of the ADM3260 components must operate at a very high frequency to allow efficient power transfer through the small transformers. This high frequency operation creates high frequency currents that propagate in circuit board ground and power planes, causing edge and dipole radiation. Grounded enclosures are recommended for applications that use these devices. If grounded enclosures are not possible, follow good RF design practices in the layout of the PCB. See the AN-0971 Application Note for the most current PCB layout recommendations for the ADM3260.

### INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. Analog Devices conducts an extensive set of evaluations to determine the lifetime of the insulation structure within the ADM3260.

Accelerated life testing is performed using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined, allowing calculation of the time to failure at the working voltage of interest. The values shown in Table 14 summarize the peak voltages for 50 years of service life in several operating conditions. In many cases, the working voltage approved by agency testing is higher than the 50-year service life voltage. Operation at working voltages higher than the service life voltage listed leads to premature insulation failure.

The insulation lifetime of the ADM3260 depends on the voltage waveform type imposed across the isolation barrier. The iCoupler insulation structure degrades at different rates, depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 24, Figure 25, and Figure 26 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. A 50-year operating lifetime under the bipolar ac condition determines the Analog Devices recommended maximum working voltage. In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 14 can be applied while maintaining the 50-year minimum lifetime, provided that the voltage conforms to either the unipolar ac or dc voltage cases. Any cross-insulation voltage waveform that does not conform to Figure 25 or Figure 26 must be treated as a bipolar ac waveform, and its peak voltage must be limited to the 50-year lifetime voltage value listed in Table 14.

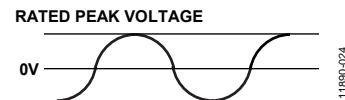


Figure 24. Bipolar AC Waveform

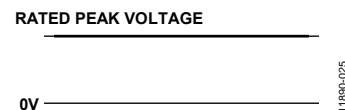
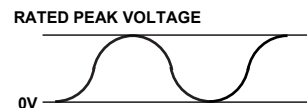


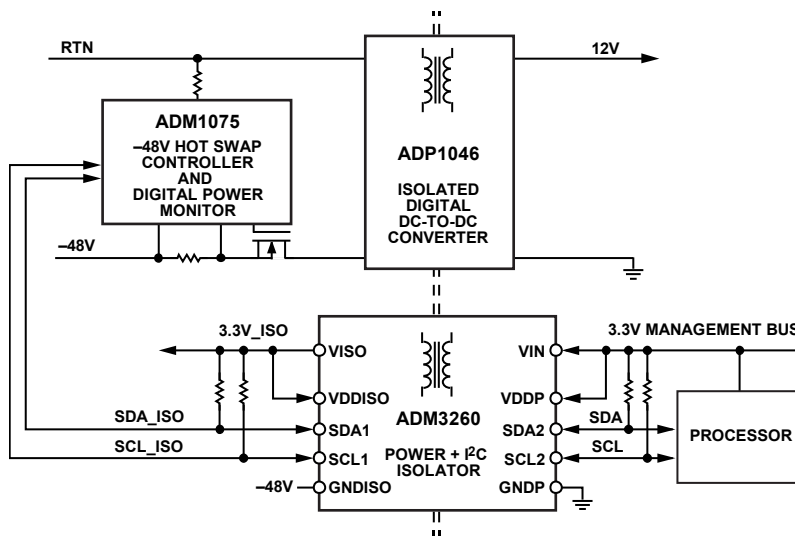
Figure 25. DC Waveform



NOTES  
1. THE VOLTAGE IS SHOWN AS SINO SOIDAL FOR ILLUSTRATION PUPOSES ONLY. IT IS MEANT TO REPRESENT ANY VOLTAGE WAVEFORM VARYING BETWEEN 0V AND SOME LIMITING VALUE. THE LIMITING VALUE CAN BE POSITIVE OR NEGATIVE, BUT THE VOLTAGE CANNOT CROSS 0V.

Figure 26. Unipolar AC Waveform

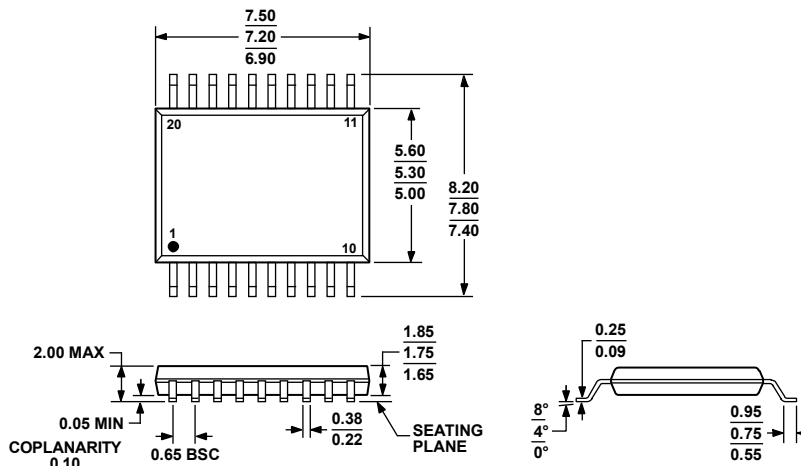
APPLICATIONS EXAMPLE



11880-027

Figure 27. The ADM3260 Used in -48 V Power Monitoring and Control

# OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-150-AE  
 Figure 28. 20-Lead Shrink Small Outline Package [SSOP] (RS-20)  
 Dimensions shown in millimeters

08010E-A

## ORDERING GUIDE

| Model <sup>1</sup> | Temperature Range | Package Description                         | Package Option |
|--------------------|-------------------|---|----------------|
| ADM3260ARSZ        | -40°C to +105°C   | 20-Lead Shrink Small Outline Package [SSOP] | RS-20          |
| ADM3260ARSZ-RL7    | -40°C to +105°C   | 20-Lead Shrink Small Outline Package [SSOP] | RS-20          |
| EVAL-ADM3260EBZ    |                   | Evaluation Board                            |                |

<sup>1</sup> Z = RoHS Compliant Part.

I<sup>2</sup>C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).