MT9M113PACSTCH-GEVB

MT9M113 Evaluation Board User's Manual

ON Semiconductor®

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EVAL BOARD USER'S MANUAL

Evaluation Board Overview

The evaluation boards are designed to demonstrate the features of ON Semiconductor's image sensors products. This headboard is intended to plug directly into the Demo 2X system. Test points and jumpers on the board provide access to clock, I/Os and other miscellaneous signals.

Features

- Clock Input
  - Default – 10 MHz crystal oscillator
  - Optional Demo 2X controlled MClk
- Two Wire Serial Interface
  - Selectable base address
- Parallel Interface
- MIPI Interface
- ROHS Compliant

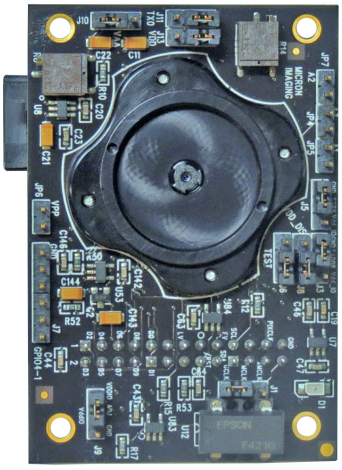

Figure 1. MT9M113 Evaluation Board

Block Diagram

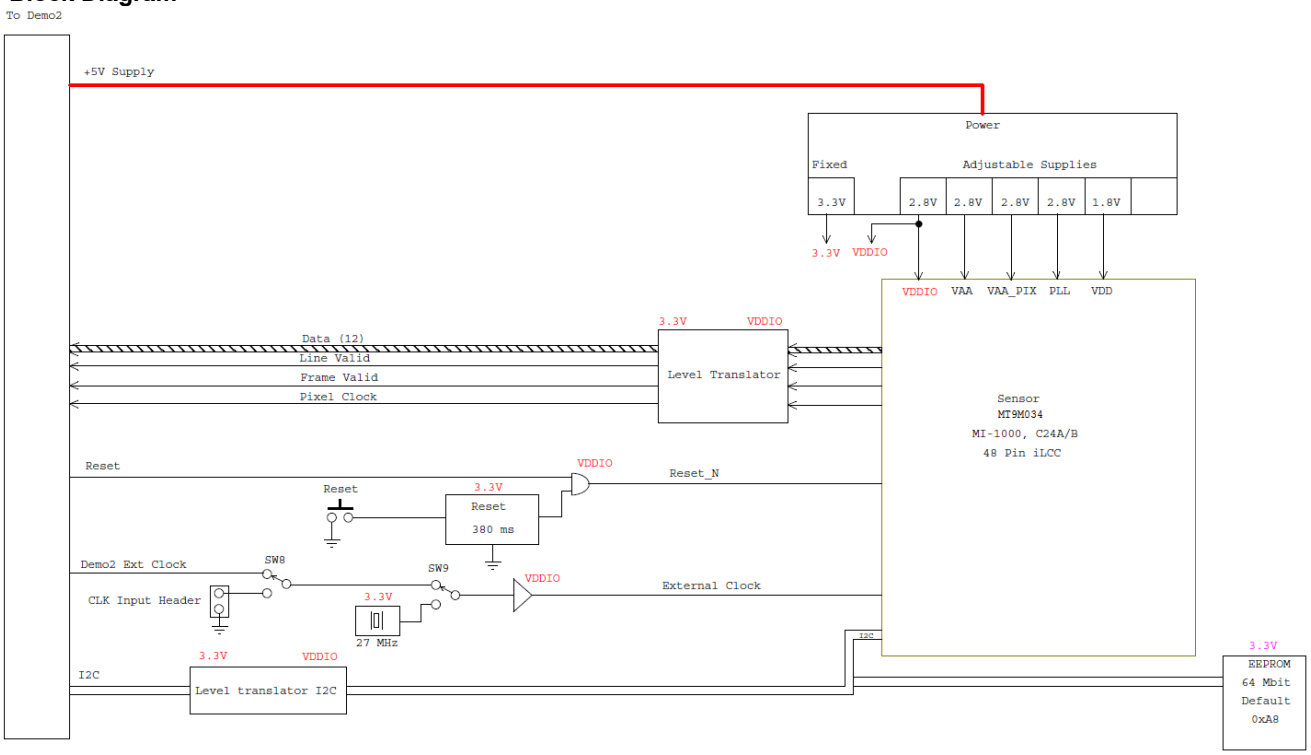

Figure 2. Block Diagram of MT9M113PACSTCH−GEVB

Top View

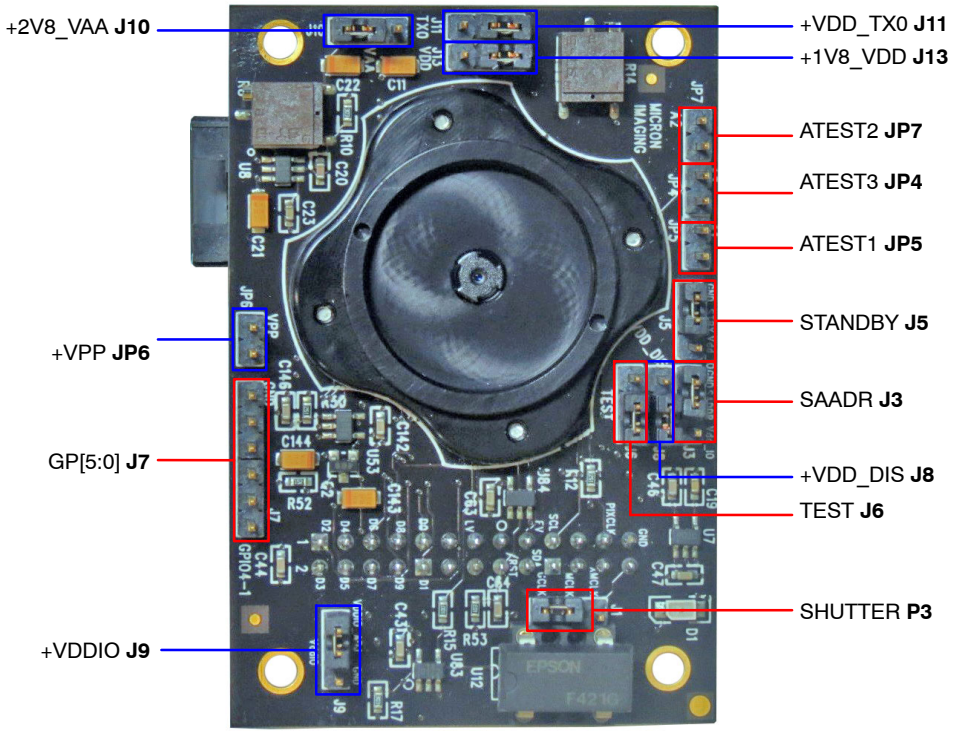

Figure 3. Top View of Evaluation Board − Default Jumpers

Bottom View

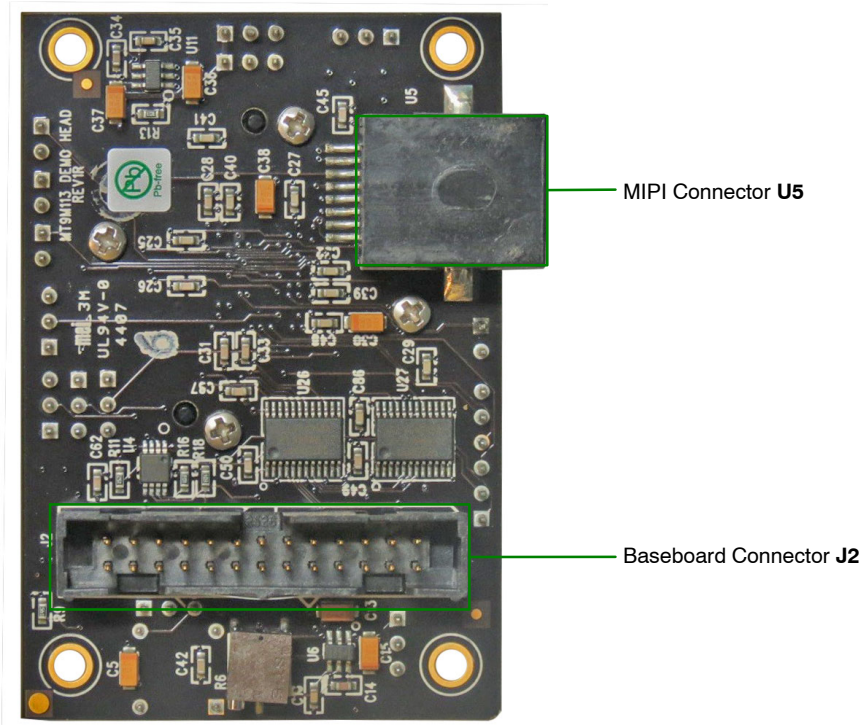

Figure 4. Bottom View of the Evaluation Board − Connector

Jumper Pin Locations

The jumpers on headboards start with Pin 1 on the leftmost side of the pin. Grouped jumpers increase in pin size with each jumper added.

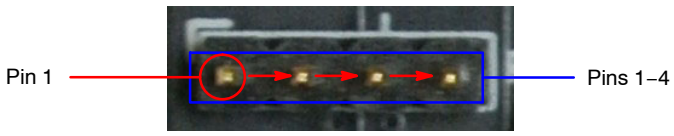

Figure 5. Pin Locations for a Single Jumper.
Pin 1 is Located at the Leftmost Side and Increases as it Moves to the Right

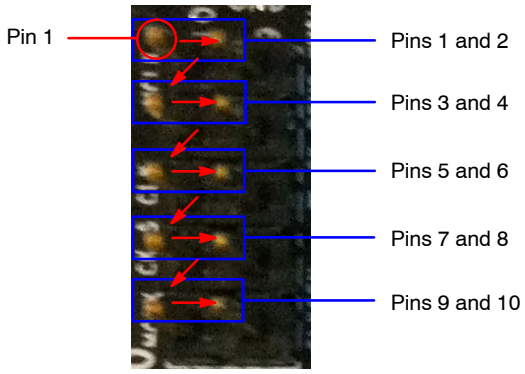

Figure 6. Pin Locations and Assignments of Grouped Jumpers.
Pin 1 is Located at the Top-Left Corner and Increases in a Zigzag Fashion Shown in the Picture

Jumper/Header Functions & Default Positions

Table 1. JUMPERS AND HEADERS

Jumper/Header No.	Jumper/Header Name	Pins	Description
J1	CLK_SELECT	2−3 (Default)	Connects to on-board oscillator
		1−2	Connects to XMCLK from Demo 2X Board
J3	SADDR	1−2 (Default)	I^2C Address set to 0x78
		2−3	I^2C Address set to 0x7A
J5	STANDBY	1−2 (Default)	Normal operation
		2−3	Sensor standby mode
J6	TEST	2−3 (Default)	Normal operation
		1−2	Test mode
J7	GP[5:0]	Open (Default)	For connection to various sensor's settings
J8	+VDD_DIS	2−3 (Default)	Normal operation
		1−2	Connects to on-board +VDDIO power supply
J9	+VDDIO	1−2 (Default)	Connects to on-board +VDDIO power supply
		2−3	External power supply connection
J10	+2V8_VAA	1−2 (Default)	Connects to on-board +2V8_VAA power supply
		2−3	External power supply connection
J11	+VDD_TX0	1−2 (Default)	Connects to on-board +VDD_TX0 power supply
		2−3	External power supply connection

Table 1. JUMPERS AND HEADERS (continued)

Jumper/Header No.	Jumper/Header Name	Pins	Description
J13	+1V8_VDD	1−2 (Default)	Connects to on-board +1V8_VDD power supply
		2−3	External power supply connection
JP4	ATEST3	Open (Default)	For Debug/Test
JP5	ATEST1	Open (Default)	For Debug/Test
JP6	+VPP	Open (Default)	For connection to external +VPP power supply for OTPM
JP7	ATEST2	Open (Default)	For Debug/Test

Interfacing to ON Semiconductor Demo 2X Baseboard

The ON Semiconductor Demo 2X baseboard has a similar 26-pin connector which mates with J2 of the headboard. The four mounting holes secure the baseboard and the headboard with spacers and screws.

PUBLICATION ORDERING INFORMATION

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