8-Channel Differential DAS with 18-Bit, Bipolar, Simultaneous Sampling ADC

Data Sheet **AD7609**

FEATURES

- 8 simultaneously sampled inputs
- True differential inputs
- True bipolar analog input ranges: ±20 V, ±10 V
- Single 5 V analog supply and 2.3 V to 5.25 V V_{DRIVE}
- Fully integrated data acquisition solution
  - Analog input clamp protection
  - Input buffer with 1 MΩ analog input impedance
  - Second-order antialiasing analog filter
  - On-chip accurate reference and reference buffer
  - 18-bit ADC with 200 kSPS on all channels
  - Oversampling capability with digital filter
- Flexible parallel/serial interface
- SPI/QSPI™/MICROWIRE™/DSP compatible
- Performance
  - 7 kV ESD rating on analog input channels
  - 98 dB SNR, −107 dB THD
  - Dynamic range: up to 105 dB typical
  - Low power: 100 mW
  - Standby mode: 25 mW
- 64-lead LQFP package

APPLICATIONS

- Power line monitoring and protection systems
- Multiphase motor control
- Instrumentation and control systems
- Multiaxis positioning systems
- Data acquisition systems (DAS)

COMPANION PRODUCTS

External References: ADR421, ADR431
Digital Isolators: ADuM1402, ADuM5000, ADuM5402
Power: ADIsimPower, Supervisor Parametric Search
Additional companion products on the AD7609 product page

Table 1. High Resolution, Bipolar Input, Simultaneous Sampling DAS Solutions

Resolution	Single-Ended Inputs	True Differential Inputs	Number of Simultaneous Sampling Channels
18 Bits	AD7608[1]	AD7609	8
16 Bits	AD7606B		8
	AD7606		8
	AD7606-6		6
	AD7606-4		4
14 Bits	AD7607		8

[1] Protected by U.S. Patent Number 8,072,360.

FUNCTIONAL BLOCK DIAGRAM

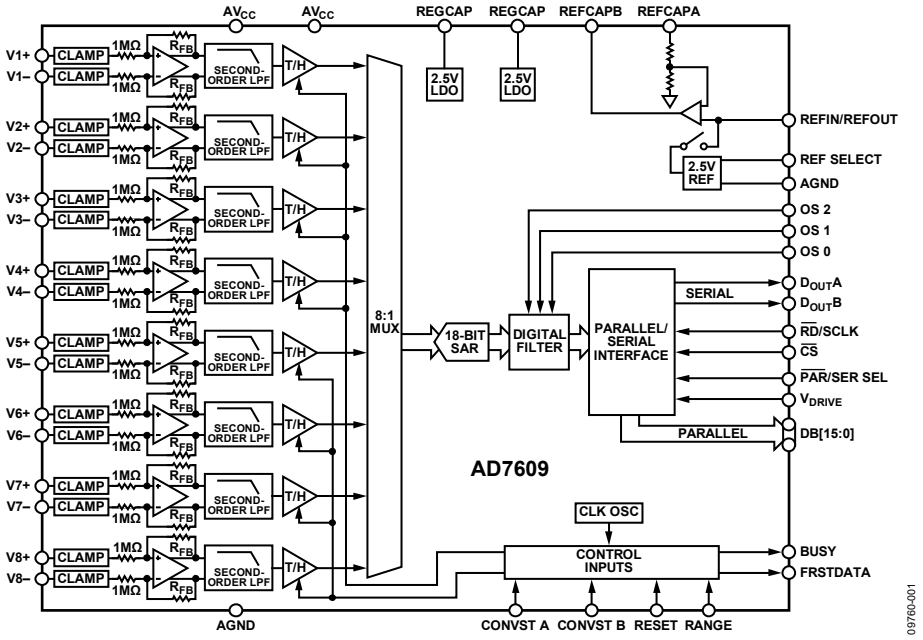

Figure 1.

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REVISION HISTORY

8/2019—Rev. C to Rev. D

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Changes to Figure 8 through Figure 13 ... 15
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7/2011—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD7609 is an 18-bit, 8-channel, true differential, simultaneous sampling analog-to-digital data acquisition system (DAS). The part contains analog input clamp protection, a second-order antialiasing filter, a track-and-hold amplifier, an 18-bit charge redistribution successive approximation analog-to-digital converter (ADC), a flexible digital filter, a 2.5 V reference and reference buffer, and high speed serial and parallel interfaces.

The AD7609 operates from a single 5 V supply and can accommodate ±20 V and ±10 V true bipolar differential input signals while sampling at throughput rates up to 200 kSPS for all channels. The input clamp protection circuitry can tolerate voltages up to ±16.5 V on each analog input pin. The AD7609 has 1 MΩ analog input impedance regardless of sampling frequency. The single supply operation, on-chip filtering, and high input impedance eliminate the need for driver op amps and external bipolar supplies. The AD7609 antialiasing filter has a −3 dB cutoff frequency of 32 kHz and provides 40 dB antialias rejection when sampling at 200 kSPS. The flexible digital filter is pin driven, yields improvements in SNR, and reduces the −3 dB bandwidth.

SPECIFICATIONS

V_{REF} = 2.5 V external/internal, AV_{CC} = 4.75 V to 5.25 V, V_{DRIVE} = 2.3 V to 5.25 V; f_{SAMPLE} = 200 kSPS, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.[1]

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE	f_{IN} = 1 kHz sine wave unless otherwise noted				
Signal-to-Noise Ratio (SNR)[2, 3]	Oversampling by 16; ±20 V range; f_{IN} = 160 Hz	98	101		dB
	Oversampling by 16; ±10 V range; f_{IN} = 160 Hz		100		dB
	No oversampling; ±20 V range	90	91		dB
	No oversampling; ±10 V range	89.5	90.5		dB
Signal-to-(Noise + Distortion) (SINAD)[2]	No oversampling; ±20 V range	89.5	91		dB
	No oversampling; ±10 V range	89	90		dB
Dynamic Range	No oversampling; ±20 V range		91.5		dB
	No oversampling; ±10 V range		90.5		dB
Total Harmonic Distortion (THD)[2, 3]	No oversampling; ±20 V range		−107	−97	dB
	No oversampling; ±10 V range		−110	−96	dB
Peak Harmonic or Spurious Noise (SFDR)[2]			−108		dB
Intermodulation Distortion (IMD)[2]	fa = 1 kHz, fb = 1.1 kHz				
Second-Order Terms			−110		dB
Third-Order Terms			−106		dB
Channel-to-Channel Isolation[2]	f_{IN} on unselected channels up to 160 kHz		−95		dB
ANALOG INPUT FILTER					
Full Power Bandwidth	−3 dB, ±20 V range		32		kHz
	−3 dB, ±10 V range		23		kHz
	−0.1 dB, ±20 V range		13		kHz
	−0.1 dB, ±10 V range		10		kHz
$t_{GROUP\ DELAY}$	±20 V range		7.1		µs
	±10 V range		10.2		µs
DC ACCURACY					
Resolution	No missing codes	18			Bits
Differential Nonlinearity[2]			±0.75	−0.99/+2	LSB[4]
Integral Nonlinearity[2]			±3	±7.5	LSB
Total Unadjusted Error (TUE)	±20 V range		±10		LSB
	±10 V range		±90		LSB
Positive Full-Scale Error[2, 5]	External reference		±8	±140	LSB
	Internal reference		±40		LSB
Positive Full-Scale Error Drift	External reference		±2		ppm/°C
	Internal reference		±7		ppm/°C
Positive Full-Scale Error Matching[2]	±20 V range		12	80	LSB
	±10 V range		40	100	LSB
Bipolar Zero Code Error[2, 6]	±20 V range		±3	±24	LSB
	± 10 V range		±3	±48	LSB
Bipolar Zero Code Error Drift	±20 V range		10		µV/°C
	± 10 V range		5		µV/°C
Bipolar Zero Code Error Matching[2]	±20 V range		2.7	30	LSB
	±10 V range		13	65	LSB
Negative Full-Scale Error[2, 5]	External reference		±8	±140	LSB
	Internal reference		±40		LSB
Negative Full-Scale Error Drift	External reference		±4		ppm/°C
	Internal reference		±8		ppm/°C
Negative Full-Scale Error Matching[2]	±20 V range		12	80	LSB
	±10 V range		40	100	LSB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG INPUT					
Differential Input Voltage Ranges	VIN = Vx+ − (Vx−)				
	RANGE = 1; ±20 V range	−20		+20	V
	RANGE = 0; ±10 V range	−10		+10	V
Absolute Voltage Input	±20 V range, see the Analog Input Clamp Protection section	−10		+10	V
	±10 V range, see the Analog Input Clamp Protection section	−5		+5	V
Common-Mode Input Range		−4	±5	+4	V
CMRR			−70		dB
Analog Input Current	±20 V range, see Figure 28		5.4		µA
	±10 V range, see Figure 28		2.5		µA
Input Capacitance[7]			5		pF
Input Impedance			1		MΩ
REFERENCE INPUT/OUTPUT					
Reference Input Voltage Range		2.475	2.5	2.525	V
DC Leakage Current				±1	µA
Input Capacitance[7]	REF SELECT = 1		7.5		pF
Reference Output Voltage	REFIN/REFOUT		2.49/ 2.505		V
Reference Temperature Coefficient			±10		ppm/°C
LOGIC INPUTS					
Input High Voltage (V_{INH})		$0.7 \times V_{DRIVE}$			V
Input Low Voltage (V_{INL})				$0.3 \times V_{DRIVE}$	V
Input Current (I_{IN})				±2	µA
Input Capacitance (C_{IN})[7]			5		pF
LOGIC OUTPUTS					
Output High Voltage (V_{OH})	I_{SOURCE} = 100 µA	$V_{DRIVE} - 0.2$			V
Output Low Voltage (V_{OL})	I_{SINK} = 100 µA			0.2	V
Floating-State Leakage Current			±1	±20	µA
Floating-State Output Capacitance[7]			5		pF
Output Coding	Twos complement				
CONVERSION RATE					
Conversion Time	All eight channels included		4		µs
Track-and-Hold Acquisition Time			1		µs
Throughput Rate	Per channel, all eight channels included			200	kSPS
POWER REQUIREMENTS					
AV_{CC}		4.75		5.25	V
V_{DRIVE}		2.3		5.25	V
I_{TOTAL}	Digital inputs = 0 V or V_{DRIVE}				
Normal Mode (Static)			16	22	mA
Normal Mode (Operational)[8]	f_{SAMPLE} = 200 kSPS		20	28.5	mA
Standby Mode			5	8	mA
Shutdown Mode			2	11	µA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Power Dissipation					
Normal Mode (Static)			80	115.5	mW
Normal Mode (Operational)[8]	f_{SAMPLE} = 200 kSPS		100	157	mW
Standby Mode			25	42	mW
Shutdown Mode			10	60.5	µW

[1] Temperature range for B version is −40°C to +85°C.
[2] See the Terminology section.
[3] This specification applies when reading during a conversion or after a conversion. If reading during a conversion in parallel and serial modes with V_{DRIVE} = 5 V, SNR typically reduces by 1.5 dB and THD by 3 dB.
[4] LSB means least significant bit. With ±10 V input range, 1 LSB = 76.29 µV. With ±20 V input range, 1 LSB = 152.58 µV.
[5] These specifications include the full temperature range variation and contribution from the internal reference buffer but do not include the error contribution from the external reference.
[6] Bipolar zero code error is calculated with respect to the analog input voltage. See the Analog Input Clamp Protection section.
[7] Sample tested during initial release to ensure compliance.
[8] Operational power/current figure includes contribution when running in oversampling mode.

TIMING SPECIFICATIONS

AV_{CC} = 4.75 V to 5.25 V, V_{DRIVE} = 2.3 V to 5.25 V, V_{REF} = 2.5 V external reference/ internal reference, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.[1]

Table 3.

Parameter	Limit at T_{MIN}, T_{MAX} Min	Typ	Max	Unit	Description
PARALLEL/SERIAL/BYTE MODE					
t_{CYCLE}					1/throughput rate
			5	µs	Parallel mode, reading during; or after conversion V_{DRIVE} = 2.7 V to 5.25 V; or serial mode: V_{DRIVE} = 3.3 V to 5.25 V, reading during a conversion using $D_{OUT}A$ and $D_{OUT}B$ lines
		5		µs	Parallel mode reading after conversion V_{DRIVE} = 2.3 V
			10.1	µs	Serial mode reading after conversion; V_{DRIVE} = 2.7 V, $D_{OUT}A$ and $D_{OUT}B$ lines
			11.5	µs	Serial mode reading after a conversion; V_{DRIVE} = 2.3 V, $D_{OUT}A$ and $D_{OUT}B$ lines
t_{CONV}					Conversion time
	3.45	4	4.2	µs	Oversampling off
	7.87		9.1	µs	Oversampling by 2
	16.05		18.8	µs	Oversampling by 4
	33		39	µs	Oversampling by 8
	66		78	µs	Oversampling by 16
	133		158	µs	Oversampling by 32
	257		315	µs	Oversampling by 64
$t_{WAKE\text{-}UP\ STANDBY}$			100	µs	$\overline{STBY}$ rising edge to CONVST x rising edge; power-up time from standby mode
$t_{WAKE\text{-}UP\ SHUTDOWN}$					
Internal Reference			30	ms	$\overline{STBY}$ rising edge to CONVST x rising edge; power-up time from shutdown mode
External Reference			13	ms	$\overline{STBY}$ rising edge to CONVST x rising edge; power-up time from shutdown mode
t_{RESET}	50			ns	RESET high pulse width
t_{OS_SETUP}	20			ns	BUSY to OS x pin setup time
t_{OS_HOLD}	20			ns	BUSY to OS x pin hold time
t_1			45	ns	CONVST x high to BUSY high
t_2	25			ns	Minimum CONVST x low pulse
t_3	25			ns	Minimum CONVST x high pulse
t_4	0			ns	BUSY falling edge to $\overline{CS}$ falling edge setup time
t_5[2]			0.5	ms	Maximum delay allowed between CONVST A, CONVST B rising edges
t_6			25	ns	Maximum time between last $\overline{CS}$ rising edge and BUSY falling edge
t_7	25			ns	Minimum delay between RESET low to CONVST x high
PARALLEL READ OPERATION					
t_8	0			ns	$\overline{CS}$ to $\overline{RD}$ setup time
t_9	0			ns	$\overline{CS}$ to $\overline{RD}$ hold time
t_{10}					$\overline{RD}$ low pulse width
	19			ns	V_{DRIVE} above 4.75 V
	24			ns	V_{DRIVE} above 3.3 V
	30			ns	V_{DRIVE} above 2.7 V
	37			ns	V_{DRIVE} above 2.3 V
t_{11}	15			ns	$\overline{RD}$ high pulse width
t_{12}	22			ns	$\overline{CS}$ high pulse width (see Figure 5); $\overline{CS}$ and $\overline{RD}$ linked

Parameter	Limit at T_{MIN}, T_{MAX} Min	Typ	Max	Unit	Description
t_{13}					Delay from $\overline{CS}$ until DB[15:0] three-state disabled
			19	ns	V_{DRIVE} above 4.75 V
			24	ns	V_{DRIVE} above 3.3 V
			30	ns	V_{DRIVE} above 2.7 V
			37	ns	V_{DRIVE} above 2.3 V
t_{14}[3]					Data access time after $\overline{RD}$ falling edge
			19	ns	V_{DRIVE} above 4.75 V
			24	ns	V_{DRIVE} above 3.3 V
			30	ns	V_{DRIVE} above 2.7 V
			37	ns	V_{DRIVE} above 2.3 V
t_{15}	6			ns	Data hold time after $\overline{RD}$ falling edge
t_{16}	6			ns	$\overline{CS}$ to DB[15:0] hold time
t_{17}			22	ns	Delay from $\overline{CS}$ rising edge to DB[15:0] three-state enabled
SERIAL READ OPERATION					
f_{SCLK}					Frequency of serial read clock
			20	MHz	V_{DRIVE} above 4.75 V
			15	MHz	V_{DRIVE} above 3.3 V
			12.5	MHz	V_{DRIVE} above 2.7 V
			10	MHz	V_{DRIVE} above 2.3 V
t_{18}					Delay from $\overline{CS}$ until $D_{OUT}A/D_{OUT}B$ three-state disabled/delay from $\overline{CS}$ until MSB valid
			18	ns	V_{DRIVE} above 4.75 V
			23	ns	V_{DRIVE} above 3.3 V
			35	ns	V_{DRIVE} = 2.3 V to 2.7 V
t_{19}[3]					Data access time after SCLK rising edge
			20	ns	V_{DRIVE} above 4.75 V
			26	ns	V_{DRIVE} above 3.3 V
			32	ns	V_{DRIVE} above 2.7 V
			39	ns	V_{DRIVE} above 2.3 V
t_{20}	0.4 t_{SCLK}			ns	SCLK low pulse width
t_{21}	0.4 t_{SCLK}			ns	SCLK high pulse width
t_{22}	7				SCLK rising edge to $D_{OUT}A/D_{OUT}B$ valid hold time
t_{23}			22	ns	$\overline{CS}$ rising edge to $D_{OUT}A/D_{OUT}B$ three-state enabled
FRSTDATA OPERATION					
t_{24}					Delay from $\overline{CS}$ falling edge until FRSTDATA three-state disabled
			18	ns	V_{DRIVE} above 4.75 V
			23	ns	V_{DRIVE} above 3.3 V
			30	ns	V_{DRIVE} above 2.7 V
			35	ns	V_{DRIVE} above 2.3 V
t_{25}				ns	Delay from $\overline{CS}$ falling edge until FRSTDATA high, serial mode
			18	ns	V_{DRIVE} above 4.75 V
			23	ns	V_{DRIVE} above 3.3 V
			30	ns	V_{DRIVE} above 2.7 V
			35	ns	V_{DRIVE} above 2.3 V
t_{26}					Delay from $\overline{RD}$ falling edge to FRSTDATA high
			19	ns	V_{DRIVE} above 4.75 V
			23	ns	V_{DRIVE} above 3.3 V
			30	ns	V_{DRIVE} above 2.7 V
			35	ns	V_{DRIVE} above 2.3 V

Parameter	Limit at T_{MIN}, T_{MAX} Min	Typ	Max	Unit	Description
t_{27}					Delay from $\overline{RD}$ falling edge to FRSTDATA low
			22	ns	V_{DRIVE} = 3.3 V to 5.25 V
			29	ns	V_{DRIVE} = 2.3 V to 2.7 V
t_{28}					Delay from 18th SCLK falling edge to FRSTDATA low
			20	ns	V_{DRIVE} = 3.3 V to 5.25 V
			27	ns	V_{DRIVE} = 2.3 V to 2.7 V
t_{29}			29	ns	Delay from $\overline{CS}$ rising edge until FRSTDATA three-state enabled

[1] Sample tested during initial release to ensure compliance. All input signals are specified with $t_R = t_F$ = 5 ns (30% to 70% of V_{DD}) and timed from a voltage level of 1.6 V.
[2] The delay between the CONVST x signals was measured as the maximum time allowed while ensuring a <40 LSB performance matching between channel sets.
[3] A buffer is used on the data output pins for these measurements, which is equivalent to a load of 20 pF on the output pins.

Timing Diagrams

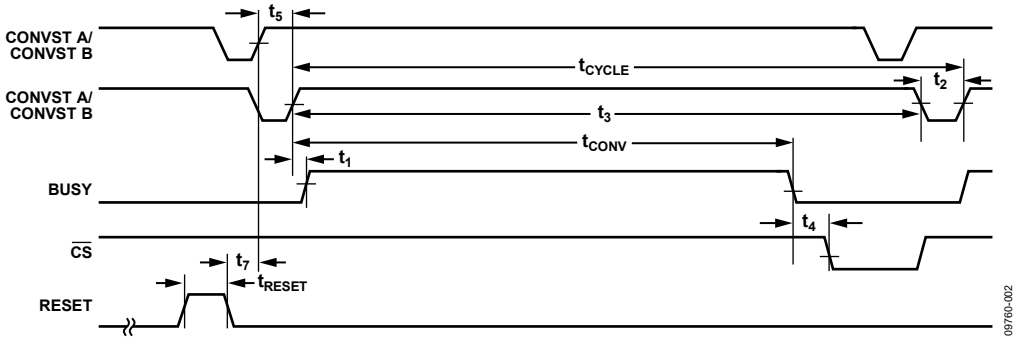


Figure 2. CONVST x Timing—Reading After a Conversion

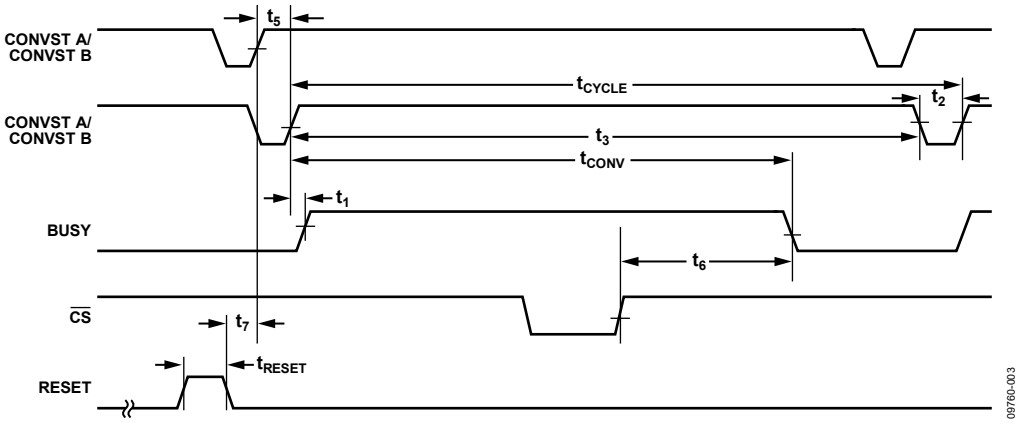


Figure 3. CONVST x Timing—Reading During a Conversion

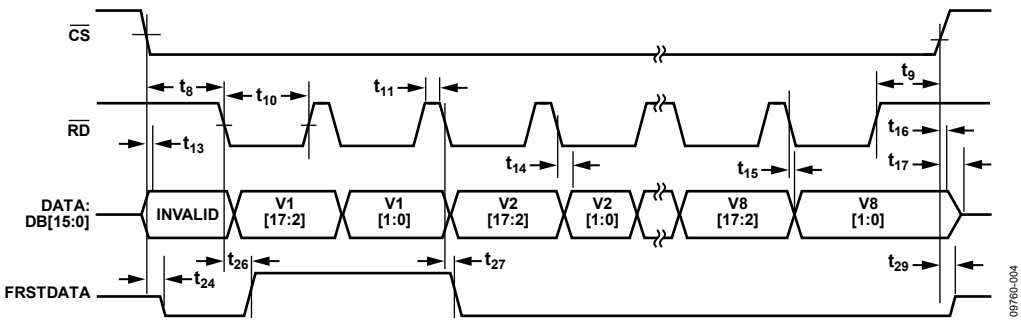


Figure 4. Parallel Mode Separate $\overline{CS}$ and $\overline{RD}$ Pulses

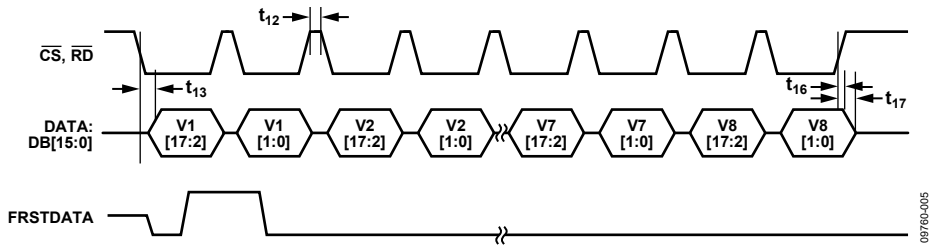


Figure 5. $\overline{CS}$ and $\overline{RD}$ Linked Parallel Mode

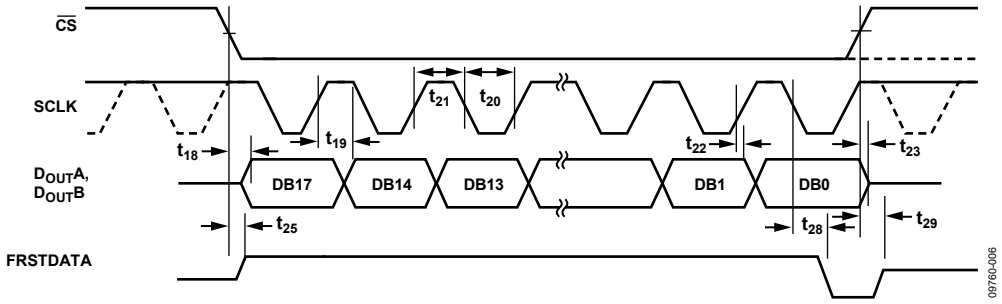


Figure 6. Serial Read Operation

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
AV_{CC} to AGND	−0.3 V to +7 V
V_{DRIVE} to AGND	−0.3 V to AV_{CC} + 0.3 V
Analog Input Voltage to AGND[1]	±16.5 V
Digital Input Voltage to AGND	−0.3 V to V_{DRIVE} + 0.3 V
Digital Output Voltage to AGND	−0.3 V to V_{DRIVE} + 0.3 V
REFIN to AGND	−0.3 V to AV_{CC} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	
B Version	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Pb/SN Temperature, Soldering	
Reflow (10 sec to 30 sec)	240(+0)°C
Pb-Free Temperature, Soldering Reflow	260(+0)°C
ESD (All Pins Except Analog Inputs)	2 kV
ESD (Analog Input Pins Only)	7 kV

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. These specifications apply to a 4-layer board.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
64-Lead LQFP	45	11	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

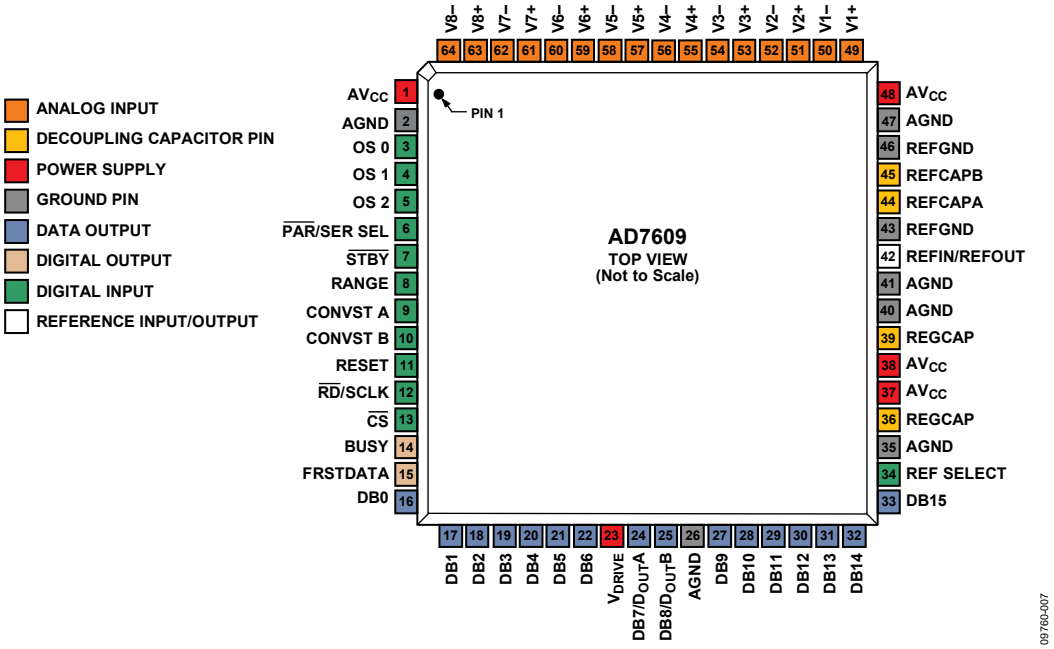


Figure 7. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Type[1]	Mnemonic	Description
1, 37, 38, 48	P	AV_{CC}	Analog Supply Voltage 4.75 V to 5.25 V. This supply voltage is applied to the internal front-end amplifiers and to the ADC core. These supply pins should be decoupled to AGND.
2, 26, 35, 40, 41, 47	P	AGND	Analog Ground. This pin is the ground reference point for all analog circuitry on the AD7609. All analog input signals and external reference signals should be referred to these pins. All six of these AGND pins should connect to the AGND plane of a system.
23	P	V_{DRIVE}	Logic Power Supply Input. The voltage (2.3 V to 5 V) supplied at this pin determines the operating voltage of the interface. This pin is nominally at the same supply as the supply of the host interface (that is, DSP, FPGA).
36, 39	P	REGCAP	Decoupling Capacitor Pins for Voltage Output from Internal Regulator. These output pins should be decoupled separately to AGND using a 1 µF capacitor. The voltage on these output pins is in the range of 2.5 V to 2.7 V.
49, 51, 53, 55, 57, 59, 61, 63	AI+	V1+ to V8+	Analog Input V1+ to Analog Input V8+. These pins are the positive terminal of the true differential analog inputs. The analog input range of these channels is determined by the RANGE pin.
50, 52, 54, 56, 58, 60, 62, 64	AI−	V1− to V8−	Analog Input V1− to Analog Input V8−. These are the negative terminals of the true differential analog inputs. The analog input range of these channels is determined by the RANGE pin. The signal on this pin should be 180° out of phase with the corresponding Vx+ pin.
42	REF	REFIN/ REFOUT	Reference Input/ Reference Output. The on-chip reference of 2.5 V is available on this pin for external use if the REF SELECT pin is set to a logic high. Alternatively, the internal reference can be disabled by setting the REF SELECT pin to a logic low and an external reference of 2.5 V can be applied to this input. See the Internal/External Reference section. Decoupling is required on this pin for both the internal or external reference options. A 10 µF capacitor should be applied from this pin to ground close to the REFGND pins.
34	DI	REF SELECT	Internal/External Reference Selection Input. Logic input. If this pin is set to logic high, the internal reference is selected and is enabled. If this pin is set to logic low, the internal reference is disabled and an external reference voltage must be applied to the REFIN/REFOUT pin.
44, 45	REF	REFCAPA, REFCAPB	Reference Buffer Output Force/Sense Pins. These pins must be connected together and decoupled to AGND using a low ESR 10 µF ceramic capacitor.
43, 46	REF	REFGND	Reference Ground Pins. These pins should be connected to AGND.

Pin No.	Type[1]	Mnemonic	Description
8	DI	RANGE	Analog Input Range Selection. Logic input. The polarity on this pin determines the input range of the analog input channels. If this pin is tied to a logic high, the analog input range is ±20 V for all channels. If this pin is tied to a logic low, the analog input range is ±10 V for all channels. A logic change on this pin has an immediate effect on the analog input range. Changing this pin during a conversion is not recommended. See the Analog Input section for more details.
6	DI	$\overline{\text{PAR}}$/ SER SEL	Parallel/Serial Interface Selection Input. Logic input. If this pin is tied to a logic low, the parallel interface is selected. If this pin is tied to a logic high, the serial interface is selected. In serial mode, the $\overline{\text{RD}}$/SCLK pin functions as the serial clock input. The DB7/D_{OUT}A and DB8/D_{OUT}B pins function as serial data outputs. When the serial interface is selected, the DB[15:9] and DB[6:0] pins should be tied to AGND.
9, 10	DI	CONVST A, CONVST B	Conversion Start Input A, Conversion Start Input B. Logic inputs. These logic inputs are used to initiate conversions on the analog input channels. For simultaneous sampling of all input channels, CONVST A and CONVST B can be shorted together and a single conversion start signal applied. Alternatively, CONVST A can be used to initiate simultaneous sampling for V1, V2, V3, and V4, and CONVST B can be used to initiate simultaneous sampling on the other analog inputs (V5, V6, V7, and V8). This is only possible when oversampling is not switched on. When the CONVST A or CONVST B pin transitions from low to high, the front-end track-and-hold circuitry for their respective analog inputs is set to hold. This function allows a phase delay to be created inherently between the sets of analog inputs.
13	DI	$\overline{\text{CS}}$	Chip Select. This active low logic input frames the data transfer. When both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are logic low in parallel mode, the output bus (DB[15:0]) is enabled and the conversion result is output on the parallel data bus lines. In serial mode, the $\overline{\text{CS}}$ is used to frame the serial read transfer and clocks out the MSB of the serial output data.
12	DI	$\overline{\text{RD}}$/SCLK	Parallel Data Read Control Input When Parallel Interface is Selected ($\overline{\text{RD}}$)/Serial Clock Input When Serial Interface is Selected (SCLK). When both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are logic low in parallel mode, the output bus is enabled. In parallel mode, two $\overline{\text{RD}}$ pulses are required to read the full 18 bits of conversion results from each channel. The first $\overline{\text{RD}}$ pulse outputs DB[17:2], and the second $\overline{\text{RD}}$ pulses outputs DB[1:0]. In serial mode, this pin acts as the serial clock input for data transfers. The $\overline{\text{CS}}$ falling edge takes the data output lines, D_{OUT}A and D_{OUT}B, out of three-state and clocks out the MSB of the conversion result. The rising edge of SCLK clocks all subsequent data bits onto the serial data outputs, D_{OUT}A and D_{OUT}B. For further information, see the Conversion Control section.
14	DO	BUSY	Busy Output. This pin transitions to a logic high after both CONVST A and CONVST B rising edges and indicates that the conversion process has started. The BUSY output remains high until the conversion process for all channels is complete. The falling edge of BUSY signals that the conversion data is being latched into the output data registers and will be available to be read after a time, t_4. Any data read while BUSY is high should be complete before the falling edge of BUSY occurs. Rising edges on CONVST A or CONVST B have no effect while the BUSY signal is high.
11	DI	RESET	Reset Input. When set to logic high, the rising edge of RESET resets the AD7609. The part must receive a RESET pulse after power-up. To achieve the specified performance after the RESET signal, the $t_{WAKE\_UP\ SHUTDOWN}$ time should elapse between power-on and the RESET pulse. The RESET high pulse should be typically 100 ns wide. If a RESET pulse is applied during a conversion, the conversion is aborted. If a RESET pulse is applied during a read, the contents of the output registers reset to all zeros.
15	DO	FRSTDATA	Digital Output. The FRSTDATA output signal indicates when the first channel, V1, is being read back on either the parallel or serial interface. When the $\overline{\text{CS}}$ input is high, the FRSTDATA output pin is in three-state. The falling edge of $\overline{\text{CS}}$ takes FRSTDATA out of three-state. In parallel mode, the falling edge of $\overline{\text{RD}}$ corresponding to the result of V1 then sets the FRSTDATA pin high, indicating that the result from V1 is available on the output data bus. The FRSTDATA output returns to a logic low following the third falling edge of $\overline{\text{RD}}$. In serial mode, FRSTDATA goes high on the falling edge of $\overline{\text{CS}}$ as this clocks out the MSB of V1 on DOUTA. It returns low on the 18th SCLK falling edge after the $\overline{\text{CS}}$ falling edge. See the Conversion Control section for more details.
7	DI	$\overline{\text{STBY}}$	Standby Mode Input. This pin is used to place the AD7609 into one of two power-down modes: standby mode or shutdown mode. The power-down mode entered depends on the state of the RANGE pin, as shown in Table 8. When in standby mode, all circuitry except the on-chip reference, regulators, and regulator buffers is powered down. When in shutdown mode, all circuitry is powered down.

Pin No.	Type[1]	Mnemonic	Description
5, 4, 3	DI	OS [2:0]	Oversampling Mode Pins. Logic inputs. These inputs are used to select the oversampling ratio. OS 2 is the MSB control bit, and OS 0 is the LSB control bit. See the Digital Filter section for additional details on the oversampling mode of operation and Table 9 for oversampling bit decoding.
33	DO/DI	DB15	Parallel Output Data Bits, Data Bit 15. When $\overline{PAR}$/SER SEL = 0, this pin acts as three-state parallel digital output pin. This pin is used to output DB17 of the conversion result during the first $\overline{RD}$ pulse and DB1 of the same conversion result during the second $\overline{RD}$ pulse. When $\overline{PAR}$/SER SEL = 1, this pin should be tied to AGND.
32	DO/DI	DB14	Parallel Output Data Bits, Data Bit 14. When $\overline{PAR}$/SER SEL = 0, this pin acts as three-state parallel digital output pin. When $\overline{CS}$ and $\overline{RD}$ are low, this pin is used to output DB16 of the conversion result during the first $\overline{RD}$ pulse and DB0 of the same conversion result during the second $\overline{RD}$ pulse. When $\overline{PAR}$/SER SEL = 1, this pin should be tied to AGND.
31 to 27	DO	DB[13:9]	Parallel Output Data Bits, Data Bit 13 to Data Bit 9. When $\overline{PAR}$/SER SEL = 0, these pins act as three-state parallel digital input/output pins. When $\overline{CS}$ and $\overline{RD}$ are low, these pins are used to output DB15 to DB11 of the conversion result during the first $\overline{RD}$ pulse and output 0 during the second $\overline{RD}$ pulse. When $\overline{PAR}$/SER SEL = 1, these pins should be tied to AGND.
24	DO	DB7/D_{OUT}A	Parallel Output Data Bit 7 (DB7)/Serial Interface Data Output Pin (D_{OUT}A). When $\overline{PAR}$/SER SEL = 0, this pin acts as a three-state parallel digital input/output pin. When $\overline{CS}$ and $\overline{RD}$ are low, this pin is used to output DB9 of the conversion result. When $\overline{PAR}$/SER SEL = 1, this pin functions as D_{OUT}A and outputs serial conversion data. See the Conversion Control section for further details.
25	DO	DB8/D_{OUT}B	Parallel Output Data Bit 8 (DB8)/Serial Interface Data Output Pin (D_{OUT}B). When $\overline{PAR}$/SER SEL = 0, this pin acts as a three-state parallel digital input/output pin. When $\overline{CS}$ and $\overline{RD}$ are low, this pin is used to output DB10 of the conversion result. When $\overline{PAR}$/SER SEL = 1, this pin functions as D_{OUT}B and outputs serial conversion data. See the Conversion Control section for further details.
22 to 16	DO	DB[6:0]	Parallel Output Data Bits, Data Bit 6 to Data Bit 0. When $\overline{PAR}$/SER SEL = 0, these pins act as three-state parallel digital input/output pins. When $\overline{CS}$ and $\overline{RD}$ are low, these pins are used to output DB8 to DB2 of the conversion result during the first $\overline{RD}$ pulse and output 0 during the second $\overline{RD}$ pulse. When $\overline{PAR}$/SER SEL = 1, these pins should be tied to AGND.

[1] Refers to classification of pin type; P denotes power, AI denotes analog input, REF denotes reference, DI denotes digital input, DO denotes digital output.

TYPICAL PERFORMANCE CHARACTERISTICS

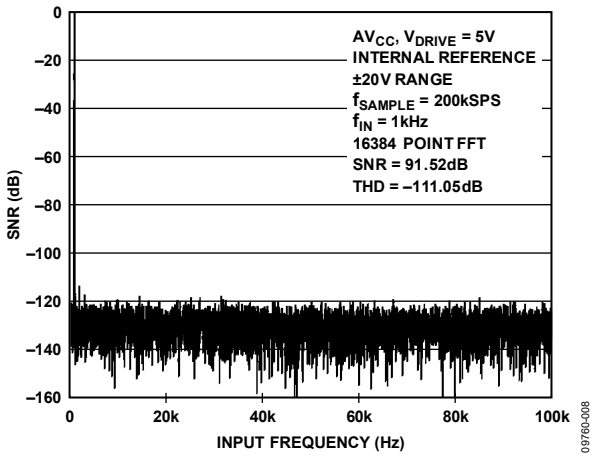


Figure 8. FFT Plot, ±20 V Range

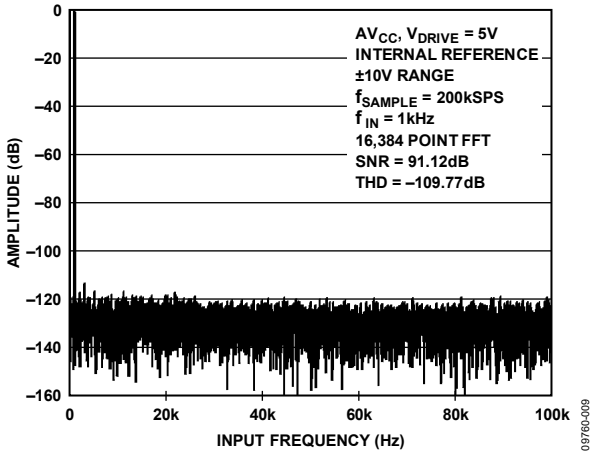


Figure 9. FFT Plot, ±10 V Range

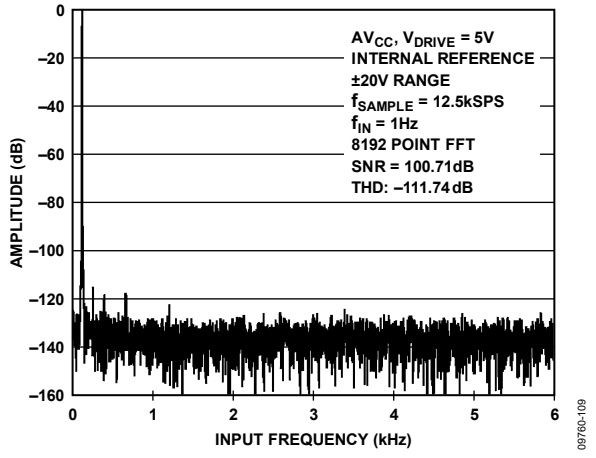


Figure 10. FFT Plot, ±20 V Range

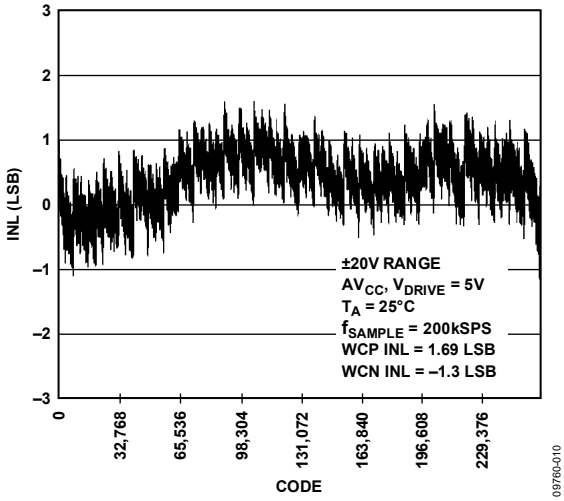


Figure 11. Typical INL, ±20 V Range

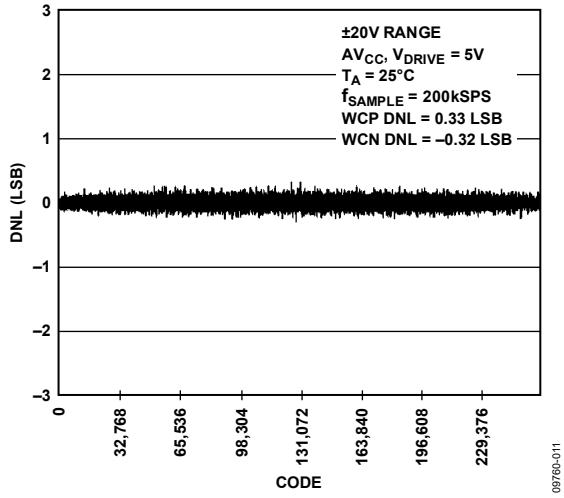


Figure 12. Typical DNL, ±20 V Range

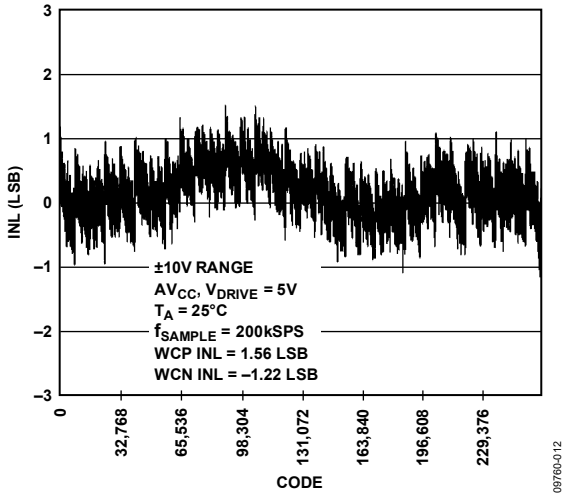


Figure 13. Typical INL, ±10 V Range

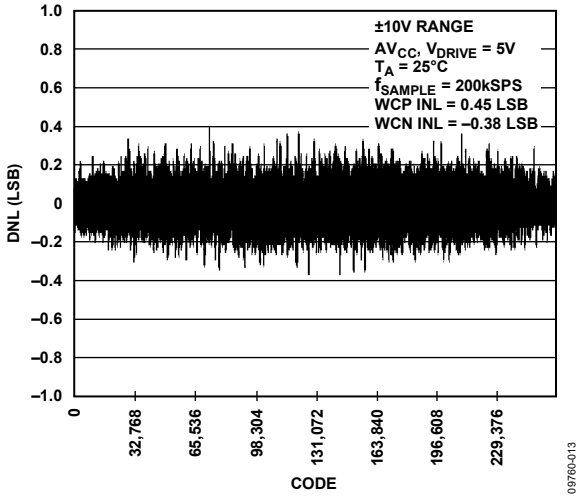


Figure 14. Typical DNL, ±10 V Range

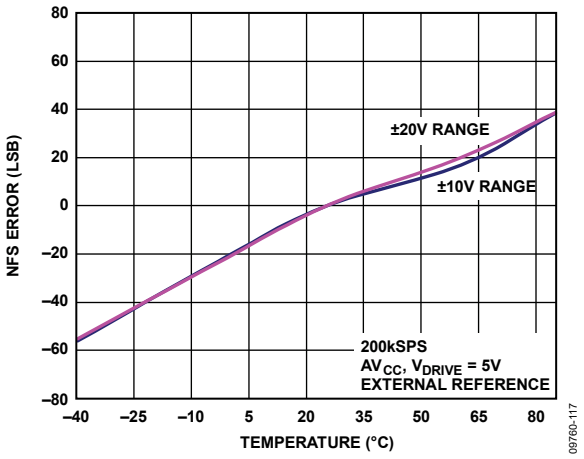


Figure 15. NFS Error vs. Temperature

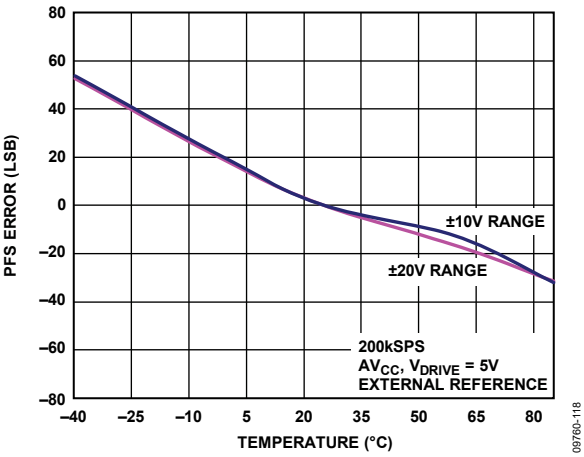


Figure 16. PFS Error vs. Temperature

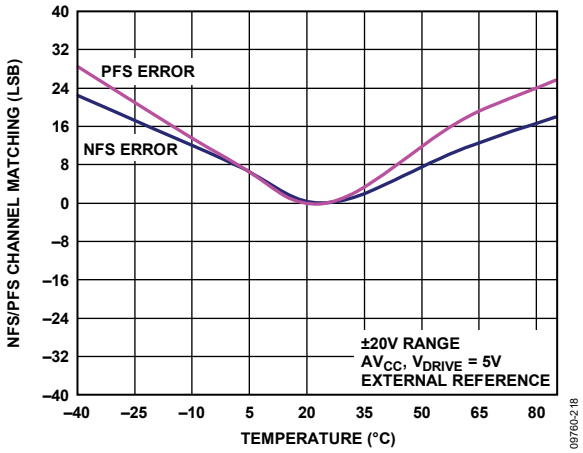


Figure 17. NFS and PFS Error Matching

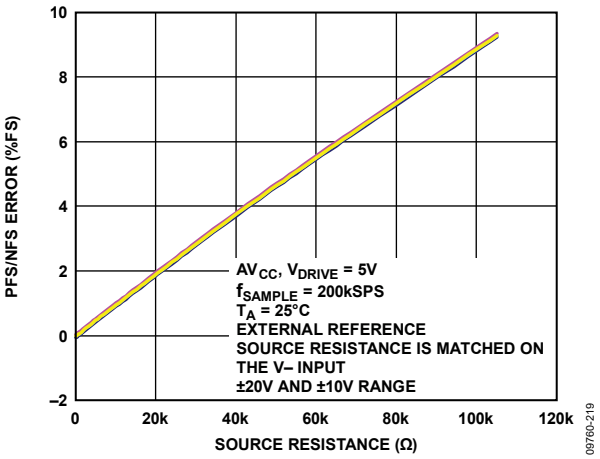


Figure 18. PFS and NFS Error vs. Source Resistance

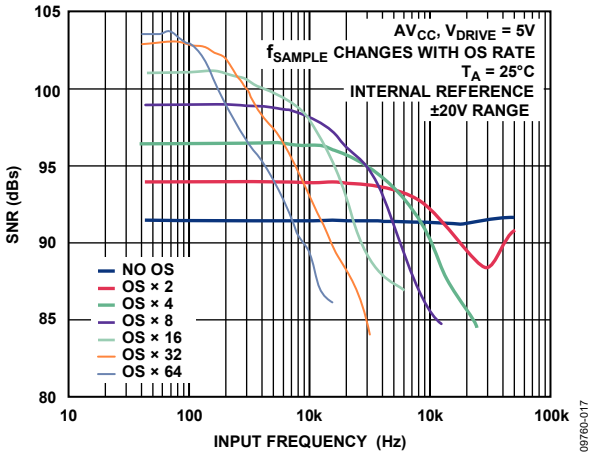


Figure 19. SNR vs. Input Frequency, ±20 V Range

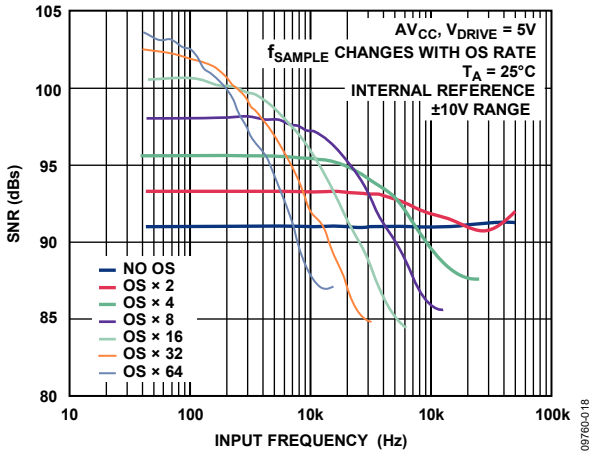


Figure 20. SNR vs. Input Frequency, ±10 V Range

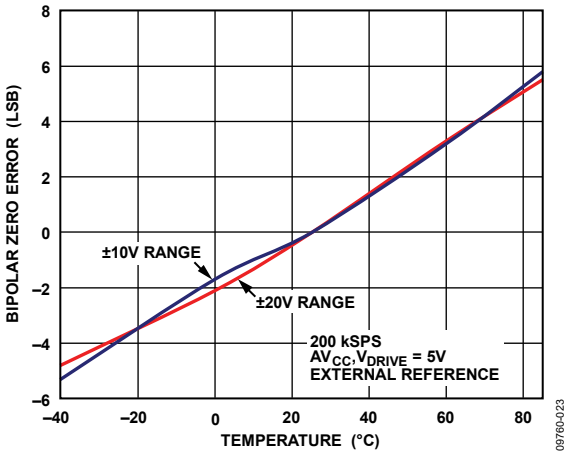


Figure 23. Bipolar Zero Code Error vs. Temperature

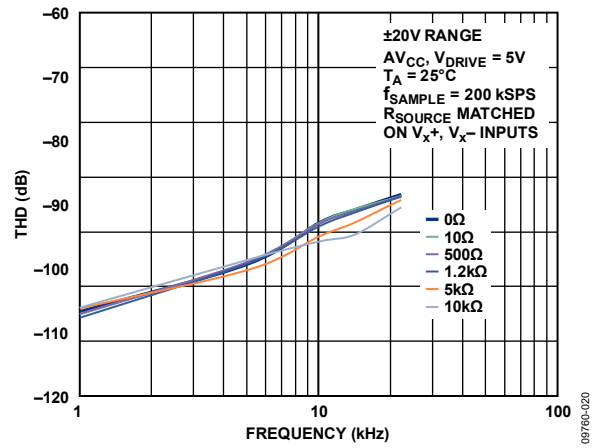


Figure 21. THD vs. Input Frequency for Various Source Impedances, ±20 V Range

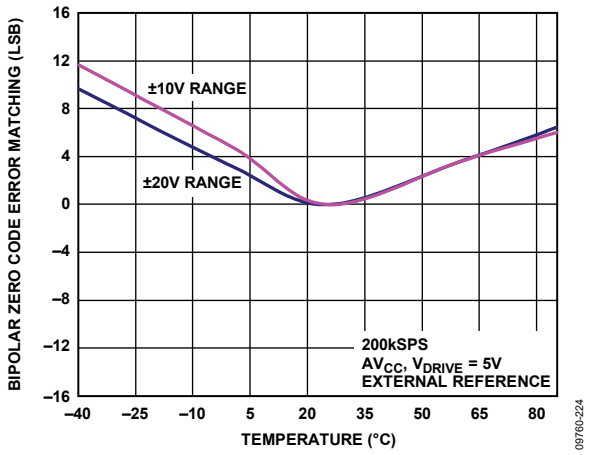


Figure 24. Bipolar Zero Code Error Matching Between Channels

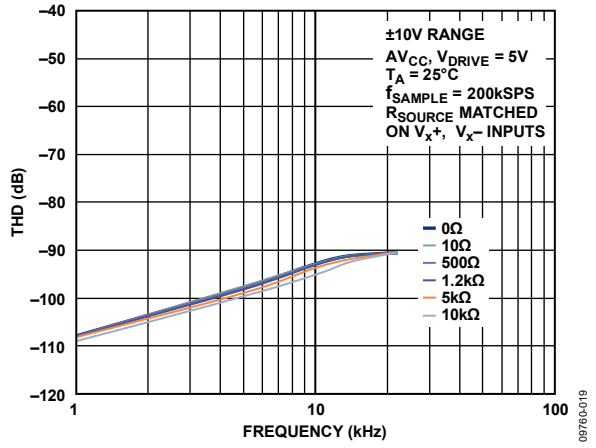


Figure 22. THD vs. Input Frequency for Various Source Impedances, ±10 V Range

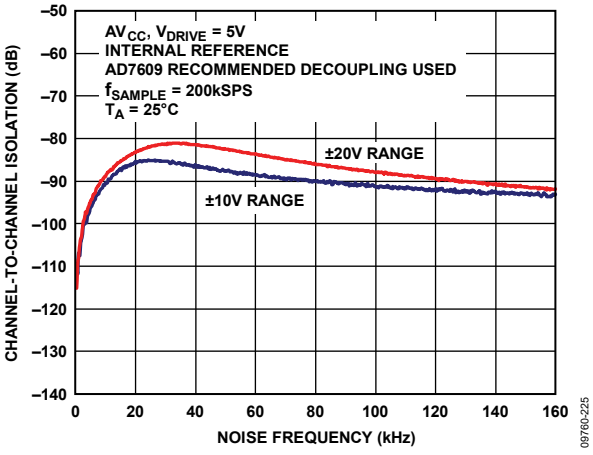


Figure 25. Channel-to-Channel Isolation

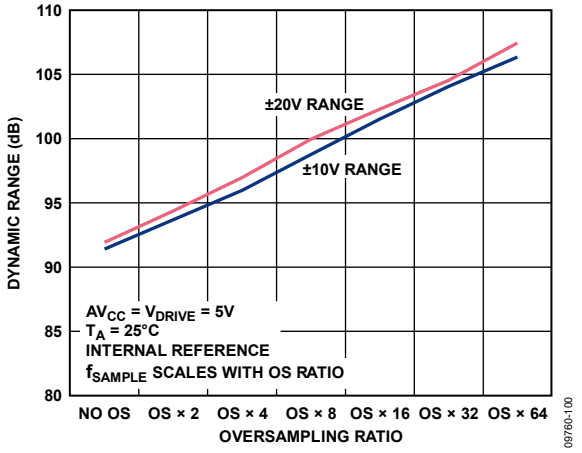


Figure 26. Dynamic Range vs. Oversampling Ratio

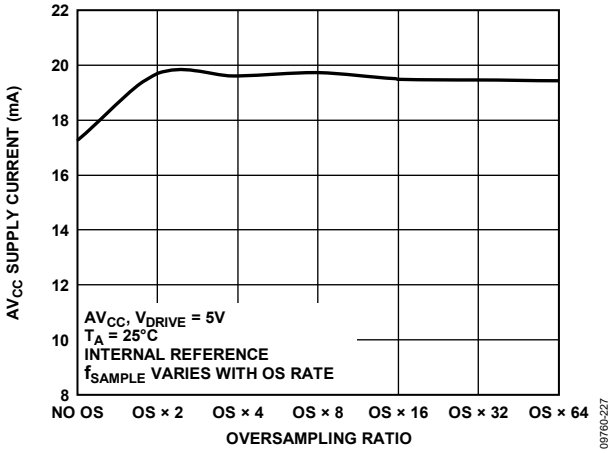


Figure 29. Supply Current vs. Oversampling Rate

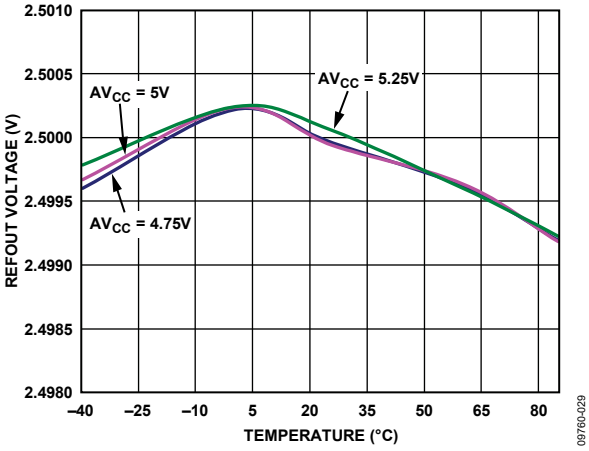


Figure 27. Reference Output Voltage vs. Temperature for Different Supply Voltages

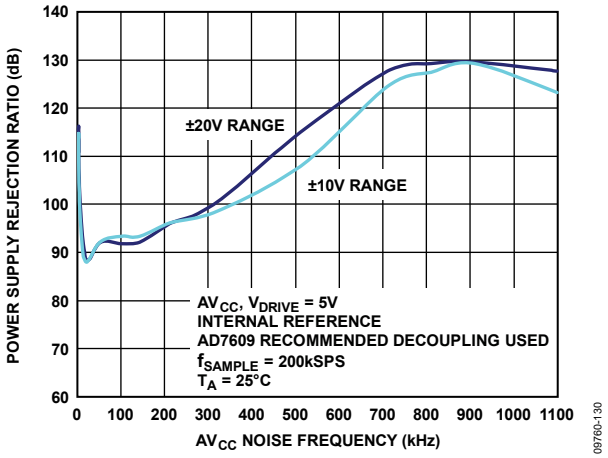


Figure 30. PSRR

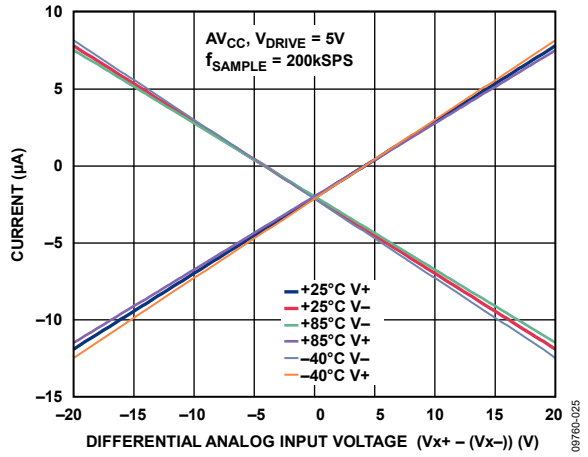


Figure 28. Analog Input Current vs. Input Voltage Over Temperature

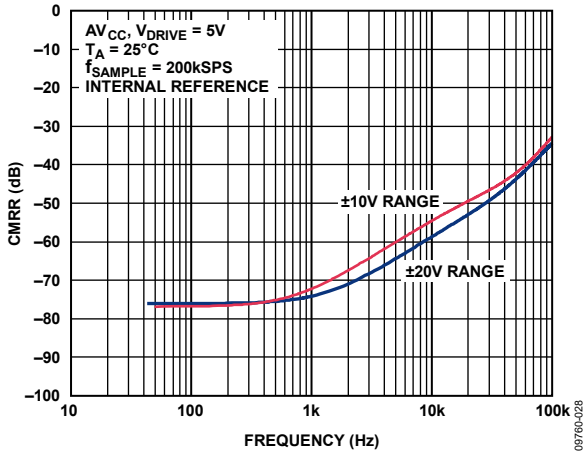


Figure 31. CMRR vs. Common-Mode Ripple Frequency

TERMINOLOGY

Integral Nonlinearity
The maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a ½ LSB below the first code transition, and full scale at ½ LSB above the last code transition.

Differential Nonlinearity
The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Bipolar Zero Code Error
The deviation of the midscale transition (all 1s to all 0s) from the ideal V_{IN} voltage, that is, AGND.

Bipolar Zero Code Error Match
The difference in bipolar zero code error between any two input channels.

Positive Full-Scale Error
The last transition (from 011 . . . 10 to 011 . . . 11 in twos complement coding) should occur for an analog voltage 1½ LSB below the nominal full scale (9.99977 V for the ±10 V range and 4.99988 V for the ±5 V range). The positive full-scale error is the deviation of the actual level of the last transition from the ideal level.

Positive Full-Scale Error Match
The difference in positive full-scale error between any two input channels.

Negative Full-Scale Error
The first transition (from 100 . . . 00 to 100 . . . 01 in twos complement coding) should occur for an analog voltage ½ LSB above the negative full scale (−9.999923 V for the ±10 V range and −4.9999618 for the ±5 V range). The negative full-scale error is the deviation of the actual level of the first transition from the ideal level.

Negative Full-Scale Error Match
The difference in negative full-scale error between any two input channels.

Track-and-Hold Acquisition Time
The track-and-hold amplifier returns to track mode at the end of the conversion. The track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±1 LSB, after the end of the conversion. See the Track-and-Hold Amplifiers section for more details.

Signal-to-(Noise + Distortion) Ratio
The measured ratio of signal-to-(noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$, excluding dc). The ratio depends on the number of quantization levels in the digitization process: the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

$$Signal\text{-}to\text{-}(Noise + Distortion) = (6.02\ N + 1.76)\ \text{dB}$$

Thus, for an 18-bit converter, this is 110.12 dB.

Total Harmonic Distortion (THD)
The ratio of the rms sum of the harmonics to the fundamental. For the AD7609, it is defined as

$$THD\ (\text{dB}) = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2 + V_7^2 + V_8^2 + V_9^2}}{V_1}$$

where:
V_1 is the rms amplitude of the fundamental.
V_2 to V_9 are the rms amplitudes of the second through ninth harmonics.

Peak Harmonic or Spurious Noise
The ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$, excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is determined by a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3. Intermodulation distortion terms are those for which neither m nor n is equal to 0. For example, the second-order terms include (fa + fb) and (fa − fb), and the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The calculation of the intermodulation distortion is per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in decibels (dB).

Power Supply Rejection (PSR)
Variations in power supply affect the full-scale transition but not the converter's linearity. Power supply rejection is the maximum change in full-scale transition point due to a change in power supply voltage from the nominal value. The power supply rejection ratio is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 200 mV p-p sine wave applied to the ADC V_{DD} and V_{SS} supplies of Frequency f_S.

$$PSRR \text{ (dB)} = 10 \log (Pf/Pf_S)$$

where:
Pf is equal to the power at Frequency f in the ADC output.
Pf_S is equal to the power at Frequency f_S coupled onto the V_{DD} and V_{SS} supplies.

Channel-to-Channel Isolation
Channel-to-channel isolation is a measure of the level of crosstalk between any two channels. It is measured by applying a full-scale, 10 kHz sine wave signal to all unselected input channels and determining the degree to which the signal attenuates in the selected channel with a 1 kHz signal.

Common-Mode Rejection Ratio (CMRR)
CMRR is defined as the ratio of the power in the ADC common-mode input at full-scale frequency, f, to the power in the output of a full-scale p-p sine wave applied to the common-mode voltage of $V_{IN}X+$ and $V_{IN}X-$ of frequency, f_S,

$$CMRR \text{ (dB)} = 20 \log (Pf/Pf_S)$$

where:
Pf is equal to the power at Frequency f in the ADC input.
Pf_S is equal to the power at Frequency f_S in the ADC output.

THEORY OF OPERATION

CONVERTER DETAILS

The AD7609 is a data acquisition system that employs a high speed, low power, charge redistribution successive approximation analog-to-digital converter (ADC) and allows the simultaneous sampling of eight true differential analog input channels. The analog inputs on the AD7609 can accept true bipolar input signals. The RANGE pin is used to select either ±20 V or ±10 V as the input range. The AD7609 operates from a single 5 V supply.

The AD7609 contains input clamp protection, input signal scaling amplifiers, a second-order antialiasing filter, track-and-hold amplifiers, an on-chip reference, reference buffers, a high speed ADC, a digital filter, and high speed parallel and serial interfaces. Sampling on the AD7609 is controlled using CONVST x signals.

ANALOG INPUT

Analog Input Ranges

The AD7609 can handle true bipolar input voltages. The logic level on the RANGE pin determines the analog input range of all analog input channels. If this pin is tied to a logic high, the analog input range is ±20 V for all channels. If this pin is tied to a logic low, the analog input range is ±10 V for all channels. A logic change on this pin has an immediate effect on the analog input range; however, there is a settling time of 80 µs typically, in addition to the normal acquisition time requirement. The recommended practice is to hardwire the RANGE pin according to the desired input range for the system signals.

During normal operation, the applied analog input voltage should remain within the analog input range selected via the RANGE pin. A RESET pulse must be applied to the part to ensure the analog input channels are configured for the range selected.

When in a power-down mode, it is recommended to tie the analog inputs together or both analog input pins (Vx+, Vx−) to GND. As per the Analog Input Clamp Protection section, the overvoltage clamp protection is recommended for use in transient overvoltage conditions, and should not remain active for extended periods. Stressing the analog inputs outside of these conditions may degrade the Bipolar Zero Code error and THD performance of the AD7609.

Analog Input Impedance

The analog input impedance of the AD7609 is 1 MΩ. This is a fixed input impedance and does not vary with the AD7609 sampling frequency. This high analog input impedance eliminates the need for a driver amplifier in front of the AD7609 allowing for direct connection to the source or sensor. With the need for a driver amplifier eliminated, bipolar supplies can be removed from the signal chain, which are often a source of noise in a system.

Analog Input Clamp Protection

Figure 32 shows the analog input structure of the AD7609. Each AD7609 analog input contains clamp protection circuitry. Despite a single 5 V supply operation, this analog input clamp protection allows for an input overvoltage up to ±16.5 V.

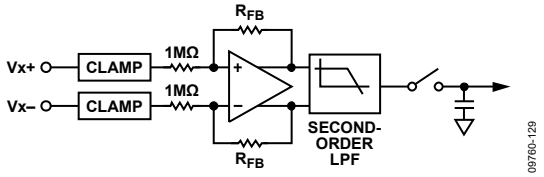


Figure 32. Analog Input Circuitry

Figure 33 shows the current vs. voltage characteristic of the clamp circuit. For input voltages up to ±16.5 V, no current flows in the clamp circuit. For input voltages above ±16.5 V, the AD7609 clamp circuitry turns on and clamps the analog input to ±16.5 V. A series resister should be placed on the analog input channels to limit the current to ±10 mA for input voltages above ±16.5 V. In an application where there is a series resistance on an analog input channel, VINx+, a corresponding resistance is required on the VINx− channel (see Figure 34). If there is no corresponding resister on the Vx− channel, this results in an offset error on that channel. It is recommended that the input overvoltage clamp protection circuitry be used to protect the AD7609 against transient overvoltage events. It is not recommended to leave the AD7609 in a condition where the clamp protection circuitry is active (in normal or power-down conditions) for extended periods because this may degrade the bipolar zero code error performance of the AD7609.

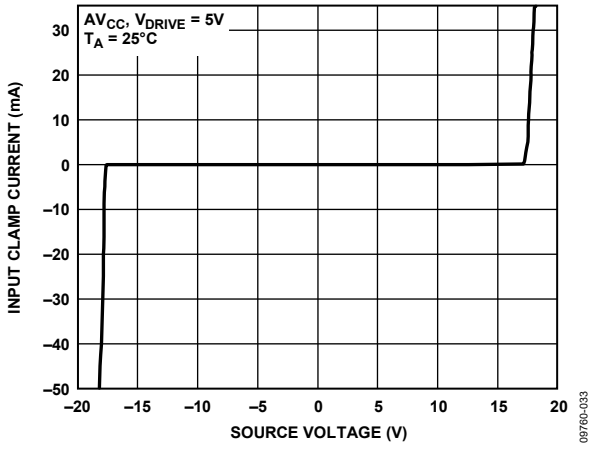


Figure 33. Input Protection Clamp Profile

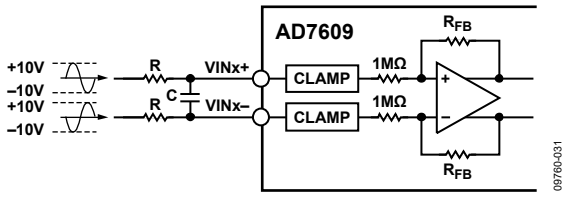
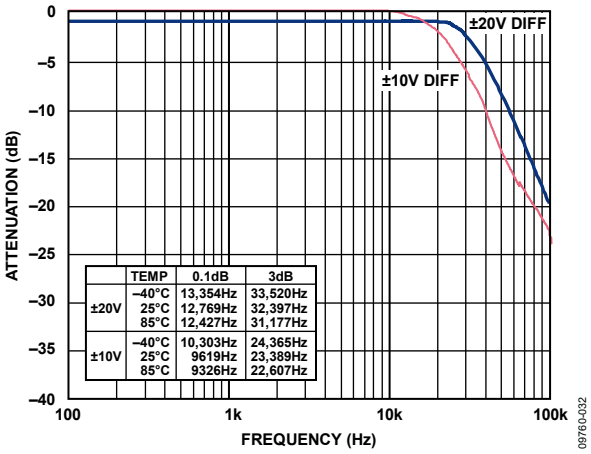


Figure 34. Input Resistance Matching on the Analog Input (±20 V Range)

Analog Input Antialiasing Filter

An analog antialiasing filter is also provided on the AD7609. The filter is a second-order Butterworth. Figure 35 and Figure 36 show the frequency and phase response respectively of the analog antialiasing filter. In the ±10 V range, the −3 dB frequency is typically 23 kHz. In the ±20 V range, the −3 dB frequency is typically 32 kHz.



	TEMP	0.1dB	3dB
±20V	–40°C	13,354Hz	33,520Hz
	25°C	12,769Hz	32,397Hz
	85°C	12,427Hz	31,177Hz
±10V	–40°C	10,303Hz	24,365Hz
	25°C	9619Hz	23,389Hz
	85°C	9326Hz	22,607Hz

Figure 35. Analog Antialiasing Filter Frequency Response

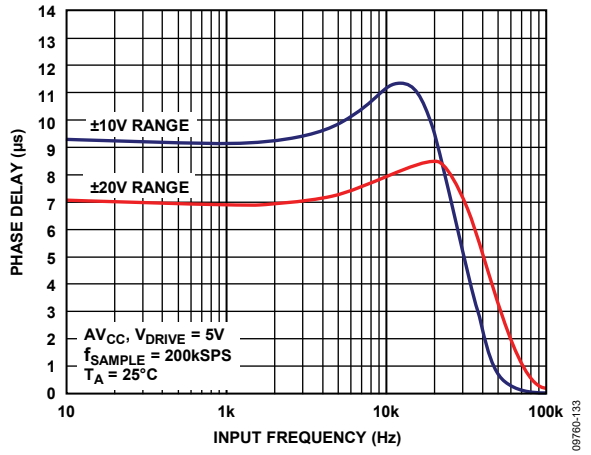


Figure 36. Analog Antialiasing Filter Phase Response

Track-and-Hold Amplifiers

The track-and-hold amplifiers on the AD7609 allow the ADC to accurately acquire an input sine wave of full-scale amplitude to 18-bit resolution. The track-and-hold amplifiers sample their respective inputs simultaneously on the rising edge of CONVST x. The aperture time for track-and-hold (that is, the delay time between the external CONVST x signal and the track-and-hold actually going into hold) is well matched, by design, across all eight track-and-holds on one device and from device to device. This matching allows more than one AD7609 device to be sampled simultaneously in a system.

The end of the conversion process across all eight channels is indicated by the falling edge of BUSY; and it is at this point that the track-and-holds return to track mode and the acquisition time for the next set of conversions begins.

The conversion clock for the part is internally generated, and the conversion time for all channels is 4 µs on the AD7609. The BUSY signal returns low after all eight conversions to indicate the end of the conversion process. On the falling edge of BUSY, the track-and-hold amplifiers return to track mode. New data can be read from the output register via the parallel or serial interface after BUSY goes low; or, alternatively, data from the previous conversion can be read while BUSY is high. Reading data from the AD7609 while a conversion is in progress has little effect on performance and allows a faster throughput to be achieved. With a V_{DRIVE} > 3.3 V, the SNR is reduced by ~1.5 dB when reading during a conversion.

ADC TRANSFER FUNCTION

The output coding of the AD7609 is twos complement. The designed code transitions occur midway between successive integer LSB values, that is, 1/2 LSB, 3/2 LSB. The LSB size is FSR/262,144 for the AD7609. The FSR for the AD7609 is 40 V for the ±20 V range and 20 V for the ±10 V range. The ideal transfer characteristic for the AD7609 is shown in Figure 37.

$$\pm 20\text{V CODE} = \frac{V+ \pm (V-)}{20\text{V}} \times 131{,}072 \times \frac{\text{REF}}{2.5\text{V}}$$

$$\pm 10\text{V CODE} = \frac{V+ \pm (V-)}{10\text{V}} \times 131{,}072 \times \frac{\text{REF}}{2.5\text{V}}$$

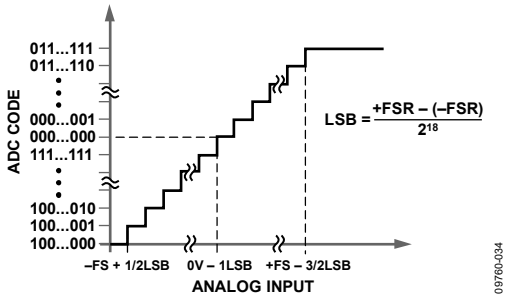


Figure 37. AD7609 Transfer Characteristic

The LSB size is dependent on the analog input range selected (see Table 7).

Table 7. Output Codes and Ideal Input Values

Description	Analog Input (V+ – (V–) 20 V Range	Analog Input V+ – (V–) 10 V Range	Digital Output Code (Hex)
FSR – 0.5 LSB	+19.99992 V	9.999961 V	0x1FFFF
Midscale + 1 LSB	+152.58 µV	76 µV	0x00001
Midscale	0 V	0 V	0x00000
Midscale – 1 LSB	−152.58 µV	−76 µV	0x3FFFF
−FSR + 1 LSB	−19.99984 V	−9.99992 V	0x20001
−FSR	−20 V	−10 V	0x20000

INTERNAL/EXTERNAL REFERENCE

The AD7609 contains an on-chip 2.5 V band gap reference. The REFIN/REFOUT pin allows access to the 2.5 V reference that generates the on-chip 4.5 V reference internally, or it allows an external reference of 2.5 V to be applied to the AD7609. An externally applied reference of 2.5 V is also amplified to 4.5 V using the internal buffer. This 4.5 V buffered reference is the reference used by the SAR ADC.

The REF SELECT pin is a logic input pin that allows the user to select between the internal reference and the external reference. If this pin is set to logic high, the internal reference is selected and is enabled; if this pin is set to logic low, the internal reference is disabled and an external reference voltage must be applied to the REFIN/REFOUT pin. The internal reference buffer is always enabled. After a reset, the AD7609 operates in the reference mode selected by the REF SELECT pin. Decoupling is required on the REFIN/REFOUT pin for both the internal or external reference options. A 10 µF ceramic capacitor is required on the REFIN/REFOUT to ground close to the REFGND pins. The AD7609 contains a reference buffer configured to amplify the REF voltage up to ~4.5 V, as shown in Figure 38. The REFCAPA and REFCAPB pins must be shorted together externally and a ceramic capacitor of 10 µF applied to REFGND to ensure the reference buffer is in closed-loop operation. The reference voltage available at the REFIN/REFOUT pin is 2.5 V.

When the AD7609 is configured in external reference mode, the REFIN/REFOUT pin is a high input impedance pin. For applications using multiple AD7609 devices, the following configurations are recommended depending on the application requirements.

External Reference Mode

One ADR421 external reference can be used to drive the REFIN/REFOUT pins of all AD7609 devices (see Figure 39). In this configuration, each AD7609 REFIN/REFOUT pin should be decoupled with a 100 nF decoupling capacitor.

Internal Reference Mode

One AD7609 device, configured to operate in the internal reference mode, can be used to drive the remaining AD7609 devices, which are configured to operate in external reference mode (see Figure 40). The REFIN/REFOUT pin of the AD7609, configured in internal reference mode, should be decoupled using a 10 µF ceramic decoupling capacitor. The other AD7609 devices, configured in external reference mode, should use a 100 nF decoupling capacitor on their REFIN/REFOUT pins.

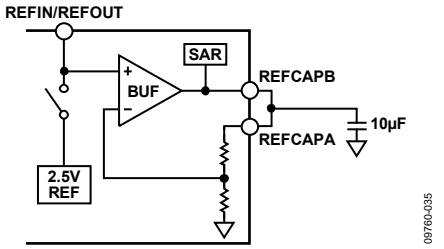


Figure 38. Reference Circuitry

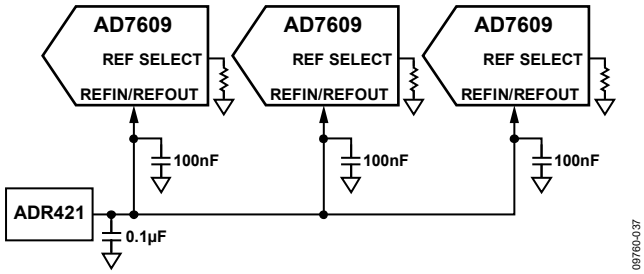


Figure 39. Single External Reference Driving Multiple AD7609 REFIN/REFOUT Pins

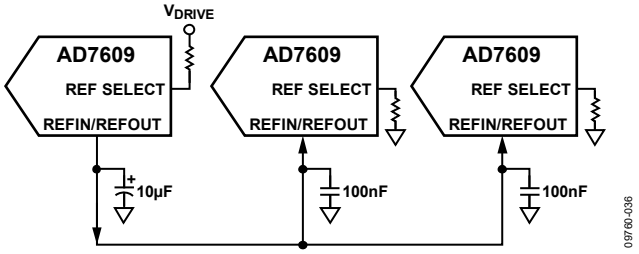


Figure 40. Internal Reference Driving Multiple AD7609 REFIN Pins

TYPICAL CONNECTION DIAGRAM

Figure 41 shows the typical connection diagram for the AD7609. There are four AV_{CC} supply pins on the part that can be tied together and decoupled using a 100 nF capacitor at each supply pin and a 10 µF capacitor at the supply source. The AD7609 can operate with the internal reference or an externally applied reference. In this configuration, the AD7609 is configured to operate with the internal reference. When using a single AD7609 device on the board, the REFIN/REFOUT pin should be decoupled with a 10 µF capacitor. In an application with multiple AD7609 devices, see the Internal/External Reference section. The REFCAPA and REFCAPB pins are shorted together and decoupled with a 10 µF ceramic capacitor.

The V_{DRIVE} supply is connected to the same supply as the processor. The voltage on V_{DRIVE} controls the voltage value of the output logic signals. For layout, decoupling, and grounding hints, see the Layout Guidelines section.

After supplies are applied to the AD7609, a reset should be applied to the AD7609 to ensure that it is configured for the correct mode of operation.

POWER-DOWN MODES

There are two power-down modes available on the AD7609. The $\overline{STBY}$ pin controls whether the AD7609 is in normal mode or one of the two power-down modes. The two power-down modes available are standby mode and shutdown mode. The power-down mode is selected through the state of the RANGE pin when the $\overline{STBY}$ pin is low. Table 8 shows the configurations required to choose the desired power-down mode. When the AD7609 is placed in standby mode, the current consumption is 8 mA maximum and power-up time is approximately 100 µs because the capacitor on the REFCAPA/REFCAPB pins must charge up. In standby mode, the on-chip reference and regulators remain powered up and the amplifiers and ADC core are powered down. When the AD7609 is placed in shutdown mode, the current consumption is 11 µA maximum and power up time is about 13 ms. In shutdown mode, all circuitry is powered down. When the AD7609 is powered up from shutdown mode, a reset signal must be applied to the AD7609 after the required power-up time has elapsed.

Table 8. Power-Down Mode Selection

Power-Down Mode	$\overline{STBY}$	RANGE
Standby	0	1
Shutdown	0	0

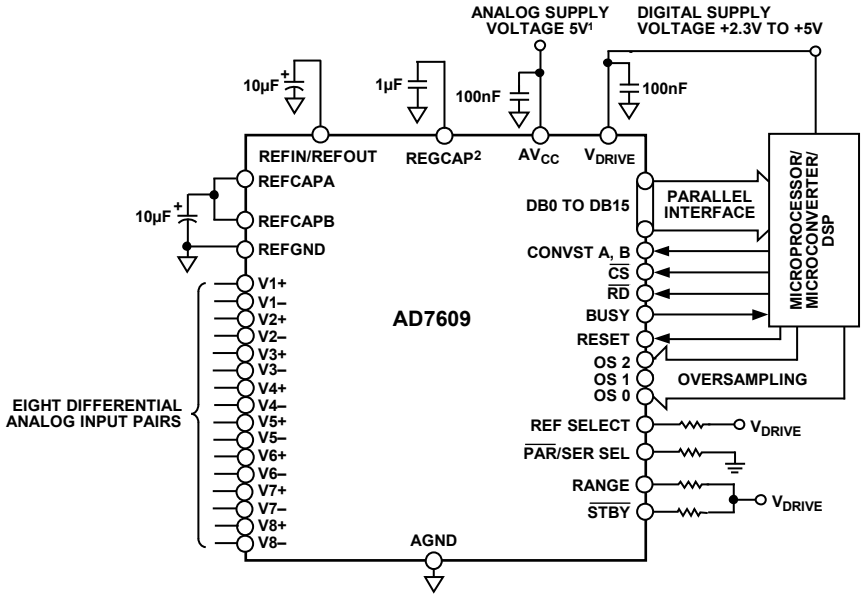


Figure 41. Typical Connection Diagram

CONVERSION CONTROL

Simultaneous Sampling on All Analog Input Channels

The AD7609 allows simultaneous sampling of all analog input channels. All channels are sampled simultaneously when both CONVST x pins (CONVST A, CONVST B) are tied together. A single CONVST x signal is used to control both CONVST x inputs. The rising edge of this common CONVST x signal initiates simultaneous sampling on all analog input channels.

The AD7609 contains an on-chip oscillator that is used to perform the conversions. The conversion time for all ADC channels is t_{CONV}. The BUSY signal indicates to the user when conversions are in progress, so that when the rising edge of CONVST x is applied, BUSY goes logic high and transitions low at the end of the entire conversion process. The falling edge of the BUSY signal is used to place all eight track-and-hold amplifiers back into track mode. The falling edge of BUSY also indicates that the new data can now be read from the parallel bus (DB[15:0]) or the serial data lines, $D_{OUT}A$ and $D_{OUT}B$.

Simultaneously Sampling Two Sets of Channels

The AD7609 also allows the analog input channels to be sampled simultaneously in two sets. This can be used in power line protection and measurement systems to compensate for phase differences between PT and CT transformers. In a 50 Hz system, this allows for up to 9° of phase compensation, and in a 60 Hz system, it allows for up to 10° of phase compensation.

This is accomplished by pulsing the two CONVST x pins independently and is only possible if oversampling is not in use. CONVST A is used to initiate simultaneous sampling of the first set of channels (V1 to V4). CONVST B is used to initiate simultaneous sampling on the second set of analog input channels (V5 to V8), as illustrated in Figure 42. On the rising edge of CONVST A, the track-and-hold amplifiers for the first set of channels are placed into hold mode. On the rising edge of CONVST B, the track-and-hold amplifiers for the second set of channels are placed into hold mode. The conversion process begins after both rising edges of CONVST x have occurred; therefore, BUSY goes high on the rising edge of the later CONVST x signal. The falling edge of BUSY also indicates that the new data can now be read from the parallel bus or the serial data lines, $D_{OUT}A$ and $D_{OUT}B$. There is no change to the data read process when using two separate CONVST x signals.

Connect all unused analog input channel to AGND. The results for any unused channels are still included in the data read because all channels are always converted.

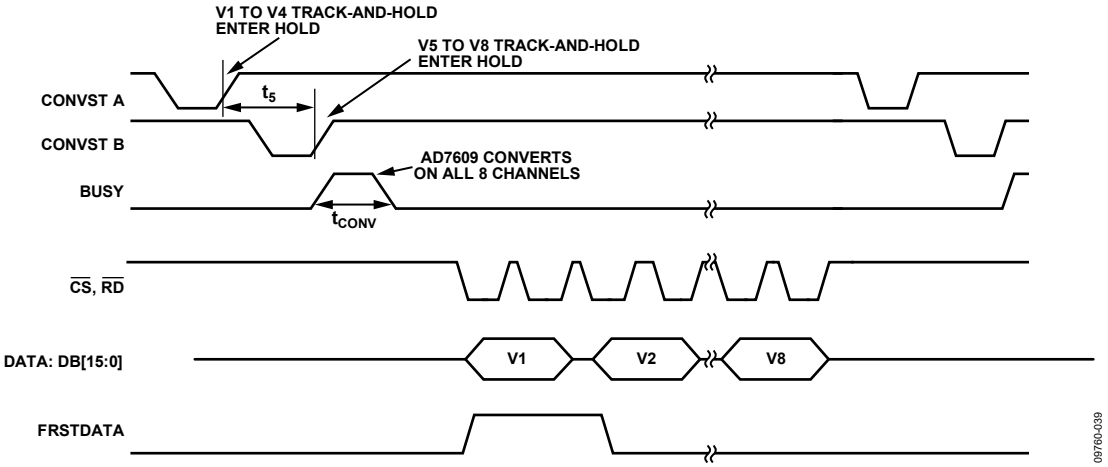


Figure 42. Simultaneous Sampling on Channel Sets Using Independent CONVST A/CONVST B Signals—Parallel Mode

DIGITAL INTERFACE

The AD7609 provides two interface options: a parallel interface and a high speed serial interface. The required interface mode is selected via the PAR/SER SEL pin.

The operation of the interface modes is described in the following sections.

PARALLEL INTERFACE (PAR/SER SEL = 0)

Data can be read from the AD7609 via the parallel data bus with standard CS and RD signals. To read the data over the parallel bus, the PAR/SER SEL pin should be tied low. The CS and RD input signals are internally gated to enable the conversion result onto the data bus. The data lines, DB15 to DB0, leave their high impedance state when both CS and RD are logic low.

The rising edge of the CS input signal three-states the bus and the falling edge of the CS input signal takes the bus out of the high impedance state. CS is the control signal that enables the data lines; it is the function that allows multiple AD7609 devices to share the same parallel data bus. The CS signal can be permanently tied low, and the RD signal can be used to access the conversion results, as shown in Figure 4. A read operation of new data can take place after the BUSY signal goes low (Figure 2), or, alternatively, a read operation of data from the previous conversion process can take place while BUSY is high (Figure 3).

The RD pin is used to read data from the output conversion results register. Two RD pulses are required to read the full 18-bit conversion result from each channel. Applying a sequence of 16 RD pulses to the AD7609 RD pin clocks the conversion results out from each channel onto the parallel output bus, DB[15:0], in ascending order. The first RD falling edge after BUSY goes low clocks out DB[17:2] of the V1 result, and the next RD falling edge updates the bus with DB[1:0] of the V1 result. It takes 16 RD pulses to read the eight 18-bit conversion results from the AD7609. The 16th falling edge of RD clocks out the DB[1:0] conversion result for Channel V8. When the RD signal is logic low, it enables the data conversion result from each channel to be transferred to the digital host (DSP, FPGA).

When there is only one AD7609 in a system/board and it does not share the parallel bus, data can be read using only one control signal from the digital host. The CS and RD signals can be tied together, as shown in Figure 5. In this case, the data bus comes out of three-state on the falling edge of CS/RD. The combined CS and RD signal allows the data to be clocked out of the AD7609 and to be read by the digital host. In this case, CS is used to frame the data transfer of each data channel and 16 CS pulses are required to read the eight channels of data.

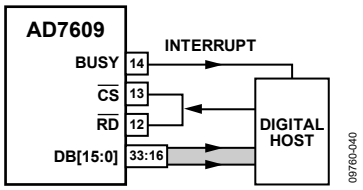


Figure 43. AD7609 Interface Diagram: One AD7609 Using the Parallel Bus; CS and RD Shorted Together

SERIAL INTERFACE (PAR/SER SEL = 1)

To read data back from the AD7609 over the serial interface, the PAR/SER SEL pin should be tied high. The CS and SCLK signals are used to transfer data from the AD7609. The AD7609 has two serial data output pins, DOUTA and DOUTB. Data can be read back from the AD7609 using one or both of these DOUT lines. For the AD7609, conversion results from Channel V1 to Channel V4 first appear on DOUTA, whereas conversion results from Channel V5 to Channel V8 first appear on DOUTB.

The CS falling edge takes the data output lines (DOUTA and DOUTB) out of three-state and clocks out the MSB of the conversion result. The rising edge of SCLK clocks all subsequent data bits onto the serial data outputs, DOUTA and DOUTB. The CS input can be held low for the entire serial read or it can be pulsed to frame each channel read of 18 SCLK cycles.

Figure 44 shows a read of eight simultaneous conversion results using two DOUT lines on the AD7609. In this case, a 72 SCLK transfer is used to access data from the AD7609 and CS is held low to frame the entire 72 SCLK cycles. Data can also be clocked out using only one DOUT line, in which case DOUTA is recommended to access all conversion data, because the channel data is output in ascending order. For the AD7609 to access all eight conversion results on one DOUT line, a total of 144 SCLK cycles are required. These 144 SCLK cycles can be framed by one CS signal or each group of 18 SCLK cycles can be individually framed by the CS signal. The disadvantage of using only one DOUT line is that the throughput rate is reduced if reading after conversion. The unused DOUT line should be left unconnected in serial mode. For the AD7609, if DOUTB is to be used as a single DOUT line, the channel results are output in the following order: V5, V6, V7, V8, V1, V2, V3, V4; however, the FRSTDATA indicator returns low after V5 is read on DOUTB.

Figure 6 shows the timing diagram for reading one channel of data, framed by the $\overline{CS}$ signal, from the AD7609 in serial mode. The SCLK input signal provides the clock source for the serial read operation. $\overline{CS}$ goes low to access the data from the AD7609. The falling edge of $\overline{CS}$ takes the bus out of three-state and clocks out the MSB of the 18-bit conversion result. This MSB is valid on the first falling edge of the SCLK after the $\overline{CS}$ falling edge. The subsequent 17 data bits are clocked out of the AD7609 on the SCLK rising edge. Data is valid on the SCLK falling edge. Eighteen clock cycles must be provided to the AD7609 to access each conversion result.

The FRSTDATA output signal indicates when the first channel, V1, is being read back. When the $\overline{CS}$ input is high, the FRSTDATA output pin is in three-state. In serial mode, the falling edge of $\overline{CS}$ takes FRSTDATA out of three-state and sets the FRSTDATA pin high indicating that the result from V1 is available on the $D_{OUT}A$ output data line. The FRSTDATA output returns to a logic low following the 18th SCLK falling edge. If all channels are read on $D_{OUT}B$, the FRSTDATA output does not go high when V1 is being output on this serial data output pin. It only goes high when V1 is available on $D_{OUT}A$ (and this is when V5 is available on $D_{OUT}B$).

READING DURING CONVERSION

Data can be read from the AD7609 while BUSY is high and conversions are in progress. This has little effect on the performance of the converter and allows a faster throughput rate to be achieved. A parallel or serial read can be performed during conversions and when oversampling may or may not be in use. Figure 3 shows the timing diagram for reading while BUSY is high in parallel or serial mode. Reading during conversions allows the full throughput rate to be achieved when using the serial interface with a V_{DRIVE} of 3.3 V to 5.25 V.

Data can be read from the AD7609 at any time other than on the falling edge of BUSY because this is when the output data registers are updated with the new conversion data. t_6, outlined in Table 3, should be observed in this condition.

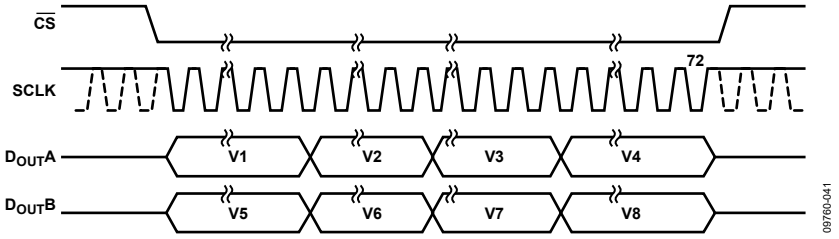


Figure 44. AD7609 Serial Interface with Two D_{OUT} Lines

DIGITAL FILTER

The AD7609 contains an optional digital filter. This digital filter is a first-order sinc filter. This digital filter should be used in applications where slower throughput rates are used or where higher signal-to-noise ratio or dynamic range is desirable. The oversampling ratio of the digital filter is controlled using the oversampling pins, OS [2:0] (see Table 9). OS 2 is the MSB control bit and OS 0 is the LSB control bit. Table 9 provides the oversampling bit decoding to select the different oversample rates. The OS pins are latched on the falling edge of BUSY. This sets the oversampling rate for the next conversion (see Figure 45). In addition to the oversampling function, the output result is decimated to 18-bit resolution.

If the OS pins are set to select an OS ratio of 8, the next CONVST x rising edge takes the first sample for each channel and the remaining seven samples for all channels are taken with an internally generated sampling signal. These samples are then averaged to yield an improvement in SNR performance. Table 9 shows typical SNR performance for both the ±20 V and the ±10 V ranges. As Table 9 indicates, there is an improvement in SNR as the OS ratio increases. As the OS ratio increases, the 3 dB frequency is reduced and the allowed sampling frequency is also reduced. In an application where the required sampling frequency is 10 kSPS, an OS ratio of up to 16 can be used. In this case, the application sees an improvement in SNR but the input −3 dB bandwidth is limited to ~6 kHz.

The CONVST A and CONVST B pins must be tied/driven together when oversampling is turned on. When the oversampling function is turned on, the BUSY high time for the conversion process extends. The actual BUSY high time depends on the oversampling rate selected; the higher the oversampling rate, the longer the BUSY high, or total conversion time, see Table 9.

Figure 46 shows that the conversion time extends as the oversampling rate is increased, and the BUSY signal lengthens for the different oversampling rates. For example, a sampling frequency of 10 kSPS yields a cycle time of 100 µs. Figure 46 shows OS × 2 and OS × 4; for a 10 kSPS example, there is adequate cycle time to further increase the oversampling rate and yield greater improvements in SNR performance. In an application where the initial sampling or throughput rate is at 200 kSPS, for example, and oversampling is turned on, the throughput rate must be reduced to accommodate the longer conversion time and to allow for the read. To achieve the fastest throughput rate possible when oversampling is turned on, the read can be performed during the BUSY high time. The falling edge of BUSY is used to update the output data registers with the new conversion data; therefore, the reading of conversion data should not occur on this edge. Figure 47 to Figure 53 illustrate the effect of oversampling on the code spread in a dc histogram plot. As the oversample rate is increased, the spread of codes is reduced. (In Figure 47 to Figure 53, AV_{CC} = V_{DRIVE} = 5 V and the sampling rate was scaled with OS ratio.)

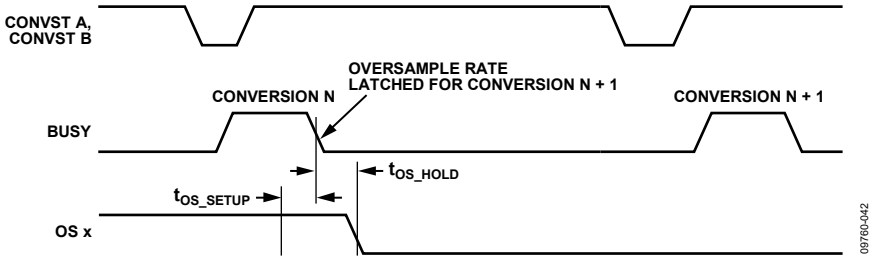


Figure 45. OS Pin Timing

Table 9. Oversampling Bit Decoding (100 Hz Input Signal)

OS [2:0]	OS Ratio	SNR ±10 V Range (dB)	SNR ±20 V Range (dB)	−3 dB BW 10 V Range (kHz)	−3 dB BW 20 V Range (kHz)	Maximum Throughput CONVST x Frequency (kHz)
000	No OS	90.8	91.5	22	33	200
001	2	93.3	93.9	22	28.9	100
010	4	95.5	96.4	18.5	21.5	50
011	8	98	98.9	11.9	12	25
100	16	100.6	101	6	6	12.5
101	32	101.8	102	3	3	6.25
110	64	102.7	102.9	1.5	1.5	3.125
111	Invalid					

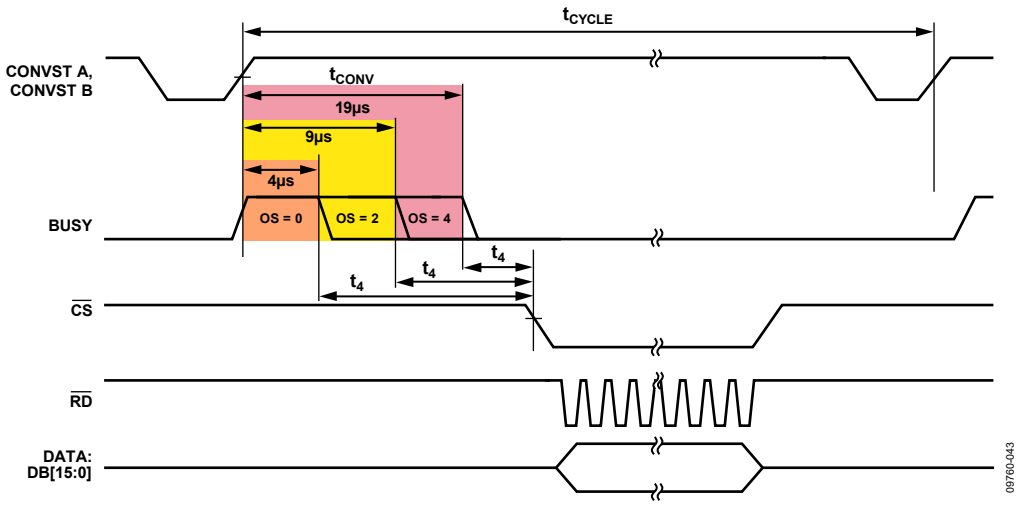


Figure 46. AD7609—No Oversampling, Oversampling × 4, and Oversampling × 8 Using Read After Conversion

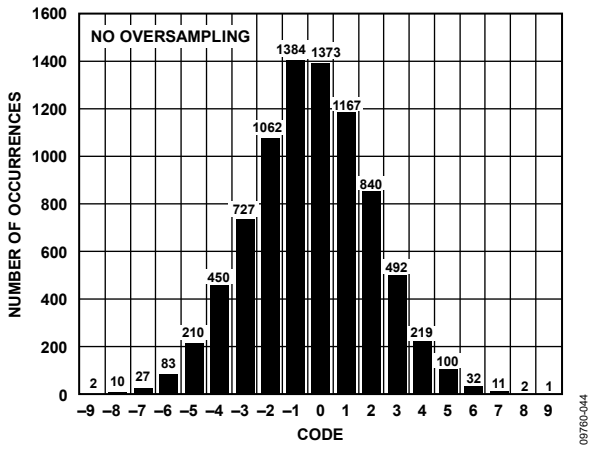


Figure 47. Histogram of Codes—No OS (19 Codes)

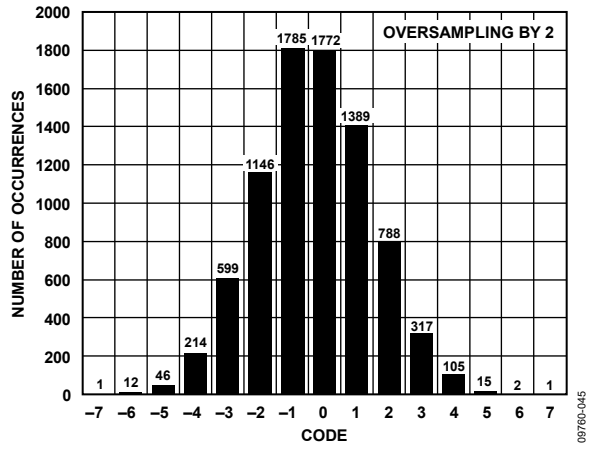


Figure 48. Histogram of Codes—OS × 2 (15 Codes)

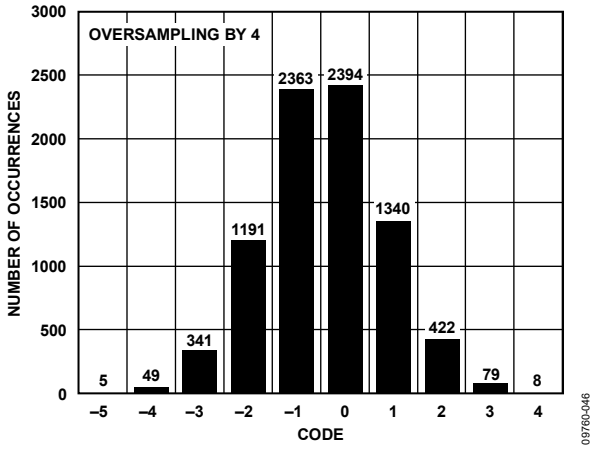


Figure 49. Histogram of Codes—OS × 4 (10 Codes)

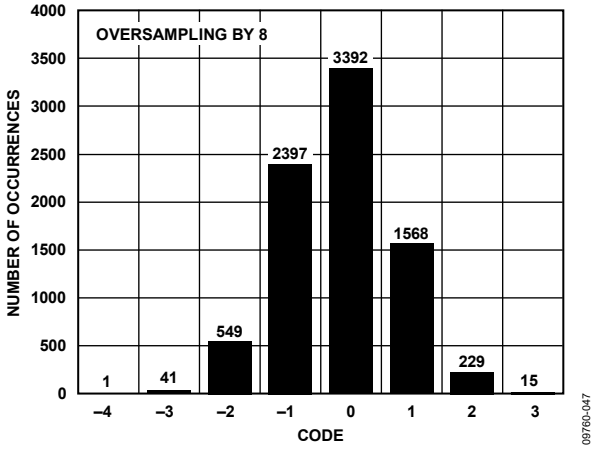


Figure 50. Histogram of Codes—OS × 8 (Eight Codes)

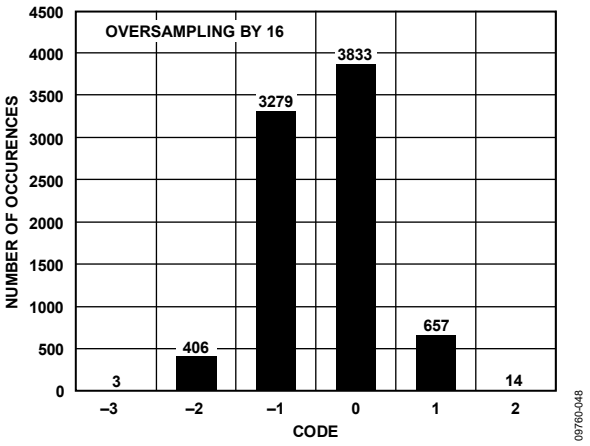


Figure 51. Histogram of Codes—OS × 16 (Six Codes)

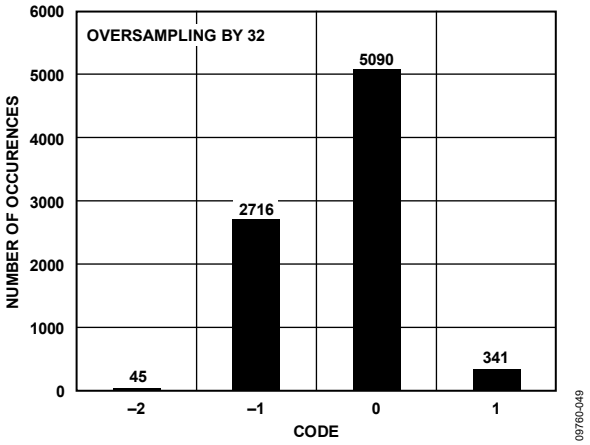


Figure 52. Histogram of Codes—OS × 32 (Four Codes)

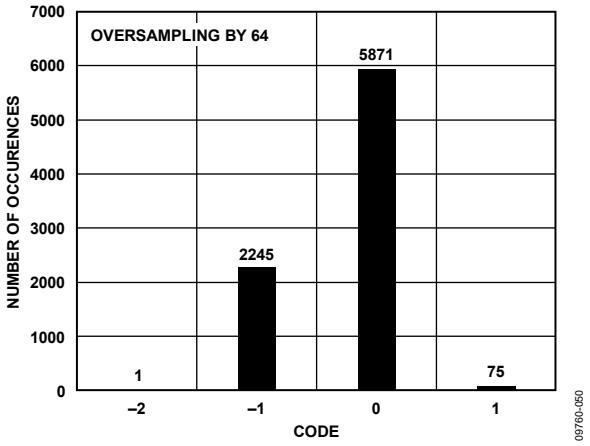


Figure 53. Histogram of Codes – OS × 64 (Four Codes)

When the oversampling mode is selected, this has the effect of adding a digital filter function after the ADC. The different oversampling rates and the CONVST x sampling frequency produces different digital filter frequency profiles.

Figure 54 to Figure 59 show the digital filter frequency profiles for the different oversampling rates. The combination of the analog antialiasing filter and the oversampling digital filter can be used to eliminate or reduce the complexity of the design of the filter before the AD7609. The digital filtering combines steep roll-off and linear phase response.

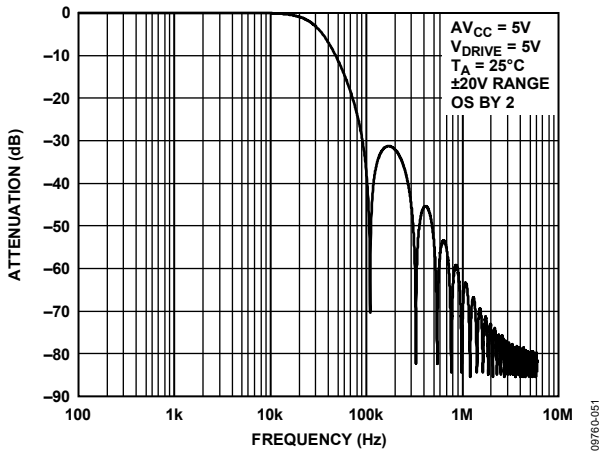


Figure 54. Digital Filter Response for OS × 2

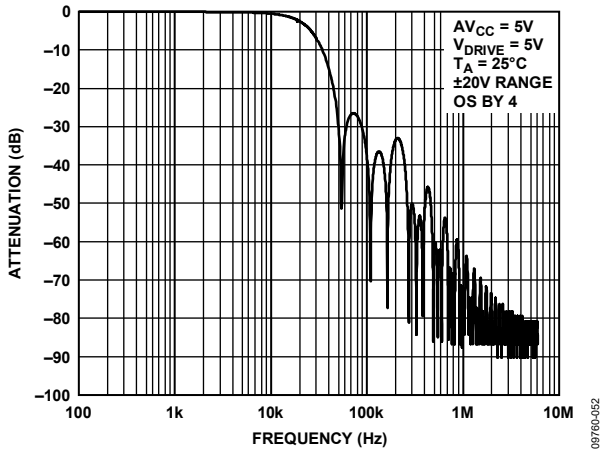


Figure 55. Digital Filter Response for OS × 4

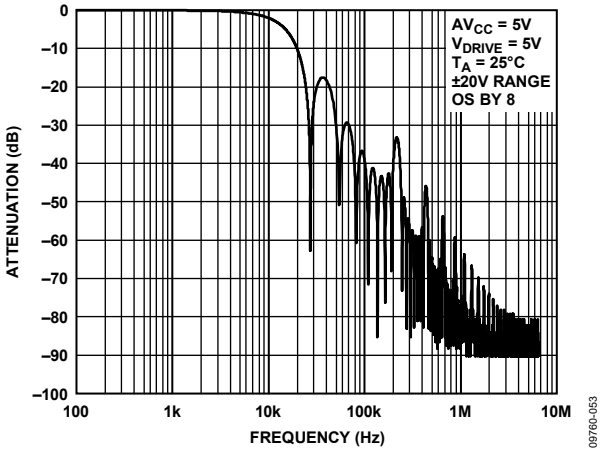


Figure 56. Digital Filter Response for OS × 8

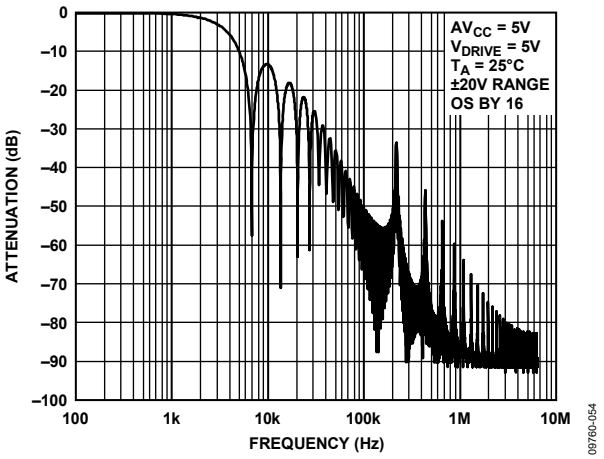


Figure 57. Digital Filter Response for OS × 16

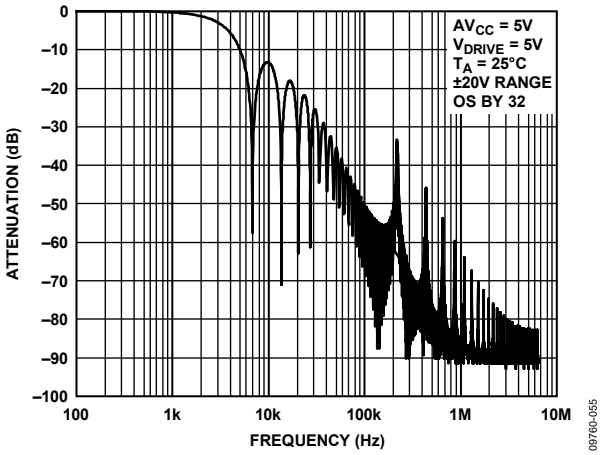


Figure 58. Digital Filter Response for OS × 32

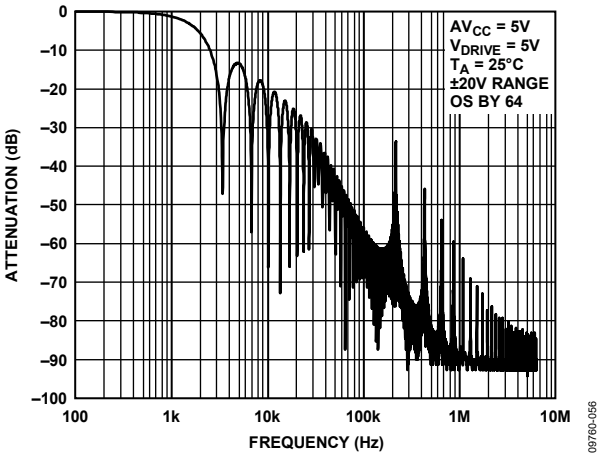


Figure 59. Digital Filter Response for OS × 64

LAYOUT GUIDELINES

The printed circuit board that houses the AD7609 should be designed so that the analog and digital sections are separated and confined to different areas of the board.

Use at least one ground plane. It can be common or split between the digital and analog sections. In the case of the split plane, the digital and analog ground planes should be joined in only one place, preferably as close as possible to the AD7609.

If the AD7609 is in a system where multiple devices require analog-to-digital ground connections, the connection should still be made at only one point, a star ground point, which should be established as close as possible to the AD7609. Good connections should be made to the ground plane. Avoid sharing one connection for multiple ground pins. Individual vias or multiple vias to the ground plane should be used for each ground pin.

Avoid running digital lines under the devices because doing so couples noise onto the die. Allow the analog ground plane to run under the AD7609 to avoid noise coupling. Shield fast-switching signals like CONVST A, CONVST B, or clocks with digital ground to avoid radiating noise to other sections of the board, and they should never run near analog signal paths. Avoid crossover of digital and analog signals. Run traces on layers in close proximity on the board at right angles to each other to reduce the effect of feedthrough through the board.

The power supply lines to the AV_{CC} and V_{DRIVE} pins on the AD7609 should use as large a trace as possible to provide low impedance paths and reduce the effect of glitches on the power supply lines. Where possible, use supply planes. Good connections should be made between the AD7609 supply pins and the power tracks on the board; this should involve the use of a single via or multiple vias for each supply pin.

Good decoupling is also important to lower the supply impedance presented to the AD7609 and to reduce the magnitude of the supply spikes. Place the decoupling capacitors close to, ideally right up against, these pins and their corresponding ground pins. Place the decoupling capacitors for the REFIN/REFOUT pin and the REFCAPA and REFCAPB pins as close as possible to their respective AD7609 pins. Where possible, they should be placed on the same side of the board as the AD7609 device. Figure 60 shows the recommended decoupling on the top layer of the AD7609 board. Figure 61 shows bottom layer decoupling. Bottom layer decoupling is for the four AV_{CC} pins and the V_{DRIVE} pin.

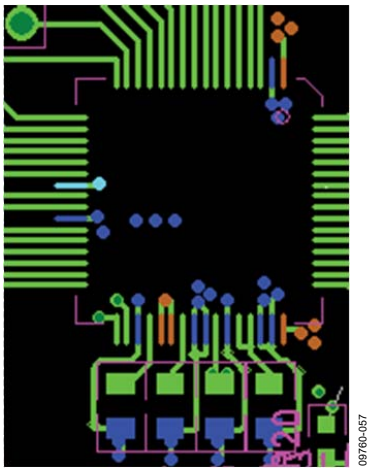


Figure 60. Top Layer Decoupling REFIN/REFOUT, REFCAPA, REFCAPB, and REGCAP Pins

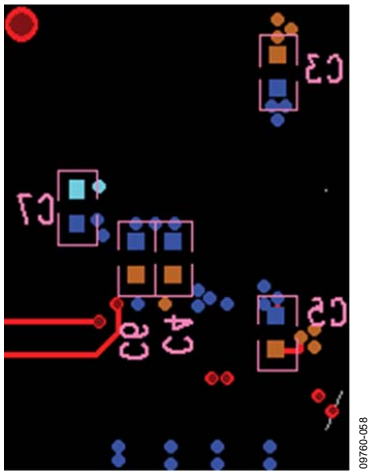


Figure 61. Bottom Layer Decoupling

To ensure good device-to-device performance matching in a system that contains multiple AD7609 devices, a symmetrical layout between the AD7609 devices is important. Figure 62 shows a layout with two AD7609 devices. The AV_{CC} supply plane runs to the right of both devices. The V_{DRIVE} supply track runs to the left of the two AD7609 devices. The reference chip is positioned between both AD7609 devices and the reference voltage track runs north to Pin 42 of U1 and south to Pin 42 to U2. A solid ground plane is used. These symmetrical layout principles can be applied to a system that contains more than two AD7609 devices. The AD7609 devices can be placed in a north-to-south direction with the reference voltage located midway between the AD7609 devices and the reference track running in the north-to-south direction similar to Figure 62.

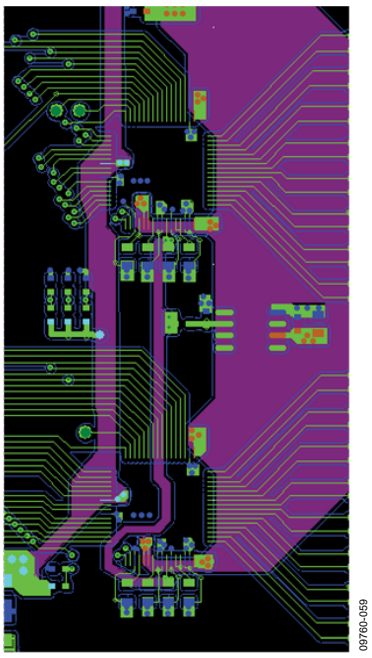


Figure 62. Multiple AD7609 Layout, Top Layer and Supply Plane Layer

OUTLINE DIMENSIONS

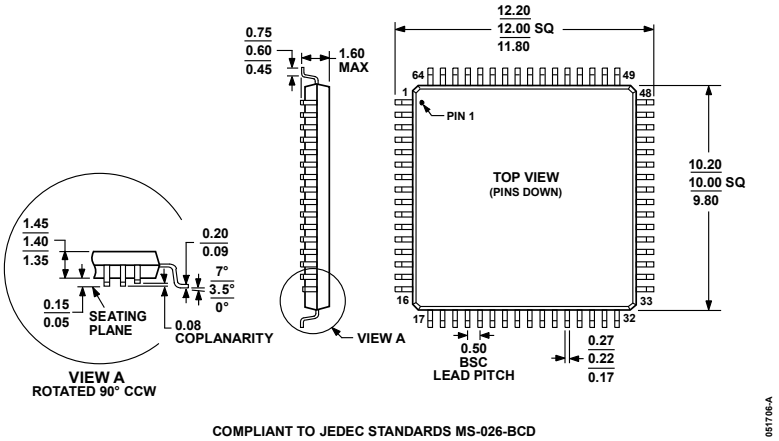


Figure 63. 64-Lead Low Profile Quad Flat Package [LQFP]
(ST-64-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD7609BSTZ	−40°C to +85°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
AD7609BSTZ-RL	−40°C to +85°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
EVAL-AD7609EDZ		Evaluation Board for the AD7609	
EVAL-CED1Z		Converter Evaluation Development	

[1] Z = RoHS Compliant Part.

NOTES

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D09760-0-8/19(D)