3.3 VOLT CMOS SyncFIFO™
512 x 36
1,024 x 36

IDT72V3631
IDT72V3641

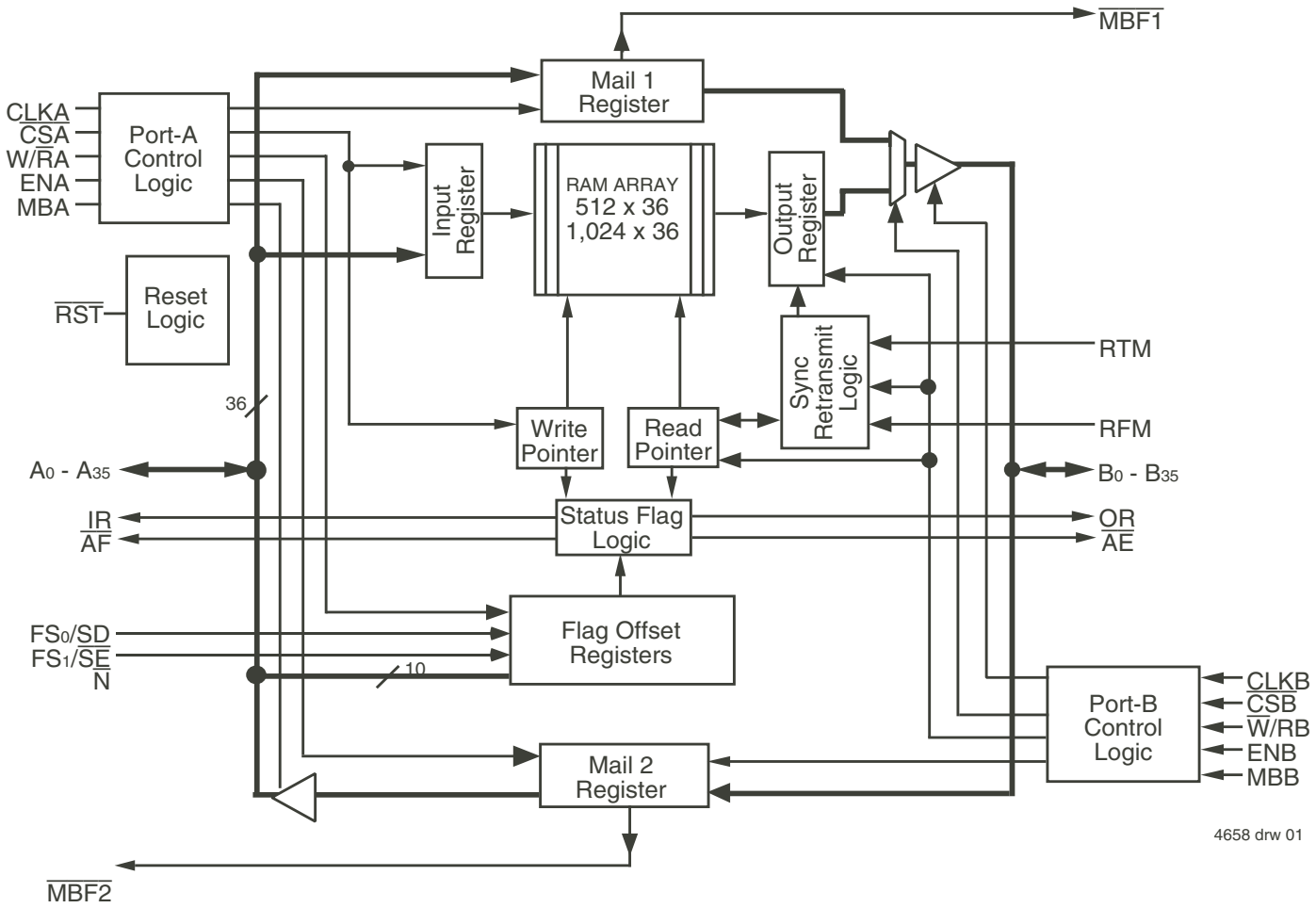
FEATURES

- Storage capacity:
  - IDT72V3631 - 512 x 36
  - IDT72V3641 - 1,024 x 36
- Supports clock frequencies up to 67 MHz
- Fast access times of 10ns
- Free-running CLKA and CLKB can be asynchronous or coincident (permits simultaneous reading and writing of data on a single clock edge)
- Clocked FIFO buffering data from Port A to Port B
- Synchronous read retransmit capability
- Mailbox register in each direction
- Programmable Almost-Full and Almost-Empty flags
- Microprocessor interface control logic
- Input Ready (IR) and Almost-Full ($\overline{AF}$) flags synchronized by CLKA
- Output Ready (OR) and Almost-Empty ($\overline{AE}$) flags synchronized by CLKB
- Available in space-saving 120-pin thin quad flat package (TQFP)
- Pin and functionally compatible versions of the 5V operating IDT723631/723641
- Easily expandable in width and depth
- Green parts are available, see ordering information

DESCRIPTION

The IDT72V3631/72V3641 are pin and functionally compatible versons of the IDT723631/723641, designed to run off a 3.3V supply for exceptionally low-power consumption. These devices are monolithic high-speed, low-power, CMOS clocked FIFO memory. It supports clock frequencies up to 67 MHz and has read access times as fast as 10ns. The 512/1,024 x 36 dual-port SRAM FIFO buffers data from port A to Port B. The FIFO memory has retransmit capability, which allows previously read data to be accessed again. The FIFO operates in First Word Fall Through mode and has flags to indicate empty and full conditions and conditions and two programmable flags (Almost-Full and Almost-Empty) to indicate when a selected number of words is stored in memory.

FUNCTIONAL BLOCK DIAGRAM



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DESCRIPTION (CONTINUED)

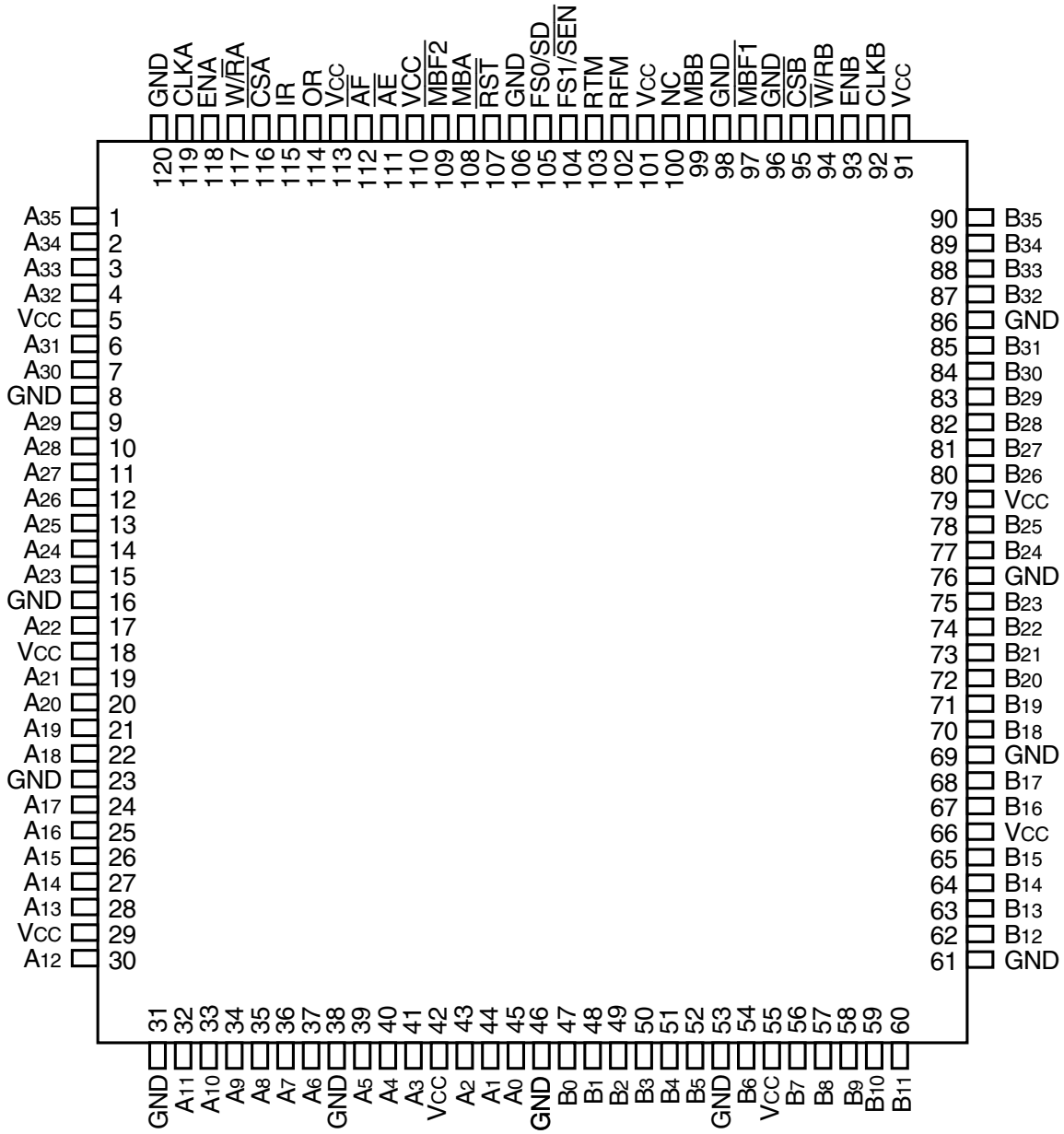
Communication between each port may take place with two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Two or more devices may be used in parallel to create wider data paths. Expansion is also possible in word depth.

These devices are a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the LOW-to-HIGH transition of a continuous (free-running) port clock by enable signals. The continuous clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple interface between microprocessors and/or buses with synchronous control.

The Input Ready (IR) flag and Almost-Full ($\overline{AF}$) flag of the FIFO are two-stage synchronized to CLKA. The Output Ready (OR) flag and Almost-Empty ($\overline{AE}$) flag of the FIFO are two-stage synchronized to CLKB. Offset values for the Almost-Full and Almost-Empty flags of the FIFO can be programmed from port A or through a serial input.

The IDT72V3631/72V3641 are characterized for operation from 0°C to 70°C. These devices are fabricated using high speed, submicron CMOS technology.

PIN CONFIGURATION



NOTE:
1. NC – No internal connection.

4658 drw 03

TQFP (PNG120, order code: PF)
TOP VIEW

PIN DESCRIPTION

Symbol	Name	I/O	Description
A0-A35	Port-A Data	I/O	36-bit bidirectional data port for side A.
$\overline{AE}$	Almost-Empty Flag	O	Programmable flag synchronized to CLKB. It is LOW when the number of words in the FIFO is less than or equal to the value in the Almost-Empty register (X).
$\overline{AF}$	Almost-Full Flag	O	Programmable flag synchronized to CLKA. It is LOW when the number of empty locations in the FIFO is less than or equal to the value in the Almost-Full Offset register (Y).
B0-B35	Port-B Data	I/O	36-bit bidirectional data port for side B.
CLKA	Port-A Clock	I	CLKA is a continuous clock that synchronizes all data transfers through port-A and may be asynchronous or coincident to CLKB. IR and $\overline{AF}$ are synchronous to the LOW-to-HIGH transition of CLKA.
CLKB	Port-B Clock	I	CLKB is a continuous clock that synchronizes all data transfers through port-B and may be asynchronous or coincident to CLKA. OR and $\overline{AE}$ are synchronous to the LOW-to-HIGH transition of CLKB.
$\overline{CSA}$	Port-A Chip	I	$\overline{CSA}$ must be LOW to enable a LOW-to-HIGH transition of CLKA to read or write data on port-A. The A0-A35 Select outputs are in the high-impedance state when $\overline{CSA}$ is HIGH.
$\overline{CSB}$	Port-B Chip	I	$\overline{CSB}$ must be LOW to enable a LOW-to-HIGH transition of CLKB to read or write data on port-B. The B0-B35 Select outputs are in the high-impedance state when $\overline{CSB}$ is HIGH.
ENA	Port-A Enable	I	ENA must be HIGH to enable a LOW-to-HIGH transition of CLKA to read or write data on port-A.
ENB	Port-B Enable	I	ENB must be HIGH to enable a LOW-to-HIGH transition of CLKB to read or write data on port-B.
FS1/ $\overline{SEN}$,	Flag-Offset Select 1/ Serial Enable	I	FS1/$\overline{SEN}$ and FS0/SD are dual-purpose inputs used for flag Offset register programming. During a device reset, FS1/$\overline{SEN}$ and FS0/SD selects the flag offset programming method. Three Offset register programming methods are available: automatically load one of two preset values, parallel load from port A, and serial load.
FS0/SD	Flag Offset 0/ Serial Data		When serial load is selected for flag Offset register programming, FS1/$\overline{SEN}$ is used as an enable synchronous to the LOW-to-HIGH transition of CLKA. When FS1/$\overline{SEN}$ is LOW, a rising edge on CLKA load the bit present on FS0/SD into the X and Y registers. The number of bit writes required to program the Offset registers is 18/20 for the IDT72V3631/72V3641 respectively. The first bit write stores the Y-register MSB and the last bit write stores the X-register LSB.
IR	Input Ready Flag	O	IR is synchronized to the LOW-to-HIGH transition of CLKA. When IR is LOW, the FIFO is full and writes to its array are disabled. When the FIFO is in retransmit mode, IR indicates when the memory has been filled to the point of the retransmit data and prevents further writes. IR is set LOW during reset and is set HIGH after reset.
MBA	Port-A Mailbox Select	I	A HIGH level chooses a mailbox register for a port-A read or write operation.
MBB	Port-B Mailbox Select	I	A HIGH level chooses a mailbox register for a port-B read or write operation. When the B0-B35 outputs are active, a HIGH level on MBB selects data from the mail1 register for output and a LOW level selects FIFO data for output.
$\overline{MBF1}$	Mail1 Register Flag	O	$\overline{MBF1}$ is set LOW by the LOW-to-HIGH transition of CLKA that writes data to the mail1 register. $\overline{MBF1}$ is set HIGH by a LOW-to-HIGH transition of CLKB when a port-B read is selected and MBB is HIGH. $\overline{MBF1}$ is set HIGH by a reset.
$\overline{MBF2}$	Mail2 Register Flag	O	$\overline{MBF2}$ is set LOW by the LOW-to-HIGH transition of CLKB that writes data to the mail2 register. $\overline{MBF2}$ is set HIGH by a LOW-to-HIGH transition of CLKA when a port-A read is selected and MBA is HIGH. $\overline{MBF2}$ is set HIGH by a reset.
OR	Output Ready Flag	O	OR is synchronized to the LOW-to-HIGH transition of CLKB. When OR is LOW, the FIFO is empty and reads are disabled. Ready data is present in the output register of the FIFO when OR is HIGH. OR is forced LOW during the reset and goes HIGH on the third LOW-to-HIGH transition of CLKB after a word is loaded to empty memory.
RFM	Read From Mark	I	When the FIFO is in retransmit mode, a HIGH on RFM enables a LOW-to-HIGH transition of CLKB to reset the read pointer to the beginning retransmit location and output the first selected retransmit data.
$\overline{RST}$	Reset	I	To reset the device, four LOW-to-HIGH transitions of CLKA and four LOW-to-HIGH transitions of CLKB must occur while $\overline{RST}$ is LOW. The LOW-to-HIGH transition of $\overline{RST}$ latches the status of FS0 and FS1 for $\overline{AF}$ and $\overline{AE}$ offset selection.
RTM	Retransmit Mode	I	When RTM is HIGH and valid data is present in the FIFO output register (OR is HIGH), a LOW-to-HIGH transition of CLKB selects the data for the beginning of a retransmit and puts the FIFO in retransmit mode. The selected word remains the initial retransmit point until a LOW- to-HIGH transition of CLKB occurs while RTM is LOW, taking the FIFO out of retransmit mode.
W/$\overline{RA}$	Port-A Write/ Read Select	I	A HIGH selects a write operation and a LOW selects a read operation on port A for a LOW-to-HIGH transition of CLKA. The A0-A35 outputs are in the high-impedance state when W/$\overline{RA}$ is HIGH.
$\overline{W}$/RB	Port-B Write/ Read Select	I	A LOW selects a write operation and a HIGH selects a read operation on port B for a LOW-to-HIGH transition of CLKB. The B0-B35 outputs are in the high-impedance state when $\overline{W}$/RB is LOW.

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (Unless otherwise noted)(2)

Symbol	Rating	Commercial	Unit
V_{CC}	Supply Voltage Range	–0.5 to +4.6	V
V_I(2)	Input Voltage Range	–0.5 to V_{CC}+0.5(3)	V
V_O(2)	Output Voltage Range	–0.5 to V_{CC}+0.5	V
I_{IK}	Input Clamp Current, (V_I < 0 or V_I > V_{CC})	±20	mA
I_{OK}	Output Clamp Current, (V_O = < 0 or V_O > V_{CC})	±50	mA
I_{OUT}	Continuous Output Current, (V_O = 0 to V_{CC})	±50	mA
I_{CC}	Continuous Current Through V_{CC} or GND	±400	mA
T_{STG}	Storage Temperature Range	–65 to 150	°C

NOTES:
1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.
3. Control Inputs: maximum V_I = 5.0V.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{IH}	HIGH Level Input Voltage	2	—	V_{CC}+0.5	V
V_{IL}	LOW-Level Input Voltage	—	—	0.8	V
I_{OH}	HIGH-Level Output Current	—	—	–4	mA
I_{OL}	LOW-Level Output Current	—	—	8	mA
T_A	Operating Free-air Temperature	0	—	70	°C

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (Unless otherwise noted)

Symbol	Parameter	Test Conditions		IDT72V3631 IDT72V3641 Commercial t_{CLK} = 15 ns Min.	Typ.(1)	Max.	Unit
V_{OH}	Output Logic "1" Voltage	V_{CC} = 3.0V,	I_{OH} = –4 mA	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage	V_{CC} = 3.0V,	I_{OL} = 8 mA	—	—	0.5	V
I_{LI}	Input Leakage Current (Any Input)	V_{CC} = 3.6V,	V_I = V_{CC} or 0	—	—	±5	µA
I_{LO}	Output Leakage Current	V_{CC} = 3.6V,	V_O = V_{CC} or 0	—	—	±5	µA
I_{CC2}(2)	Standby Current	V_{CC} = 3.6V,	V_I = V_{CC} –0.2V or 0	—	—	400	µA
C_{IN}	Input Capacitance	V_I = 0,	f = 1 MHz	—	4	—	pF
C_{OUT}	Output Capacitance	V_O = 0,	f = 1 MHZ	—	8	—	pF

NOTES:
1. All typical values are at V_{CC} = 3.3V, T_A = 25°C.
2. For additional I_{CC} information, see Figure 1, *Typical Characteristics: Supply Current (I_{CC}) vs. Clock Frequency (fs)*.

DETERMINING ACTIVE CURRENT CONSUMPTION AND POWER DISSIPATION

The $I_{CC}(f)$ current for the graph in Figure 1 was taken while simultaneously reading and writing the FIFO on the IDT72V3641 with CLKA and CLKB set to f_S. All data inputs and data outputs change state during each clock cycle to consume the highest supply current. Data outputs were disconnected to normalize the graph to a zero-capacitance load. Once the capacitance load per data-output channel and the number of IDT72V3631/72V3641 inputs driven by TTL HIGH levels are known, the power dissipation can be calculated with the equation below.

CALCULATING POWER DISSIPATION

With $I_{CC}(f)$ taken from Figure 1, the maximum power dissipation (P_T) of these FIFOs may be calculated by:

$$P_T = V_{CC} \times I_{CC(f)} + \sum_{N}(C_L \times V_{CC}^2 \times f_O)$$

where:

N = number of outputs = 36
C_L = output capacitance load
f_O = switching frequency of an output

When no reads or writes are occurring on these devices, the power dissipated by a single clock (CLKA or CLKB) input running at frequency f_S is calculated by:

$$P_T = V_{CC} \times f_S \times 0.025 \text{ mA/MHz}$$

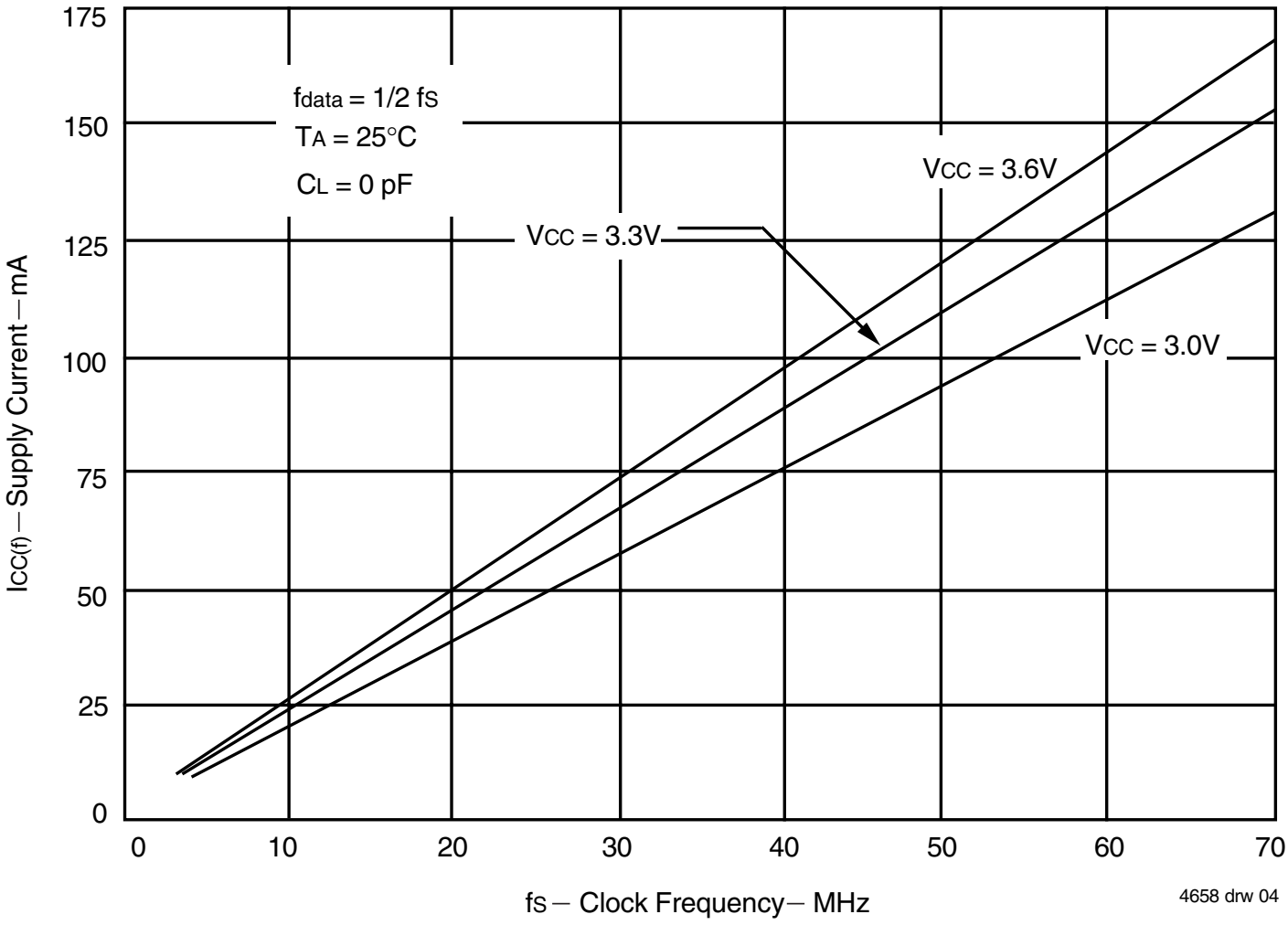


Figure 1. Typical Characteristics: Supply Current (I_{CC}) vs. Clock Frequency (f_S)

AC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE

Symbol	Parameter	IDT72V3631L15 IDT72V3641L15 Min.	Max.	Unit
f_S	Clock Frequency, CLKA or CLKB	–	66.7	MHz
t_{CLK}	Clock Cycle Time, CLKA or CLKB	15	–	ns
t_{CLKH}	Pulse Duration, CLKA or CLKB HIGH	6	–	ns
t_{CLKL}	Pulse Duration, CLKA or CLKB LOW	6	–	ns
t_{DS}	Setup Time, A0-A35 before CLKA↑ and B0-B35 before CLKB↑	5	–	ns
t_{ENS1}	Setup Time, ENA to CLKA↑; ENB to CLKB↑	5	–	ns
t_{ENS2}	Setup Time, $\overline{CSA}$, W/$\overline{RA}$, and MBA to CLKA↑; $\overline{CSB}$, $\overline{W}$/RB, and MBB to CLKB↑	7	–	ns
t_{RMS}	Setup Time, RTM and RFM to CLKB↑	6	–	ns
t_{RSTS}	Setup Time, $\overline{RST}$ LOW before CLKA↑ or CLKB↑[1]	5	–	ns
t_{FSS}	Setup Time, FS0 and FS1 before $\overline{RST}$ HIGH	9	–	ns
t_{SDS}[2]	Setup Time, FS0/SD before CLKA↑	5	–	ns
t_{SENS}[2]	Setup Time, FS1/$\overline{SEN}$ before CLKA↑	5	–	ns
t_{DH}	Hold Time, A0-A35 after CLKA↑ and B0-B35 after CLKB↑	0.5	–	ns
t_{ENH1}	Hold Time, ENA after CLKA↑; ENB after CLKB↑	0.5	–	ns
t_{ENH2}	Hold Time, $\overline{CSA}$, W/$\overline{RA}$, and MBA after CLKA↑; $\overline{CSB}$, $\overline{W}$/RB, and MBB after CLKB↑	0.5	–	ns
t_{RMH}	Hold Time, RTM and RFM after CLKB↑	0.5	–	ns
t_{RSTH}	Hold Time, $\overline{RST}$ LOW after CLKA↑ or CLKB↑[1]	5	–	ns
t_{FSH}	Hold Time, FS0 and FS1 after $\overline{RST}$ HIGH	0	–	ns
t_{SPH}[2]	Hold Time, FS1/$\overline{SEN}$ HIGH after $\overline{RST}$ HIGH	0	–	ns
t_{SDH}[2]	Hold Time, FS0/SD after CLKA↑	0	–	ns
t_{SENH}[2]	Hold Time, FS1/$\overline{SEN}$ after CLKA↑	0	–	ns
t_{SKEW1}[3]	Skew Time, between CLKA↑ and CLKB↑ for OR and IR	9	–	ns
t_{SKEW2}[3,4]	Skew Time, between CLKA↑ and CLKB↑ for $\overline{AE}$ and $\overline{AF}$	12	–	ns

NOTES:
1. Requirement to count the clock edge as one of at least four needed to reset a FIFO.
2. Only applies when serial load method is used to program flag Offset registers.
3. Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle.
4. Design simulated, not tested.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	IDT72V3631L15 IDT72V3641L15 Min.	Max.	Unit
f_S	Clock Frequency, CLKA or CLKB	–	66.7	MHz
t_A	Access Time, CLKB↑ to B0-B35	2	10	ns
t_{PIR}	Propagation Delay Time, CLKA↑ to IR	1	8	ns
t_{POR}	Propagation Delay Time, CLKB↑ to OR	1	8	ns
t_{PAE}	Propagation Delay Time, CLKB↑ to $\overline{AE}$	1	8	ns
t_{PAF}	Propagation Delay Time, CLKA↑ to $\overline{AF}$	1	8	ns
t_{PMF}	Propagation Delay Time, CLKA↑ to $\overline{MBF1}$ LOW or $\overline{MBF2}$ HIGH and CLKB↑ to $\overline{MBF2}$ LOW or $\overline{MBF1}$ HIGH	0	8	ns
t_{PMR}	Propagation Delay Time, CLKA↑ to B0-B35[1] and CLKB↑ to A0-A35[2]	2	10	ns
t_{MDV}	Propagation Delay Time, MBB to B0-B35 Valid	2	10	ns
t_{RSF}	Propagation Delay Time, $\overline{RST}$ LOW to $\overline{AE}$ LOW and $\overline{AF}$ HIGH	1	15	ns
t_{EN}	Enable Time, $\overline{CSA}$ and W/$\overline{R}$A LOW to A0-A35 Active and $\overline{CSB}$ LOW and $\overline{W}$/RB HIGH to B0-B35 Active	2	10	ns
t_{DIS}	Disable Time, $\overline{CSA}$ or W/$\overline{R}$A HIGH to A0-A35 at high impedance and $\overline{CSB}$ HIGH or $\overline{W}$/RB LOW to B0-B35 at high impedance	1	8	ns

NOTES:
1. Writing data to the mail1 register when the B0-B35 outputs are active and MBB is HIGH.
2. Writing data to the mail2 register when the A0-A35 outputs are active and MBA is HIGH.

SIGNAL DESCRIPTION

RESET

The IDT72V3631/72V3641 is reset by taking the Reset ($\overline{RST}$) input LOW for at least four port-A Clock (CLKA) and four port-B (CLKB) LOW-to-HIGH transitions. The Reset input may switch asynchronously to the clocks. A reset initializes the memory read and write pointers and forces the Input Ready (IR) flag LOW, the Output Ready (OR) flag LOW, the Almost-Empty ($\overline{AE}$) flag LOW, and the Almost-Full ($\overline{AF}$) flag HIGH. Resetting the device also forces the Mailbox Flags ($\overline{MBF1}$, $\overline{MBF2}$) HIGH. After a FIFO is reset, its Input Ready flag is set HIGH after at least two clock cycles to begin normal operation. A FIFO must be reset after power up before data is written to its memory. The relevant FIFO Reset timing diagram can be found in Figure 2.

FIRST WORD FALL THROUGH MODE (FWFT)

These devices operate in the First Word Fall Through mode (FWFT). This mode uses the Output Ready function (OR) to indicate whether or not there is valid data at the data outputs (B0-B35). It also uses the Input Ready (IR) function to indicate whether or not the FIFO memory has any free space for writing. In the FWFT mode, the first word written to an empty FIFO goes directly to data outputs, no read request necessary. Subsequent words must be accessed by performing a formal read operation.

ALMOST-EMPTY FLAG AND ALMOST-FULL FLAG OFFSET PROGRAMMING

Two registers in these devices are used to hold the offset values for the Almost-Empty and Almost-Full flags. The Almost-Empty ($\overline{AE}$) flag Offset register is labeled X, and the Almost-Full ($\overline{AF}$) flag Offset register is labeled Y. The Offset register can be loaded with a value in three ways: one of two preset values are loaded into the Offset registers, parallel load from port A, or serial load. The Offset register programming mode is chosen by the flag select (FS1, FS0) inputs during a LOW-to-HIGH transition on the $\overline{RST}$ input (See Table 1).

— PRESET VALUES

If the preset value of 8 or 64 is chosen by the FS1 and FS0 inputs at the time of a $\overline{RST}$ LOW-to-HIGH transition according to Table 1, the preset value is automatically loaded into the X and Y registers. No other device initialization is necessary to begin normal operation, and the IR flag is set HIGH after two LOW-to-HIGH transitions on CLKA. For the Preset value loading timing diagram, see Figure 2.

— PARALLEL LOAD FROM PORT A

To program the X and Y registers from port A, the device is reset with FS0 and FS1 LOW during the LOW-to-HIGH transition of $\overline{RST}$. After this reset is complete, the IR flag is set HIGH after two LOW-to-HIGH transitions on CLKA. The first two writes to the FIFO do not store data in its memory but load the Offset registers in the order Y, X. Each Offset register of the IDT72V3631 and IDT72V3641 uses port-A inputs (A8-A0), (A9-A0), and (A10-A0), respectively. The highest number input is used as the most significant bit of the binary number in each case. Each register value can be programmed from 1 to 508 (IDT72V3631) and 1 to 1,020 (IDT72V3641). After both Offset registers are programmed from port A, subsequent FIFO writes store data in the RAM. The timing diagram for parallel load of offset registers can be found in Figure 3.

— SERIAL LOAD

To program the X and Y registers serially, the device is reset with FS0/SD and FS1/$\overline{SEN}$ HIGH during the LOW-to-HIGH transition of $\overline{RST}$. After this reset is complete, the X and Y register values are loaded bitwise through the FS0/SD input on each LOW-to-HIGH transition of CLKA that the FS1/$\overline{SEN}$ input is LOW. There are 18- or 20-bit writes needed to complete the programming for the IDT72V3631 or IDT72V3641 respectively. The first-bit write stores the most significant bit of the Y register, and the last-bit write stores the least significant bit of the X register. Each register value can be programmed from 1 to 508 (IDT72V3631) or 1 to 1,020 (IDT72V3641).

When the option to program the Offset registers serially is chosen, the Input Ready (IR) flag remains LOW until all register bits are written. The IR flag is set HIGH by the LOW-to-HIGH transition of CLKA after the last bit is loaded to allow normal FIFO operation. The timing diagram for serial load of offset registers can be found in Figure 4.

FIFO WRITE/READ OPERATION

The state of the port-A data (A0-A35) outputs is controlled by the port-A Chip Select ($\overline{CSA}$) and the port-A Write/Read select (W/$\overline{RA}$). The A0-A35 outputs are in the high-impedance state when either $\overline{CSA}$ or W/$\overline{RA}$ is HIGH. The A0-A35 outputs are active when both $\overline{CSA}$ and W/$\overline{RA}$ are LOW.

Data is loaded into the FIFO from the A0-A35 inputs on a LOW-to-HIGH transition of CLKA when $\overline{CSA}$ and the port-A Mailbox select (MBA) are LOW, W/$\overline{RA}$, the port-A Enable (ENA), and the Input Ready (IR) flag are HIGH (see Table 2). Writes to the FIFO are independent of any concurrent FIFO read. For the *Write Cycle Timing* diagram, see Figure 5.

The port-B control signals are identical to those of port-A with the exception that the port-B Write/Read select ($\overline{W}$/RB) is the inverse of the port-A Write/Read select (W/$\overline{RA}$). The state of the port-B data (B0-B35) outputs is controlled by the port-B Chip Select ($\overline{CSB}$) and the port-B Write/Read select ($\overline{W}$/RB). The B0-B35 outputs are in the high-impedance state when either $\overline{CSB}$ is HIGH or $\overline{W}$/RB is LOW. The B0-B35 outputs are active when $\overline{CSB}$ is LOW and $\overline{W}$/RB is HIGH.

Data is read from the FIFO to its output register on a LOW-to-HIGH transition of CLKB when $\overline{CSB}$ and the port-B Mailbox select (MBB) are LOW, $\overline{W}$/RB, the port-B Enable (ENB), and the Output Ready (OR) flag are HIGH (see Table 3). Reads from the FIFO are independent of any concurrent FIFO writes. For the *Read Cycle Timing* diagram, see Figure 6.

The setup- and hold-time constraints to the port clocks for the port Chip Selects and Write/Read selects are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port Enable is LOW during a clock cycle, the port Chip Select and Write/Read select may change states during the setup- and hold time window of the cycle.

When the OR flag is LOW, the next data word is sent to the FIFO output register automatically by the CLKB LOW-to-HIGH transition that sets the OR flag HIGH. When OR is HIGH, an available data word is clocked to the FIFO output register only when a FIFO read is selected by the port-B Chip Select ($\overline{CSB}$), Write/Read select ($\overline{W}$/RB), Enable (ENB), and Mailbox select (MBB).

TABLE 1 — FLAG PROGRAMMING

FS1	FS0	$\overline{RST}$	X and Y Registers (1)
H	H	↑	Serial Load
H	L	↑	64
L	H	↑	8
L	L	↑	Parallel Load From Port A

NOTE:
1. X register holds the offset for $\overline{AE}$; Y register holds the offset for $\overline{AF}$.

SYNCHRONIZED FIFO FLAGS

Each IDT72V3631/72V3641 FIFO flag is synchronized to its port Clock through at least two flip-flop stages. This is done to improve the flags' reliability by reducing the probability of metastable events on their outputs when CLKA and CLKB operate asynchronously to one another. OR and $\overline{AE}$ are synchronized to CLKB. IR and $\overline{AF}$ are synchronized to CLKA. Table 4 shows the relationship of each flag to the number of words stored in memory.

OUTPUT READY FLAG (OR)

The Output Ready flag of a FIFO is synchronized to the port Clock that reads data from its array (CLKB). When the OR flag is HIGH, new data is present in the FIFO output register. When the OR flag is LOW, the previous data word is present in the FIFO output register and attempted FIFO reads are ignored.

A FIFO read pointer is incremented each time a new word is clocked to its output register. The state machine that controls an OR flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO memory status is empty, empty+1, or empty+2. From the time a word is written to a FIFO, it can be shifted to the FIFO output register in a minimum of three cycles of CLKB. Therefore, an OR flag is LOW if a word in memory is the next data to be sent to the FIFO output register and three CLKB cycles have not elapsed since the time the word was written. The OR flag of the FIFO remains LOW until the third LOW-to-HIGH transition of CLKB occurs, simultaneously forcing the OR flag HIGH and shifting the word to the FIFO output register.

A LOW-to-HIGH transition on CLKB begins the first synchronization cycle of a write if the clock transition occurs at time t_{SKEW1} or greater after the write. Otherwise, the subsequent CLKB cycle may be the first synchronization cycle (see Figure 7).

INPUT READY FLAG (IR)

The Input Ready flag of a FIFO is synchronized to the port Clock that writes data to its array (CLKA). When the IR flag is HIGH, a memory location is free in the FIFO to write new data. No memory locations are free when the IR flag is LOW and attempted writes to the FIFO are ignored.

Each time a word is written to a FIFO, its write pointer is incremented. The state machine that controls an IR flag monitors a write-pointer and read pointer comparator that indicates when the FIFO memory status is full, full-1, or full-2. From the time a word is read from a FIFO, its previous memory location is ready to be written in a minimum of three cycles of CLKA. Therefore, an IR flag is LOW if less than two cycles of CLKA have elapsed since the next memory write location has been read. The second LOW-to-HIGH transition on CLKA after the read sets the Input Ready flag HIGH, and data can be written in the following cycle.

A LOW-to-HIGH transition on CLKA begins the first synchronization cycle of a read if the clock transition occurs at time t_{SKEW1} or greater after the read. Otherwise, the subsequent CLKA cycle may be the first synchronization cycle (see Figure 8).

ALMOST-EMPTY FLAG ($\overline{AE}$)

The Almost-Empty flag of a FIFO is synchronized to the port Clock that reads data from its array (CLKB). The state machine that controls an $\overline{AE}$ flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO memory status is almost-empty, almost-empty+1, or almost-empty+2. The almost-empty state is defined by the contents of register X. This register is loaded with a preset value during a FIFO reset, programmed from port A, or programmed serially (see Almost-Empty flag and Almost-Full flag offset pro-

TABLE 2 — PORT-A ENABLE FUNCTION TABLE

$\overline{CSA}$	W/$\overline{RA}$	ENA	MBA	CLKA	Data A (A0-A35) I/O	Port Functions
H	X	X	X	X	Input	None
L	H	L	X	X	Input	None
L	H	H	L	↑	Input	FIFO Write
L	H	H	H	↑	Input	Mail1 Write
L	L	L	L	X	Output	None
L	L	H	L	↑	Output	None
L	L	L	H	X	Output	None
L	L	H	H	↑	Output	Mail2 Read (Set $\overline{MBF2}$ HIGH)

TABLE 3 — PORT-B ENABLE FUNCTION TABLE

$\overline{CSB}$	$\overline{W}$/RB	ENB	MBB	CLKB	Data B (B0-A35) I/O	Port Functions
H	X	X	X	X	Input	None
L	L	L	X	X	Input	None
L	L	H	L	↑	Input	None
L	L	H	H	↑	Input	Mail2 Write
L	H	L	L	X	Output	None
L	H	H	L	↑	Output	FIFO read
L	H	L	H	X	Output	None
L	H	H	H	↑	Output	Mail1 Read (Set $\overline{MBF1}$ HIGH)

gramming section). The $\overline{AE}$ flag is LOW when the FIFO contains X or less words and is HIGH when the FIFO contains (X+1) or more words. A data word present in the FIFO output register has been read from memory.

Two LOW-to-HIGH transitions of CLKB are required after a FIFO write for the $\overline{AE}$ flag to reflect the new level of fill; therefore, the $\overline{AE}$ flag of a FIFO containing (X+1) or more words remains LOW if two cycles of CLKB have not elapsed since the write that filled the memory to the (X+1) level. An $\overline{AE}$ flag is set HIGH by the second LOW-to-HIGH transition of CLKB after the FIFO write that fills memory to the (X+1) level. A LOW-to-HIGH transition of CLKB begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the write that fills the FIFO to (X+1) words. Otherwise, the subsequent CLKB cycle may be the first synchronization cycle (see Figure 9).

ALMOST-FULL FLAG ($\overline{AF}$)

The Almost-Full flag of a FIFO is synchronized to the port Clock that writes data to its array (CLKA). The state machine that controls an $\overline{AF}$ flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO memory status is almost-full, almost-full-1, or almost-full-2. The almost-full state is defined by the contents of register Y. This register is loaded with a preset value during a FIFO reset, programmed from port A, or programmed serially (see Almost-Empty flag and Almost-Full flag offset programming section). The $\overline{AF}$ flag is LOW when the number of words in the FIFO is greater than or equal to (512-Y) or (1,024-Y) for the IDT72V3631 or IDT72V3641 respectively. The $\overline{AF}$ flag is HIGH when the number of words in the FIFO is less than or equal to [512-(Y+1)] or [1,024-(Y+1)] for the IDT72V3631 or IDT72V3641 respectively. A data word present in the FIFO output register has been read from memory.

Two LOW-to-HIGH transitions of CLKA are required after a FIFO read for its $\overline{AF}$ flag to reflect the new level of fill. Therefore, the $\overline{AF}$ flag of a FIFO containing [512/1,024-(Y+1)] or less words remains LOW if two cycles of CLKA have not elapsed since the read that reduced the number of words in memory to [512/1,024-(Y+1)]. An $\overline{AF}$ flag is set HIGH by the second LOW-to-HIGH transition of CLKA after the FIFO read that reduces the number of words in memory to [512/1,024-(Y+1)]. A LOW-to-HIGH transition of CLKA begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the read that reduces the number of words in memory to [512/1,024-(Y+1)]. Otherwise, the subsequent CLKA cycle may be the first synchronization cycle (see Figure 10).

SYNCHRONOUS RETRANSMIT

The synchronous retransmit feature of these devices allow FIFO data to be read repeatedly starting at a user-selected position. The FIFO is first put into retransmit mode to select a beginning word and prevent ongoing FIFO write operations from destroying retransmit data. Data vectors with a minimum length of three words can retransmit repeatedly starting at the selected word. The FIFO can be taken out of retransmit mode at any time and allow normal device operation.

The FIFO is put in retransmit mode by a LOW-to-HIGH transition on CLKB when the retransmit mode (RTM) input is HIGH and OR is HIGH. The rising CLKB edge marks the data present in the FIFO output register as the first retransmit data. The FIFO remains in retransmit mode until a LOW-to-HIGH transition occurs while RTM is LOW.

When two or more reads have been done past the initial marked retransmit word, a retransmit is initiated by a LOW-to-HIGH transition on CLKB when the read-from-mark (RFM) input is HIGH. This rising CLKB edge shifts the first retransmit word to the FIFO output register and subsequent reads can begin immediately. Retransmit loops can be done endlessly while the FIFO is in retransmit mode. RFM must be LOW during the CLKB rising edge that takes the FIFO out of retransmit mode (see Figure 11).

When the FIFO is put into retransmit mode, it operates with two read pointers. The current read pointer operates normally, incrementing each time when a new word is shifted to the FIFO output register. This read pointer position is used by the OR and $\overline{AE}$ flags. The shadow read pointer stores the memory location at the time the device is put into retransmit mode and does not change until the device is taken out of retransmit mode. The shadow read pointer position is used by the IR and $\overline{AF}$ flags. Data writes can proceed while the FIFO is in retransmit mode, but $\overline{AF}$ is set LOW by the write that stores (512-Y) or (1,024-Y) words after the first retransmit word for the IDT72V3631 or IDT72V3641 respectively. The IR flag is set LOW by the 512th or 1,024th write after the first retransmit word for the IDT72V3631 or IDT72V3641 respectively.

When the FIFO is in retransmit mode and RFM is HIGH, a rising CLKB edge loads the current read pointer with the shadow read-pointer value and the OR flag reflects the new level of fill immediately. If the retransmit changes the FIFO status out of the almost-empty range, up to two CLKB rising edges after the retransmit cycle are needed to switch $\overline{AE}$ high (see Figure 12). The rising CLKB edge that takes the FIFO out of retransmit mode shifts the read pointer used by

TABLE 4 — FIFO FLAG OPERATION

Number of Words in the FIFO[1,2]		Synchronized to CLKB		Synchronized to CLKA	
IDT72V3631[3]	IDT72V3641[3]	OR	$\overline{AE}$	$\overline{AF}$	IR
0	0	L	L	H	H
1 to X	1 to X	H	L	H	H
(X+1) to [512-(Y+1)]	(X+1) to [1,024-(Y+1)]	H	H	H	H
(512-Y) to 511	(1,024-Y) to 1,023	H	H	L	H
512	1,024	H	H	L	L

NOTES:
1. When a word is present in the FIFO output register, its previous memory location is free.
2. Data in the output register does not count as a "word i n FIFO memory". Since in FWFT mode, the first words written to an empty FIFO goes unrequested to the output register (no read operation necessary), it is not included in the memory count.
3. X is the Almost-Empty Offset for $\overline{AE}$. Y is the Almost-Full Offset for $\overline{AF}$.

the IR and $\overline{AF}$ flags from the shadow to the current read pointer. If the change of read pointer used by IR and $\overline{AF}$ should cause one or both flags to transmit HIGH, at least two CLKA synchronizing cycles are needed before the flags reflect the change. A rising CLKA edge after the FIFO is taken out of retransmit mode is the first synchronizing cycle of IR if it occurs at time t_{SKEW1} or greater after the rising CLKB edge (see Figure 13). A rising CLKA edge after the FIFO is taken out of retransmit mode is the first synchronizing cycle of $\overline{AF}$ if it occurs at time t_{SKEW2} or greater after the rising CLKB edge (see Figure 14).

MAILBOX REGISTERS

Two 36-bit bypass registers are on the IDT72V3631/72V3641 to pass command and control information between port A and port B. The Mailbox select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data transfer operation. A LOW-to-HIGH transition on CLKA writes A0-A35 data to the mail1 register when a port-A Write is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA with MBA HIGH. A LOW-to-HIGH transition on CLKB writes B0-B35 data to the mail2 register when a port-B Write is selected by $\overline{CSB}$, $\overline{W}$/RB, and ENB with MBB HIGH. Writing data to a mail register sets its corresponding flag ($\overline{MBF1}$ or $\overline{MBF2}$) LOW. Attempted writes to a mail register are ignored while its mail flag is LOW.

When the port-B data (B0-B35) outputs are active, the data on the bus comes from the FIFO output register when the port-B Mailbox select (MBB) input is LOW and from the Mail1 register when MBB is HIGH. Mail2 data is always present on the port-A data (A0-A35) outputs when they are active. The Mail1 register Flag ($\overline{MBF1}$) is set HIGH by a LOW-to-HIGH transition on CLKB when a port-B Read is selected by $\overline{CSB}$, $\overline{W}$/RB, and ENB with MBB HIGH. The Mail2 register Flag (MBF2) is set HIGH by a LOW-to-HIGH transition on CLKA when a port-A Read is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA with MBA HIGH. The data in a mail register remains intact after it is read and changes only when new data is written to the register. Mail Register and Mail Register Flag timing can be found in Figure 15 and 16.

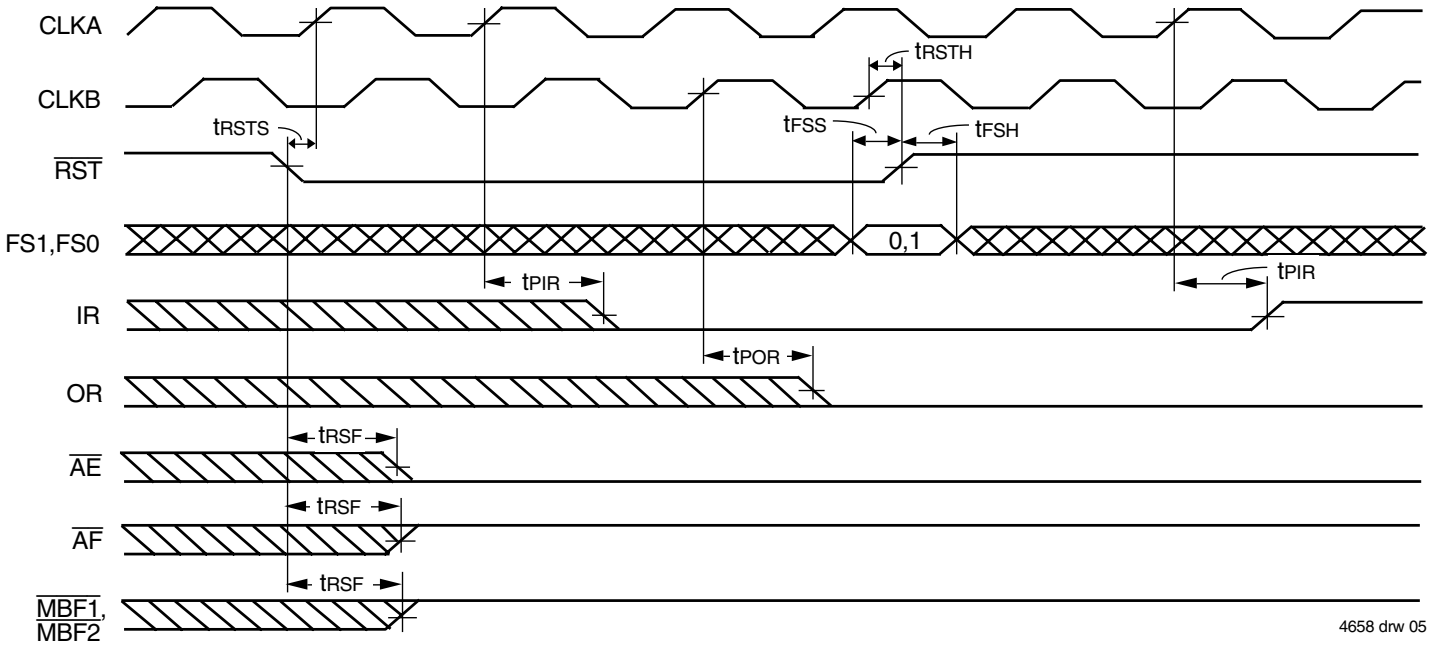
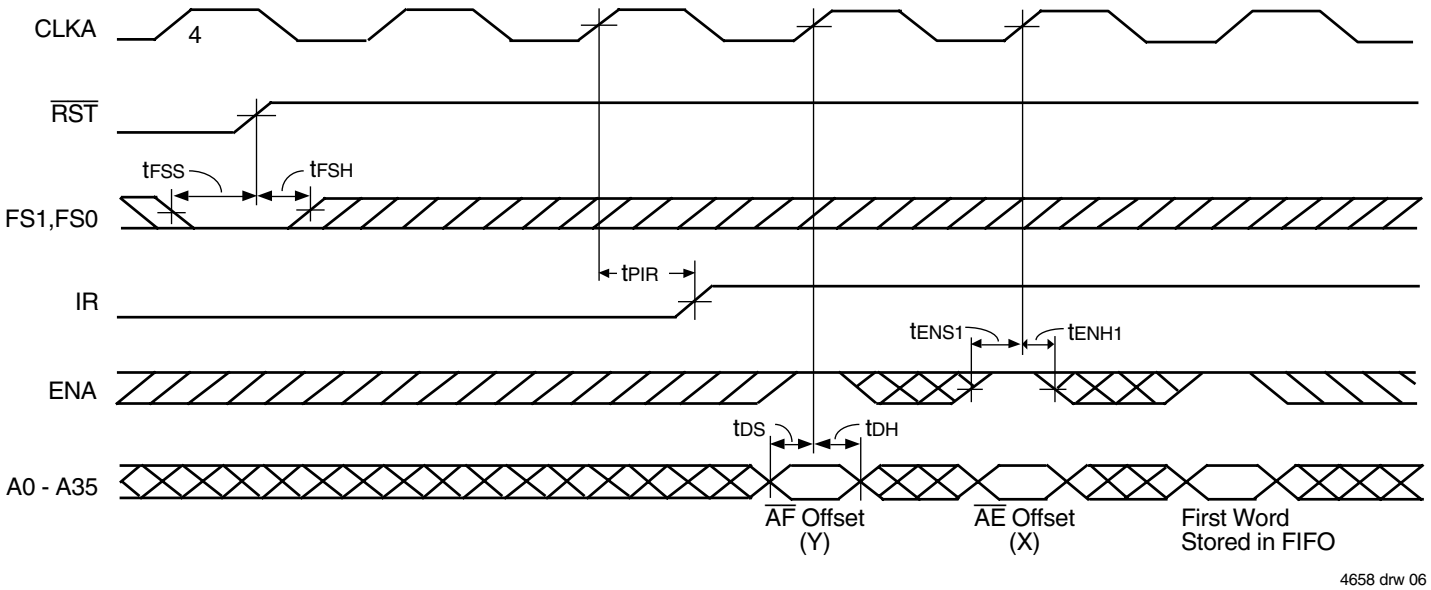
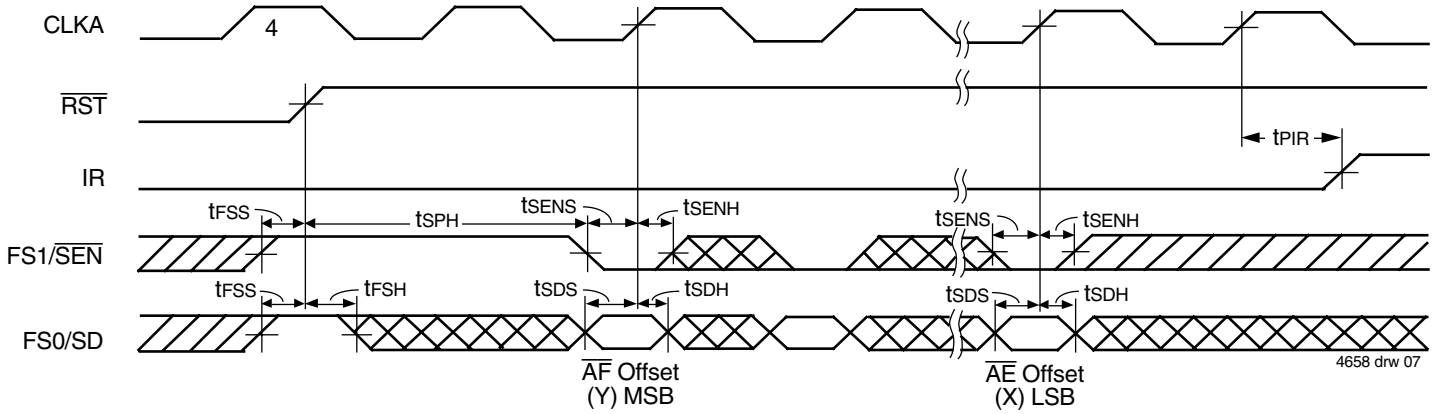


Figure 2. FIFO Reset and Loading X and Y with a Preset Value of Eight



NOTE:
1. $\overline{CSA}$ = LOW, W/$\overline{RA}$ = HIGH, MBA = LOW. It is not necessary to program Offset register on consecutive clock cycles.

Figure 3. Programming the Almost-Full Flag and Almost-Empty Flag Offset Values from Port A



NOTE:
1. It is not necessary to program Offset register bits on consecutive clock cycles. FIFO write attempts are ignored until IR is set HIGH.

Figure 4. Programming the Almost-Full Flag and Almost-Empty Flag Offset Values Serially

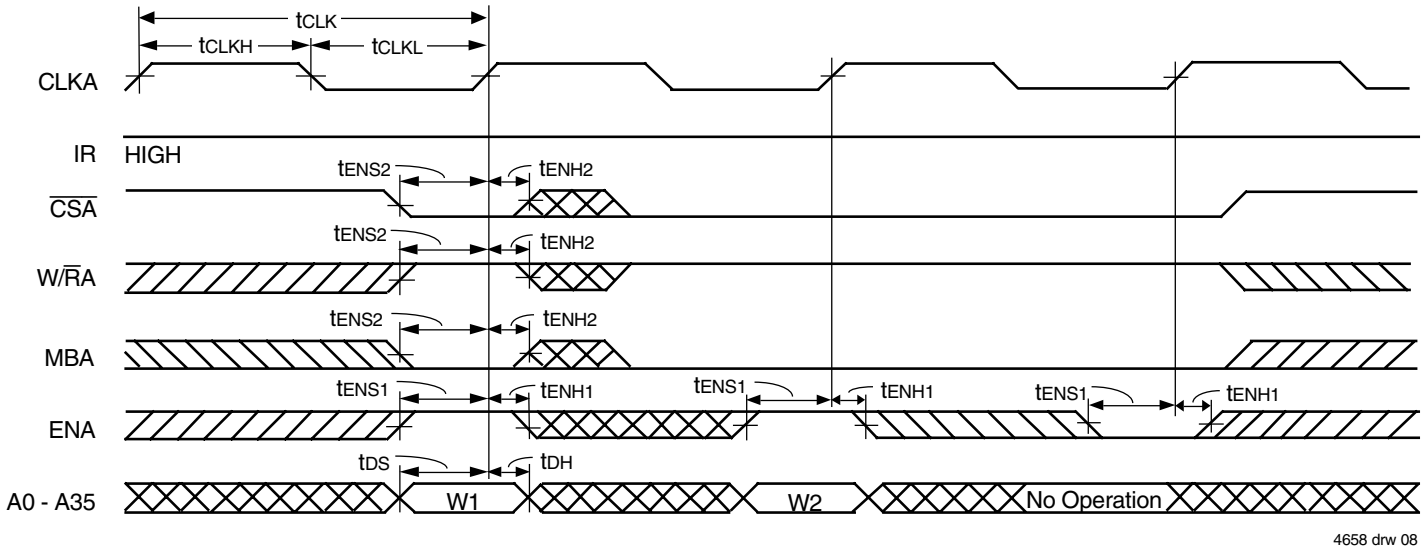


Figure 5. FIFO Write Cycle Timing

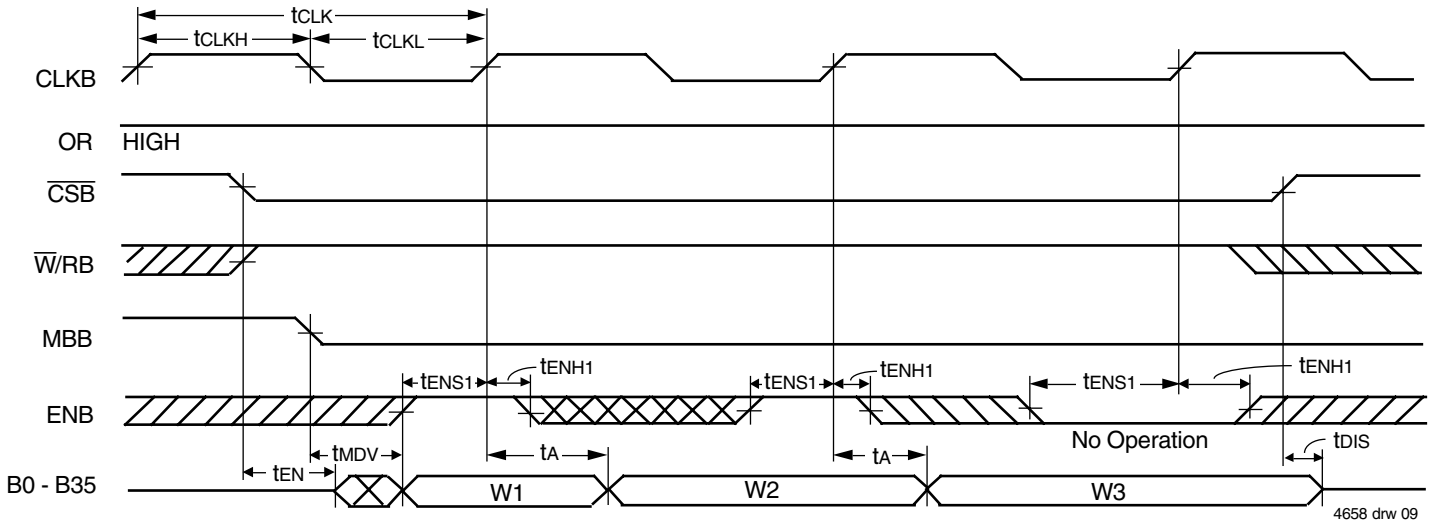
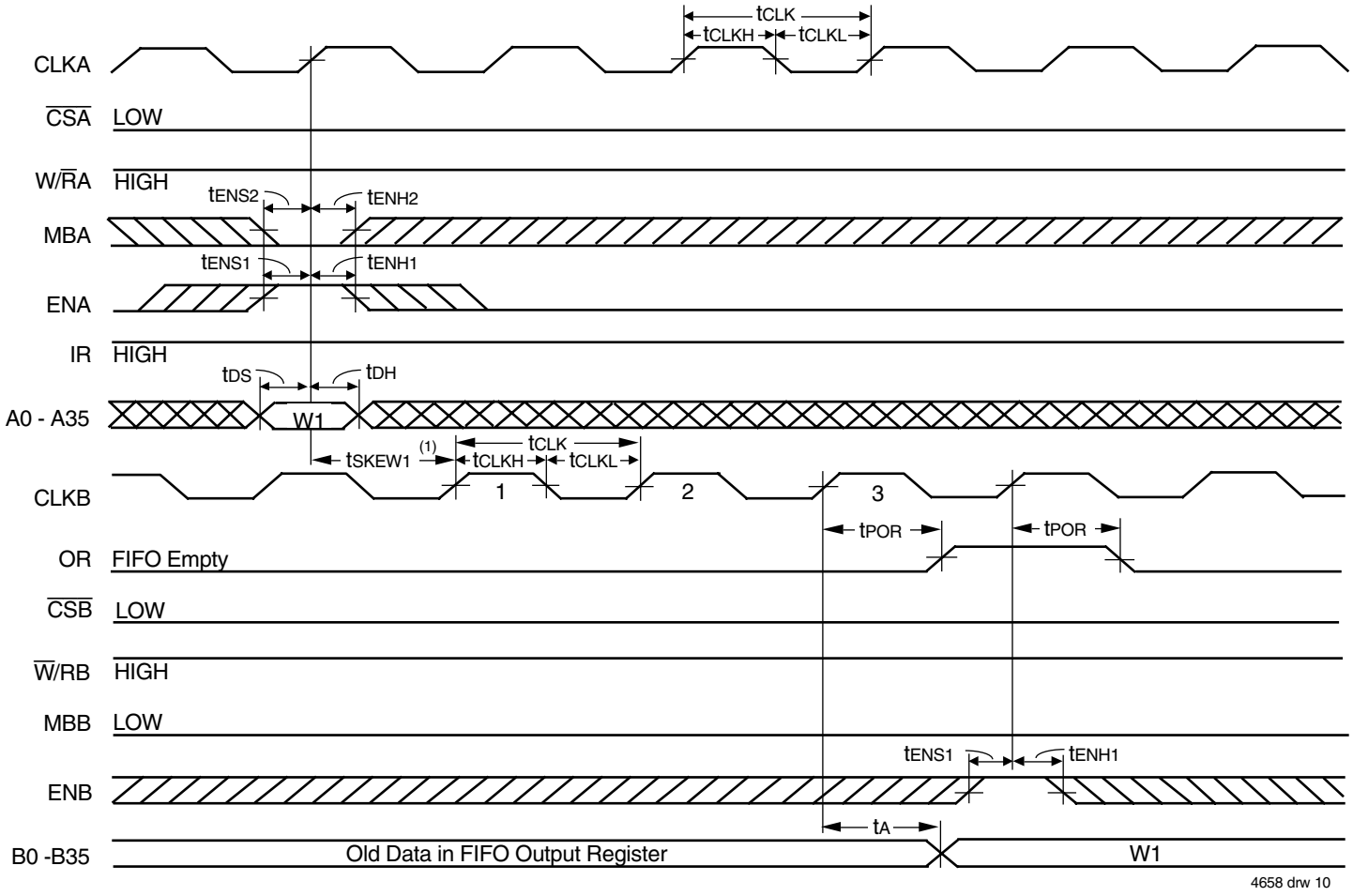


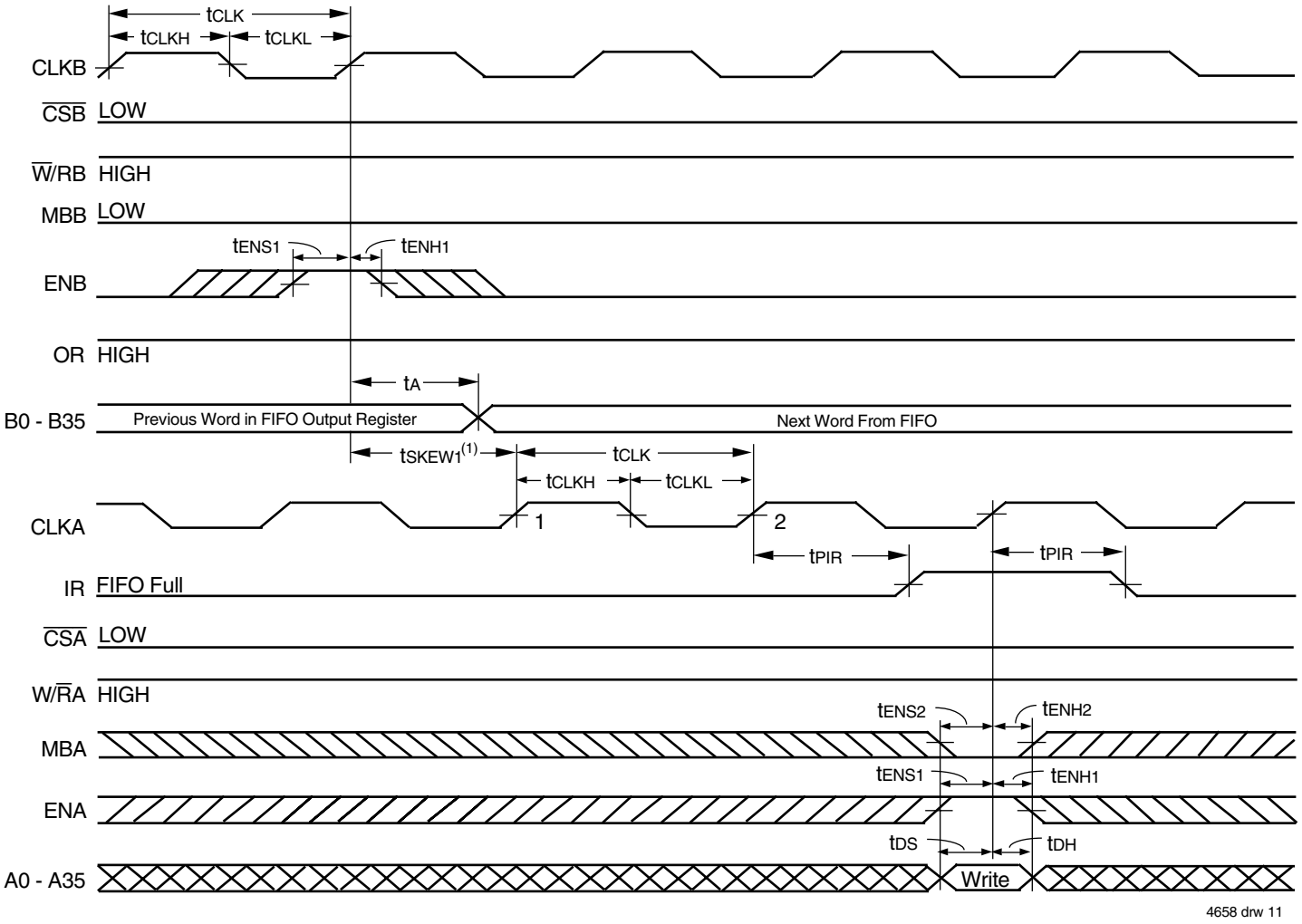
Figure 6. FIFO Read Cycle Timing



NOTE:

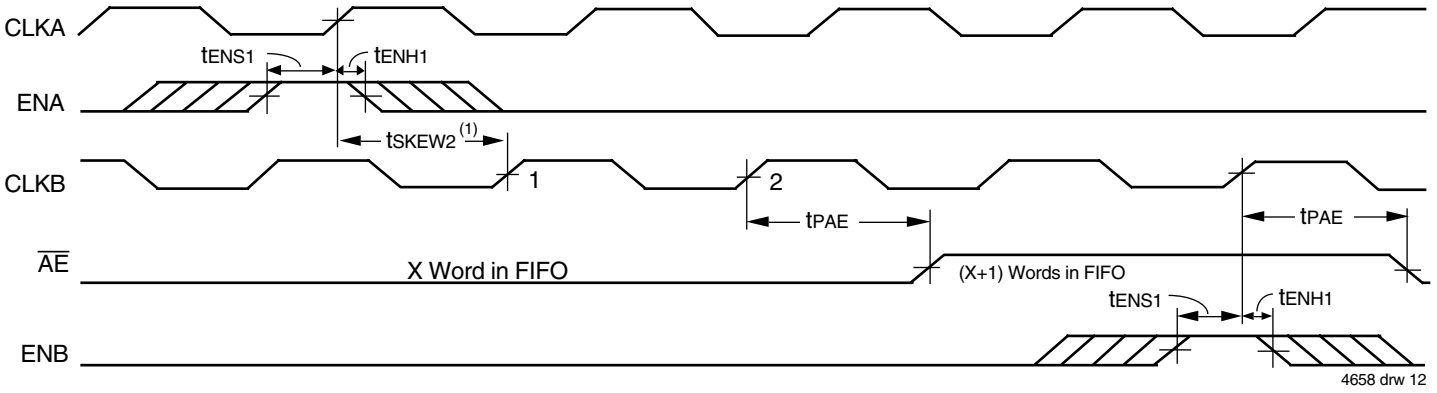
1. t_{SKEW1} is the minimum time between a rising CLKA edge and a rising CLKB edge for OR to transition HIGH and to clock the next word to the FIFO output register in three CLKB cycles. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW1}, then the transition of OR HIGH and the first word load to the output register may occur one CLKB cycle later than shown.

Figure 7. OR Flag Timing and First Data Word Fall Through when the FIFO is Empty



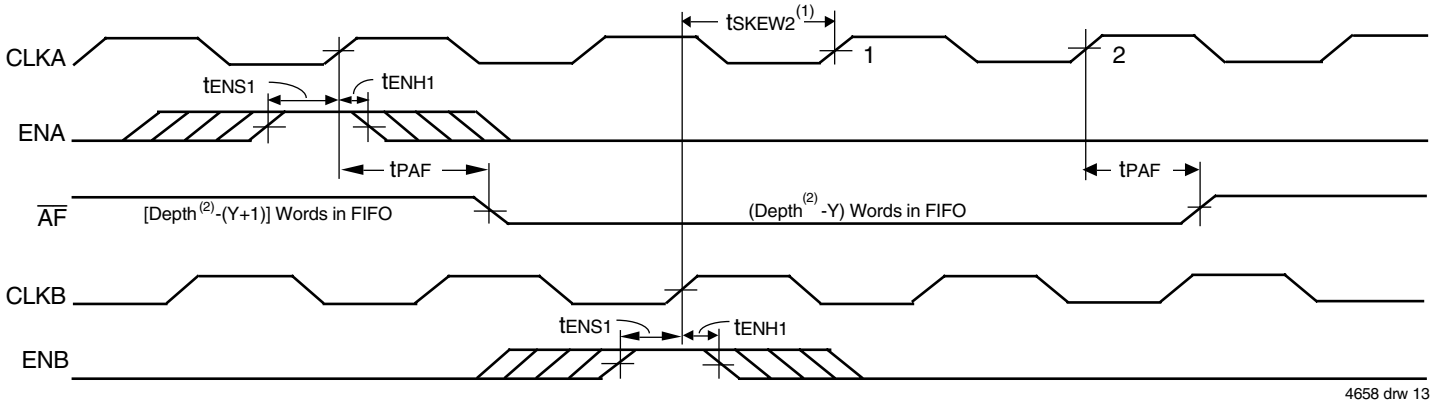
NOTE:
1. t_{SKEW1} is the minimum time between a rising CLKB edge and a rising CLKA edge for IR to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW1}, then IR may transition HIGH one CLKA cycle later than shown.

Figure 8. IR Flag Timing and First Available Write when the FIFO is Full



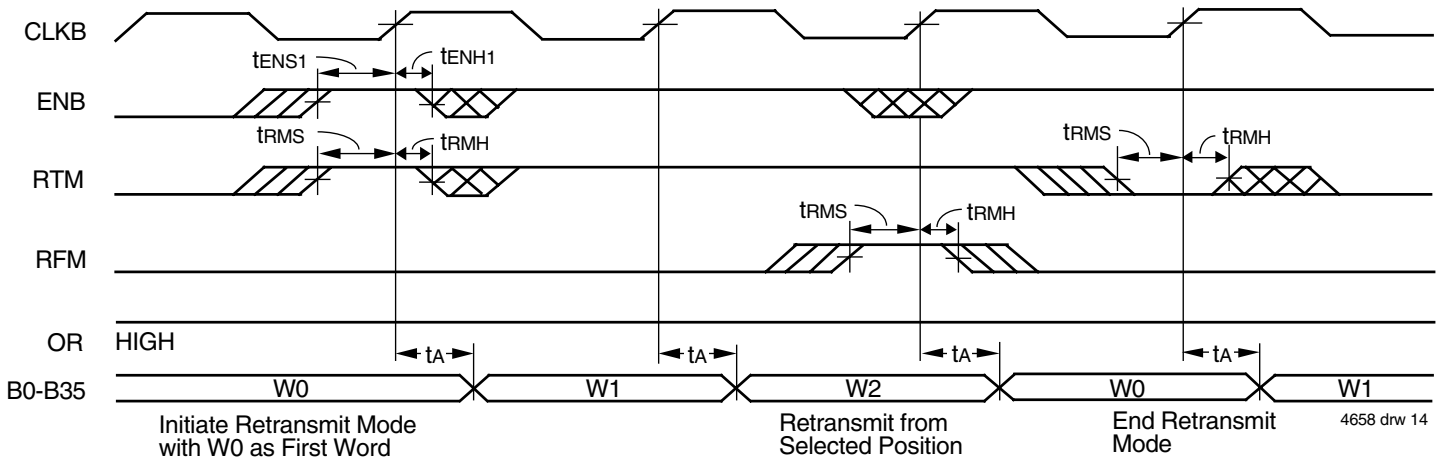
NOTES:
1. t_{SKEW2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AE}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW2}, then $\overline{AE}$ may transition HIGH one CLKB cycle later than shown.
2. FIFO write ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = HIGH, MBA = LOW), FIFO read ($\overline{CSB}$ = LOW, $\overline{W}$/RB = HIGH, MBB = LOW).

Figure 9. Timing for $\overline{AE}$ when FIFO is Almost-Empty



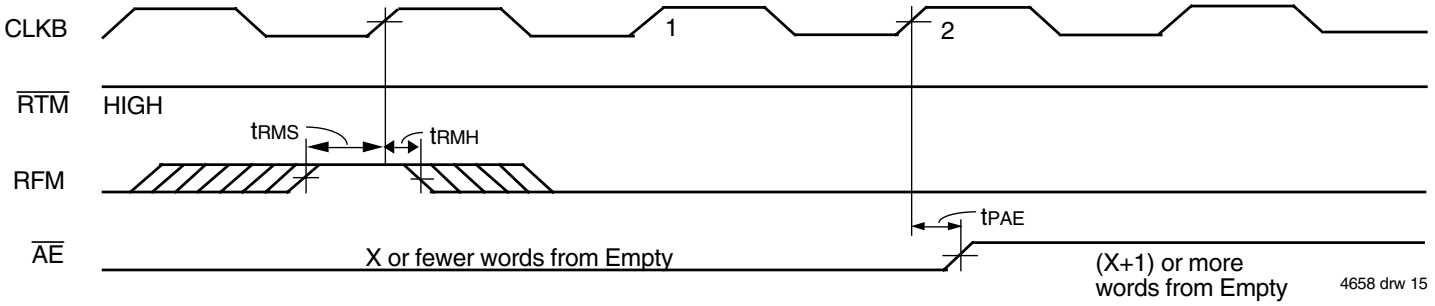
NOTES:
1. t_{SKEW2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AF}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW2}, then $\overline{AF}$ may transition HIGH one CLKA cycle later than shown.
2. Depth is 512 for the IDT72V3631 and 1,024 for the IDT72V3641.
3. FIFO write ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = HIGH, MBA = LOW), FIFO read ($\overline{CSB}$ = LOW, $\overline{W}$/RB = HIGH, MBB = LOW).

Figure 10. Timing for $\overline{AF}$ when FIFO is Almost-Full



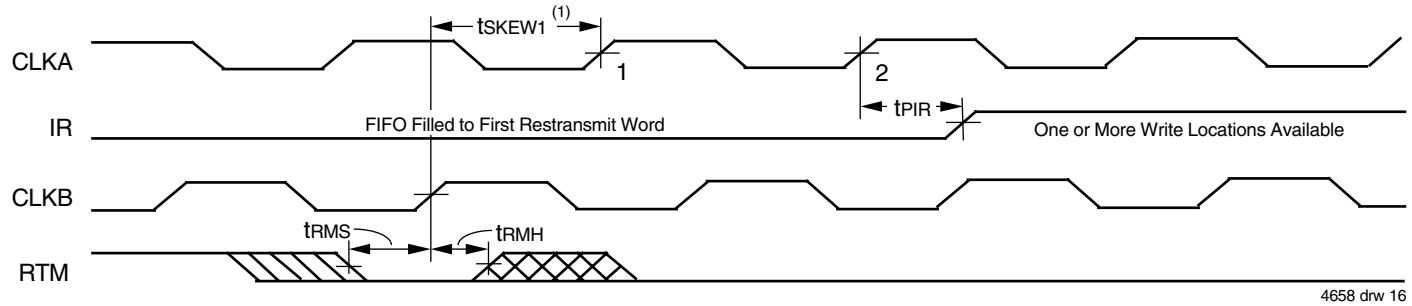
NOTE:
1. CSB = LOW, W/RB = HIGH, MBB = LOW. No input enables other than RTM and RFM are needed to control retransmit mode or begin a retransmit. Other enables are shown only to relate retransmit operations to the FIFO output register.

Figure 11. Retransmit Timing Showing Minimum Retransmit Length



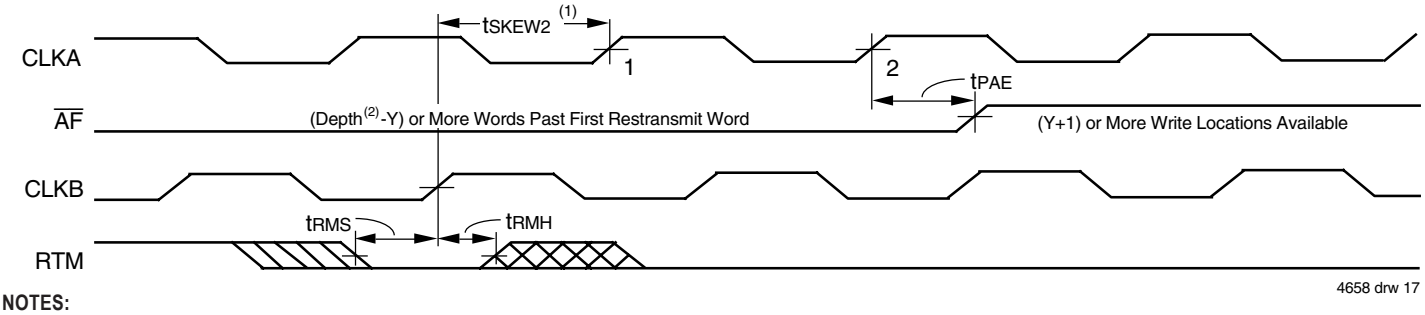
NOTE:
1. X is the value loaded in the Almost-Empty flag Offset register.

Figure 12. $\overline{AE}$ Maximum Latency When Retransmit Increases the Number of Stored Words Above X.



NOTE:
1. tSKEW1 is the minimum time between a rising CLKB edge and a rising CLKA edge for IR to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than tSKEW1, then IR may transition HIGH one CLKA cycle later than shown.

Figure 13. IR Timing from the End of Retransmit Mode when One or More Write Locations are Available



NOTES:
1. tSKEW2 is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AF}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than tSKEW2, then $\overline{AF}$ may transition HIGH one CLKA cycle later than shown.
2. Depth is 512 for the IDT72V3631 and 1,024 for the IDT72V3641.
3. Y is the value loaded in the Almost-Full flag Offset register.

Figure 14. $\overline{AF}$ Timing from the End of Retransmit Mode when (Y+1) or More Write Locations are Available

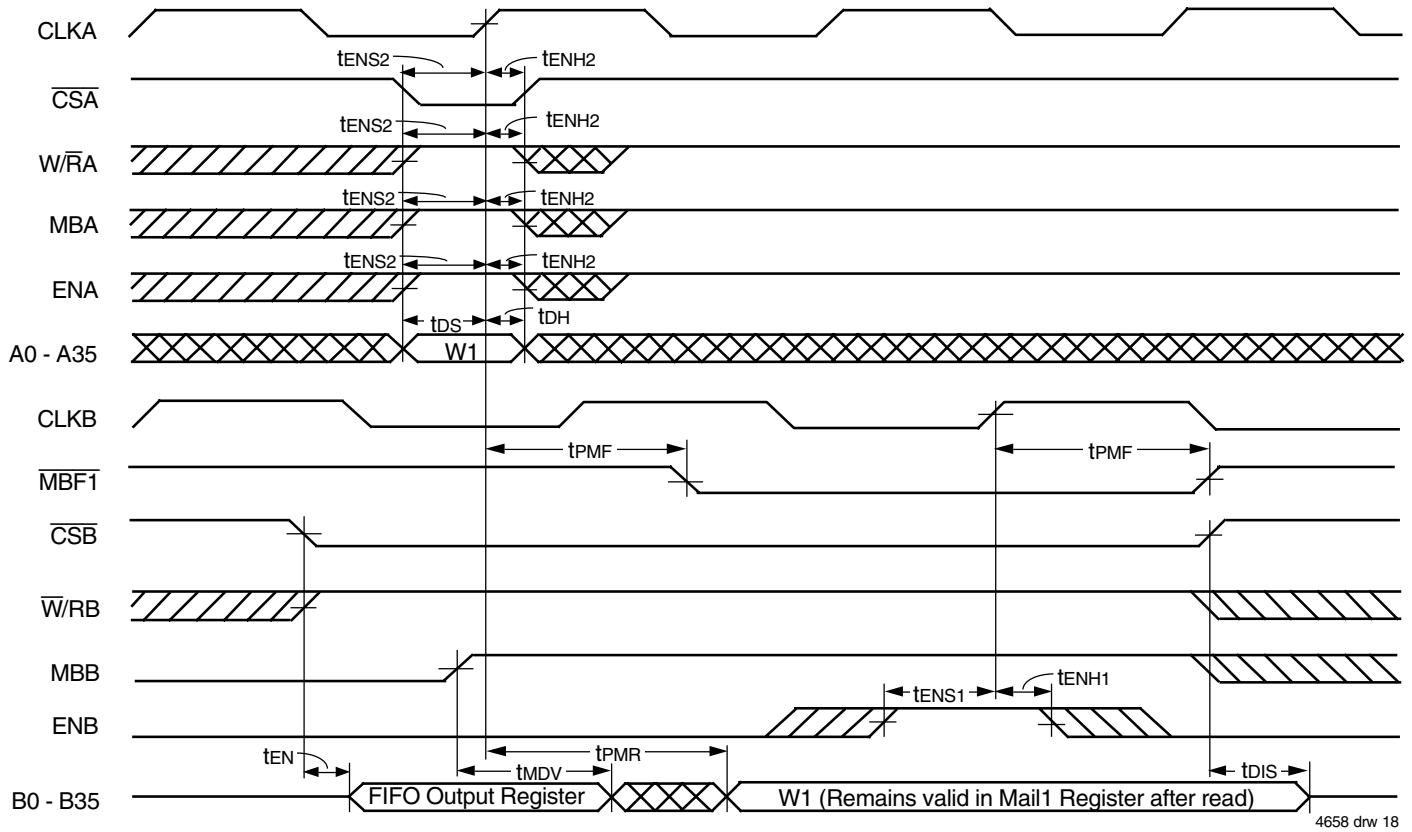


Figure 15. Timing for Mail1 Register and $\overline{MBF1}$ Flag

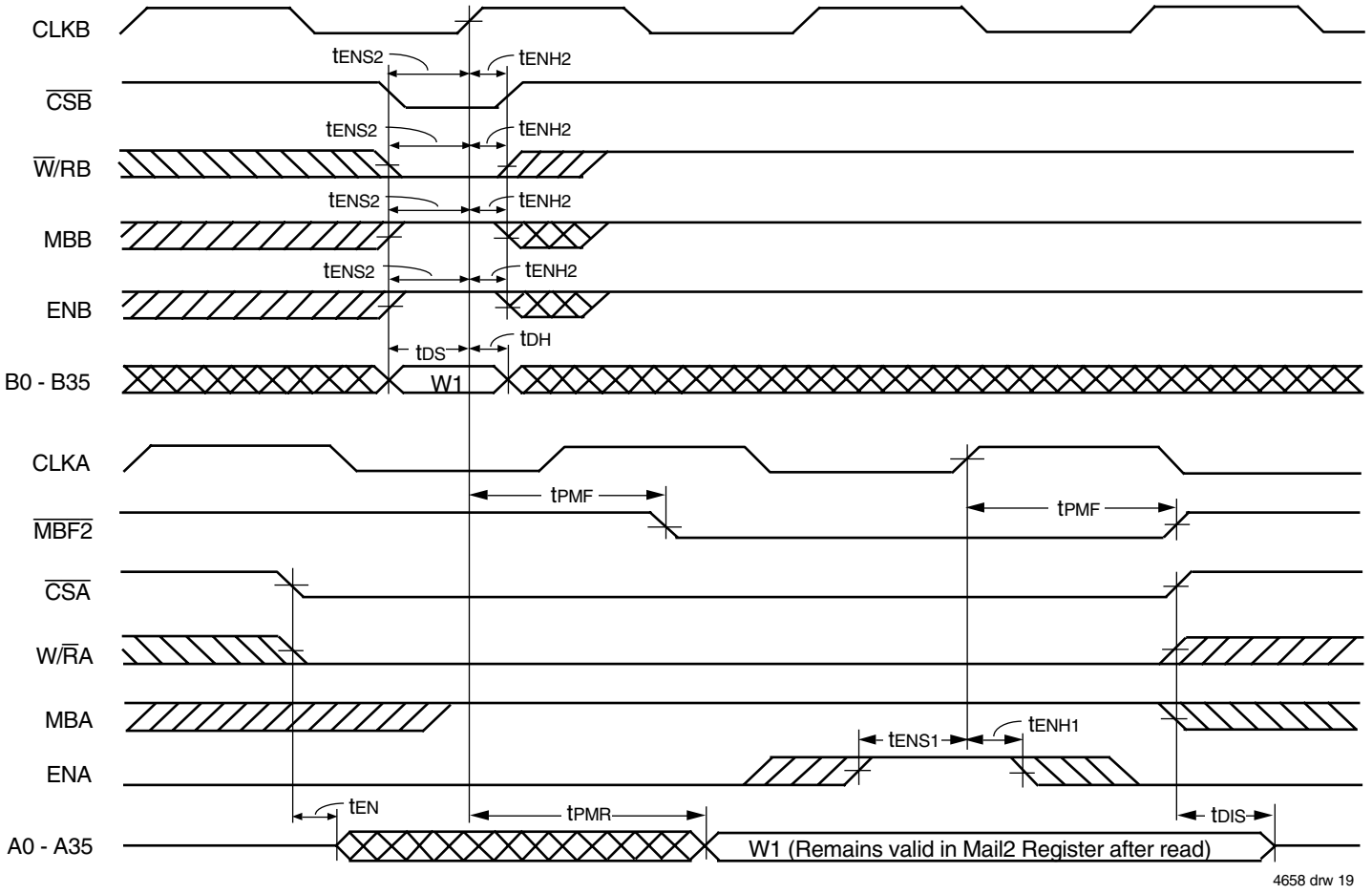
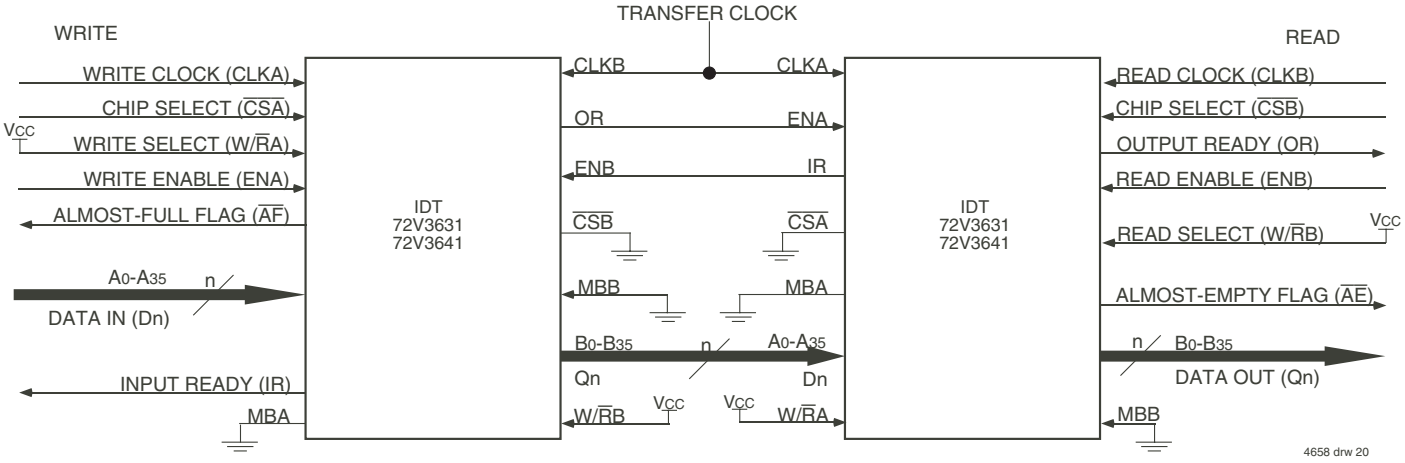


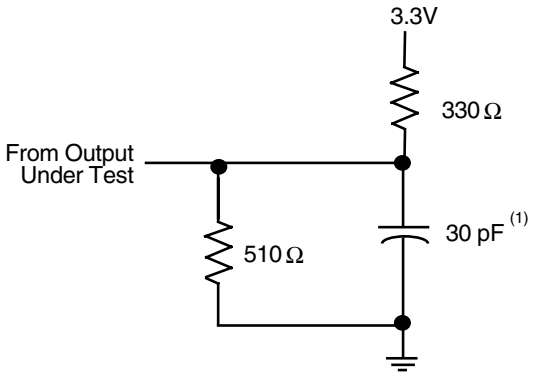
Figure 16. Timing for Mail2 Register and MBF2 Flag

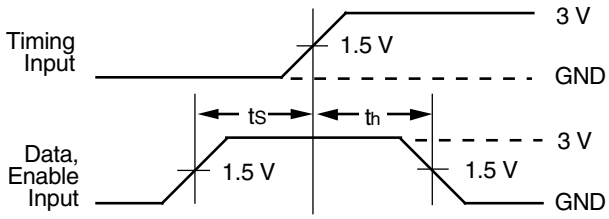


NOTES:
1. Mailbox feature is not supported in depth expansion applications. (MBA + MBB tie to GND)
2. Transfer clock should be set either to the Write Port Clock (CLKA) or the Read Port Clock (CLKB), whichever is faster.
3. Retransmit feature is not supported in depth expansion applications.
4. The amount of time it takes for OR of the last FIFO in the chain to go HIGH (i.e. valid data to appear on the last FIFO's outputs) after a word has been written to the first FIFO is the sum of the delays for each individual FIFO: (N - 1)*(4*transfer clock) + 3*TRCLK, where N is the number of FIFOs in the expansion and TRCLK is the CLKB period.
5. The amount of time is takes for IR of the first FIFO in the chain to go HIGH after a word has been read from the last FIFO is the sum of the delays for each individual FIFO: (N - 1)*(3*transfer clock) + 2*TWCLK, where N is the number of FIFOs in the expansion and TWCLK is the CLKA period.

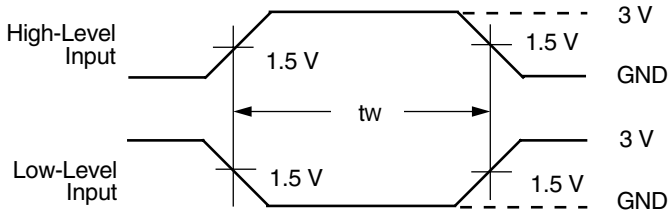
Figure 17. Block Diagram of 512 x 36, 1,024 x 36 Synchronous FIFO Memory with Programmable Flags used in Depth Expansion Configuration

PARAMETER MEASUREMENT INFORMATION

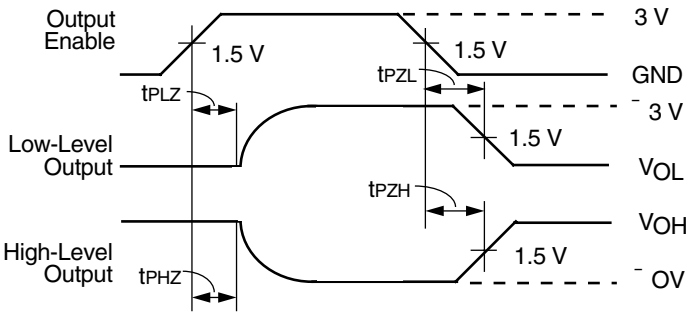




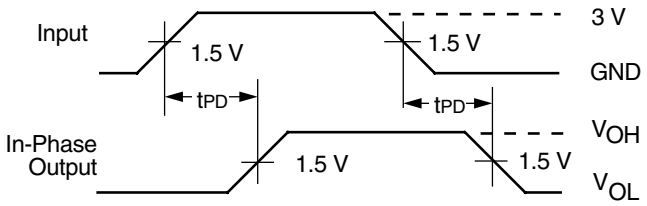
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



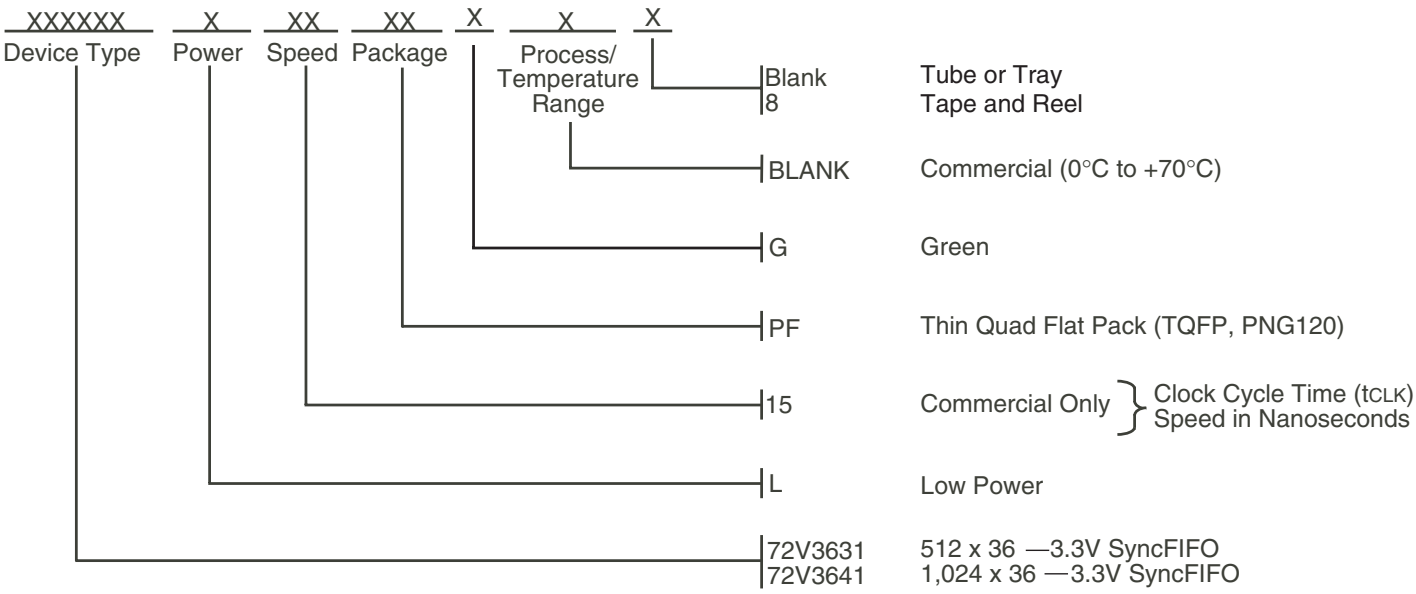
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

4658 drw 21

NOTE:
1. Includes probe and jig capacitance

Figure 18. Load Circuit and Voltage Waveforms

ORDERING INFORMATION



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DATASHEET DOCUMENT HISTORY

07/31/2000	pgs.	1, 14, 21.
11/04/2003	pg.	1.
02/05/2009	pgs.	1 and 21.
06/18/2014	pgs.	1-20.

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