

## FEATURES

- Maximum temperature coefficient (TCV<sub>OUT</sub>):**
  - 1 ppm/°C (C grade 0°C to 70°C)
  - 2 ppm/°C (B grade -40°C to +125°C)
- Output noise (0.1 Hz to 10 Hz):**
  - 1  $\mu$ V p-p at V<sub>OUT</sub> of 2.048 V typical
- Initial output voltage error:**
  - C grade:  $\pm 0.02\%$  (maximum)
- Input voltage range: 3 V to 15 V**
- Operating temperature:**
  - A grade and B grade: -40°C to +125°C
  - C grade: 0°C to +70°C
- Output current: +10 mA source/-10 mA sink**
- Low quiescent current: 950  $\mu$ A (maximum)**
- Low dropout voltage: 300 mV at 2 mA (V<sub>OUT</sub>  $\geq$  3 V)**
- 8-lead SOIC package**
- AEC-Q100 qualified for automotive applications**
- Long-term drift: 51 ppm typical at 4500 hours**

## APPLICATIONS

- Precision data acquisition systems
- High resolution data converters
- High precision measurement devices
- Industrial instrumentation
- Medical devices
- Automotive battery monitoring

## GENERAL DESCRIPTION

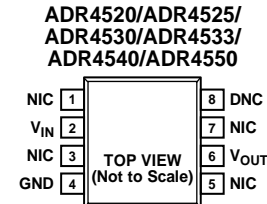
The ADR4520/ADR4525/ADR4530/ADR4533/ADR4540/ADR4550 devices are high precision, low power, low noise voltage references featuring  $\pm 0.02\%$  C grade maximum initial error, excellent temperature stability, and low output noise.

This family of voltage references uses an innovative core topology to achieve high accuracy while offering industry-leading temperature stability and noise performance. The low, thermally induced output voltage hysteresis and low long-term output voltage drift of the devices also improve system accuracy over time and temperature variations.

A maximum operating current of 950  $\mu$ A and a maximum low dropout voltage of 300 mV allow the devices to function very well in portable equipment.

The ADR4520/ADR4525/ADR4530/ADR4533/ADR4540/ADR4550 series of references are each provided in an 8-lead SOIC package and are available in a wide range of output voltages, all of which are specified over the extended industrial temperature range of -40°C to +125°C. The ADR4525, ADR4540,

## PIN CONFIGURATION



### NOTES

1. NIC = NOT INTERNALLY CONNECTED. THIS PIN IS NOT CONNECTED INTERNALLY.
2. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.

Figure 1. 8-Lead SOIC

10203-901

and ADR4550 are also available in C grade with a temperature range of 0°C to 70°C. The ADR4525W, available in an 8-lead SOIC package, is qualified for automotive applications.

Table 1. Selection Guide

Model	Output Voltage (V)	Grade
ADR4520	2.048	A, B
ADR4525	2.5	A, B, C
ADR4525W	2.5	B
ADR4530	3.0	A, B
ADR4533	3.3	A, B
ADR4540	4.096	A, B, C
ADR4550	5.0	A, B, C

Table 2. Voltage Reference Choices from Analog Devices, Inc.

V <sub>OUT</sub> (V)	Micropower	Low Power	Ultralow Noise
2.048	ADR3420 LT6656	ADR360 LTC6652 LT6654	ADR440 LTC6655
2.5	ADR3425 LT1461 LT6656	ADR361 LTC6652 LT6654	ADR441 LTC6655
5.0	ADR3450 LT1461 LT6656	ADR365 LTC6652 LT6654	ADR445 LTC6655

### Rev. C

### Document Feedback

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**REVISION HISTORY**

<b>4/2020—Rev. B to Rev. C</b>	
Added ADR4540 C Grade and ADR4550 C Grade...Throughout	
Changes to Table 4.....	5
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Deleted Figure 32, Renumbered Sequentially .....	18
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Added Electrostatic Discharge (ESD) Human Body Model (HBM) Parameter and Moisture Sensitivity Level Rating Parameter, Table 9.....	10
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Deleted Figure 4; Renumbered Sequentially.....	12
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Changed TP Pin to DNC Pin and NC Pin to  
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Changes to Features Section, Figure 1, and General Description  
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**4/2012—Revision 0: Initial Version**

## SPECIFICATIONS

### ADR4520 ELECTRICAL CHARACTERISTICS

Unless otherwise noted, supply voltage ( $V_{IN}$ ) = 3 V to 15 V,  $I_L$  = 0 mA,  $T_A$  = 25°C.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT VOLTAGE	$V_{OUT}$			2.048		V
INITIAL OUTPUT VOLTAGE ERROR	$V_{OUT\_ERR}$					
B Grade					±0.02	%
					410	μV
A Grade					±0.04	%
					820	μV
SOLDER HEAT RESISTANCE SHIFT				±0.02		%
TEMPERATURE COEFFICIENT	$TCV_{OUT}$	See Terminology section				
B Grade		−40°C ≤ $T_A$ ≤ +125°C (box method)			2	ppm/°C
		−40°C ≤ $T_A$ ≤ +125°C (bowtie method)			4	ppm/°C
A Grade		−40°C ≤ $T_A$ ≤ +125°C (box method)			4	ppm/°C
		−40°C ≤ $T_A$ ≤ +125°C (bowtie method)			8	ppm/°C
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	−40°C ≤ $T_A$ ≤ +125°C		1	10	ppm/V
LOAD REGULATION	$\Delta V_{OUT}/\Delta I_L$	$I_L$ = 0 mA to +10 mA source, −40°C ≤ $T_A$ ≤ +125°C		30	80	ppm/mA
		$I_L$ = 0 mA to −10 mA sink, −40°C ≤ $T_A$ ≤ +125°C		100	120	ppm/mA
QUIESCENT CURRENT	$I_Q$	−40°C ≤ $T_A$ ≤ +125°C, no load		700	950	μA
DROPOUT VOLTAGE	$V_{DO}$	−40°C ≤ $T_A$ ≤ +125°C, no load			1	V
		−40°C ≤ $T_A$ ≤ +125°C, $I_L$ = 2 mA			1	V
RIPPLE REJECTION RATIO	RRR	Input frequency ( $f_{IN}$ ) = 1 kHz		90		dB
OUTPUT CURRENT CAPACITY	$I_L$					
Sinking					−8	mA
Sourcing					10	mA
OUTPUT VOLTAGE NOISE	$e_{NP-p}$	0.1 Hz to 10.0 Hz		1.0		μV p-p
OUTPUT VOLTAGE NOISE DENSITY	$e_N$	1 kHz		35.8		nV/√Hz
OUTPUT VOLTAGE HYSTERESIS	$\Delta V_{OUT\_HYS}$	$T_A$ = temperature cycled from +25°C to +125°C to −40°C to +25°C (full cycle) 25°C to 125°C to 25°C (half cycle) 25°C to 70°C to 0°C to 25°C (full cycle) 25°C to 70°C to 25°C (half cycle)		−13		ppm
				−97		ppm
				−8		ppm
				−17		ppm
LONG-TERM DRIFT	$\Delta V_{OUT\_LTD}$	$T_A$ = 25°C 250 hours (early life drift) 1000 hours 4500 hours		19		ppm
				25		ppm
				51		ppm
TURN-ON SETTLING TIME	$t_R$	Output capacitor ( $C_{OUT}$ ) = 1 μF, input capacitor ( $C_{IN}$ ) = 0.1 μF, load resistance ( $R_{LOAD}$ ) = 1 kΩ		90		μs
LOAD CAPACITANCE			1		100	μF

**ADR4525 ELECTRICAL CHARACTERISTICS**Unless otherwise noted,  $V_{IN} = 3\text{ V}$  to  $15\text{ V}$ ,  $I_L = 0\text{ mA}$ ,  $T_A = 25^\circ\text{C}$ .**Table 4.**

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT VOLTAGE	$V_{OUT}$			2.500		V
INITIAL OUTPUT VOLTAGE ERROR	$V_{OUT\_ERR}$					
C Grade					±0.02	%
B Grade					500	µV
A Grade					±0.02	%
					500	µV
					±0.04	%
					1	mV
SOLDER HEAT RESISTANCE SHIFT				±0.02		%
A, B, C Grade						
TEMPERATURE COEFFICIENT	$TCV_{OUT}$	See Terminology section				
C Grade		$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ (box method)			1	ppm/°C
B Grade		$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ (bowtie method)			2	ppm/°C
A Grade		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ (box method)			2	ppm/°C
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ (bowtie method)			4	ppm/°C
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ (box method)			4	ppm/°C
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ (bowtie method)			8	ppm/°C
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1	10	ppm/V
LOAD REGULATION	$\Delta V_{OUT}/\Delta I_L$					
A, B, C Grade		$I_L = 0\text{ mA}$ to $+10\text{ mA}$ source, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		30	80	ppm/mA
		$I_L = 0\text{ mA}$ to $-10\text{ mA}$ sink, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		60	120	ppm/mA
QUIESCENT CURRENT	$I_Q$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , no load		700	950	µA
DROPOUT VOLTAGE	$V_{DO}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , no load			500	mV
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , $I_L = 2\text{ mA}$			500	mV
RIPPLE REJECTION RATIO	RRR	$f_{IN} = 1\text{ kHz}$		90		dB
OUTPUT CURRENT CAPACITY	$I_L$					
Sinking					-10	mA
Sourcing					10	mA
OUTPUT VOLTAGE NOISE	$e_{NP-P}$	0.1 Hz to 10.0 Hz		1.25		µV p-p
OUTPUT VOLTAGE NOISE DENSITY	$e_N$	1 kHz		41.3		nV/√Hz
OUTPUT VOLTAGE HYSTERESIS	$\Delta V_{OUT\_HYS}$	$T_A =$ temperature cycled from				
A, B, C Grade		$+25^\circ\text{C}$ to $+125^\circ\text{C}$ to $-40^\circ\text{C}$ to $+25^\circ\text{C}$ (full cycle)		-13		ppm
		$25^\circ\text{C}$ to $125^\circ\text{C}$ to $25^\circ\text{C}$ (half cycle)		-97		ppm
		$25^\circ\text{C}$ to $70^\circ\text{C}$ to $0^\circ\text{C}$ to $25^\circ\text{C}$ (full cycle)		-8		ppm
		$25^\circ\text{C}$ to $70^\circ\text{C}$ to $25^\circ\text{C}$ (half cycle)		-17		ppm
LONG-TERM DRIFT	$\Delta V_{OUT\_LTD}$	$T_A = 25^\circ\text{C}$				
A, B, C Grade		250 hours (early life drift)		19		ppm
		1000 hours		25		ppm
		4500 hours		51		ppm
TURN-ON SETTLING TIME	$t_R$	$C_{OUT} = 1\text{ }\mu\text{F}$ , $C_{IN} = 0.1\text{ }\mu\text{F}$ , $R_{LOAD} = 1\text{ k}\Omega$		125		µs
LOAD CAPACITANCE			1		100	µF

**ADR4530 ELECTRICAL CHARACTERISTICS**

Unless otherwise noted,  $V_{IN} = 3.1\text{ V}$  to  $15\text{ V}$ ,  $I_L = 0\text{ mA}$ ,  $T_A = 25^\circ\text{C}$ .

Table 5.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT VOLTAGE	$V_{OUT}$			3.000		V
INITIAL OUTPUT VOLTAGE ERROR B Grade	$V_{OUT\_ERR}$				$\pm 0.02$ 600	% $\mu\text{V}$
A Grade					$\pm 0.04$ 1.2	% mV
SOLDER HEAT RESISTANCE SHIFT				$\pm 0.02$		%
TEMPERATURE COEFFICIENT B Grade	$TCV_{OUT}$	See Terminology section $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ (box method) $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ (bowtie method)			2 4	ppm/ $^\circ\text{C}$ ppm/ $^\circ\text{C}$
A Grade		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ (box method) $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ (bowtie method)			4 8	ppm/ $^\circ\text{C}$ ppm/ $^\circ\text{C}$
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1	10	ppm/V
LOAD REGULATION	$\Delta V_{OUT}/\Delta I_L$	$I_L = 0\text{ mA}$ to $+10\text{ mA}$ source, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ $I_L = 0\text{ mA}$ to $-10\text{ mA}$ sink, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		30 60	80 120	ppm/mA ppm/mA
QUIESCENT CURRENT	$I_Q$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , no load		700	950	$\mu\text{A}$
DROPOUT VOLTAGE	$V_{DO}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , no load $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , $I_L = 2\text{ mA}$			100 300	mV mV
RIPPLE REJECTION RATIO	RRR	$f_{IN} = 1\text{ kHz}$		90		dB
OUTPUT CURRENT CAPACITY Sinking Sourcing	$I_L$				-10 10	mA mA
OUTPUT VOLTAGE NOISE	$e_{Np-p}$	0.1 Hz to 10.0 Hz		1.6		$\mu\text{V p-p}$
OUTPUT VOLTAGE NOISE DENSITY	$e_N$	1 kHz		60		nV/ $\sqrt{\text{Hz}}$
OUTPUT VOLTAGE HYSTERESIS	$\Delta V_{OUT\_HYS}$	$T_A =$ temperature cycled from $+25^\circ\text{C}$ to $+125^\circ\text{C}$ to $-40^\circ\text{C}$ to $+25^\circ\text{C}$ (full cycle) $25^\circ\text{C}$ to $125^\circ\text{C}$ to $25^\circ\text{C}$ (half cycle) $25^\circ\text{C}$ to $70^\circ\text{C}$ to $0^\circ\text{C}$ to $25^\circ\text{C}$ (full cycle) $25^\circ\text{C}$ to $70^\circ\text{C}$ to $25^\circ\text{C}$ (half cycle)		-13 -97 -8 -17		ppm ppm ppm ppm
LONG-TERM DRIFT	$\Delta V_{OUT\_LTD}$	$T_A = 25^\circ\text{C}$ 250 hours (early life drift) 1000 hours 4500 hours		19 25 51		ppm ppm ppm
TURN-ON SETTLING TIME	$t_r$	$C_{OUT} = 0.1\ \mu\text{F}$ , $C_{IN} = 0.1\ \mu\text{F}$ , $R_{LOAD} = 1\ \text{k}\Omega$		130		$\mu\text{s}$
LOAD CAPACITANCE			0.1		100	$\mu\text{F}$

**ADR4533 ELECTRICAL CHARACTERISTICS**

Unless otherwise noted,  $V_{IN} = 3.4\text{ V}$  to  $15\text{ V}$ ,  $I_L = 0\text{ mA}$ ,  $T_A = 25^\circ\text{C}$ .

**Table 6.**

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT VOLTAGE	$V_{OUT}$			3.300		V
INITIAL OUTPUT VOLTAGE ERROR	$V_{OUT\_ERR}$					
B Grade					$\pm 0.02$	%
A Grade					660	$\mu\text{V}$
					$\pm 0.04$	%
					1.32	mV
SOLDER HEAT RESISTANCE SHIFT				$\pm 0.02$		%
TEMPERATURE COEFFICIENT	$TCV_{OUT}$	See Terminology section				
B Grade		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ (box method)			2	ppm/ $^\circ\text{C}$
A Grade		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ (bowtie method)			4	ppm/ $^\circ\text{C}$
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ (box method)			4	ppm/ $^\circ\text{C}$
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ (bowtie method)			8	ppm/ $^\circ\text{C}$
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1	10	ppm/V
LOAD REGULATION	$\Delta V_{OUT}/\Delta I_L$	$I_L = 0\text{ mA}$ to $+10\text{ mA}$ source, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ $I_L = 0\text{ mA}$ to $-10\text{ mA}$ sink, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		30	80	ppm/mA
				60	120	ppm/mA
QUIESCENT CURRENT	$I_Q$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , no load		700	950	$\mu\text{A}$
DROPOUT VOLTAGE	$V_{DO}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , no load $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , $I_L = 2\text{ mA}$			100	mV
					300	mV
RIPPLE REJECTION RATIO	RRR	$f_{IN} = 1\text{ kHz}$		90		dB
OUTPUT CURRENT CAPACITY	$I_L$					
Sinking					-10	mA
Sourcing					10	mA
OUTPUT VOLTAGE NOISE	$e_{Np-p}$	0.1 Hz to 10.0 Hz		2.1		$\mu\text{V p-p}$
OUTPUT VOLTAGE NOISE DENSITY	$e_N$	1 kHz		64.2		nV/ $\sqrt{\text{Hz}}$
OUTPUT VOLTAGE HYSTERESIS	$\Delta V_{OUT\_HYS}$	$T_A =$ temperature cycled from $+25^\circ\text{C}$ to $+125^\circ\text{C}$ to $-40^\circ\text{C}$ to $+25^\circ\text{C}$ (full cycle) $25^\circ\text{C}$ to $125^\circ\text{C}$ to $25^\circ\text{C}$ (half cycle) $25^\circ\text{C}$ to $70^\circ\text{C}$ to $0^\circ\text{C}$ to $25^\circ\text{C}$ (full cycle) $25^\circ\text{C}$ to $70^\circ\text{C}$ to $25^\circ\text{C}$ (half cycle)		-13		ppm
				-97		ppm
				-8		ppm
				-17		ppm
LONG-TERM DRIFT	$\Delta V_{OUT\_LTD}$	$T_A = 25^\circ\text{C}$ 250 hours (early life drift) 1000 hours 4500 hours		19		ppm
				25		ppm
				51		ppm
TURN-ON SETTLING TIME	$t_R$	$C_{OUT} = 0.1\ \mu\text{F}$ , $C_{IN} = 0.1\ \mu\text{F}$ , $R_{LOAD} = 1\ \text{k}\Omega$		135		$\mu\text{s}$
LOAD CAPACITANCE			0.1		100	$\mu\text{F}$

**ADR4540 ELECTRICAL CHARACTERISTICS**

Unless otherwise noted,  $V_{IN} = 4.2\text{ V to }15\text{ V}$ ,  $I_L = 0\text{ mA}$ ,  $T_A = 25^\circ\text{C}$ .

Table 7.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT VOLTAGE	$V_{OUT}$			4.096		V
INITIAL OUTPUT VOLTAGE ERROR	$V_{OUT\_ERR}$					
C Grade					±0.02	%
B Grade					820	µV
A Grade					±0.02	%
					820	µV
					±0.04	%
					1.64	mV
SOLDER HEAT RESISTANCE SHIFT						
A, B, C Grade				±0.02		%
TEMPERATURE COEFFICIENT	$TCV_{OUT}$	See Terminology section				
C Grade		$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ (box method)			1	ppm/°C
B Grade		$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ (bowtie method)			2	ppm/°C
A Grade		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ (box method)			2	ppm/°C
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ (bowtie method)			4	ppm/°C
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ (box method)			4	ppm/°C
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ (bowtie method)			8	ppm/°C
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1	10	ppm/V
LOAD REGULATION	$\Delta V_{OUT}/\Delta I_L$					
A, B, C Grade		$I_L = 0\text{ mA to }+10\text{ mA source, }-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		25	80	ppm/mA
		$I_L = 0\text{ mA to }-10\text{ mA sink, }-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		50	120	ppm/mA
QUIESCENT CURRENT	$I_Q$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , no load		700	950	µA
DROPOUT VOLTAGE	$V_{DO}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , no load			100	mV
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , $I_L = 2\text{ mA}$			300	mV
RIPPLE REJECTION RATIO	RRR	$f_{IN} = 1\text{ kHz}$		90		dB
OUTPUT CURRENT CAPACITY	$I_L$					
Sinking					-10	mA
Sourcing					10	mA
OUTPUT VOLTAGE NOISE	$e_{NP-P}$	0.1 Hz to 10.0 Hz		2.7		µV p-p
OUTPUT VOLTAGE NOISE DENSITY	$e_N$	1 kHz		83.5		nV/√Hz
OUTPUT VOLTAGE HYSTERESIS	$\Delta V_{OUT\_HYS}$	$T_A = \text{temperature cycled from}$				
A, B, C Grade		$+25^\circ\text{C to }+125^\circ\text{C to }-40^\circ\text{C to }+25^\circ\text{C}$ (full cycle)		-13		ppm
		$25^\circ\text{C to }125^\circ\text{C to }25^\circ\text{C}$ (half cycle)		-97		ppm
		$25^\circ\text{C to }70^\circ\text{C to }0^\circ\text{C to }25^\circ\text{C}$ (full cycle)		-8		ppm
		$25^\circ\text{C to }70^\circ\text{C to }25^\circ\text{C}$ (half cycle)		-17		ppm
LONG-TERM DRIFT	$\Delta V_{OUT\_LTD}$	$T_A = 25^\circ\text{C}$				
A, B, C Grade		250 hours (early life drift)		19		ppm
		1000 hours		25		ppm
		4500 hours		51		ppm
TURN-ON SETTLING TIME	$t_R$	$C_{OUT} = 0.1\text{ }\mu\text{F}$ , $C_{IN} = 0.1\text{ }\mu\text{F}$ , $R_{LOAD} = 1\text{ k}\Omega$		155		µs
LOAD CAPACITANCE			0.1		100	µF



**ADR4550 ELECTRICAL CHARACTERISTICS**Unless otherwise noted,  $V_{IN} = 5.1\text{ V}$  to  $15\text{ V}$ ,  $I_L = 0\text{ mA}$ ,  $T_A = 25^\circ\text{C}$ .**Table 8.**

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit	
OUTPUT VOLTAGE	$V_{OUT}$			5.000		V	
INITIAL OUTPUT VOLTAGE ERROR	$V_{OUT\_ERR}$						
C Grade					±0.02	μV	
B Grade					1	%	
A Grade					±0.02	1	mV
					±0.04	2	%
SOLDER HEAT RESISTANCE SHIFT				±0.02		%	
A, B, C Grade							
TEMPERATURE COEFFICIENT	$TCV_{OUT}$	See Terminology section					
C Grade		$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ (box method)			1	ppm/°C	
		$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ (bowtie method)			2	ppm/°C	
B Grade		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ (box method)			2	ppm/°C	
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ (bowtie method)			4	ppm/°C	
A Grade		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ (box method)			4	ppm/°C	
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ (bowtie method)			8	ppm/°C	
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1	10	ppm/V	
LOAD REGULATION	$\Delta V_{OUT}/\Delta I_L$						
A, B, C Grade		$I_L = 0\text{ mA}$ to $+10\text{ mA}$ source, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		25	80	ppm/mA	
		$I_L = 0\text{ mA}$ to $-10\text{ mA}$ sink, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		35	120	ppm/mA	
QUIESCENT CURRENT	$I_Q$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , no load		700	950	μA	
DROPOUT VOLTAGE	$V_{DO}$						
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , no load			100	mV	
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , $I_L = 2\text{ mA}$			300	mV	
RIPPLE REJECTION RATIO	RRR	$f_{IN} = 1\text{ kHz}$		90		dB	
OUTPUT CURRENT CAPACITY	$I_L$						
Sinking					-10	mA	
Sourcing					10	mA	
OUTPUT VOLTAGE NOISE	$e_{NP-P}$	0.1 Hz to 10.0 Hz		2.8		μV p-p	
OUTPUT VOLTAGE NOISE DENSITY	$e_N$	1 kHz		95.3		nV/√Hz	
OUTPUT VOLTAGE HYSTERESIS	$\Delta V_{OUT\_HYS}$						
A, B, C Grade		$T_A =$ temperature cycled from $+25^\circ\text{C}$ to $+125^\circ\text{C}$ to $-40^\circ\text{C}$ to $+25^\circ\text{C}$ (full cycle)		-13		ppm	
		$25^\circ\text{C}$ to $125^\circ\text{C}$ to $25^\circ\text{C}$ (half cycle)		-97		ppm	
		$25^\circ\text{C}$ to $70^\circ\text{C}$ to $0^\circ\text{C}$ to $25^\circ\text{C}$ (full cycle)		-8		ppm	
		$25^\circ\text{C}$ to $70^\circ\text{C}$ to $25^\circ\text{C}$ (half cycle)		-17		ppm	
LONG-TERM DRIFT	$\Delta V_{OUT\_LTD}$						
A, B, C Grade		$T_A = 25^\circ\text{C}$					
		250 hours (early life drift)		19		ppm	
		1000 hours		25		ppm	
		4500 hours		51		ppm	
TURN-ON SETTLING TIME	$t_R$	$C_{OUT} = 0.1\text{ }\mu\text{F}$ , $C_{IN} = 0.1\text{ }\mu\text{F}$ , $R_{LOAD} = 1\text{ k}\Omega$		160		μs	
LOAD CAPACITANCE			0.1		100	μF	

## ABSOLUTE MAXIMUM RATINGS

T<sub>A</sub> = 25°C, unless otherwise noted.

Table 9.

Parameter	Rating
Supply Voltage	16 V
Operating Temperature Range	−40°C to +125°C
ADR4525, ADR4540, ADR4550	0°C to 70°C
C Grade Only	
Storage Temperature Range	−65°C to +150°C
Junction Temperature Range	−65°C to +150°C
Electrostatic Discharge (ESD)	6 kV
Human Body Model (HBM)	
Moisture Sensitivity Level Rating	MSL-1

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

Table 10. Thermal Resistance

Package Type	θ <sub>JA</sub>	θ <sub>JC</sub> <sup>1</sup>	Unit
8-Lead SOIC <sup>2</sup>			
1-Layer JEDEC Board	N/A <sup>3</sup>	63	°C/W
2-Layer JEDEC Board	120	N/A <sup>3</sup>	°C/W

<sup>1</sup> For the θ<sub>JC</sub> test, 100 μm thermal interface material (TIM) is used. TIM is assumed to have 3.6 W/mK.

<sup>2</sup> Thermal impedance simulated values are based on a JEDEC thermal test board. See JEDEC JESD51.

<sup>3</sup> N/A means not applicable.

## ESD CAUTION



### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



## NOTES

1. NIC = NOT INTERNALLY CONNECTED.  
THIS PIN IS NOT CONNECTED INTERNALLY.
2. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.

102013-002

Figure 2. Pin Configuration

Table 11. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	NIC	Not Internally Connected. This pin is not connected internally.
2	V <sub>IN</sub>	Input Voltage Connection.
3	NIC	Not Internally Connected. This pin is not connected internally.
4	GND	Ground.
5	NIC	Not Internally Connected. This pin is not connected internally.
6	V <sub>OUT</sub>	Output Voltage.
7	NIC	Not Internally Connected. This pin is not connected internally.
8	DNC	Do Not Connect. Do not connect to this pin.

# TYPICAL PERFORMANCE CHARACTERISTICS

T<sub>A</sub> = 25°C, unless otherwise noted.

## ADR4520



Figure 3. ADR4520 B Grade Output Voltage vs. Temperature



Figure 6. ADR4520 Load Regulation vs. Temperature (Sourcing)

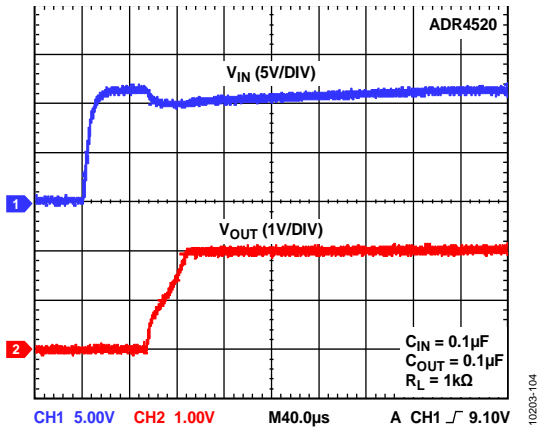


Figure 4. ADR4520 Output Voltage Start-Up Response



Figure 7. ADR4520 Load Regulation vs. Temperature (Sinking)



Figure 5. ADR4520 Dropout Voltage vs. Load Current

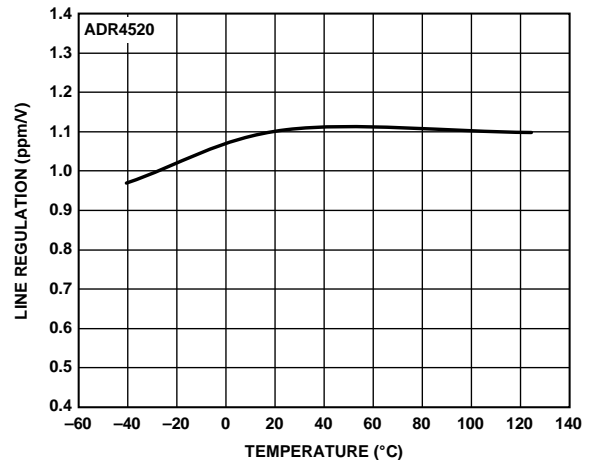


Figure 8. ADR4520 Line Regulation vs. Temperature



Figure 9. ADR4520 Supply Current ( $I_{SV}$ ) vs. Supply Voltage

10203-110



Figure 11. ADR4520 Output Noise Spectral Density

10203-112

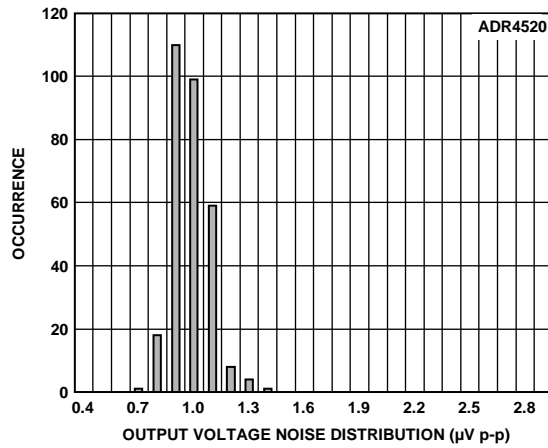


Figure 10. ADR4520 Output Voltage Noise (Maximum Amplitude from 0.1 Hz to 10 Hz)

10203-111

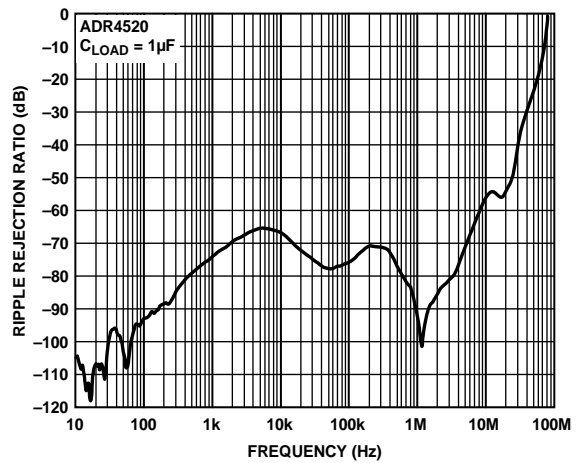


Figure 12. ADR4520 Ripple Rejection Ratio vs. Frequency

10203-113



Figure 13. ADR4520 Line Transient Response



Figure 15. ADR4520 Solder Heat Resistance Shift (3 × Reflow)



Figure 14. ADR4520 Output Impedance vs. Frequency

ADR4525



Figure 16. ADR4525 B Grade Output Voltage vs. Temperature

10203-201



Figure 19. ADR4525 Dropout Voltage vs. Load Current

10203-206

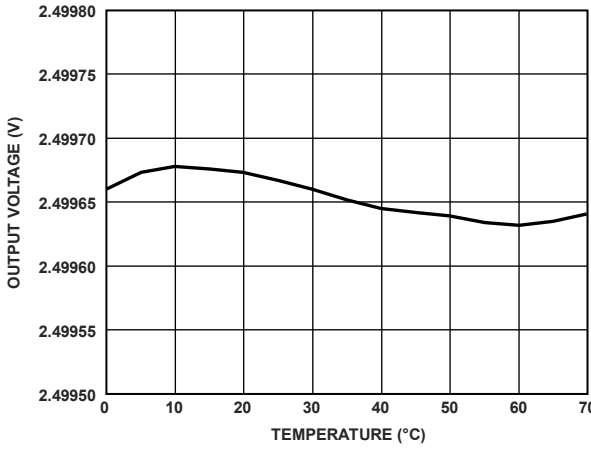


Figure 17. ADR4525 C Grade Output Voltage vs. Temperature

10203-417



Figure 20. ADR4525 Load Regulation vs. Temperature (Sourcing)

10203-207



Figure 18. ADR4525 Output Voltage Start-Up Response

10203-204



Figure 21. ADR4525 Load Regulation vs. Temperature (Sinking)

10203-208



Figure 22. ADR4525 Line Regulation vs. Temperature

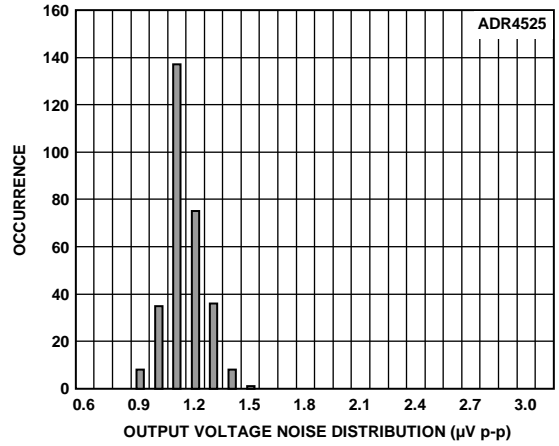


Figure 24. ADR4525 Output Voltage Noise (Maximum Amplitude from 0.1 Hz to 10 Hz)



Figure 23. ADR4525 Supply Current vs. Supply Voltage

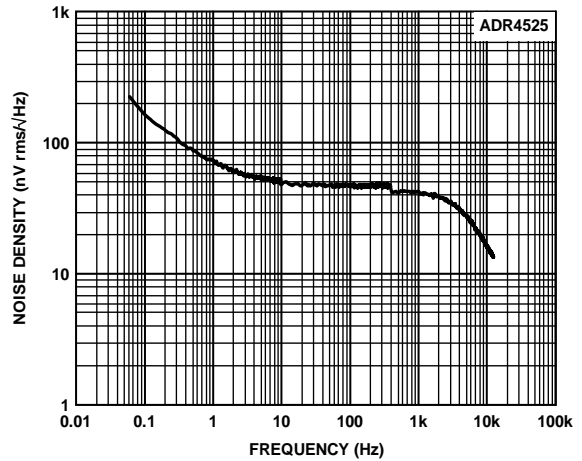


Figure 25. ADR4525 Output Noise Spectral Density



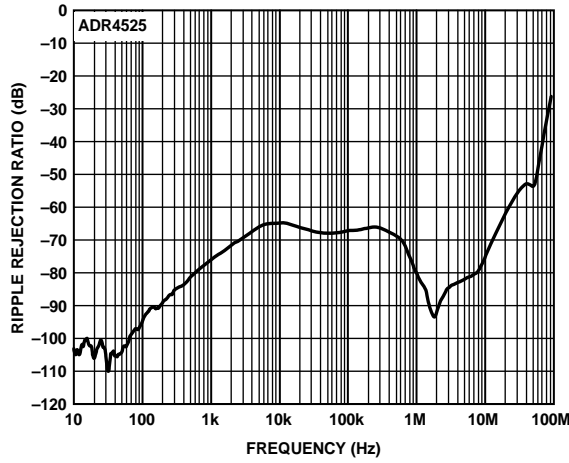


Figure 26. ADR4525 Ripple Rejection Ratio vs. Frequency



Figure 28. ADR4525 Output Impedance vs. Frequency



Figure 27. ADR4525 Line Transient Response



Figure 29. ADR4525 Solder Heat Resistance Shift (3 × Reflow)

ADR4530



Figure 30. ADR4530 B Grade Output Voltage vs. Temperature



Figure 33. ADR4530 Load Regulation vs. Temperature (Sourcing)



Figure 31. ADR4530 Output Voltage Start-Up Response



Figure 34. ADR4530 Load Regulation vs. Temperature (Sinking)



Figure 32. ADR4530 Dropout Voltage vs. Load Current

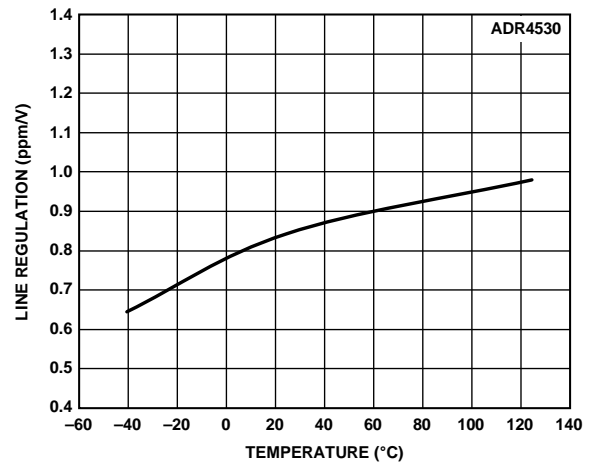


Figure 35. ADR4530 Line Regulation vs. Temperature



Figure 36. ADR4530 Supply Current vs. Supply Voltage

10203-310

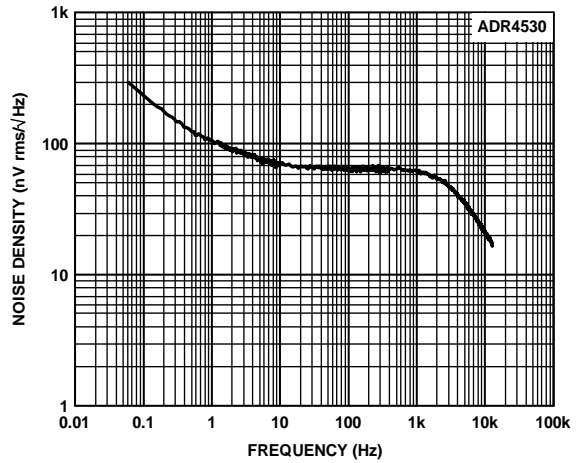


Figure 38. ADR4530 Output Noise Spectral Density

10203-312



Figure 37. ADR4530 Output Voltage Noise (Maximum Amplitude from 0.1 Hz to 10 Hz)

10203-311

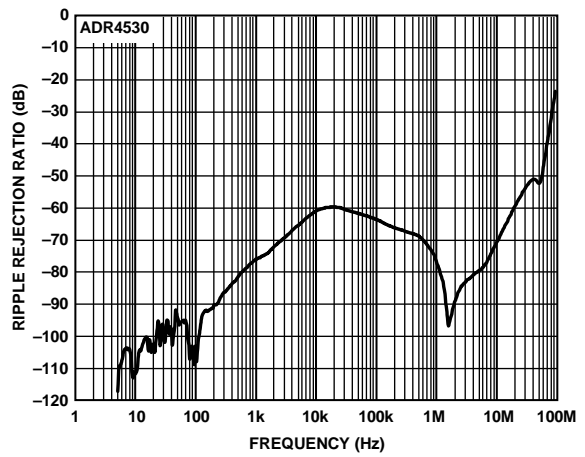


Figure 39. ADR4530 Ripple Rejection Ratio vs. Frequency

10203-313

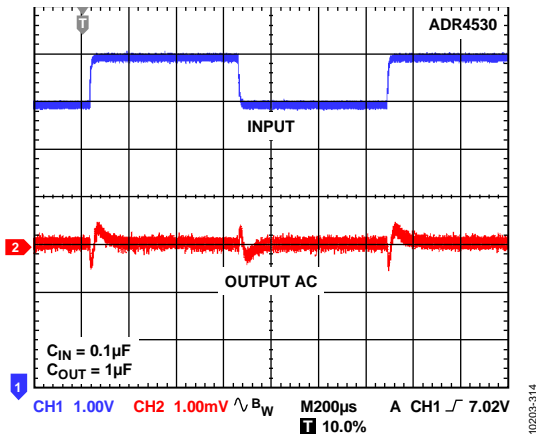


Figure 40. ADR4530 Line Transient Response



Figure 42. ADR4530 Solder Heat Resistance Shift (3 × Reflow)



Figure 41. ADR4530 Output Impedance vs. Frequency

ADR4533



Figure 43. ADR4533 B Grade Output Voltage vs. Temperature



Figure 46. ADR4533 Load Regulation vs. Temperature (Sourcing)

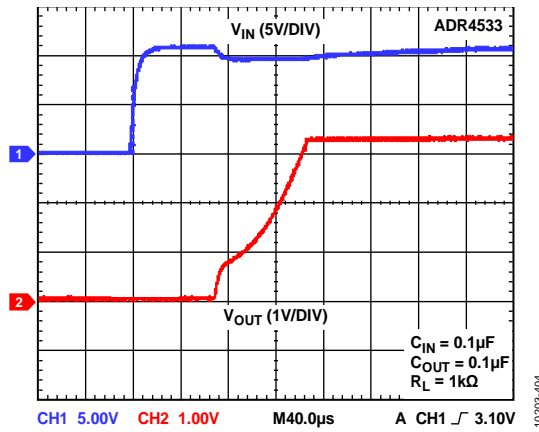


Figure 44. ADR4533 Output Voltage Start-Up Response



Figure 47. ADR4533 Load Regulation vs. Temperature (Sinking)



Figure 45. ADR4533 Dropout Voltage vs. Load Current



Figure 48. ADR4533 Line Regulation vs. Temperature



Figure 49. ADR4533 Supply Current vs. Supply Voltage



Figure 51. ADR4533 Output Noise Spectral Density



Figure 50. ADR4533 Output Voltage Noise (Maximum Amplitude from 0.1 Hz to 10 Hz)



Figure 52. ADR4533 Ripple Rejection Ratio vs. Frequency



Figure 53. ADR4533 Line Transient Response



Figure 55. ADR4533 Solder Heat Resistance Shift (3 × Reflow)

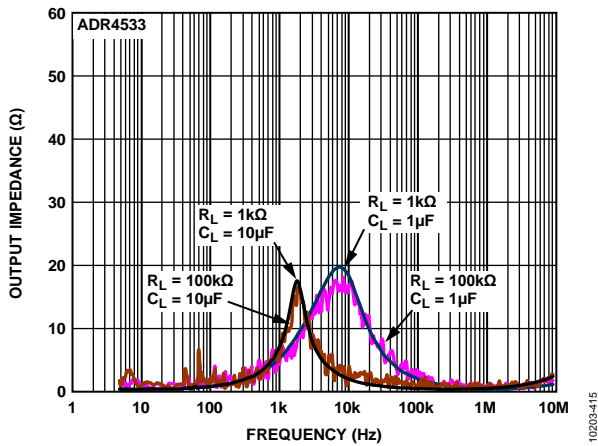


Figure 54. ADR4533 Output Impedance vs. Frequency

ADR4540



Figure 56. ADR4540 B Grade Output Voltage vs. Temperature



Figure 59. ADR4540 Load Regulation vs. Temperature (Sourcing)



Figure 57. ADR4540 Output Voltage Start-Up Response



Figure 60. ADR4540 Load Regulation vs. Temperature (Sinking)



Figure 58. ADR4540 Dropout Voltage vs. Load Current



Figure 61. ADR4540 Line Regulation vs. Temperature





Figure 62. ADR4540 Supply Current vs. Supply Voltage



Figure 64. ADR4540 Output Noise Spectral Density



Figure 63. ADR4540 Output Voltage Noise (Maximum Amplitude from 0.1 Hz to 10 Hz)



Figure 65. ADR4540 Ripple Rejection Ratio vs. Frequency



Figure 66. ADR4540 Line Transient Response

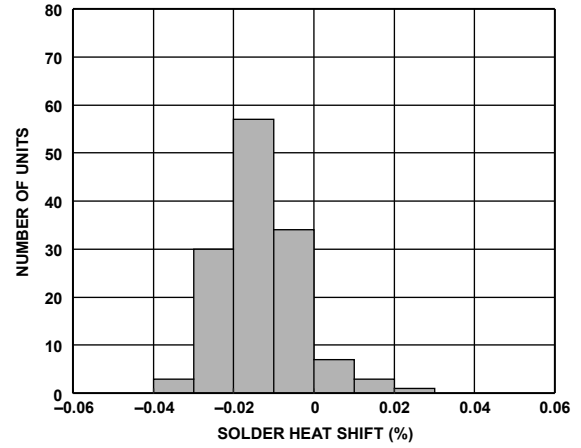


Figure 68. ADR4540 Solder Heat Resistance Shift (3 × Reflow)

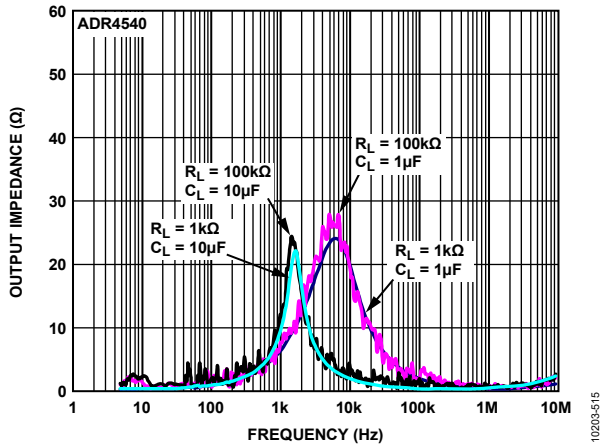


Figure 67. ADR4540 Output Impedance vs. Frequency



Figure 69. ADR4540 C Grade Output Voltage vs. Temperature

ADR4550



Figure 70. ADR4550 B Grade Output Voltage vs. Temperature



Figure 73. ADR4550 Load Regulation vs. Temperature (Sourcing)



Figure 71. ADR4550 Output Voltage Start-Up Response



Figure 74. ADR4550 Load Regulation vs. Temperature (Sinking)



Figure 72. ADR4550 Dropout Voltage vs. Load Current

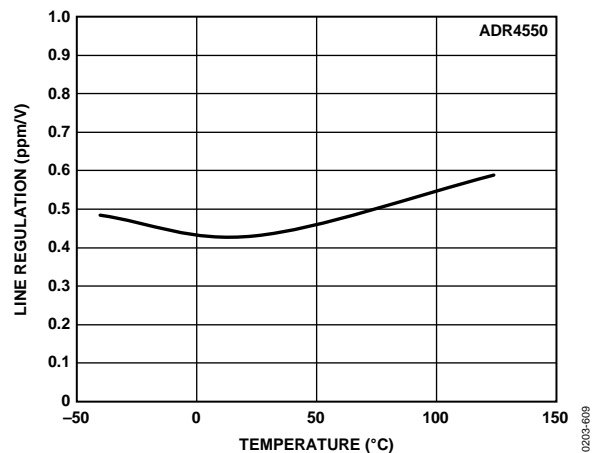


Figure 75. ADR4550 Line Regulation vs. Temperature



Figure 76. ADR4550 Supply Current vs. Supply Voltage



Figure 78. ADR4550 Output Noise Spectral Density

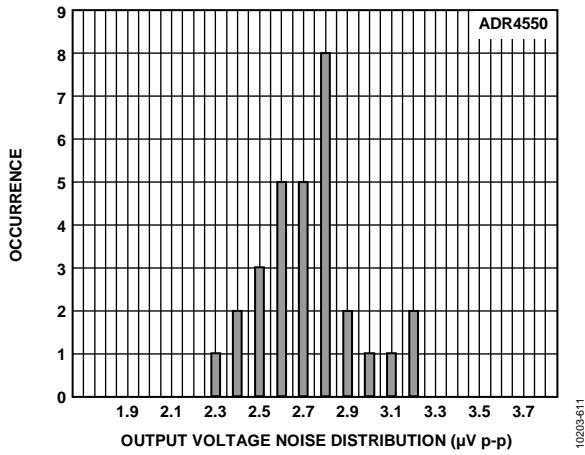


Figure 77. ADR4550 Output Voltage Noise (Maximum Amplitude from 0.1 Hz to 10 Hz)

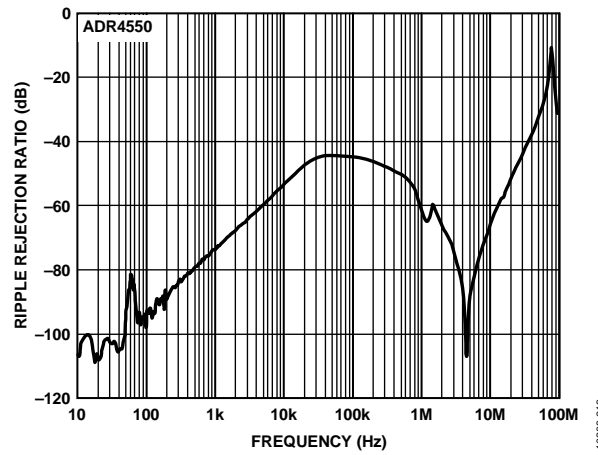


Figure 79. ADR4550 Ripple Rejection Ratio vs. Frequency



Figure 80. ADR4550 Line Transient Response



Figure 82. ADR4550 Solder Heat Resistance Shift (3 x Reflow)



Figure 81. ADR4550 Output Impedance vs. Frequency



Figure 83. ADR4550 C Grade Output Voltage vs. Temperature

## TERMINOLOGY

### Dropout Voltage ( $V_{DO}$ )

Dropout voltage, sometimes referred to as supply voltage headroom or supply output voltage differential, is defined as the minimum voltage differential between the input and output such that the output voltage is maintained to within 0.1% accuracy.

$$V_{DO} = (V_{IN} - V_{OUT})_{min}|_L = \text{constant}$$

Because the dropout voltage depends on the current passing through the device, it is always specified for a given load current. In series mode devices, the dropout voltage typically increases proportionally to the load current (see Figure 5, Figure 19, Figure 32, Figure 45, Figure 58, and Figure 72).

### Line Regulation

Line regulation refers to the change in output voltage in response to a given change in input voltage and is expressed in percent per volt, ppm per volt, or  $\mu\text{V}$  per volt change in input voltage. This parameter accounts for the effects of self heating.

### Load Regulation

Load regulation refers to the change in output voltage in response to a given change in load current and is expressed in  $\mu\text{V}$  per mA, ppm per mA, or ohms of dc output resistance. This parameter accounts for the effects of self heating.

### Solder Heat Resistance (SHR) Shift

SHR shift refers to the permanent shift in output voltage that is induced by exposure to reflow soldering and is expressed as a percentage of the output voltage. This shift is caused by changes in the stress exhibited on the die by the package materials when these materials are exposed to high temperatures. This effect is more pronounced in lead-free soldering processes due to higher reflow temperatures. SHR is calculated after three solder reflow cycles to simulate the worst case conditions when assembling a two-sided PCB with surface mount components with one additional rework cycle. The reflow cycles use the JEDEC standard reflow temperature profile.

### Temperature Coefficient ( $TCV_{OUT}$ )

The temperature coefficient relates the change in the output voltage to the change in the ambient temperature of the device, as normalized by the output voltage at 25°C. The  $TCV_{OUT}$  for the ADR4520/ADR4525/ADR4530/ADR4533/ADR4540/ADR4550 A grade and B grade is fully tested over three temperatures:  $-40^\circ\text{C}$ ,  $+25^\circ\text{C}$ , and  $+125^\circ\text{C}$ . The  $TCV_{OUT}$  for the C grade is fully tested over three temperatures:  $0^\circ\text{C}$ ,  $+25^\circ\text{C}$ , and  $+70^\circ\text{C}$ . This parameter is specified using two methods. The box method is the most common method and accounts for the temperature coefficient over the full temperature range, whereas the bowtie method calculates the worst case slope from  $+25^\circ\text{C}$  and is therefore more useful for systems which are calibrated at  $+25^\circ\text{C}$ .

### Box Method

The box method is represented by the following equation:

$$TCV_{OUT} = \left| \frac{\max\{V_{OUT}(T_1, T_2, T_3)\} - \min\{V_{OUT}(T_1, T_2, T_3)\}}{V_{OUT}(T_2) \times (T_3 - T_1)} \right| \times 10^6$$

where:

$TCV_{OUT}$  is expressed in ppm/ $^\circ\text{C}$ .

$V_{OUT}(T_x)$  is the output voltage at Temperature  $T_x$ .

$T_1 = -40^\circ\text{C}$ .

$T_2 = +25^\circ\text{C}$ .

$T_3 = +125^\circ\text{C}$ .

This box method ensures that  $TCV_{OUT}$  accurately portrays the maximum difference between any of the three temperatures at which the output voltage of the device is measured.

### Bowtie Method

The bowtie method is represented by the following equation:

$$TCV_{OUT} = |\max\{TCV_{OUT1}, TCV_{OUT2}\}|$$

where:

$$TCV_{OUT1} = \left| \frac{\max\{V_{OUT}(T_1, T_2)\} - \min\{V_{OUT}(T_1, T_2)\}}{V_{OUT}(T_2) \times (T_2 - T_1)} \right| \times 10^6$$

$$TCV_{OUT2} = \left| \frac{\max\{V_{OUT}(T_2, T_3)\} - \min\{V_{OUT}(T_2, T_3)\}}{V_{OUT}(T_2) \times (T_3 - T_2)} \right| \times 10^6$$

$TCV_{OUT}$  is expressed in ppm/ $^\circ\text{C}$ .

$V_{OUT}(T_x)$  is the output voltage at Temperature  $T_x$ .

$T_1 = 0^\circ\text{C}$ .

$T_2 = +25^\circ\text{C}$ .

$T_3 = +70^\circ\text{C}$ .

### Thermally Induced Output Voltage Hysteresis ( $\Delta V_{OUT\_HYS}$ )

Thermally induced output voltage hysteresis represents the change in the output voltage after the device is exposed to a specified temperature cycle. This is expressed as a difference in ppm from the nominal output.

$$\Delta V_{OUT\_HYS} = \frac{V_{OUT1\_25^\circ\text{C}} - V_{OUT2\_25^\circ\text{C}}}{V_{OUT\_25^\circ\text{C}}} \times 10^6 [\text{ppm}]$$

where:

$V_{OUT1\_25^\circ\text{C}}$  is the output voltage at  $25^\circ\text{C}$ .

$V_{OUT2\_25^\circ\text{C}}$  is the output voltage after temperature cycling.

### Long-Term Stability ( $\Delta V_{OUT\_LTD}$ )

Long-term stability refers to the shift in the output voltage versus time. This is expressed as a difference in ppm from the nominal output.

$$\Delta V_{OUT\_LTD} = \left| \frac{V_{OUT}(t_1) - V_{OUT}(t_0)}{V_{OUT}(t_0)} \right| \times 10^6 [\text{ppm}]$$

where:

$V_{OUT}(t_0)$  is the  $V_{OUT}$  at the starting time of the measurement.

$V_{OUT}(t_1)$  is the  $V_{OUT}$  at the end time of the measurement.

## APPLICATIONS INFORMATION

### BASIC VOLTAGE REFERENCE CONNECTION

The circuit shown in Figure 84 shows the basic configuration for the ADR4520/ADR4525/ADR4530/ADR4533/ADR4540/ADR4550 family of voltage references.

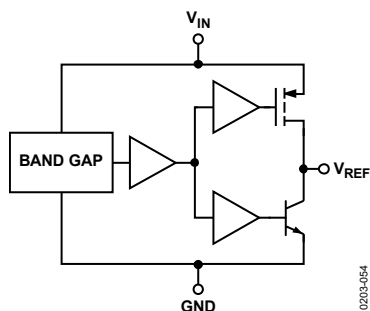


Figure 84. ADR4520/ADR4525/ADR4530/ADR4533/ADR4540/ADR4550 Simplified Schematic

### INPUT AND OUTPUT CAPACITORS

#### Input Capacitors

A 1  $\mu\text{F}$  to 10  $\mu\text{F}$  electrolytic or ceramic capacitor can be connected to the input to improve transient response in applications where the supply voltage may fluctuate. It is recommended to connect an additional 0.1  $\mu\text{F}$  ceramic capacitor in parallel to reduce supply noise.

#### Output Capacitors

An output capacitor is required for stability and to filter out low level voltage noise. The minimum value of the output capacitor ( $C_{\text{OUT}}$ ) is shown in Table 12.

Table 12. Minimum  $C_{\text{OUT}}$  Value

Part Number	Minimum $C_{\text{OUT}}$ Value
ADR4520, ADR4525	1.0 $\mu\text{F}$
ADR4530, ADR4533, ADR4540, ADR4550	0.1 $\mu\text{F}$

An additional 1  $\mu\text{F}$  to 10  $\mu\text{F}$  electrolytic or ceramic capacitor can be added in parallel to improve transient performance in response to sudden changes in load current; however, doing so increases the turn-on time of the device.

### LOCATION OF REFERENCE IN SYSTEM

It is recommended to place the ADR4520/ADR4525/ADR4530/ADR4533/ADR4540/ADR4550 reference as close to the load as possible to minimize the length of the output traces and, therefore, the error introduced by the voltage drop. Current flowing through a PCB trace produces a voltage drop; with longer traces, this drop can reach several millivolts or more, introducing considerable error into the output voltage of the reference. A 1-inch long, 5 mm wide trace of 1-ounce copper has a resistance of approximately 100 m $\Omega$  at room temperature; at a load current of 10 mA, this resistance can introduce a full millivolt of error.

### POWER DISSIPATION

The ADR4520/ADR4525/ADR4530/ADR4533/ADR4540/ADR4550 voltage references are capable of sourcing and sinking up to 10 mA of load current at room temperature across the rated input voltage range. However, when used in applications subject to high ambient temperatures, the input voltage and load current must be monitored carefully to ensure that the device does not exceed its maximum power dissipation rating. The maximum power dissipation of the device can be calculated using the following equation:

$$P_D = \frac{T_J - T_A}{\theta_{JA}}$$

where:

$P_D$  is the device power dissipation.

$T_J$  is the device junction temperature.

$T_A$  is the ambient temperature.

$\theta_{JA}$  is the package (junction to air) thermal resistance.

This relationship can cause acceptable load current in high temperature conditions to be less than the maximum current sourcing capability of the device. Do not operate the device outside of its maximum power rating, because doing so can result in premature failure or permanent damage to the device.

### SAMPLE APPLICATIONS

#### Bipolar Output Reference

Figure 85 shows a bipolar reference configuration. By connecting the output of the ADR4550 to the inverting terminal of an operational amplifier, it is possible to obtain both positive and negative reference voltages. R1 and R2 must be matched as closely as possible to ensure minimal difference between the negative and positive outputs. Resistors with low temperature coefficients must also be used if the circuit is deployed in environments with large temperature swings; otherwise, a voltage difference develops between the two outputs as the ambient temperature changes.

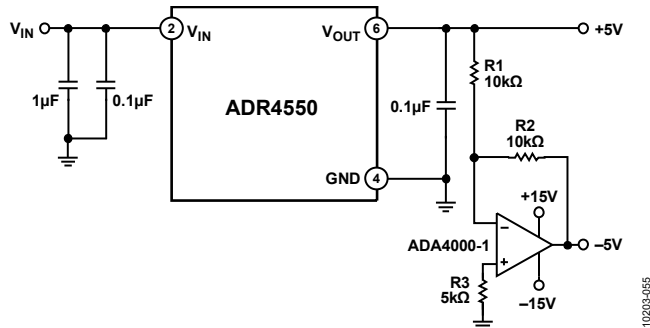


Figure 85. ADR4550 Bipolar Output Reference

**Boosted Output Current Reference**

Figure 86 shows a configuration for obtaining higher current drive capability from the ADR4520/ADR4525/ADR4530/ADR4533/ADR4540/ADR4550 references without sacrificing accuracy. The op amp regulates the current flow through the metal-oxide semiconductor field effect transistor (MOSFET) until  $V_{OUT}$  equals the output voltage of the reference; current is then drawn directly from  $V_{IN}$  instead of from the reference itself, allowing increased current drive capability.



Figure 86. Boosted Output Current Reference

Because the current sourcing capability of this circuit depends only on the current rating of the MOSFET, the output drive capability can be adjusted to the application simply by choosing an appropriate MOSFET. In all cases, tie the  $V_{OUT}$  pin directly to the load device to maintain maximum output voltage accuracy.

**LONG-TERM DRIFT**

The stability of a precision signal path over its lifetime or between calibration procedures is dependent on the long-term stability of the analog components in the path, such as op amps, references, and data converters. To help system designers predict the long-term drift of circuits that use the ADR4520/ADR4525/ADR4530/ADR4533/ADR4540/ADR4550, Analog Devices measured the output voltage of multiple units for more than 4500 hours (more than 6 months) using a high precision measurement system, including an ultrastable oil bath. To replicate real-world system performance, the devices under test (DUTs) were soldered onto an FR4 PCB using a standard reflow profile (as defined in the JEDEC J-STD-020D standard), rather than testing them in sockets. This manner of testing is important because expansion and contraction of the PCB can apply stress to the integrated circuit (IC) package and contribute to shifts in the offset voltage.

Figure 87 shows the long-term drift of the ADR4520/ADR4525/ADR4530/ADR4533/ADR4540/ADR4550. Sample 1, Sample 2, and Sample 3 plot traces show sample units. The mean drift after 4500 hours is 51 ppm. Note that the early life drift (0 hours to 250 hours) accounts for 40% of the total drift observed over 4500 hours, as shown in Figure 88. The first 1000 hours account for 50% of the total drift, and the remaining 3500 hours account for the remaining 50% of the drift. Thus, the early life drift is the dominant contributor, whereas the drift after 1000 hours is significantly lower.

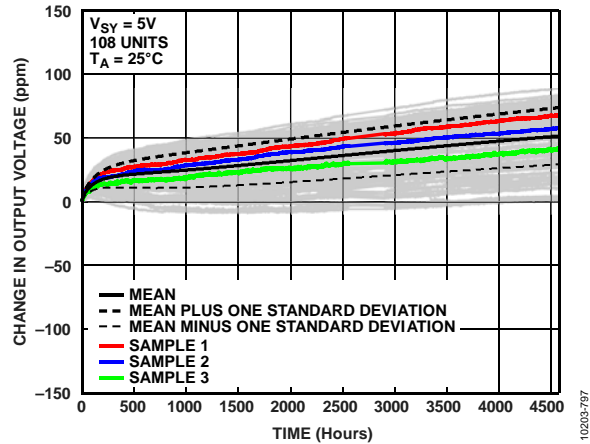


Figure 87. Measured Long-Term Drift of the ADR4520/ADR4525/ADR4530/ADR4533/ADR4540/ADR4550 over 4,500 Hours

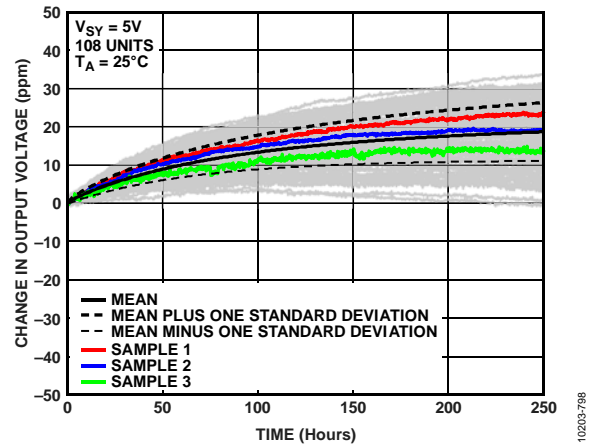


Figure 88. Measured Early Life Drift of the ADR4520/ADR4525/ADR4530/ADR4533/ADR4540/ADR4550



**THERMAL HYSTERESIS**

In addition to stability over time, as described in the Long-Term Drift section, it is useful to know the thermal hysteresis, that is, the stability vs. cycling of temperature. Thermal hysteresis is an important parameter because it tells the system designer how closely the signal returns to its starting amplitude after the ambient temperature changes and the subsequent return to room temperature. Figure 89 shows the change in output voltage as the temperature cycles three times from room temperature to +125°C to -40°C and back to room temperature.

In the three full cycles, the output hysteresis is typically -13 ppm. The histogram in Figure 90 shows that the hysteresis is larger when the device is cycled through only a half cycle, from room temperature to 125°C and back to room temperature, typically -97 ppm.



Figure 89. Change in Output Voltage over Three Full Temperature Cycles (-40°C to +125°C)

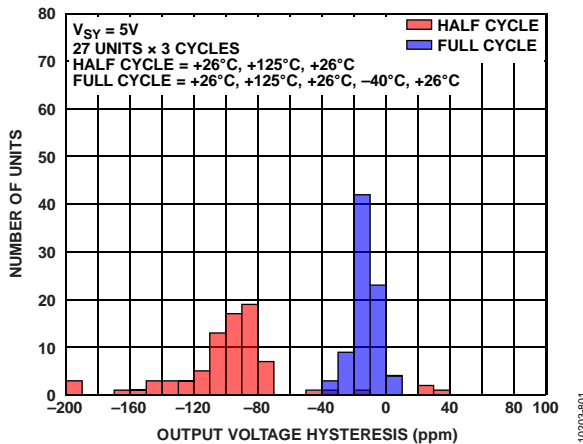


Figure 90. Histogram Showing the Temperature Hysteresis of the Output Voltage (-40°C to +125°C)

Figure 91 shows the change in input offset voltage as the temperature cycles three times from room temperature to +70°C to 0°C and back to room temperature. In the three full cycles, the output hysteresis is typically -8 ppm. The histogram in Figure 92 shows that the hysteresis is larger when the device is cycled through only a half cycle, from room temperature to +70°C and back to room temperature, typically -17 ppm.



Figure 91. Change in Output Voltage over Three Full Temperature Cycles (0°C to 70°C)



Figure 92. Histogram Showing the Temperature Hysteresis of the Output Voltage (0°C to 70°C)

Measuring thermal hysteresis over the full operating temperature range is not reflective of a typical operating environment in most applications. Instead, smaller temperature variations are more normal. The ADR4520/ADR4525/ADR4530/ADR4533/ADR4540/ADR4550 were tested over 20 different temperature cycles of increasing magnitude, centered at +25°C, starting with +25°C ± 5°C and going up to the full operating temperature range of -40°C to +125°C. The results are shown in Figure 93.

For a temperature delta of 100°C (that is, +25°C ± 50°C) the thermal hysteresis is less than 20 ppm for both the full cycle and the half cycle. Above this range, the thermal hysteresis increases significantly. These results show that the standard specification, which covers the full operating temperature range, is close to the worst case performance.

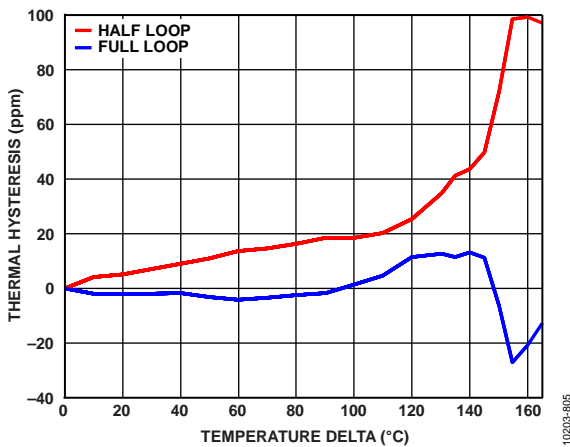


Figure 93. Thermal Hysteresis for Increasing Temperature Range

**HUMIDITY SENSITIVITY**

The ADR4520/ADR4525/ADR4530/ADR4533/ADR4540/ADR4550 is packaged in a SOIC plastic package and has a moisture sensitivity level of MSL-1, per the JEDEC standard. However, moisture absorption from the air into the package changes the internal mechanical stresses on the die causing shifts in the output voltage. Figure 94 shows the effects of a step change in relative humidity on the output voltage over time. The humidity chamber is maintained at an ambient temperature of +25°C, while the relative humidity undergoes a step change from 20% to 80% at time zero. The relative humidity is maintained at 80% for the duration of the testing. Note that the output voltage shifts quickly compared to the overall settling time, following the step change in relative humidity.

Figure 95 shows the effects of 10% increases in relative humidity from 30% to 70% and back to 30%. Note that after the relative humidity returns to 30%, the output voltage is settling back to its starting point.

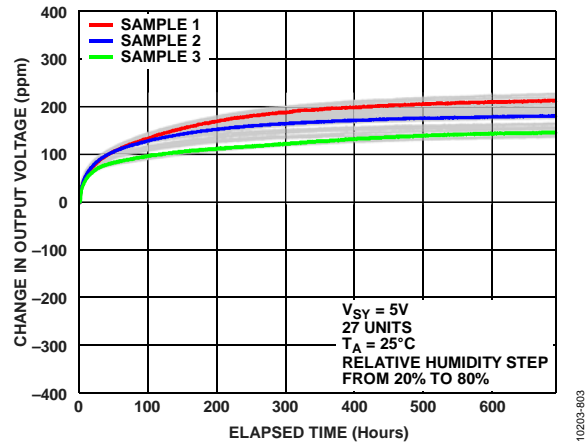


Figure 94. Change in Output Voltage vs. Time After Humidity Step Change (20% to 80% Relative Humidity)

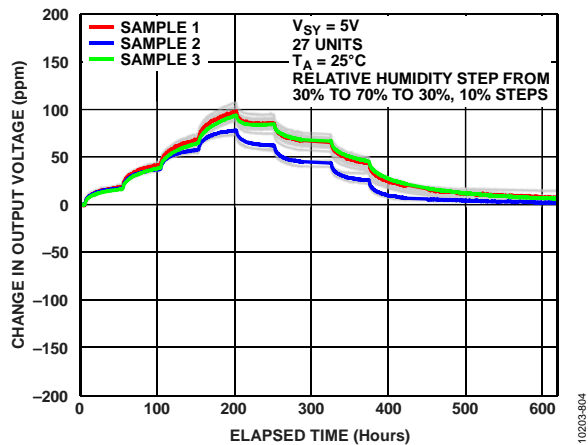


Figure 95. Change in Output Voltage vs. Time for 10% Humidity Steps (30% to 70% to 30% Relative Humidity in 10% Steps)

## POWER CYCLE HYSTERESIS

By power cycling large numbers of samples, the power cycle hysteresis can be determined. To keep this measurement independent of other variables and environmental effects, the power cycle testing was performed using a high precision measurement system, including an ultrastable oil bath.

Figure 96 shows the power cycle hysteresis. The units were powered down for approximately four hours and then powered up. The ADR4520/ADR4525/ADR4530/ADR4533/ADR4540/ADR4550 do not have any power cycle hysteresis even after a long power-down period, making these devices very suitable for equipment which must maintain its calibration accuracy between power cycles.

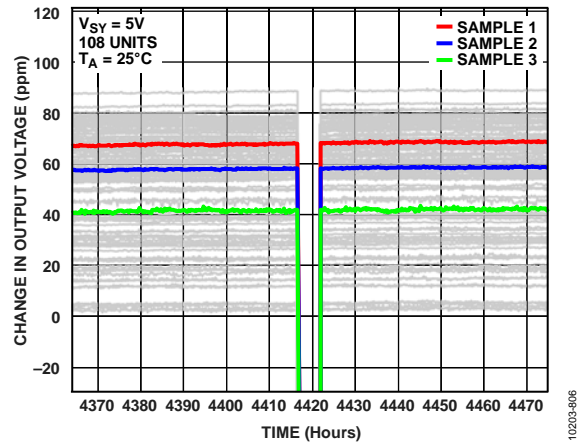


Figure 96. Power Cycle Hysteresis

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 97. 8-Lead Standard Small Outline Package [SOIC\_N]  
 Narrow Body  
 (R-8)  
 Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model <sup>1,2</sup>	Temperature Range	Package Description	Package Option	Ordering Quantity
ADR4520ARZ	-40°C to +125°C	8-Lead SOIC_N	R-8	98
ADR4520ARZ-R7	-40°C to +125°C	8-Lead SOIC_N	R-8	1,000
ADR4520BRZ	-40°C to +125°C	8-Lead SOIC_N	R-8	98
ADR4520BRZ-R7	-40°C to +125°C	8-Lead SOIC_N	R-8	1,000
ADR4525ARZ	-40°C to +125°C	8-Lead SOIC_N	R-8	98
ADR4525ARZ-R7	-40°C to +125°C	8-Lead SOIC_N	R-8	1,000
ADR4525BRZ	-40°C to +125°C	8-Lead SOIC_N	R-8	98
ADR4525BRZ-R7	-40°C to +125°C	8-Lead SOIC_N	R-8	1,000
ADR4525CRZ	0°C to 70°C	8-Lead SOIC_N	R-8	98
ADR4525CRZ-R7	0°C to 70°C	8-Lead SOIC_N	R-8	1,000
ADR4525WBRZ-R7	-40°C to +125°C	8-Lead SOIC_N	R-8	1,000
ADR4530ARZ	-40°C to +125°C	8-Lead SOIC_N	R-8	98
ADR4530ARZ-R7	-40°C to +125°C	8-Lead SOIC_N	R-8	1,000
ADR4530BRZ	-40°C to +125°C	8-Lead SOIC_N	R-8	98
ADR4530BRZ-R7	-40°C to +125°C	8-Lead SOIC_N	R-8	1,000
ADR4533ARZ	-40°C to +125°C	8-Lead SOIC_N	R-8	98
ADR4533ARZ-R7	-40°C to +125°C	8-Lead SOIC_N	R-8	1,000
ADR4533BRZ	-40°C to +125°C	8-Lead SOIC_N	R-8	98
ADR4533BRZ-R7	-40°C to +125°C	8-Lead SOIC_N	R-8	1,000
ADR4540ARZ	-40°C to +125°C	8-Lead SOIC_N	R-8	98
ADR4540ARZ-R7	-40°C to +125°C	8-Lead SOIC_N	R-8	1,000
ADR4540BRZ	-40°C to +125°C	8-Lead SOIC_N	R-8	98
ADR4540BRZ-R7	-40°C to +125°C	8-Lead SOIC_N	R-8	1,000
ADR4540CRZ	0°C to 70°C	8-Lead SOIC_N	R-8	98
ADR4540CRZ-R7	0°C to 70°C	8-Lead SOIC_N	R-8	1,000

Model <sup>1,2</sup>	Temperature Range	Package Description	Package Option	Ordering Quantity
ADR4550ARZ	–40°C to +125°C	8-Lead SOIC_N	R-8	98
ADR4550ARZ-R7	–40°C to +125°C	8-Lead SOIC_N	R-8	1,000
ADR4550BRZ	–40°C to +125°C	8-Lead SOIC_N	R-8	98
ADR4550BRZ-R7	–40°C to +125°C	8-Lead SOIC_N	R-8	1,000
ADR4550CRZ	0°C to 70°C	8-Lead SOIC_N	R-8	98
ADR4550CRZ-R7	0°C to 70°C	8-Lead SOIC_N	R-8	1,000

<sup>1</sup> Z = RoHS Compliant Part.

<sup>2</sup> W = Qualified for Automotive Applications. See the Automotive Products section.

## AUTOMOTIVE PRODUCTS

The ADR4525W model is available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that this automotive model may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade product shown is available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for this model.