EL5162, EL5163, EL5262, EL5263, EL5362

500MHz Low Power Current Feedback Amplifiers with Enable

FN7388
Rev 1.00
August 26, 2015

The EL5162, EL5163, EL5262, EL5263 and EL5362 are current feedback amplifiers with a bandwidth of 500MHz. This makes these amplifiers ideal for today's high speed video and monitor applications.

With a supply current of just 1.5mA per amplifier and the ability to run from a single supply voltage from 5V to 12V, these amplifiers are also ideal for handheld, portable or battery-powered equipment.

The EL5162, EL5262 and EL5362 also incorporate an enable and disable function to reduce the supply current to 14µA typical per amplifier. Allowing the $\overline{CE}$ pin to float or applying a low logic level enables the amplifier.

The EL5162 is available in 6 Ld SOT-23 and 8 Ld SOIC packages, the EL5163 in 5 Ld SOT-23 and SC-70 packages, the EL5262 in the 10 Ld MSOP package, the EL5263 in 8 Ld MSOP and SOIC packages, and the EL5362 in 16 Ld SOIC (0.150") and QSOP packages. All operate over the industrial temperature range of -40°C to +85°C.

Features

- 500MHz -3dB bandwidth
- 4000V/µs slew rate (EL5162 and EL5163)
- 1.5mA supply current per amplifier
- Single and dual supply operation, from 5V to 12V supply span
- Fast enable/disable (EL5162, EL5262 and EL5362 only)
- Available in SOT-23 packages
- Pb-free (RoHS compliant)
- High speed, 1.4GHz product available (EL5166 and EL5167)
- High speed, 4mA, 600MHz product available (EL5164, EL5165 and EL5364)

Applications

- Battery-powered equipment
- Handheld portable devices
- Video amplifiers
- Cable drivers
- RGB amplifiers
- Test equipment
- Instrumentation
- Current to voltage converters

Ordering Information

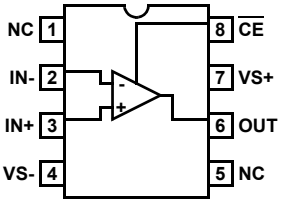
PART NUMBER (Notes 2, 3)	PART MARKING	PACKAGE (RoHS Compliant)	PKG. DWG. #
EL5162ISZ	5162ISZ	8 Ld SOIC (150mil)	M8.15E
EL5162ISZ-T7 (Note 1)	5162ISZ	8 Ld SOIC (150mil)	M8.15E
EL5162ISZ-T13 (Note 1)	5162ISZ	8 Ld SOIC (150mil)	M8.15E
EL5162ISZ-T7A	5162ISZ	8 Ld SOIC (150mil)	M8.15E
EL5162IWZ-T7 (Note 1) (No longer available, recommended replacement: EL5163IWZ-T7)	BAKA (Note 4)	6 Ld SOT-23	P6.064A
EL5162IWZ-T7A (Note 1) (No longer available, recommended replacement: EL5163IWZ-T7A)	BAKA (Note 4)	6 Ld SOT-23	P6.064A
EL5163IWZ-T7 (Note 1)	BALA (Note 4)	5 Ld SOT-23	P5.064A
EL5163IWZ-T7A (Note 1)	BALA (Note 4)	5 Ld SOT-23	P5.064A
EL5163ICZ-T7 (Note 1) (No longer available, recommended replacement: EL5163IWZ-T7)	BDA (Note 4)	5 Ld SC-70 (1.25mm)	P5.049
EL5163ICZ-T7A (Note 1) (No longer available, recommended replacement: EL5163IWZ-T7)	BDA (Note 4)	5 Ld SC-70 (1.25mm)	P5.049
EL5262IYZ	BBTAA	10 Ld MSOP (3.0mm)	M10.118A
EL5262IYZ-T7 (Note 1)	BBTAA	10 Ld MSOP (3.0mm)	M10.118A
EL5262IYZ-T13 (Note 1)	BBTAA	10 Ld MSOP (3.0mm)	M10.118A
EL5263ISZ	5263ISZ	8 Ld SOIC (150mil)	M8.15E
EL5263ISZ-T7 (Note 1)	5263ISZ	8 Ld SOIC (150mil)	M8.15E
EL5263ISZ-T13 (Note 1)	5263ISZ	8 Ld SOIC (150mil)	M8.15E
EL5263IYZ	BBBJA	8 Ld MSOP (3.0mm)	M8.118A
EL5263IYZ-T7 (Note 1)	BBBJA	8 Ld MSOP (3.0mm)	M8.118A
EL5263IYZ-T13 (Note 1)	BBBJA	8 Ld MSOP (3.0mm)	M8.118A
EL5362ISZ	EL5362ISZ	16 Ld SOIC (150mil)	MDP0027
EL5362ISZ-T7 (Note 1)	EL5362ISZ	16 Ld SOIC (150mil)	MDP0027
EL5362ISZ-T13 (Note 1)	EL5362ISZ	16 Ld SOIC (150mil)	MDP0027
EL5362IUZ	5362IUZ	16 Ld QSOP	MDP0040
EL5362IUZ-T7 (Note 1)	5362IUZ	16 Ld QSOP	MDP0040
EL5362IUZ-T13 (Note 1)	5362IUZ	16 Ld QSOP	MDP0040

NOTES:

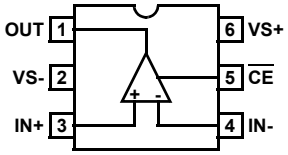
1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see product information page for EL5162, EL5163, EL5262, EL5263, EL5362. For more information on MSL, please see tech brief TB363.
4. The part marking is located on the bottom of the part.

Pin Configurations

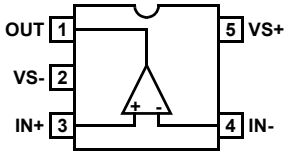
EL5162
(8 LD SOIC)
TOP VIEW



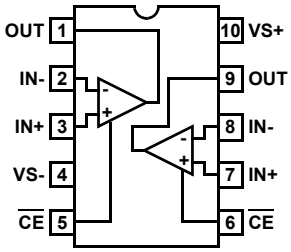
EL5162
(6 LD SOT-23)
TOP VIEW



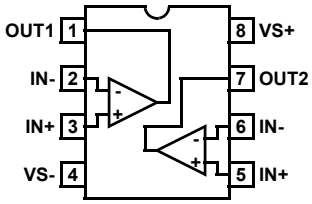
EL5163
(5 LD SOT-23, SC-70)
TOP VIEW



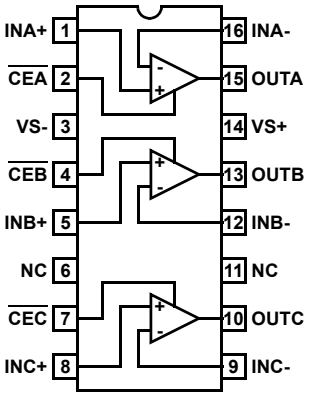
EL5262
(10 LD MSOP)
TOP VIEW



EL5263
(8 LD SOIC, MSOP)
TOP VIEW



EL5362
(16 LD SOIC, QSOP)
TOP VIEW



Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage between V_S+ and V_S- 13.2V
Maximum Continuous Output Current 50mA
Maximum Slew Rate of V_S+ to V_S- 1V/µs
Maximum Voltage between IN+ and IN-, disabled . . . . . ±1.5V
Current into IN+, IN-, CE . . . . . ±5mA
Pin Voltages. . . . . (V_S-) -0.5V to (V_S+) +0.5V

Thermal Information

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Ambient Operating Temperature Range . . . . . -40°C to +85°C
Maximum Operating Junction Temperature . . . . . +125°C
Maximum Power Dissipation . . . . . See Curves on page 8
Pb-free Reflow Profile . . . . . see TB493

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Electrical Specifications

V_S+ = +5V, V_S- = -5V, R_F = 750Ω for A_V = 1, R_F = 400Ω for A_V = 2, R_L = 150Ω, $\overline{CE}$ = 0V, T_A = +25°C unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
AC PERFORMANCE						
BW	-3dB Bandwidth	A_V = +1, R_L = 500Ω, R_F = 598Ω		500		MHz
		A_V = +2, R_L = 150Ω, R_F = 422Ω		233		MHz
BW1	0.1dB Bandwidth			30		MHz
SR	Slew Rate	V_O = -2.5V to +2.5V, A_V = +2, R_L = 100Ω (EL5262, EL5263, EL5362)	**2000**	2500	**4000**	V/µs
		V_O = -2.5V to +2.5V, A_V = +2, R_L = 100Ω (EL5162, EL5163)	**2800**	4000	**6000**	V/µs
t_S	0.1% Settling Time	V_{OUT} = -2.5V to +2.5V, A_V = +1		25		ns
e_N	Input Voltage Noise			3		nV/√Hz
i_N-	IN- Input Current Noise			10		pA/√Hz
i_N+	IN+ Input Current Noise			6.5		pA/√Hz
dG	Differential Gain Error (Note 5)	A_V = +2		0.05		%
dP	Differential Phase Error (Note 5)	A_V = +2		0.15		°
DC PERFORMANCE						
V_{OS}	Offset Voltage		**-5**	1.5	**+5**	mV
T_CV_{OS}	Input Offset Voltage Temperature Coefficient	Measured from T_{MIN} to T_{MAX}		6		µV/°C
R_{OL}	Open Loop Transimpedance Gain		**500**	1000		kΩ
INPUT CHARACTERISTICS						
CMIR	Common Mode Input Range	Guaranteed by CMRR test	**±3**	±3.3		V
CMRR	Common Mode Rejection Ratio	V_{IN} = ±3V	**50**	62	**75**	dB
-ICMR	- Input Current Common Mode Rejection		**-1**	0.22	**+1**	µA/V
+I_{IN}	+ Input Current		**-8**	0.5	**+8**	µA
-I_{IN}	- Input Current		**-10**	2	**+10**	µA
R_{IN}	Input Resistance		**0.8**	1.6	**3**	MΩ
C_{IN}	Input Capacitance			1		pF

Electrical Specifications

V_S+ = +5V, V_S- = -5V, R_F = 750Ω for A_V = 1, R_F = 400Ω for A_V = 2, R_L = 150Ω, $\overline{CE}$ = 0V, T_A = +25°C unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
OUTPUT CHARACTERISTICS						
V_O	Output Voltage Swing	R_L = 150Ω to GND	**±3.35**	±3.6	**±3.75**	V
		R_L = 1kΩ to GND	**±3.75**	±3.9	**±4.15**	V
I_{OUT}	Output Current	R_L = 10Ω to GND	**60**	100		mA
SUPPLY						
I_{SON}	Supply Current - Enabled, per Amplifier	No load, V_{IN} = 0V	**1.3**	1.5	**2.0**	mA
I_{SOFF-}	Supply Current - Disabled, per Amplifier	No load, V_{IN} = 0V (EL5162, EL5262, EL5362 Only)	**-25**	-14	**0**	µA
I_{SOFF+}			**0**	10	**+25**	µA
PSRR	Power Supply Rejection Ratio	DC, V_S = ±4.75V to ±5.25V	**65**	76		dB
-IPSR	- Input Current Power Supply Rejection	DC, V_S = ±4.75V to ±5.25V	**-0.5**	0.1	**+0.5**	µA/V
ENABLE (EL5162, EL5262, EL5362 ONLY)						
t_{EN}	Enable Time			380		ns
t_{DIS}	Disable Time			800		ns
I_{IHCE}	$\overline{CE}$ Pin Input High Current	$\overline{CE}$ = V_S+	**1**	5	**25**	µA
I_{ILCE}	$\overline{CE}$ Pin Input Low Current	$\overline{CE}$ = (V_S+) -5V	**-1**	0	**+1**	µA
V_{IHCE}	$\overline{CE}$ Input High Voltage for Power-down		**(V_S+) - 1**			V
V_{ILCE}	$\overline{CE}$ Input Low Voltage for Power-up				**(V_S+) - 3**	V

NOTES:

5. Standard NTSC test, AC signal amplitude = 286mV_{P-P}, f = 3.58MHz.
6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Performance Curves

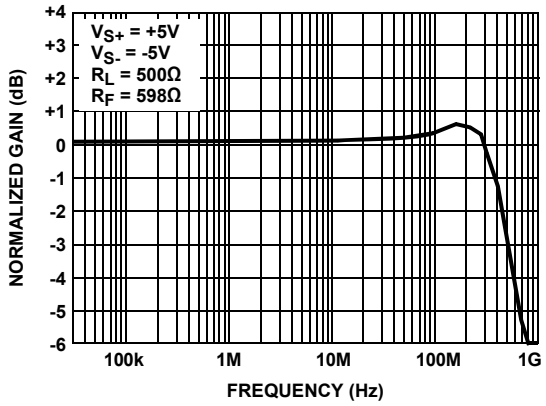


FIGURE 1. FREQUENCY RESPONSE FOR A_V = +1

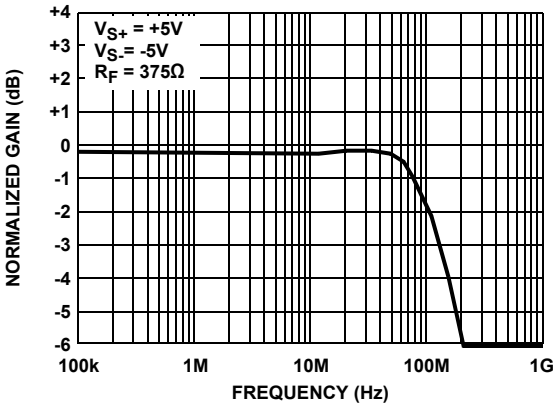


FIGURE 2. FREQUENCY RESPONSE FOR A_V = +4.6

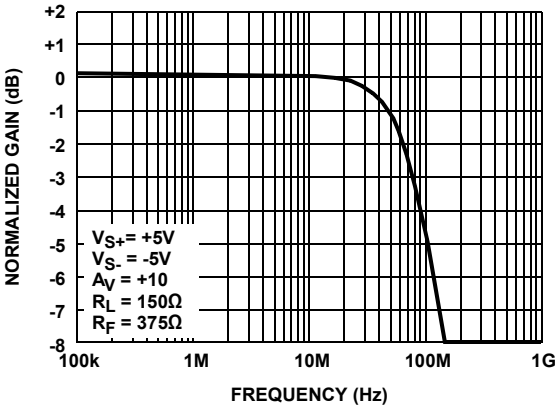


FIGURE 3. FREQUENCY RESPONSE FOR A_V = +10

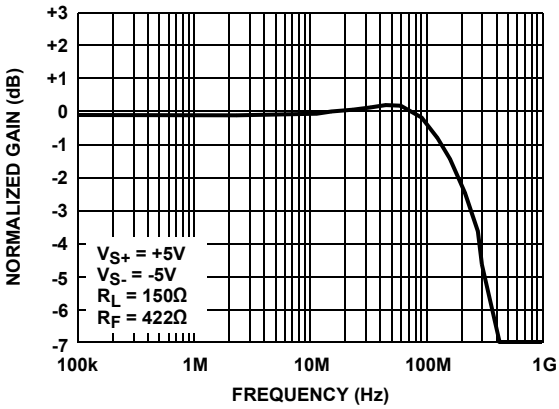


FIGURE 4. FREQUENCY RESPONSE FOR A_V = +2

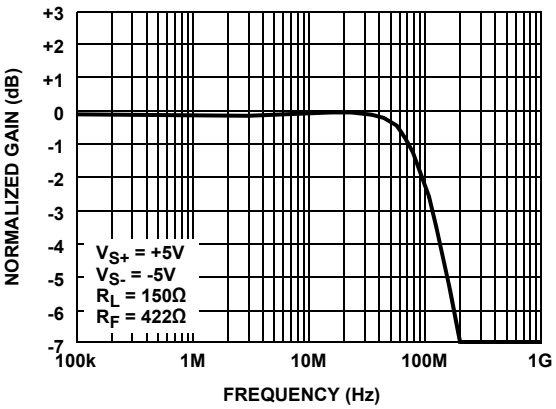


FIGURE 5. FREQUENCY RESPONSE FOR A_V = +4

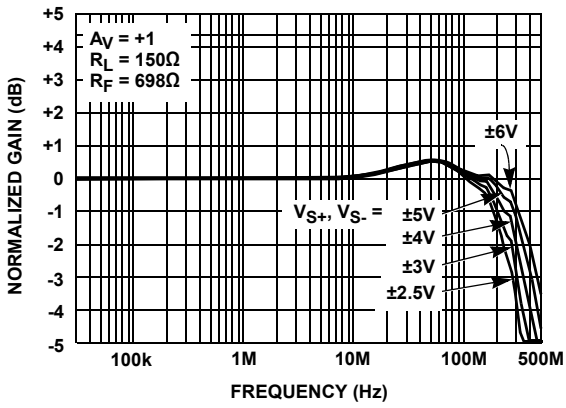


FIGURE 6. FREQUENCY RESPONSE FOR VARIOUS ±V_S

Typical Performance Curves (Continued)

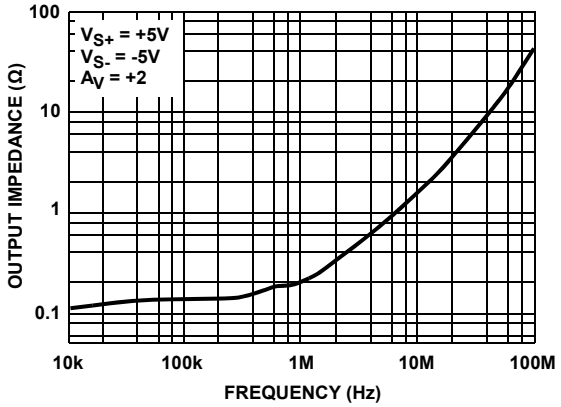


FIGURE 7. CLOSED LOOP OUTPUT IMPEDANCE vs FREQUENCY

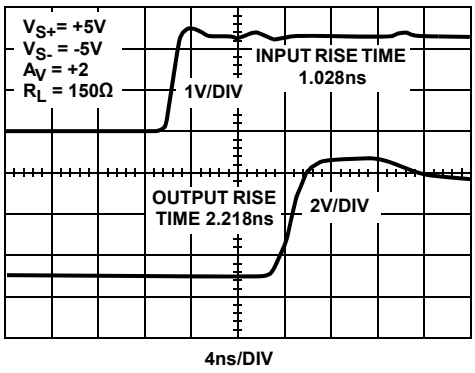


FIGURE 8. EL5262 OUTPUT RISE TIME

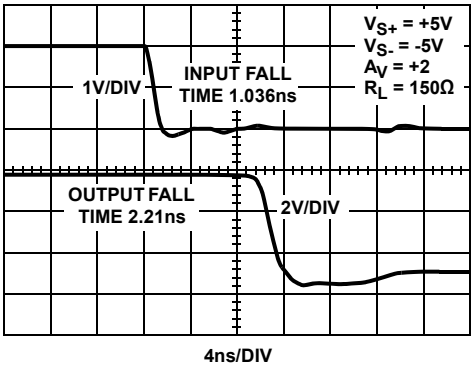


FIGURE 9. EL5262 OUTPUT FALL TIME

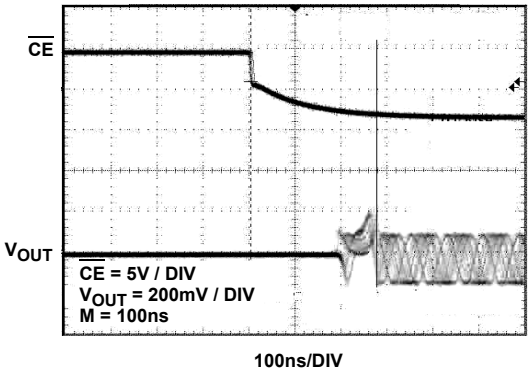


FIGURE 10. TURN ON TIME (EL5162, EL5262, EL5362)

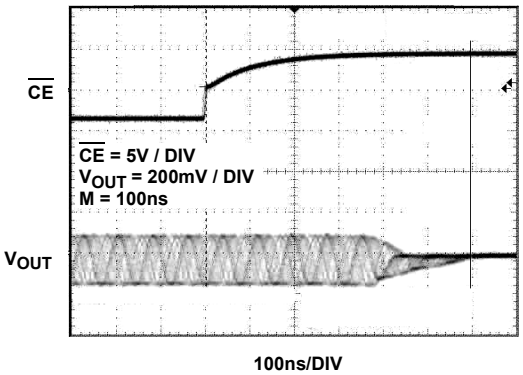


FIGURE 11. TURN OFF TIME (EL5162, EL5262, EL5362)

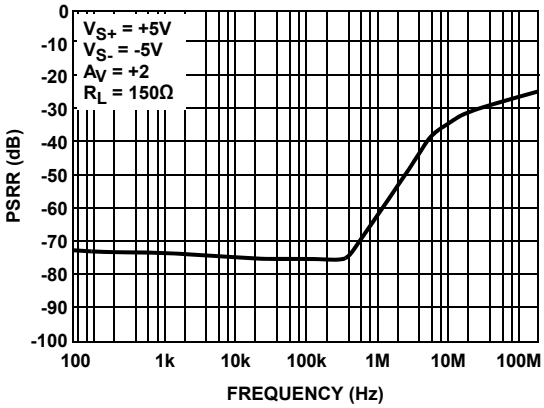


FIGURE 12. PSRR (V_{S+}) vs FREQUENCY

Typical Performance Curves (Continued)

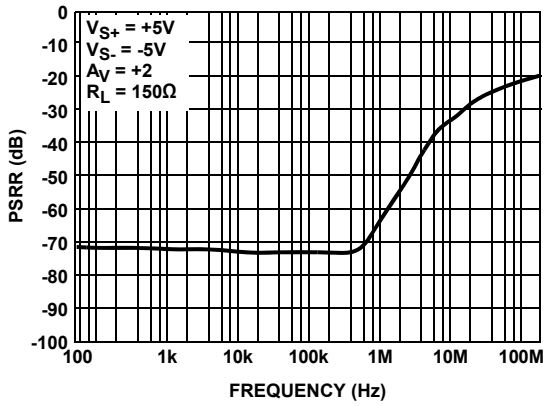


FIGURE 13. PSRR (V_{S-}) vs FREQUENCY

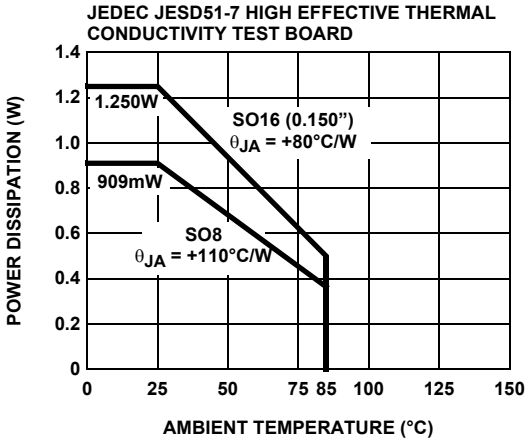


FIGURE 14. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

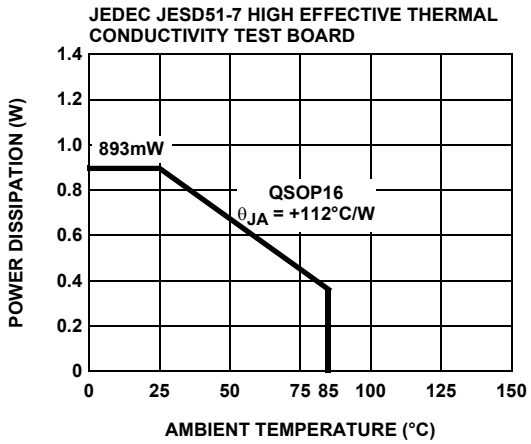


FIGURE 15. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

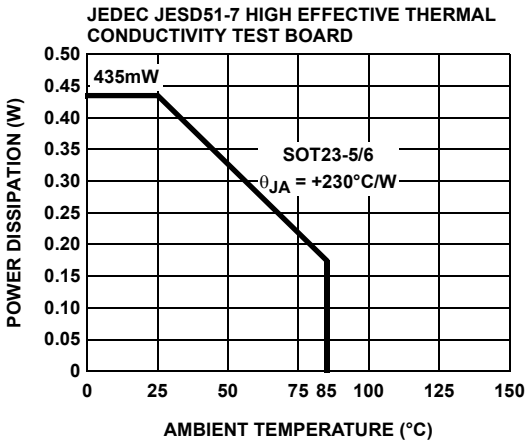


FIGURE 16. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

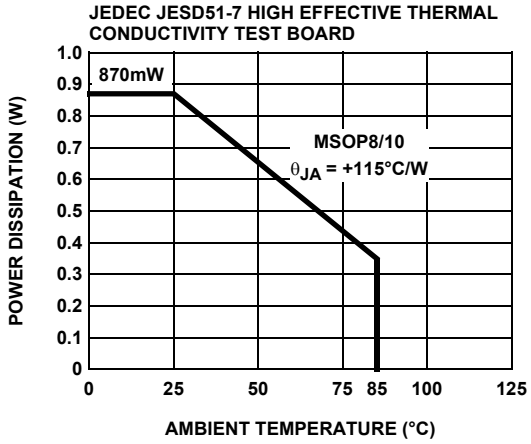


FIGURE 17. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

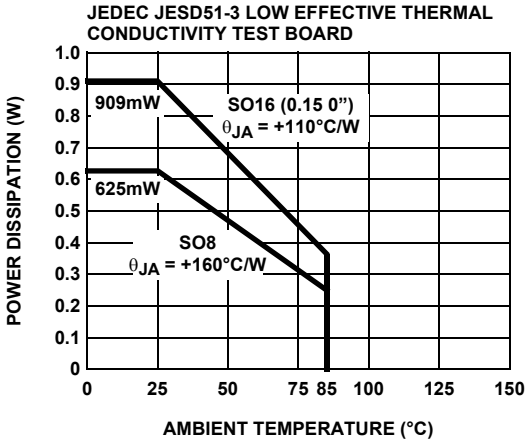


FIGURE 18. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Typical Performance Curves (Continued)

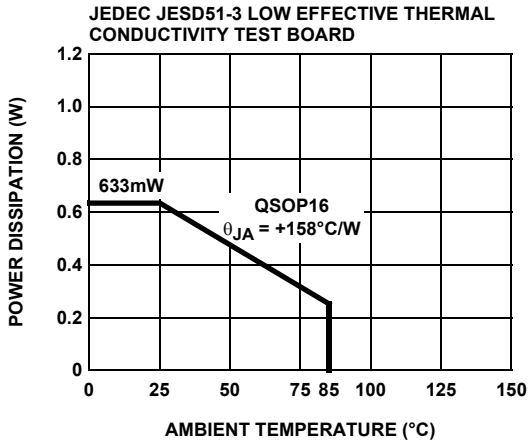


FIGURE 19. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

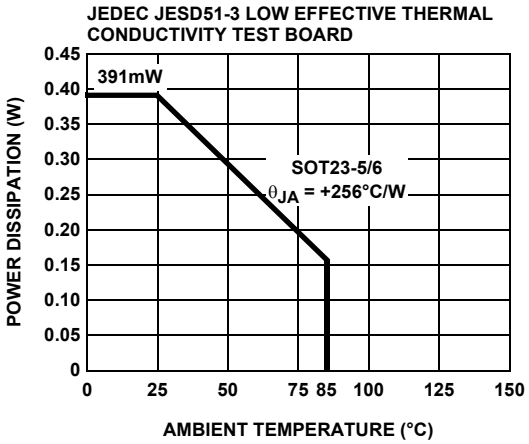


FIGURE 20. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

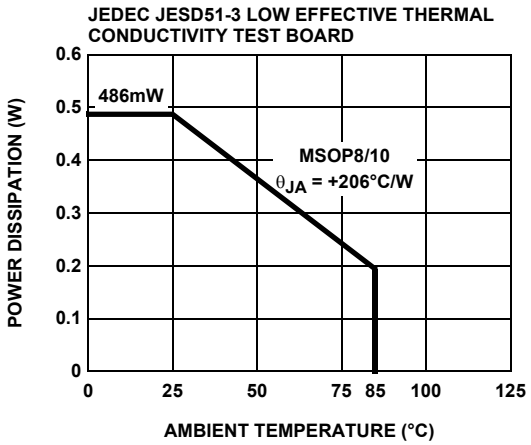


FIGURE 21. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
August 26, 2015	FN7388.13	Updated the Ordering Information table on page 2.
April 6, 2015	FN7388.12	Added Note 4 to the Ordering Information table on page 2. Added Revision History and About Intersil.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

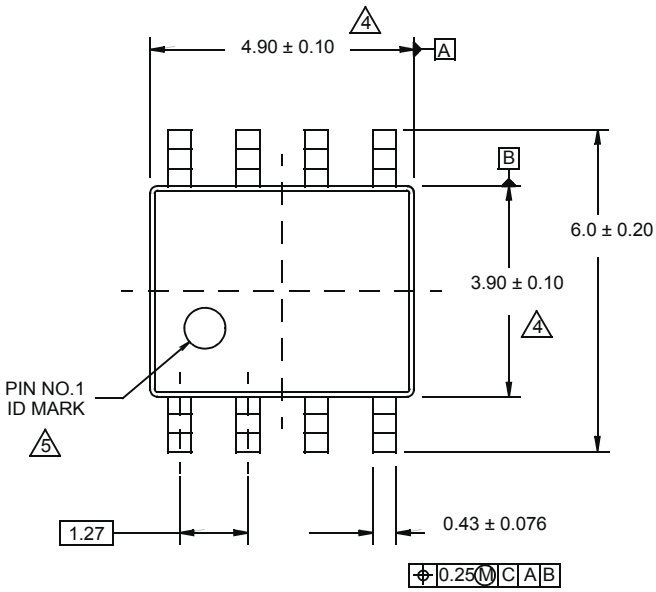
You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support

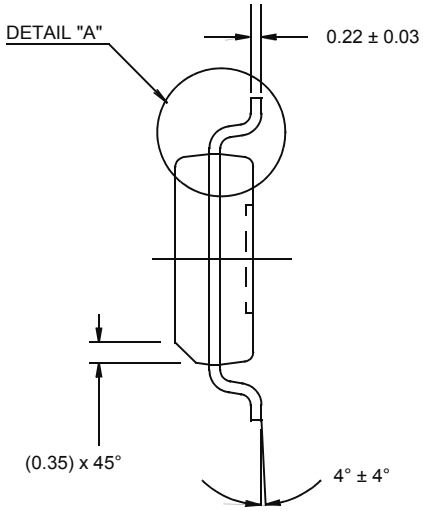
Package Outline Drawing

M8.15E

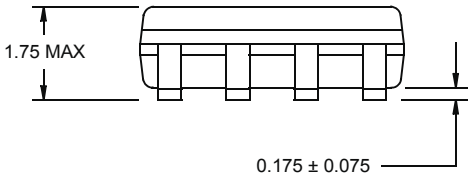
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE
Rev 0, 08/09



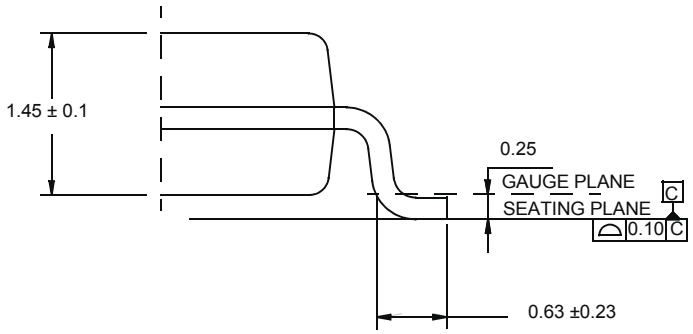
TOP VIEW



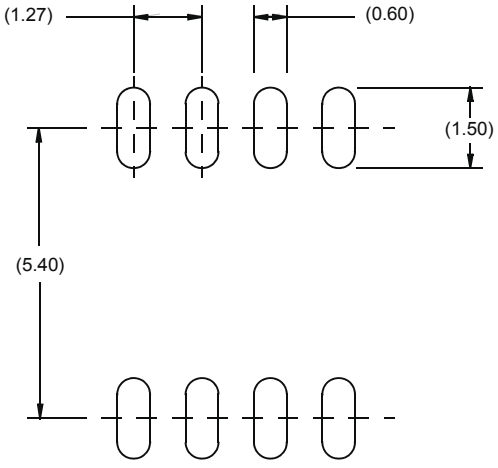
SIDE VIEW "B"



SIDE VIEW "A"



DETAIL "A"



TYPICAL RECOMMENDED LAND PATTERN

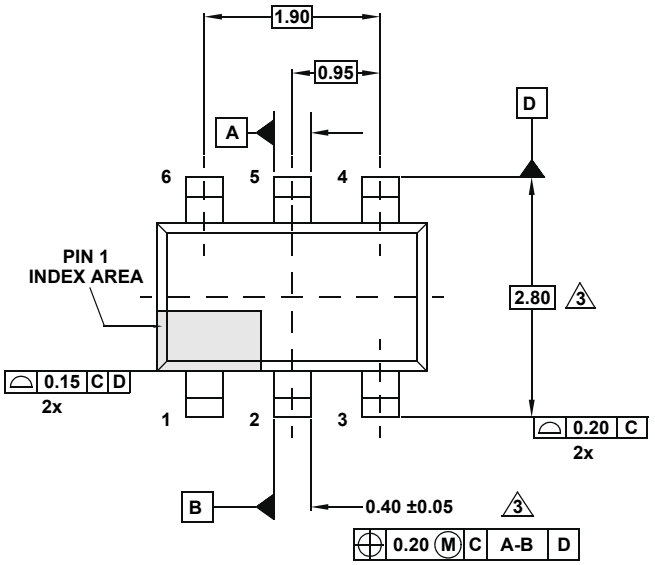
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.

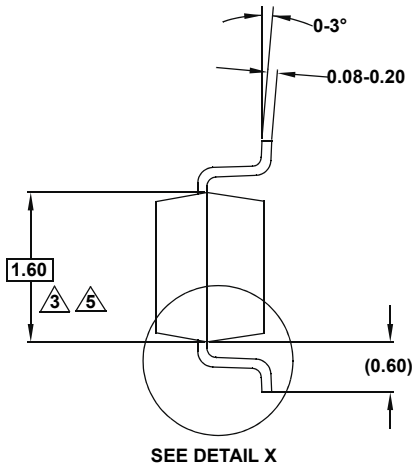
Package Outline Drawing

P6.064A

6 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE
Rev 0, 2/10

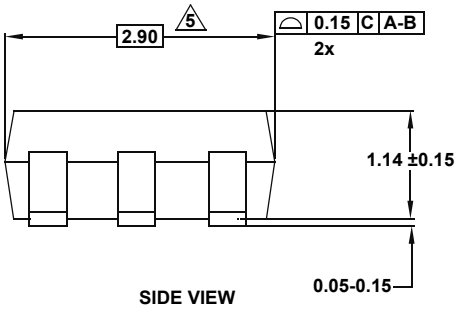


TOP VIEW

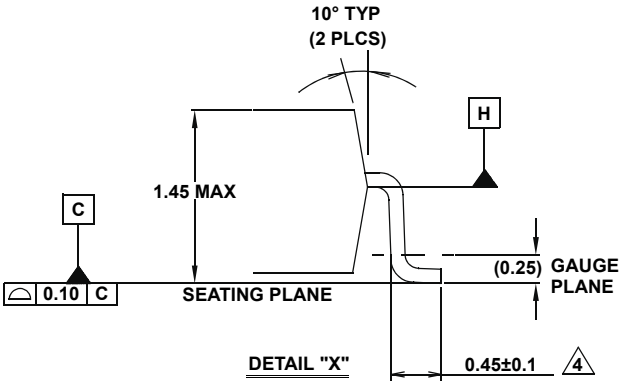


SEE DETAIL X

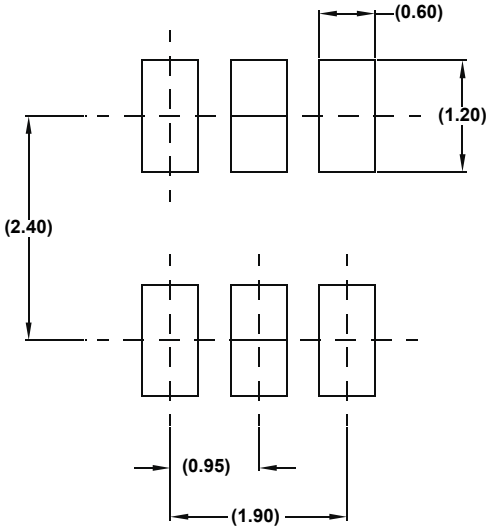
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

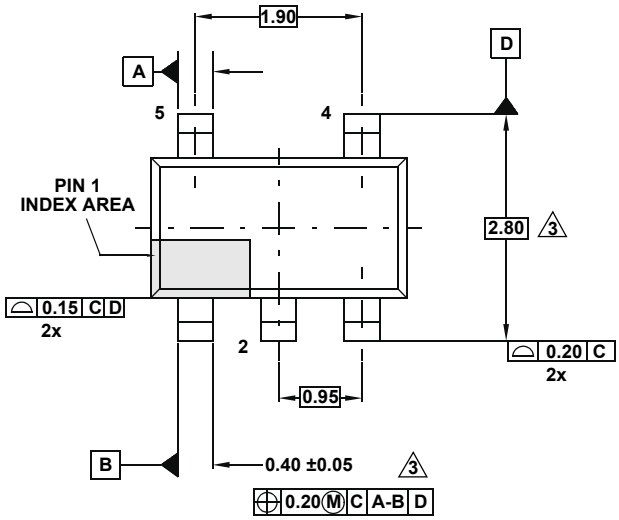
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Dimension is exclusive of mold flash, protrusions or gate burrs.
4. Foot length is measured at reference to guage plane.
5. This dimension is measured at Datum “H”.
6. Package conforms to JEDEC MO-178AA.

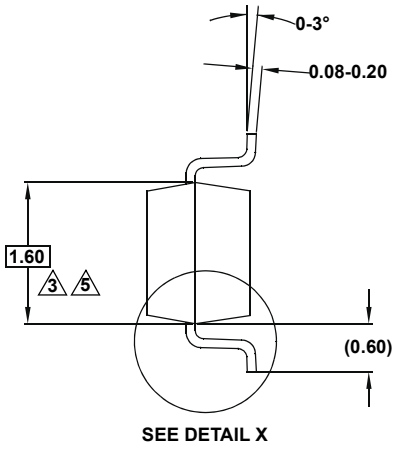
Package Outline Drawing

P5.064A

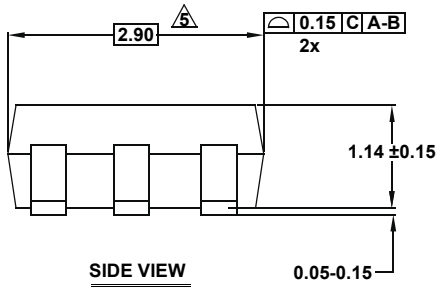
5 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE
Rev 0, 2/10



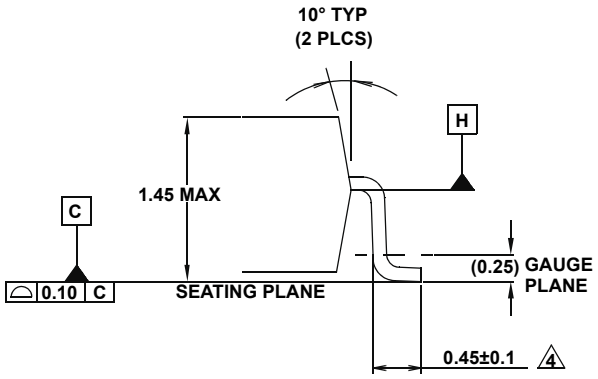
TOP VIEW



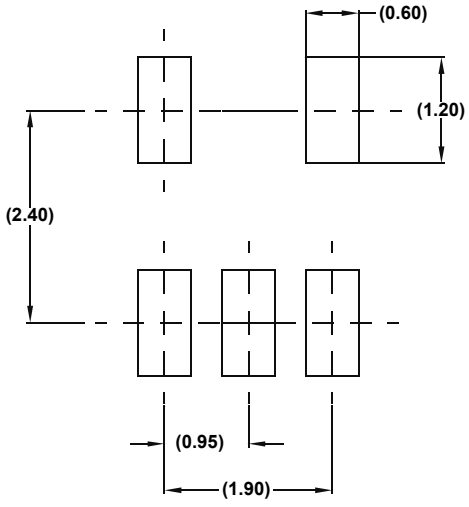
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

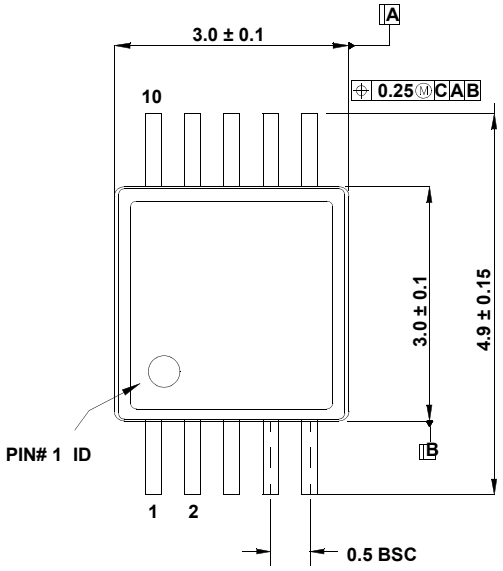
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Dimension is exclusive of mold flash, protrusions or gate burrs.
4. Foot length is measured at reference to guage plane.
5. This dimension is measured at Datum “H”.
6. Package conforms to JEDEC MO-178AA.

Package Outline Drawing

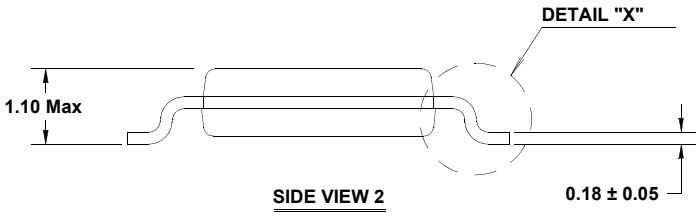
M10.118A (JEDEC MO-187-BA)

10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE (MSOP)

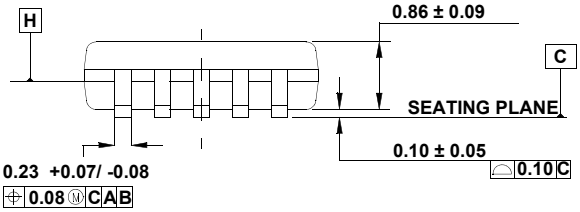
Rev 0, 9/09



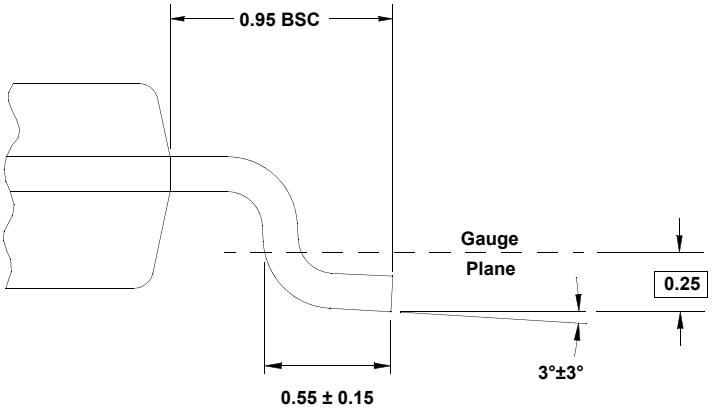
TOP VIEW



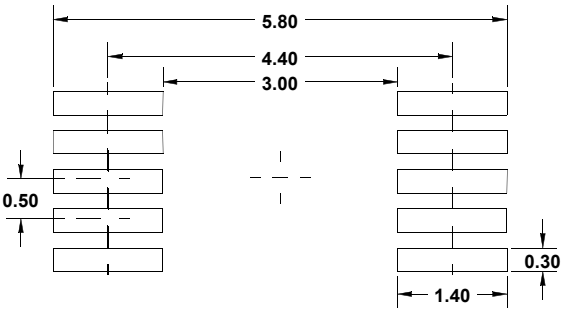
SIDE VIEW 2



SIDE VIEW 1



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

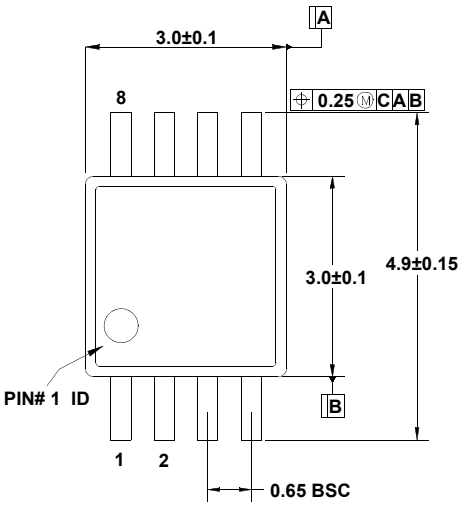
NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.25mm max per side are not included.
5. Dimensions “D” and “E1” are measured at Datum Plane “H”.
6. This replaces existing drawing # MDP0043 MSOP10L.

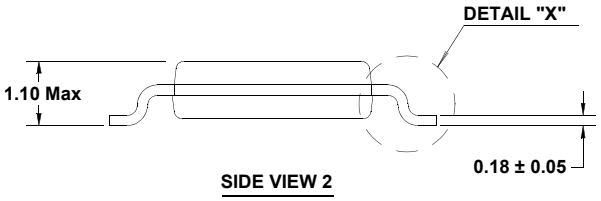
Package Outline Drawing

M8.118A

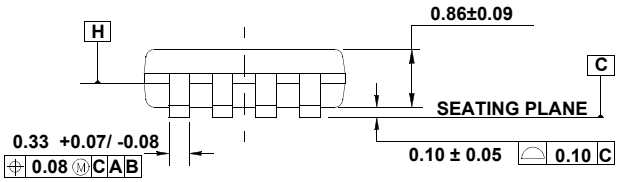
8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE (MSOP)
Rev 0, 9/09



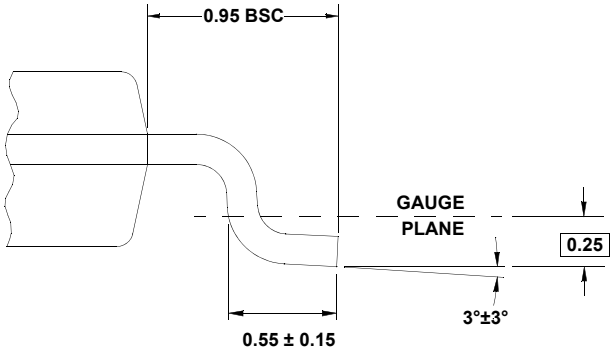
TOP VIEW



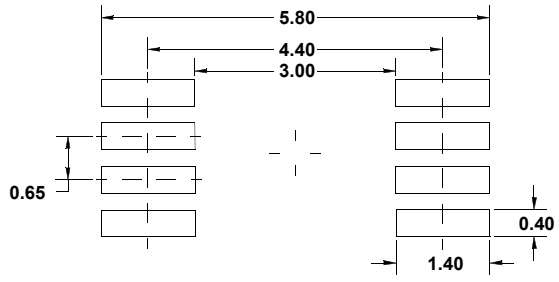
SIDE VIEW 2



SIDE VIEW 1



DETAIL "X"

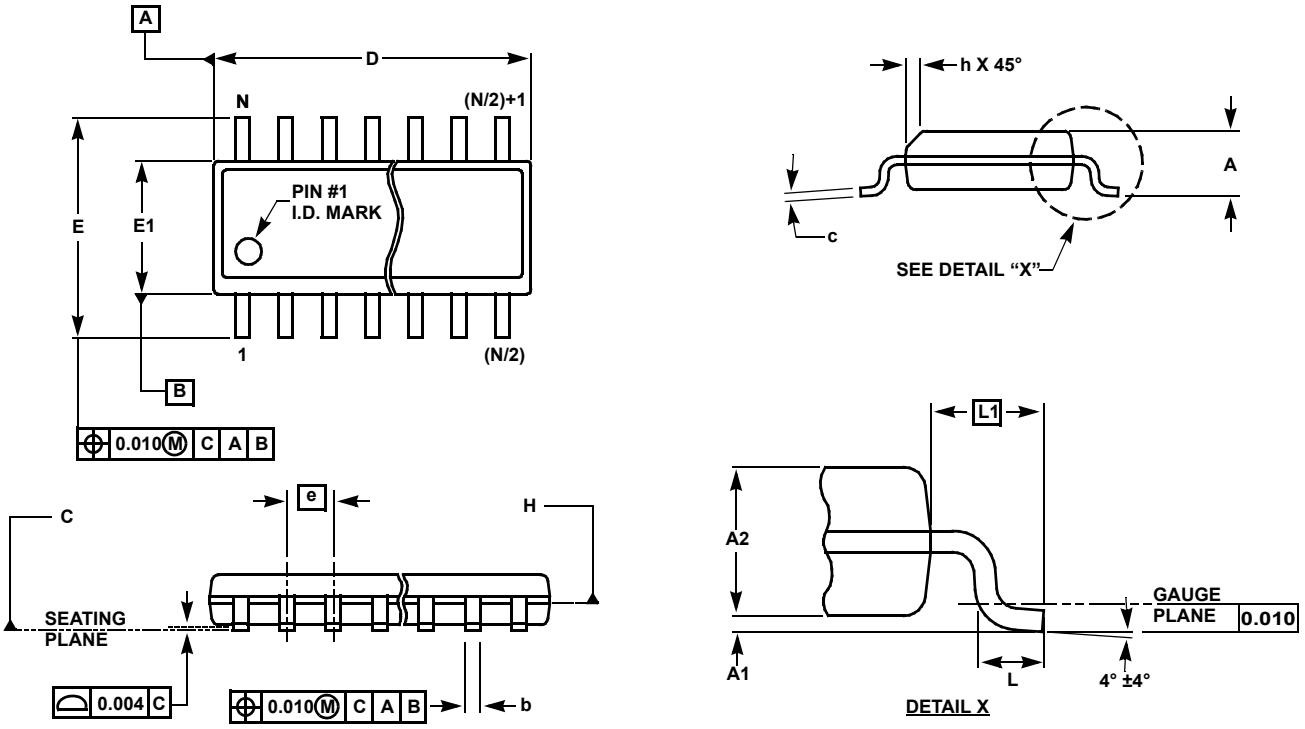


TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSE Y14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.25mm max per side are not included.
5. Dimensions “D” and “E1” are measured at Datum Plane “H”.
6. This replaces existing drawing # MDP0043 MSOP 8L.

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

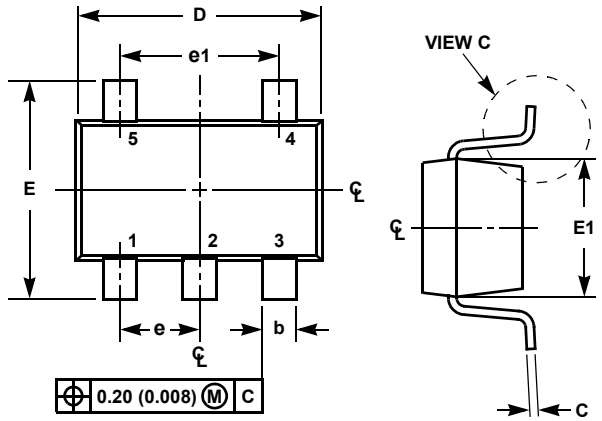
SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

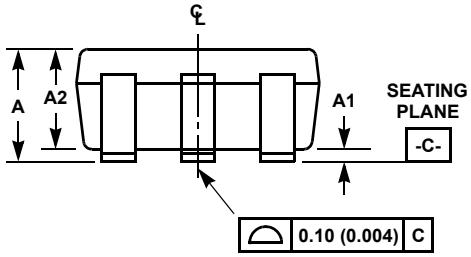
Rev. M 2/07

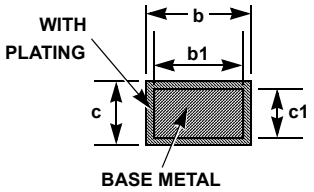
NOTES:

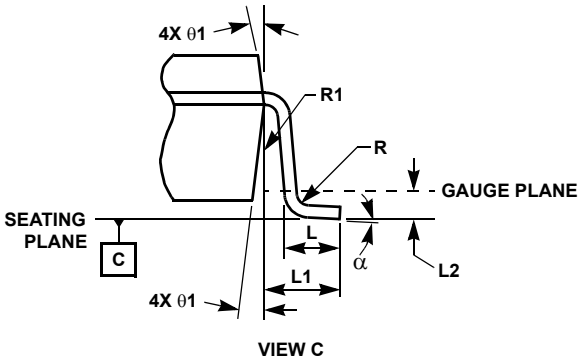
1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

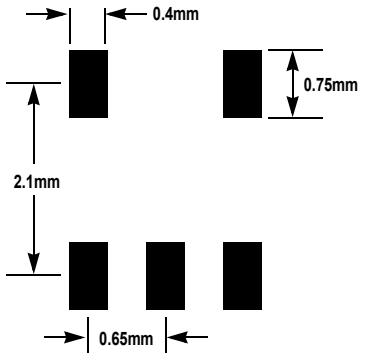
Small Outline Transistor Plastic Packages (SC70-5)











P5.049

5 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

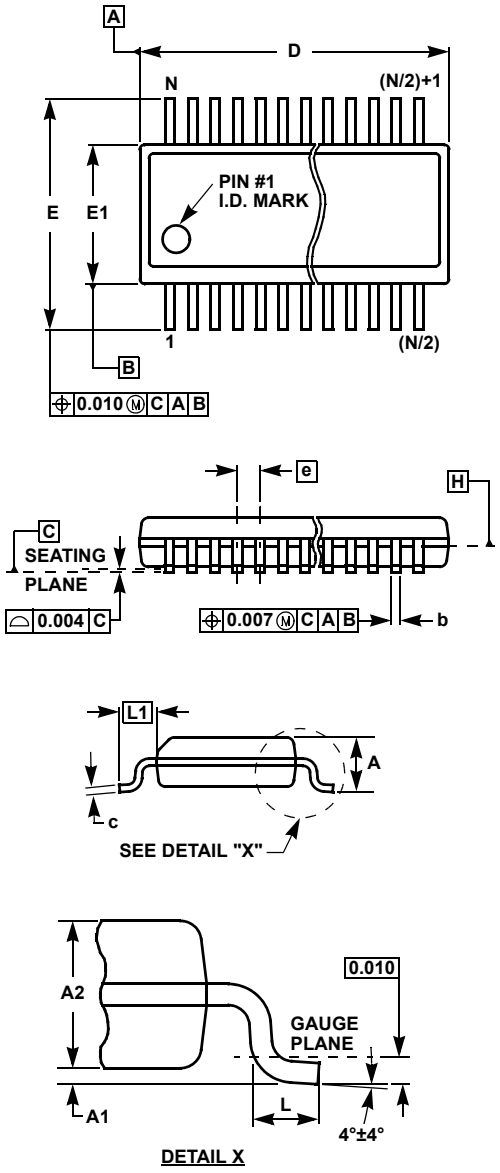
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.031	0.043	0.80	1.10	-
A1	0.000	0.004	0.00	0.10	-
A2	0.031	0.039	0.80	1.00	-
b	0.006	0.012	0.15	0.30	-
b1	0.006	0.010	0.15	0.25	
c	0.003	0.009	0.08	0.22	6
c1	0.003	0.009	0.08	0.20	6
D	0.073	0.085	1.85	2.15	3
E	0.071	0.094	1.80	2.40	-
E1	0.045	0.053	1.15	1.35	3
e	0.0256 Ref		0.65 Ref		-
e1	0.0512 Ref		1.30 Ref		-
L	0.010	0.018	0.26	0.46	4
L1	0.017 Ref.		0.420 Ref.		-
L2	0.006 BSC		0.15 BSC		
α	0^o	8^o	0^o	8^o	-
N	5		5		5
R	0.004	-	0.10	-	
R1	0.004	0.010	0.15	0.25	

Rev. 3 7/07

NOTES:

1. Dimensioning and tolerances per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC70 and JEDEC MO-203AA.
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength L measured at reference to gauge plane.
5. “N” is the number of terminal positions.
6. These Dimensions apply to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
7. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.

Quarter Size Outline Plastic Packages Family (QSOP)



MDP0040

QUARTER SIZE OUTLINE PLASTIC PACKAGES FAMILY

SYMBOL	INCHES			TOLERANCE	NOTES
	QSOP16	QSOP24	QSOP28		
A	0.068	0.068	0.068	Max.	-
A1	0.006	0.006	0.006	±0.002	-
A2	0.056	0.056	0.056	±0.004	-
b	0.010	0.010	0.010	±0.002	-
c	0.008	0.008	0.008	±0.001	-
D	0.193	0.341	0.390	±0.004	1, 3
E	0.236	0.236	0.236	±0.008	-
E1	0.154	0.154	0.154	±0.004	2, 3
e	0.025	0.025	0.025	Basic	-
L	0.025	0.025	0.025	±0.009	-
L1	0.041	0.041	0.041	Basic	-
N	16	24	28	Reference	-

Rev. F 2/07

NOTES:

1. Plastic or metal protrusions of 0.006” maximum per side are not included.
2. Plastic interlead protrusions of 0.010” maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.