

UBA2036TS

Full bridge control IC for HID automotive lighting

Rev. 01 — 30 October 2008

Product data sheet

1. General description

The UBA2036 is a high voltage monolithic Integrated Circuit (IC) manufactured in a High Voltage Silicon On Insulator (HVSOI) process. This circuit is designed for driving MOSFETs in a full bridge configuration. In addition, it features a disable function, an internal adjustable oscillator and an external clock input function with a high-voltage level shifter for driving the bridge. To guarantee an accurate 50 % duty cycle, the oscillator signal can be passed through a divider before being fed to the output drivers.

The UBA2036 is especially suitable for High Intensity Discharge (HID) lamp drivers for car headlights, projectors and general lighting applications.

2. Features

- Full bridge driver circuit
- Integrated bootstrap diodes
- 464 V integrated high voltage level shift function to drive HID lamps below ground level
- 550 V series regulator input to make the internal supply
- 550 V maximum bridge voltage
- Accurate bridge disable function
- Input for start-up delay
- Adjustable oscillator frequency
- Selectable frequency divider
- Predefined bridge position during start-up
- Adaptive non-overlap

3. Applications

- The UBA2036 can drive (via the power MOSFETs) any kind of load in a full bridge configuration
- The circuit is especially designed as a commutator controller for HID lamps in car headlights, projectors and general lighting applications

4. Ordering information

Table 1. Ordering information

| Type number | Package | | |
|-------------|---------|---|----------|
| | Name | Description | Version |
| UBA2036TS | SSOP28 | plastic shrink small outline package; 28 leads; body width 5.3 mm | SOT341-1 |

5. Block diagram

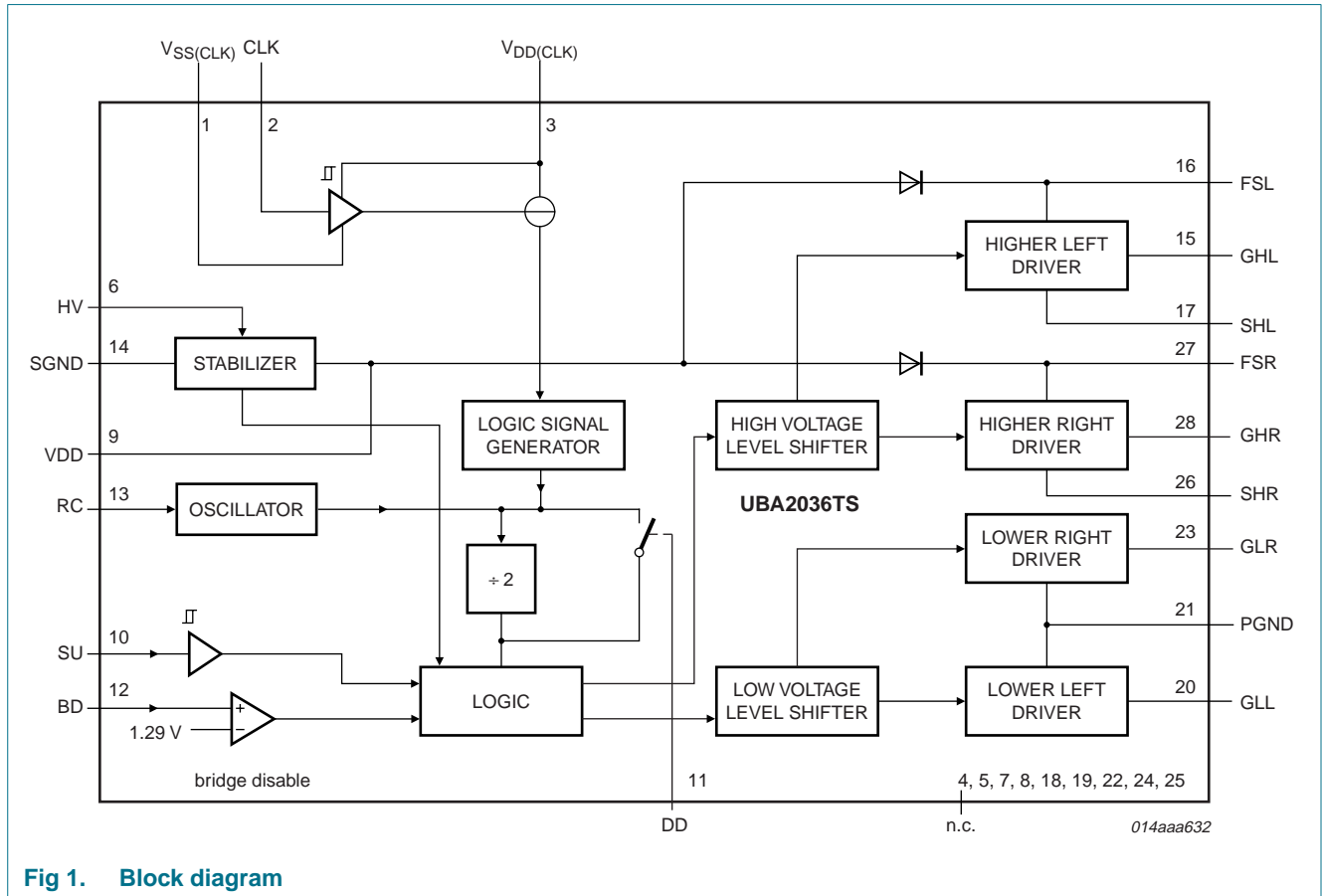


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

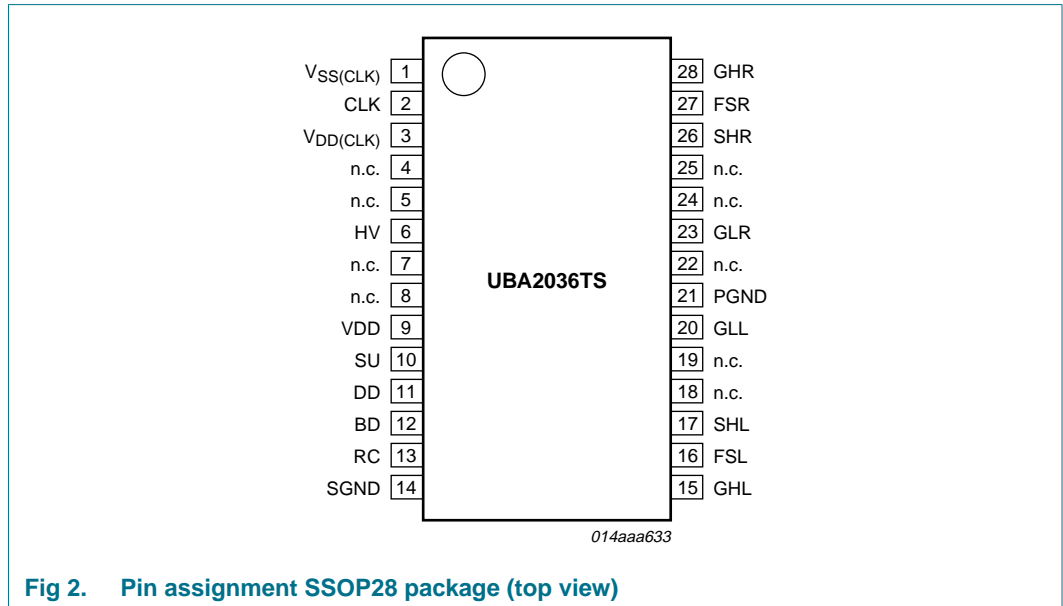


Fig 2. Pin assignment SSOP28 package (top view)

6.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|-----------------------|-----|---|
| V _{SS} (CLK) | 1 | negative supply voltage for logic oscillator input |
| CLK | 2 | oscillator input |
| V _{DD} (CLK) | 3 | positive supply voltage for logic oscillator input |
| n.c. | 4 | not connected |
| n.c. | 5 | not connected |
| HV | 6 | high voltage supply input for internal series regulator |
| n.c. | 7 | not connected |
| n.c. | 8 | not connected |
| VDD | 9 | internal low voltage supply |
| SU | 10 | input for start-up delay |
| DD | 11 | input for divider disable |
| BD | 12 | input for bridge disable |
| RC | 13 | RC input for internal oscillator |
| SGND | 14 | signal ground |
| GHF | 15 | gate driver output for upper left MOSFET |
| FSL | 16 | floating supply left |
| SHL | 17 | source upper left MOSFET |
| n.c. | 18 | not connected |
| n.c. | 19 | not connected |

Table 2. Pin description ...continued

| Symbol | Pin | Description |
|--------|-----|---|
| GLL | 20 | gate driver output for lower left MOSFET |
| PGND | 21 | power ground |
| n.c. | 22 | not connected |
| GLR | 23 | gate driver output for lower right MOSFET |
| n.c. | 24 | not connected |
| n.c. | 25 | not connected |
| SHR | 26 | source upper right MOSFET |
| FSR | 27 | floating supply right |
| GHR | 28 | gate driver upper right MOSFET |

7. Functional description

7.1 Supply voltage

The UBA2036 is powered by a supply voltage applied to pin HV, e.g. the supply voltage of the full bridge. The IC generates its own low supply voltage for its internal circuitry. Therefore an additional low voltage supply is not required. A capacitor has to be connected to pin VDD to obtain a ripple-free internal supply voltage. The circuit can also be powered by a low voltage supply directly applied to pin VDD. In this case pin HV should be connected to pin VDD or pin SGND. The maximum current that the internal series regulator can deliver, is temperature dependent. This is shown in [Figure 3](#).

7.2 Start-up

With an increasing supply voltage the IC enters the start-up state i.e. the upper power transistors are set in off-state and the lower power transistors are switched on. During the start-up state the bootstrap capacitors are charged. The start-up state is defined until $V_{VDD} = V_{startup(VDD)}$ or $V_{HV} = V_{startup(HV)}$. The state of the outputs during the start-up phase is overruled by the bridge disable function.

7.3 Oscillation state

At the moment the supply voltage on pin VDD exceeds $V_{startup(VDD)}$ or the supply voltage on pin V_{HV} exceeds $V_{startup(HV)}$, the output voltage of the full bridge depends on the control signals on pins CLK, SU, DD and BD. This is listed in [Table 3](#).

As soon as the supply voltage on pin VDD becomes lower than $V_{UVLO(VDD)}$ or the supply voltage on pin V_{HV} becomes lower than $V_{UVLO(HV)}$, the IC enters the start-up state again.

Table 3. Driver

Gate driver output voltages as function of the logical levels at the pins BD, SU, DD and CLK.

| Device state | BD | SU | DD | CLK | GHL | GHR | GLL | GLR |
|----------------|----|----|----|-----|------------------|------------------|-------------------|-------------------|
| Start-up state | 1 | - | - | - | 0 (= V_{SHL}) | 0 (= V_{SHR}) | 0 (= V_{PGND}) | 0 (= V_{PGND}) |
| state | 0 | - | - | - | 0 (= V_{SHL}) | 0 (= V_{SHR}) | 1 (= V_{VDD}) | 1 (= V_{VDD}) |

Table 3. Driver ...continued

Gate driver output voltages as function of the logical levels at the pins BD, SU, DD and CLK.

| Device state | BD | SU | DD | CLK | GHL | GHR | GLL | GLR |
|-------------------|----|----|------------------|----------------------|-------------------------|-------------------------|--------------------------|--------------------------|
| Oscillation state | 1 | - | - | - | 0 (= V _{SHL}) | 0 (= V _{SHR}) | 0 (= V _{PGND}) | 0 (= V _{PGND}) |
| | 0 | 0 | - | - | 0 (= V _{SHL}) | 0 (= V _{SHR}) | 1 (= V _{VDD}) | 1 (= V _{VDD}) |
| | 0 | 1 | 1 | 1 | 0 (= V _{SHL}) | 1 (= V _{FSR}) | 1 (= V _{VDD}) | 0 (= V _{PGND}) |
| | 0 | 1 | 1 | 0 | 1 (= V _{FSL}) | 0 (= V _{SHR}) | 0 (= V _{PGND}) | 1 (= V _{VDD}) |
| | 0 | 1 | 0 ^[1] | 1 → 0 ^[2] | $\overline{\text{GHL}}$ | $\overline{\text{GHR}}$ | $\overline{\text{GLL}}$ | $\overline{\text{GLR}}$ |

[1] If pin DD = 0 the bridge enters the state (oscillation state and pin BD = 0 and pin SU = 1) in the pre-defined position: V_{GHL} = V_{FSL}, V_{GLR} = V_{VDD}, V_{GLL} = V_{PGND}, and V_{GHR} = V_{SHR}.

[2] Only if the level of pin CLK changes from logical 1 to 0, the level of outputs GHL, GHR, GLL and GLR changes.

If there is no external clock available, the internal oscillator can be used. The design equation for the bridge oscillator frequency is shown in [Equation 1](#).

$$f_{bridge} = \frac{1}{K_{osc} \times R_{osc} \times C_{osc}} \tag{1}$$

R_{osc} and C_{osc} are external components connected to the RC pin (R_{osc} connected to pin VDD and C_{osc} connected to pin SGND). In this situation the pins V_{DD(CLK)}, CLK and V_{SS(CLK)} can be connected to SGND.

The clock signal, coming from either pin RC or pin CLK, is divided by two in order to obtain a 50 % duty-cycle gate drive signal. This can be achieved by applying a voltage to the DD input lower than V_{IL(DD)} (e.g. connect pin DD to pin SGND).

7.4 Non-overlap time

In the full bridge configuration the non-overlap time is defined as the time between turning off the two conducting MOSFETs and turning on the two other MOSFETs. The non-overlap time is realized by means of an adaptive non-overlap circuit. With an adaptive non-overlap, the application determines the duration of the non-overlap and makes the non-overlap time optimal for each frequency. The non-overlap time is determined by the duration of the falling slope of the relevant half bridge voltage. The occurrence of a slope is sensed internally. The minimum non-overlap time is internally fixed.

7.5 Start-up delay

A simple resistor-capacitor (RC) filter (R between pin VDD and pin SU; C between pin SU and pin SGND) or a control signal from a processor can be used to make a start-up delay. This can be beneficial for those applications in which building up the high voltage takes a larger amount of time: A start-up delay will ensure that the HID system will not start up before this high voltage has been reached.

7.6 Bridge disable

The bridge disable function can be used to switch off all the MOSFETs as soon as the voltage on pin BD exceeds the bridge disable voltage V_{BD}. The bridge disable function overrules all the other states.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to signal ground (pin 14); positive currents flow into the chip. The voltage ratings are valid provided other ratings are not violated.

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------------|---------------------------|---|------------|-----------|------------|
| General | | | | | |
| T_{amb} | ambient temperature | | -40 | +125 | °C |
| T_j | junction temperature | | -40 | +150 | °C |
| T_{stg} | storage temperature | | -55 | +150 | °C |
| Voltages | | | | | |
| V_{VDD} | voltage on pin VDD | DC | 0 | 14 | V |
| | | maximum pulse time = 100 ns | 0 | 17 | V |
| V_{HV} | voltage on pin HV | | 0 | 550 | V |
| V_{SHL} | voltage on pin SHL | with respect to PGND and SGND | -3 | 550 | V |
| | | with respect to SGND; maximum pulse time = 1 μ s | -14 | 550 | V |
| V_{SHR} | voltage on pin SHR | with respect to PGND and SGND | -3 | 550 | V |
| | | with respect to SGND; maximum pulse time = 1 μ s | -14 | 550 | V |
| V_{FSL} | voltage on pin FSL | with respect to SHL | 0 | 14 | V |
| V_{FSR} | voltage on pin FSR | with respect to SHR | 0 | 14 | V |
| V_{GHL} | voltage on pin GHL | | V_{SHL} | V_{FSL} | V |
| V_{GHR} | voltage on pin GHR | | V_{SHR} | V_{FSR} | V |
| V_{GLL} | voltage on pin GLL | | V_{PGND} | V_{VDD} | V |
| V_{GLR} | voltage on pin GLR | | V_{PGND} | V_{VDD} | V |
| V_{PGND} | voltage on pin PGND | | 0 | 5 | V |
| $V_{SS(CLK)}$ | CLK ground supply voltage | $t < 1$ s | 0 | 464 | V |
| $V_{DD(CLK)}$ | CLK supply voltage | $t < 1$ s | 0 | 464 | V |
| | | with respect to $V_{SS(CLK)}$: | | | |
| | | DC | 0 | 14 | V |
| | | maximum pulse time = 100 ns | 0 | 17 | V |
| V_i | input voltage | pins CLK, SU, BD, and DD; with respect to $V_{SS(CLK)}$: | | | |
| | | DC | 0 | V_{VDD} | V |
| | | maximum pulse time = 100 ns | 0 | 17 | V |
| | | pin RC: | | | |
| | | maximum pulse time = 100 ns | 0 | 17 | V |
| SR | slew rate | pins SHL and SHR | - | 6 | V/ns |
| | | pin $V_{SS(CLK)}$ | - | 0.5 | V/ μ s |
| Currents | | | | | |
| R_{osc} | oscillator resistance | connected between pins VDD and RC | 100 | - | k Ω |

Table 4. Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to signal ground (pin 14); positive currents flow into the chip. The voltage ratings are valid provided other ratings are not violated.

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|---------------------------------|---|-----|-----|------|
| ESD | | | | | |
| V _{ESD} | electrostatic discharge voltage | human body model | | | |
| | | HV, V _{SS(CLK)} , V _{DD(CLK)} , CLK, FSL, FSR, GHL, GHR, SHL, SHR | - | 900 | V |
| | | other pins | - | 2 | kV |
| | | machine model; all pins | - | 200 | V |
| | | charged device model; all pins | - | 500 | V |

9. Thermal characteristics

Table 5. Thermal characteristics

| Symbol | Parameter | Conditions | Typ | Unit |
|----------------------|---|-------------|-----|------|
| R _{th(j-a)} | thermal resistance from junction to ambient | in free air | 100 | K/W |

10. Characteristics

Table 6. Characteristics

T_j = -40 °C to 125 °C; all voltages are measured with respect to signal ground (pin 14); currents are positive when flowing into the IC, Unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------------|--|---|------|------|------|------|
| High voltage | | | | | | |
| I _{leak} | leakage current | pin HV; I _{HV} (V _{HV} = 565 V) – I _{HV} (V _{HV} = 500 V) | - | 0 | 10 | μA |
| | | pin FSL; V _{FSL} = V _{SHL} = V _{GHL} = 564 V | - | 0 | 5 | μA |
| | | pin FSR; V _{FSR} = V _{SHR} = V _{GHR} = 564 V | - | 0 | 5 | μA |
| | | pin V _{SS(CLK)} ; V _{SS(CLK)} = V _{clk} = 450 V | - | 0 | 10 | μA |
| | | pin V _{DD(CLK)} ; V _{DD(CLK)} = V _{clk} = 464 V | - | 0 | 10 | μA |
| Start-up via HV pin | | | | | | |
| I _{I(HV)} | input current on pin HV | V _{HV} = 80 V | - | 590 | 825 | μA |
| V _{startup(HV)} | start-up voltage on pin HV | | 11.3 | 13.2 | 14.7 | V |
| V _{UVLO(HV)} | undervoltage lockout voltage on pin HV | | 8.6 | 10.7 | 12.2 | V |
| V _{hys} | hysteresis voltage | | 2 | 2.5 | 3 | V |
| V _{VDD} | voltage on pin VDD | V _{HV} = 20 V | 10.5 | 12 | 13.5 | V |
| Start-up via VDD pin | | | | | | |
| I _{I(VDD)} | input current on pin VDD | V _{VDD} = 8.25 V | - | 500 | 800 | μA |
| V _{startup(VDD)} | start-up voltage on pin VDD | | 8.25 | 9.0 | 9.75 | V |

Table 6. Characteristics ...continued

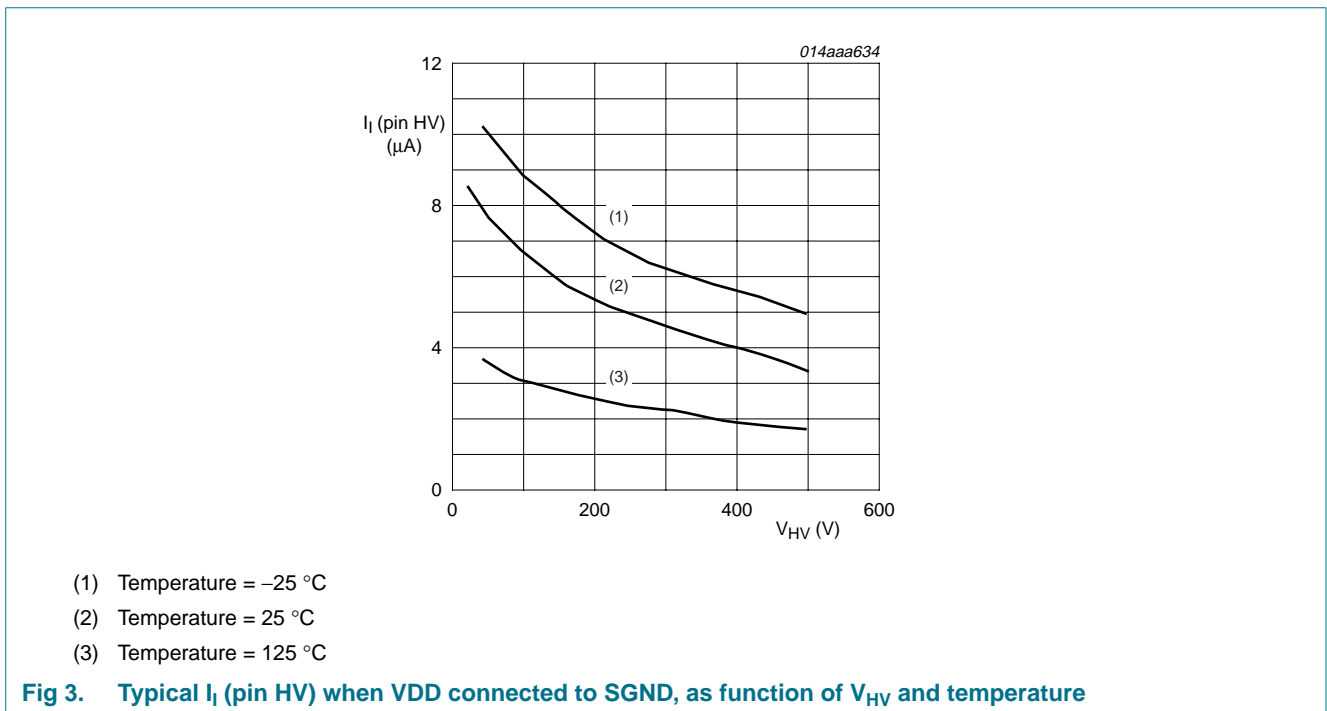
$T_j = -40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$; all voltages are measured with respect to signal ground (pin 14); currents are positive when flowing into the IC, Unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|--|---|------|-----|------|------------------|
| $V_{UVLO(VDD)}$ | undervoltage lockout voltage on pin VDD | | 5.75 | 6.5 | 7.25 | V |
| V_{hys} | hysteresis voltage | | 2 | 2.5 | 3 | V |
| Gate drivers | | | | | | |
| R_{on} | on-state resistance | GHR and GHL drivers; $V_{FSL} = V_{FSR} = 12\text{ V}$; $V_{SHL} = V_{SHR} = 0\text{ V}$; $I_{GHL} = I_{GHR} = -50\text{ mA}$ | - | 20 | 42 | Ω |
| | | GLL and GLR drivers; $V_{VDD} = 12\text{ V}$; $V_{PGND} = 0\text{ V}$; $I_{GLL} = I_{GLR} = -50\text{ mA}$ | - | 20 | 42 | Ω |
| R_{off} | off-state resistance | GHR and GHL drivers; $V_{FSL} = V_{FSR} = 12\text{ V}$; $V_{SHL} = V_{SHR} = 0\text{ V}$; $I_{GHL} = I_{GHR} = 50\text{ mA}$ | - | 12 | 26 | Ω |
| | | GLR and GLL drivers; $V_{VDD} = 12\text{ V}$; $V_{PGND} = 0\text{ V}$; $I_{GLL} = I_{GLR} = 50\text{ mA}$ | - | 12 | 26 | Ω |
| $I_{O(source)}$ | output source current | $V_{FSL} = V_{FSR} = V_{VDD} = 12\text{ V}$; $V_{SHL} = V_{SHR} = 0\text{ V}$; $V_{GHL} = V_{GHR} = V_{GLL} = V_{GLR} = 8\text{ V}$ | - | 200 | - | mA |
| $I_{O(sink)}$ | output sink current | $V_{FSL} = V_{FSR} = V_{VDD} = 12\text{ V}$; $V_{SHL} = V_{SHR} = 0\text{ V}$; $V_{GHL} = V_{GHR} = V_{GLL} = V_{GLR} = 8\text{ V}$ | - | 200 | - | mA |
| $V_{d(bs)}$ | bootstrap diode voltage | current on diode = 1 mA | 0.8 | 1.0 | 1.2 | V |
| dV/dt | rate of change of voltage | absolute values | 5 | 15 | 25 | V/ μs |
| t_{no} | non-overlap time | | 600 | 900 | 1300 | ns |
| V_{UVLO} | undervoltage lockout voltage | high side driver | - | 4.0 | 5.5 | V |
| I_{FS} | current on pin FS | $V_{FSL} = V_{FSR} = 12\text{ V}$; $V_{SHL} = V_{SHR} = 0\text{ V}$ | 1 | 4 | 7 | μA |
| I_{FSL}/I_{FSR} | current on pin FSL to current on pin FSR ratio | | 0.8 | - | 1.2 | |
| DD input | | | | | | |
| $V_{IH(DD)}$ | HIGH-level input voltage on pin DD | $V_{VDD} = 12\text{ V}$ | 6 | 4.5 | - | V |
| $V_{IL(DD)}$ | LOW-level input voltage on pin DD | $V_{VDD} = 12\text{ V}$ | - | - | 3 | V |
| I_I | input current | $V_{VDD} = 12\text{ V}$ | - | 0 | 1 | μA |
| SU input | | | | | | |
| $V_{startup}$ | start-up voltage | $V_{VDD} = 12\text{ V}$ | 1 | 1.3 | 1.5 | V |
| V_{hys} | hysteresis voltage | $V_{VDD} = 12\text{ V}$ | - | 100 | - | mV |
| I_I | input current | $V_{VDD} = 12\text{ V}$ | - | 0 | 1 | μA |
| CLK input | | | | | | |
| $V_{IH(CLK)}$ | HIGH-level input voltage on pin CLK | $V_{SS(CLK)} = 0\text{ V}$; $V_{DD(CLK)} = 12\text{ V}$ | 0.9 | 1.6 | 2.7 | V |

Table 6. Characteristics ...continued

$T_j = -40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$; all voltages are measured with respect to signal ground (pin 14); currents are positive when flowing into the IC, Unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------------|-------------------------------|--|------|------|------|---------------|
| V_{hys} | hysteresis voltage | $V_{SS(CLK)} = 0\text{ V}$; $V_{DD(CLK)} = 12\text{ V}$ | - | 100 | | mV |
| I_I | input current | | - | 0 | 1 | μA |
| f_{bridge} | bridge frequency | $V_{RC} = 0\text{ V}$ | - | - | 200 | kHz |
| supply for CLK | | | | | | |
| $I_{DD(CLK)}$ | CLK supply current | $V_{SS(CLK)} = 0\text{ V}$; $V_{DD(CLK)} = 14\text{ V}$ | - | 420 | 625 | μA |
| $V_{DD(CLK)}$ | CLK supply voltage | $V_{SS(CLK)} = 0\text{ V}$ | 5.75 | - | 14 | V |
| BD input | | | | | | |
| V_{BD} | voltage on pin BD | | 1.23 | 1.29 | 1.35 | V |
| I_I | input current | | - | 0 | 1 | μA |
| Internal oscillator | | | | | | |
| $f_{osc(int)}$ | internal oscillator frequency | $V_{CLK} = 0\text{ V}$; $V_{SS(CLK)} = 0\text{ V}$ | - | - | 100 | kHz |
| K_{osc} | oscillator constant | $f_{bridge} = 500\text{ Hz}$ | 0.89 | 0.97 | 1.05 | |



11. Quality information

This product has been qualified to the appropriate Automotive Electronics Council (AEC) standard Q100 and Q101 and is suitable for use in automotive critical applications.

12. Package outline

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3 mm

SOT341-1

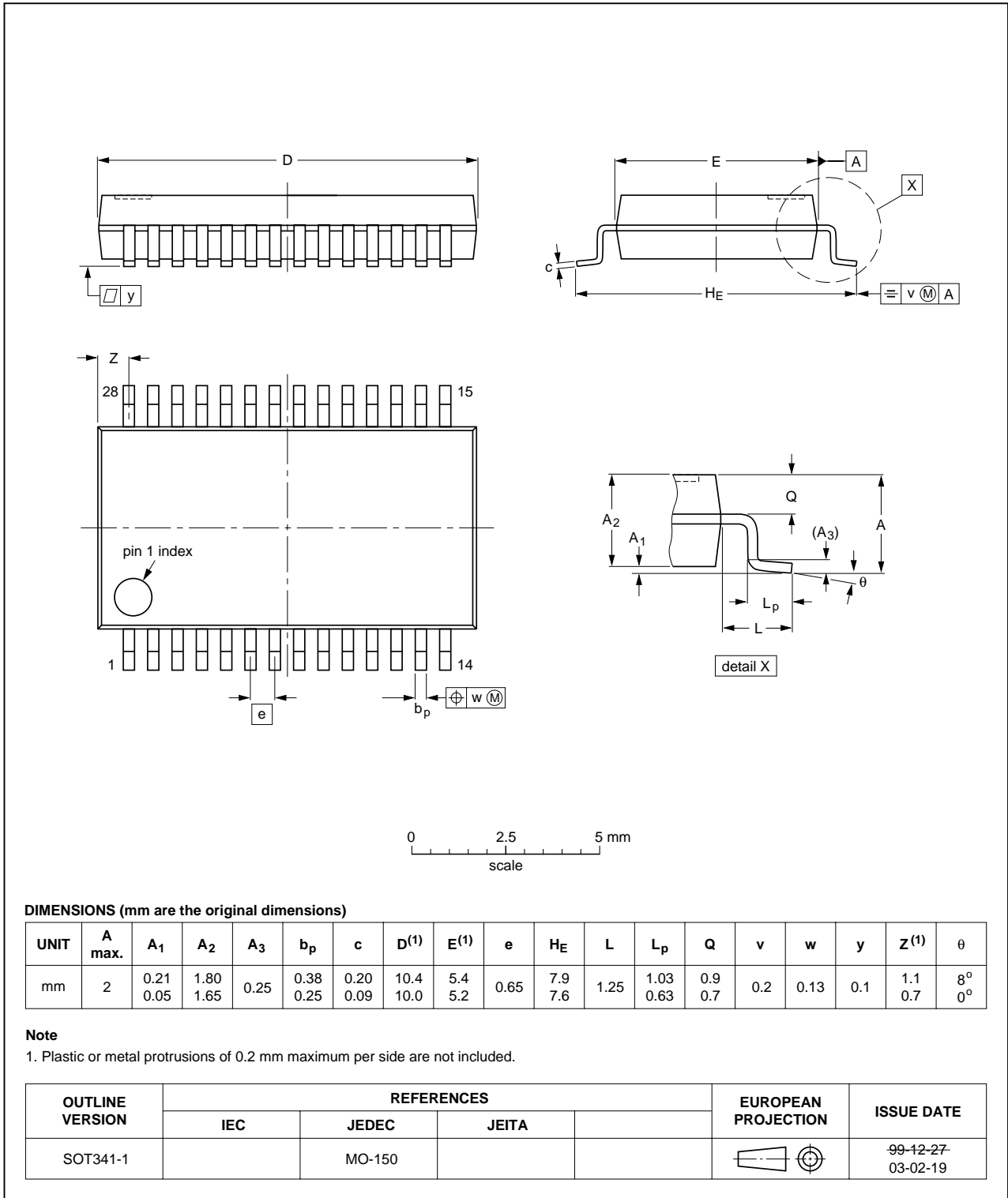


Fig 4. Package outline SSOP28 (SOT134-1)

13. Revision history

Table 7. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-------------|--------------|--------------------|---------------|------------|
| UBA2036TS_1 | 20081030 | Product data sheet | - | - |

14. Legal information

14.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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