Dual, Simultaneous Sampling, 16-Bit/14-Bit, 4 MSPS SAR ADCs, Differential Inputs

Data Sheet

AD7380/AD7381

FEATURES

16-bit/14-bit ADC family
Dual simultaneous sampling
Fully differential analog inputs
4 MSPS throughput conversion rate
SNR (typical)
- **92.5 dB, V_{REF} = 3.3 V external at AD7380 (16-bit)**
- **85.4 dB, V_{REF} = 3.3 V external at AD7381 (14-bit)**
- **101 dB with ×16 OSR**

On-chip oversampling function
Resolution boost function
INL (maximum)
- **2.0 LSBs at 16-bit**
- **1.0 LSB at 14-bit**

2.5 V internal reference
High speed serial interface
−40°C to +125°C operation
16-lead LFCSP, 3 mm × 3 mm
Wide common-mode range
Alert function

APPLICATIONS

Motor control position feedback
Motor control current sense
Sonar
Power quality
Data acquisition systems
Erbium doped fiber amplifier (EDFA) applications
I and Q demodulation

GENERAL DESCRIPTION

The AD7380/AD7381 are a 16-bit and 14-bit pin-compatible family of dual simultaneous sampling, high speed, low power, successive approximation register (SAR) analog-to-digital converters (ADCs) that operate from a 3.0 V to 3.6 V power supply and feature throughput rates up to 4 MSPS. The analog input type is differential, accepts a wide common-mode input voltage, and is sampled and converted on the falling edge of $\overline{CS}$.

An integrated on-chip oversampling block improves dynamic range and reduces noise at lower bandwidths. A buffered internal 2.5 V reference is included. Alternatively, an external reference up to 3.3 V can be used.

The conversion process and data acquisition use standard control inputs allowing simple interfacing to microprocessors or digital signal processors (DSPs). The device is compatible with 1.8 V, 2.5 V, and 3.3 V interfaces using the separate logic supply.

The AD7380/AD7381 are available in a 16-lead lead frame chip scale package (LFCSP) with operation specified from −40°C to +125°C.

PRODUCT HIGHLIGHTS

1. Dual simultaneous sampling and conversion with two complete ADC functions.
2. Pin-compatible product family.
3. High 4 MSPS throughput rate.
4. Space saving 3 mm × 3 mm LFCSP.
5. An integrated oversampling block to increase dynamic range, reduce noise, and reduce SCLK speed requirements.
6. Differential analog inputs with wide common-mode range.
7. Small sampling capacitor reduces amplifier drive burden.

FUNCTIONAL BLOCK DIAGRAM

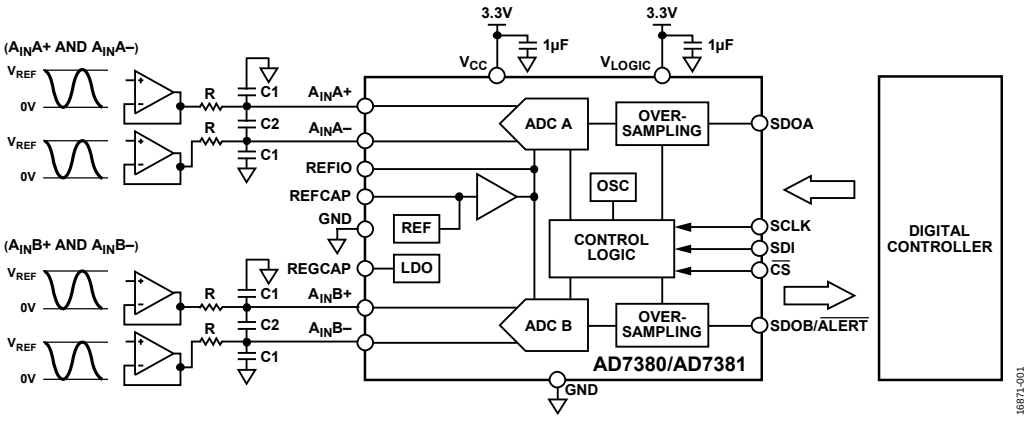


Figure 1.

Rev. A **Document Feedback**

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
©2019 Analog Devices, Inc. All rights reserved.
Technical Support **www.analog.com**

TABLE OF CONTENTS

Features ... 1
Applications ... 1
General Description ... 1
Product Highlights ... 1
Functional Block Diagram ... 1
Revision History ... 2
Specifications ... 3
Timing Specifications ... 6
Absolute Maximum Ratings ... 8
Thermal Resistance ... 8
ESD Caution ... 8
Pin Configuration and Function Descriptions ... 9
Typical Performance Characteristics ... 10
Terminology ... 13
Theory of Operation ... 14
Circuit Information ... 14
Converter Operation ... 14
Analog Input Structure ... 14
ADC Transfer Function ... 15
Applications Information ... 16
Power Supply ... 16
Modes of Operation ... 18
Oversampling ... 18
Resolution Boost ... 20
Alert ... 20
Power Modes ... 21
Internal and External Reference ... 21
Software Reset ... 21
Diagnostic Self Test ... 21
Interface ... 22
Reading Conversion Results ... 22
Low Latency Readback ... 23
Reading from Device Registers ... 24
Writing to Device Registers ... 24
CRC ... 25
Registers ... 27
Addressing Registers ... 27
CONFIGURATION1 Register ... 28
CONFIGURATION2 Register ... 29
$\overline{\text{ALERT}}$ Register ... 29
ALERT_LOW_THRESHOLD Register ... 30
ALERT_HIGH_THRESHOLD Register ... 30
Outline Dimensions ... 31
Ordering Guide ... 31

REVISION HISTORY

11/2019—Rev. 0 to Rev. A

Updated Title ... 1
Changes to Features Section, Applications Section, and Figure 1 ... 1
Changes to Table 1 ... 3
Changes to Table 2 ... 4
Changes to Aperture Delay Match Parameter, Table 3 and V_{REF} Noise Parameter, Table 3 ... 5
Changes to Table 4 ... 6
Change to Thermal Resistance Section ... 8
Change to Pin 9 Description, Table 7 ... 9
Changes to Figure 11 Caption ... 10
Changes to Figure 15 Caption, Figure 18, Figure 19, and Figure 20 ... 11
Changes to Terminology Section ... 13
Change to ADC Transfer Function Section ... 15
Changes to Applications Information Section and Power Supply Section ... 16
Added Table 9; Renumbered Sequentially ... 16
Changes to Figure 31 ... 17
Changes to Normal Average Oversampling Section, Table 10, and Figure 32 ... 18
Changes to Rolling Average Oversampling Section and Figure 33 ... 19
Changes to Resolution Boost Section ... 20
Added Figure 36; Renumbered Sequentially ... 21
Change to Figure 37 and Table 12 ... 22
Changes to Serial 2-Wire Mode Section, Resolution Boost Mode Section, Figure 38, and Figure 40 ... 23
Changes to Figure 41 and Figure 42 ... 24
Changes to Figure 43 ... 26
Changes to Table 14 and Table 16 ... 27
Change to CONFIGURATION1 Register Section and Table 17 ... 28
Changes to CONFIGURATION2 Register Section and $\overline{\text{ALERT}}$ Register Section ... 29
Changes to ALERT_LOW_THRESHOLD Register Section, Table 20, ALERT_HIGH_THRESHOLD Register Section, and Table 21 ... 30
Changes to Ordering Guide ... 31

1/2019—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 3.0 V to 3.6 V, V_{LOGIC} = 1.65 V to 3.6 V, reference voltage (V_{REF}) = 2.5 V internal, sampling frequency (f_{SAMPLE}) = 4 MSPS, and T_A = −40°C to +125°C, no oversampling enabled, unless otherwise noted.

Table 1. AD7380

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		16			Bit
THROUGHPUT					
Conversion Rate				4	MSPS
DC ACCURACY					
No Missing Codes		16			Bits
Differential Nonlinearity (DNL) Error		−1.0	±0.7	+1.0	LSB
Integral Nonlinearity (INL) Error		−2.0	±0.75	+2.0	LSB
Gain Error		−0.015	±0.002	+0.015	% FS[1]
Gain Error Temperature Drift		−11	±1	+11	ppm/°C
Gain Error Match		−0.01	±0.002	+0.01	% FS
Zero Error	At 25°C, V_{CC} = 3.3 V	−0.2	±0.01	+0.2	mV
		−0.5		+0.5	mV
Zero Error Drift		−2	±0.5	+2	µV/°C
Zero Error Matching		−0.5	±0.1	+0.5	mV
AC ACCURACY	Input frequency (f_{IN}) = 1 kHz				
Dynamic Range	V_{REF} = 3.3 V external		93.3		dB
			91.8		dB
Oversampled Dynamic Range	Oversampling ratio (OSR) = 4		95.2		dB
Signal-to-Noise Ratio (SNR)	V_{REF} = 3.3 V external	90	92.5		dB
		88.5	91.1		dB
	OSR = 8, RES = 1		98		dB
	OSR = 16, RES = 1		101		dB
	f_{IN} = 100 kHz		89		dB
Spurious-Free Dynamic Range (SFDR)			−110		dB
Total Harmonic Distortion (THD)			−113		dB
	f_{IN} = 100 kHz		−104		dB
Signal-to-(Noise + Distortion) (SINAD)	V_{REF} = 3.3 V external	89.5	92.3		dB
		88	91		dB
Channel to Channel Isolation			−110		dB
POWER SUPPLIES					
V_{CC} Current (I_{VCC})					
Normal Mode (Operational)			21.5	26	mA
Power Dissipation					
Total Power (P_{TOTAL})			83	107	mW
V_{CC} Power (P_{VCC})					
Normal Mode (Operational)			71	94	mW

[1] These specifications include full temperature range variation, but these specifications do not include the error contribution from the external reference.

V_{CC} = 3.0 V to 3.6 V, V_{LOGIC} = 1.65 V to 3.6 V, V_{REF} = 2.5 V internal, f_{SAMPLE} = 4 MSPS, and T_A = −40°C to +125°C, no oversampling enabled, unless otherwise noted.

Table 2. AD7381

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		14			Bit
THROUGHPUT					
Conversion Rate				4	MSPS
DC ACCURACY					
No Missing Codes		14			Bits
DNL Error		−1.0	±0.5	+1.0	LSB
INL Error		−1.0	±0.3	+1.0	LSB
Gain Error		−0.02	±0.002	+0.02	% FS[1]
Gain Error Temperature Drift		−20	±1	+20	ppm/°C
Gain Error Match		−0.02	±0.002	+0.02	% FS
Zero Error		−2	±0.25	+2	LSB
Zero Error Drift		+3	±0.5	+3	µV/°C
Zero Error Matching		−1.5	±0.25	+1.5	LSB
AC ACCURACY	f_{IN} = 1 kHz				
Dynamic Range			85.4		dB
Oversampled Dynamic Range	OSR = 4		87		dB
SNR	V_{REF} = 3.3 V external	85	85.4		dB
		84.5	85		dB
	OSR = 8, RES = 1		92.6		dB
	OSR = 16, RES = 1		94.5		dB
	f_{IN} = 100 kHz		84.6		dB
SFDR	V_{REF} = 3.3 V		−108		dB
			−112		dB
THD	V_{REF} = 3.3 V		−107		dB
			−112		dB
	f_{IN} = 100 kHz		−101		dB
SINAD		84.5	85.3		dB
		84	84.9		dB
Channel to Channel Isolation			−110		dB
POWER SUPPLIES					
I_{VCC}					
Normal Mode (Operational)			21.5	26	mA
Power Dissipation					
P_{TOTAL}			83	107	mW
P_{VCC}					
Normal Mode (Operational)			71	94	mW

[1] These specifications include full temperature range variation, but these specifications do not include the error contribution from the external reference.

Table 3. All Devices

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG INPUT					
Voltage Range	(A_{IN}x+) – (A_{IN}x–)	$-V_{REF}$		$+V_{REF}$	V
Absolute Input Voltage	A_{IN}x+, A_{IN}x–	–0.1		V_{REF} + 0.1	V
Common-Mode Input Range	A_{IN}x+, A_{IN}x–		0.2 to V_{REF} – 0.2		V
Analog Input Common-Mode Rejection Ratio (CMRR)	f_{IN} = 500 kHz		–75		dB
DC Leakage Current			0.1	1	µA
Input Capacitance	When in track mode		18		pF
	When in hold mode		5		pF
SAMPLING DYNAMICS					
Input Bandwidth	At –0.1 dB		6		MHz
	At –3 dB		25		MHz
Aperture Delay			2		ns
Aperture Delay Match			26	100	ps
Aperture Jitter			20		ps
REFERENCE INPUT AND OUTPUT					
V_{REF} Input Voltage Range	External reference	2.49		3.4	V
V_{REF} Input Current	External reference		0.47	0.51	mA
V_{REF} Output Voltage	At 25°C	2.498	2.5	2.502	V
	–40°C to +125°C	2.495		2.505	V
V_{REF} Temperature Coefficient			1	10	ppm/°C
V_{REF} Line Regulation			–38		ppm/V
V_{REF} Load Regulation			–106		ppm/mA
V_{REF} Noise			7		µV rms
DIGITAL INPUTS (SCLK, SDI, $\overline{CS}$)					
Logic Levels					
Input Low Voltage (V_{IL})				0.2 × V_{LOGIC}	V
Input High Voltage (V_{IH})		0.8 × V_{LOGIC}			V
Input Low Current (I_{IL})		–1		+1	µA
Input High Current (I_{IH})		–1		+1	µA
DIGITAL OUTPUTS (SDOA, SDOB/$\overline{ALERT}$)					
Output Coding			Twos complement		Bits
Output Low Voltage (V_{OL})	Sink current (I_{SINK}) = +300 µA			0.4	V
Output High Voltage (V_{OH})	Source current (I_{SOURCE}) = –300 µA	V_{LOGIC} – 0.3			V
Floating State Leakage Current				±1	µA
Floating State Output Capacitance			10		pF
POWER SUPPLIES					
V_{CC}					
		3.0	3.3	3.6	V
	External reference = 3.3 V	3.2	3.3	3.6	V
V_{LOGIC}		1.65		3.6	V
I_{VCC}					
Normal Mode (Static)			2.3	2.8	mA
Shutdown Mode			100	200	µA
V_{LOGIC} Current (I_{VLOGIC})	SDOA and SDOB at 0x1FFF				
Normal Mode (Static)			10	200	nA
Normal Mode (Operational)			3.5	3.7	mA
Shutdown Mode			10	200	nA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Power Dissipation					
P_{VCC}					
Normal Mode (Static)			7.6	10	mW
Shutdown Mode			330	720	µW
P_{VLOGIC}	SDOA and SDOB at 0x1FFF				
Normal Mode (Static)			33	720	nW
Normal Mode (Operational)			11.5	13.3	mW
Shutdown Mode			33	720	nW

TIMING SPECIFICATIONS

V_{CC} = 3.0 V to 3.6 V, V_{LOGIC} = 1.65 V to 3.6 V, V_{REF} = 2.5 V internal, and T_A = −40°C to +125°C, unless otherwise noted.

Table 4.[1, 2]

Parameter	Min	Typ	Max	Unit	Description
t_{CYC}	250			ns	Time between conversions
t_{SCLKED}	0.4			ns	$\overline{CS}$ falling edge to first SCLK falling edge
t_{SCLK}	12.5			ns	SCLK period
t_{SCLKH}	5			ns	SCLK high time
t_{SCLKL}	5			ns	SCLK low time
t_{CSH}	10			ns	$\overline{CS}$ pulse width
t_{QUIET}	10			ns	Interface quiet time prior to conversion
t_{SDOEN}					$\overline{CS}$ low to SDOA and SDOB/$\overline{ALERT}$ enabled
			5.5	ns	$V_{LOGIC} \geq 2.25$ V
			8	ns	1.65 V ≤ V_{LOGIC} < 2.25 V
t_{SDOH}	2			ns	SCLK rising edge to SDOA and the SDOB/$\overline{ALERT}$ hold time
t_{SDOS}					SCLK rising edge to SDOA and the SDOB/$\overline{ALERT}$ setup time
			5.5	ns	$V_{LOGIC} \geq 2.25$ V
			8	ns	1.65 V ≤ V_{LOGIC} < 2.25 V
t_{SDOT}			45	ns	$\overline{CS}$ rising edge to SDOA and the SDOB/$\overline{ALERT}$ high impedance
t_{SDIS}	1			ns	SDI setup time prior to SCLK falling edge
t_{SDIH}	1			ns	SDI hold time after SCLK falling edge
t_{SCLKCS}	0			ns	SCLK rising edge to $\overline{CS}$ rising edge
$t_{CONVERT}$			190	ns	Conversion time
$t_{ACQUIRE}$	110			ns	Acquire time
t_{RESET}					Valid time to start conversion after software reset (see Figure 36)
		250		ns	Valid time to start conversion after soft reset
		800		ns	Valid time to start conversion after hard reset
$t_{POWERUP}$					Supply active to conversion
			5	ms	First conversion allowed
			11	ms	Settled to within 1% with internal reference
			5	ms	Settled to within 1% with external reference
$t_{REGWRITE}$			5	ms	Supply active to register read write access allowed
$t_{STARTUP}$					Exiting power-down mode to conversion
			11	ms	Settled to within 1% with internal reference
			10	µs	Settled to within 1% with external reference
$t_{CONVERT0}$[2]	4	7	10	ns	Conversion start time for first sample in oversampling (OS) normal mode
$t_{CONVERTx}$					Conversion start time for x^{th} sample in OS normal mode
	$t_{CONVERT0} + (320 \times (x - 1))$			ns	For AD7380 at 3 MSPS
	$t_{CONVERT0} + (250 \times (x - 1))$			ns	For AD7381 at 4 MSPS
t_{ALERTS}			200	ns	Time from $\overline{CS}$ to $\overline{ALERT}$ indication (see Figure 34)
t_{ALERTC}			12	ns	Time from $\overline{CS}$ to $\overline{ALERT}$ clear (see Figure 34)
t_{ALERTS_NOS}			12	ns	Time from internal conversion with exceeded threshold to $\overline{ALERT}$ indication (see Figure 34)

[1] All specifications are 10 pF load.
[2] Guaranteed by design.

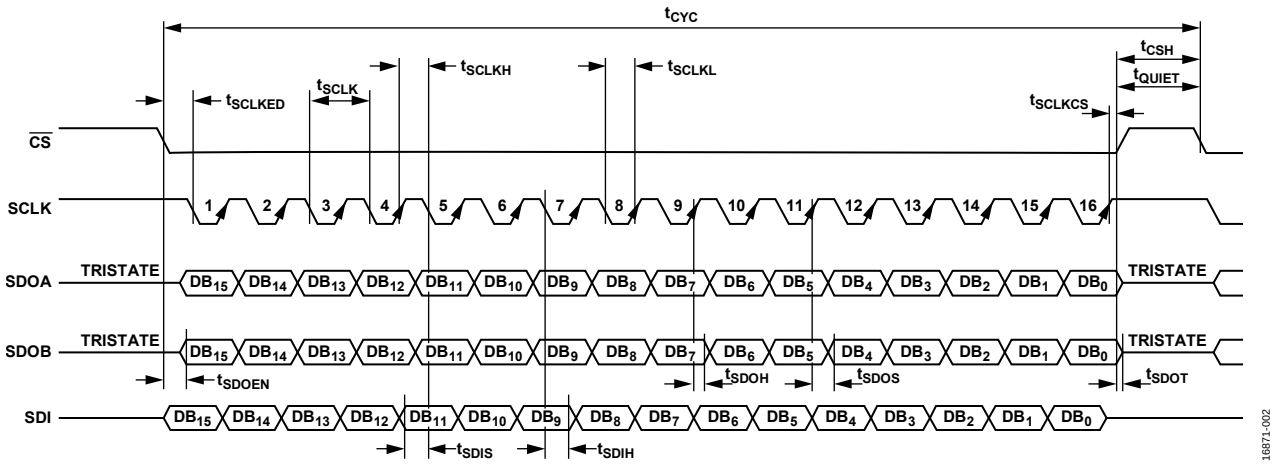


Figure 2. Serial Interface Timing Diagram

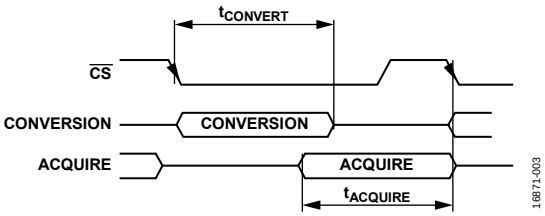


Figure 3. Internal Conversion Acquire Timing

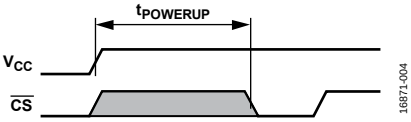


Figure 4. Power-Up Time to Conversion

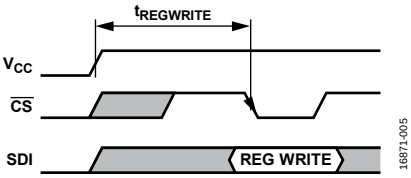


Figure 5. Power-Up Time to Register Read Write Access

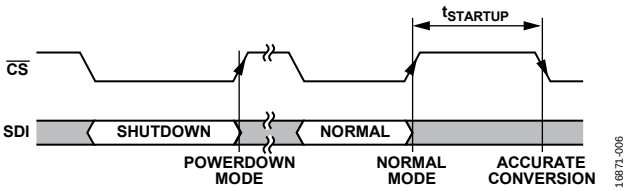
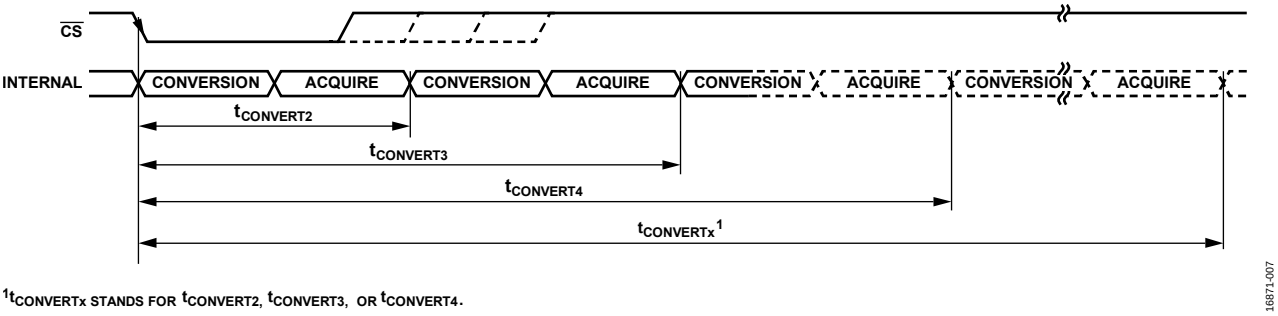


Figure 6. Power-Down to Normal Mode Timing



[1] $t_{CONVERTx}$ STANDS FOR $t_{CONVERT2}$, $t_{CONVERT3}$, OR $t_{CONVERT4}$.

Figure 7. Conversion Timing During OS Normal Mode

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
V_{CC} to Ground (GND)	−0.3 V to +4 V
V_{LOGIC} to GND	−0.3 V to +4 V
Analog Input Voltage to GND	−0.3 V to V_{REF} +0.3 V, V_{CC} + 0.3 V, 4 V
Digital Input Voltage to GND	−0.3 V to V_{LOGIC} + 0.3 V, 4 V
Digital Output Voltage to GND	−0.3 V to V_{LOGIC} + 0.3 V, 4 V
Reference Input and Output (REFIO) Input to GND	−0.3 V to V_{CC} + 0.3 V, 4 V
Input Current to Any Pin Except Supplies	±10 mA
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Pb-Free Soldering Reflow Temperature	260°C
Electrostatic Discharge (ESD) Ratings	
Human Body Model (HBM)	4 kV
Field Induced Charge Device Model (FICDM)	1.25 kV

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-16-45[1]	55.4	12.7	°C/W

[1] Test Condition 1: thermal impedance simulated values are based on JEDEC 2S2P thermal test board four thermal vias. See JEDEC JESD-51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

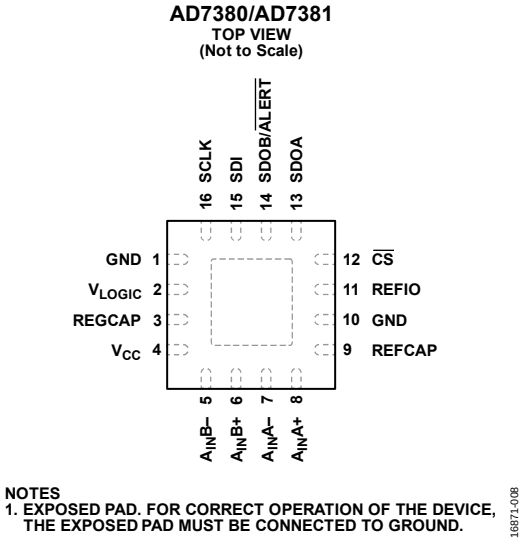


Figure 8. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 10	GND	Ground Reference Point. This pin is the ground reference point for all circuitry on the device.
2	V_{LOGIC}	Logic Interface Supply Voltage, 1.65 V to 3.6 V. Decouple this pin to GND with a 1 µF capacitor.
3	REGCAP	Decoupling Capacitor Pin for Voltage Output from Internal Regulator. Decouple this pin to GND with a 1 µF capacitor. The voltage at this pin is 1.9 V typical.
4	V_{CC}	Power Supply Input Voltage, 3.0 V to 3.6 V. Decouple this pin to GND using a 1 µF capacitor.
5, 6	$A_{IN}B–$, $A_{IN}B+$	Analog Inputs of ADC B. These analog inputs form a differential pair.
7, 8	$A_{IN}A–$, $A_{IN}A+$	Analog Inputs of ADC A. These analog inputs form a differential pair.
9	REFCAP	Decoupling Capacitor Pin for Band Gap Reference. Decouple this pin to GND with a 0.1 µF capacitor. The voltage at this pin is 2.5 V typical.
11	REFIO	Reference Input and Output. The on-chip reference of 2.5 V is available as an output on this pin for external use if the device is configured accordingly. Alternatively, an external reference of 2.5 V to 3.3 V can be input to this pin. Decoupling is required on this pin for both the internal and external reference options. A 1 µF capacitor must be applied from this pin to GND.
12	$\overline{CS}$	Chip Select Input. Active low, logic input. This input provides the dual function of initiating conversions on the AD7380 and the AD7381 and framing the serial data transfer.
13	SDOA	Serial Data Output A. This pin functions as a serial data output pin to access the ADC A or ADC B conversion results or data from any of the on-chip registers.
14	SDOB/$\overline{ALERT}$	Serial Data Output B/Alert Indication Output. This pin can operate as a serial data output pin or alert indication output. SDOB. This pin functions as a serial data output pin to access the ADC B conversion results. $\overline{ALERT}$. This pin operates as an alert pin going low to indicate that a conversion result has exceeded a configured threshold.
15	SDI	Serial Data Input. This input provides the data written to the on-chip control registers.
16	SCLK	Serial Clock Input. This serial clock input is for data transfers to and from the ADC.
	EPAD	Exposed Pad. For correct operation of the device, the exposed pad must be connected to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{REF} = 2.5 V internal, V_{CC} = 3.6 V, V_{LOGIC} = 3.3 V, f_{SAMPLE} = 4 MSPS, f_{IN} = 1 kHz, and T_A = 25°C, unless otherwise noted.

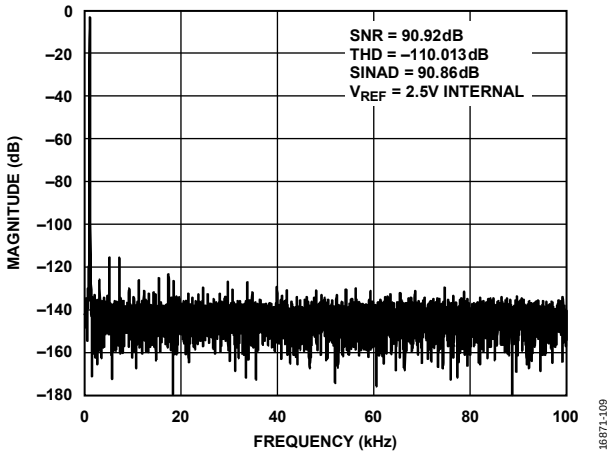


Figure 9. Fast Fourier Transform (FFT), V_{REF} = 2.5 V Internal

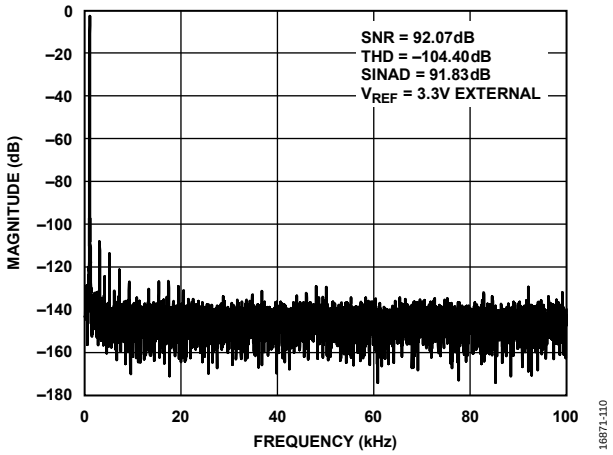


Figure 10. FFT, V_{REF} = 3.3 V External

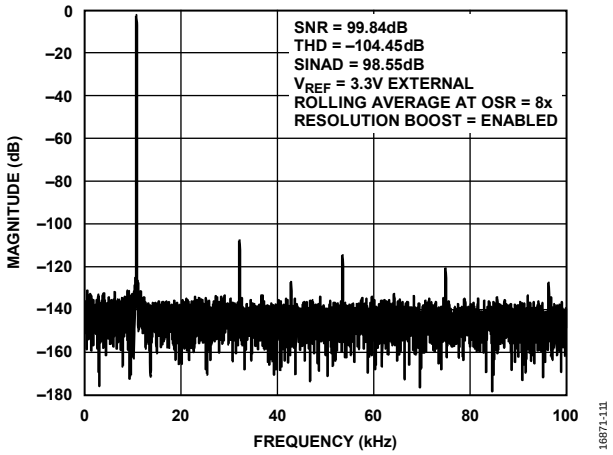


Figure 11. FFT with Oversampling, V_{REF} = 3.3 V External

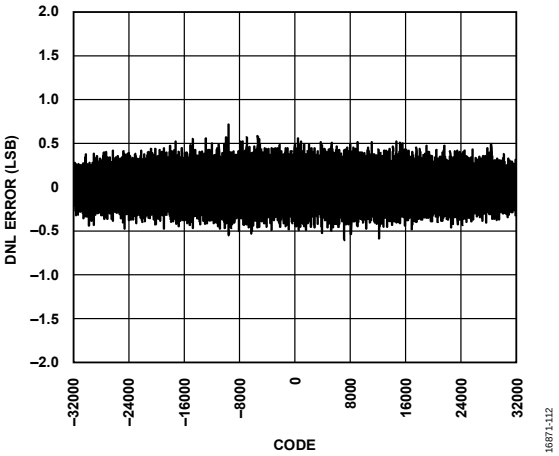


Figure 12. Typical DNL Error

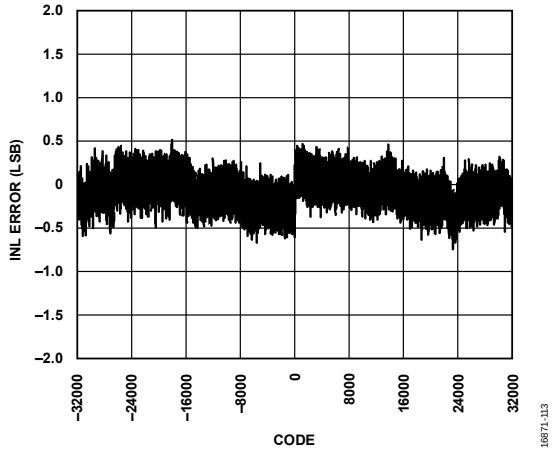


Figure 13. Typical INL Error

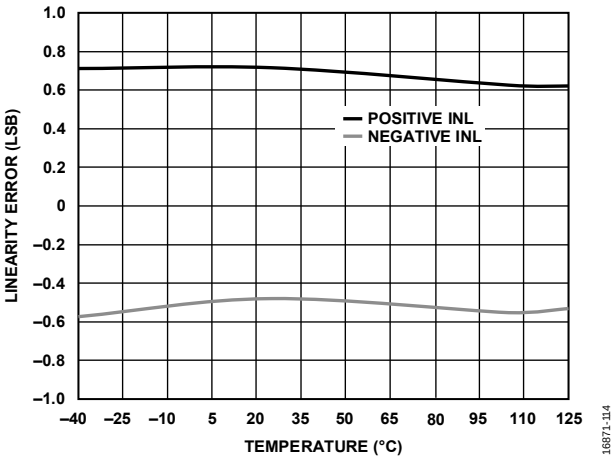


Figure 14. Linearity Error vs. Temperature

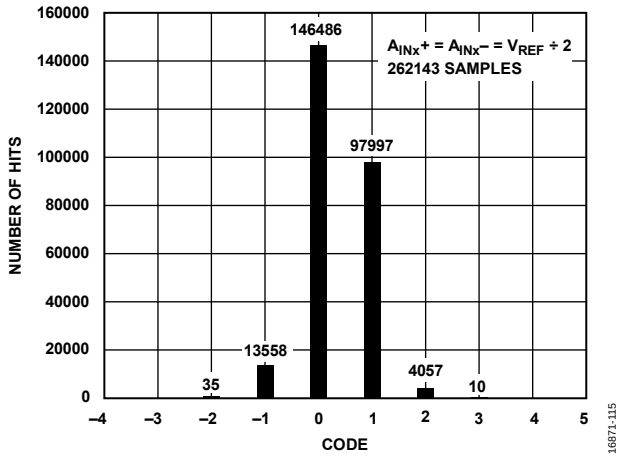


Figure 15. DC Histogram Codes at Code Center

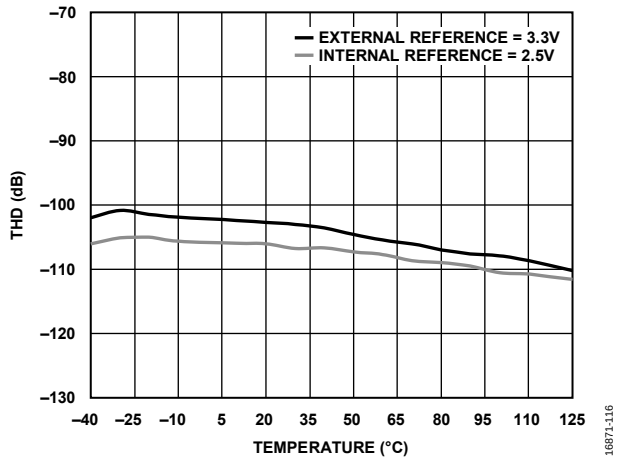


Figure 16. THD vs. Temperature

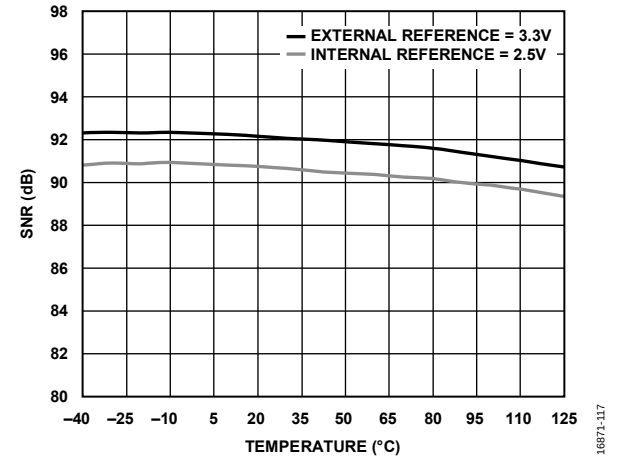


Figure 17. SNR vs. Temperature

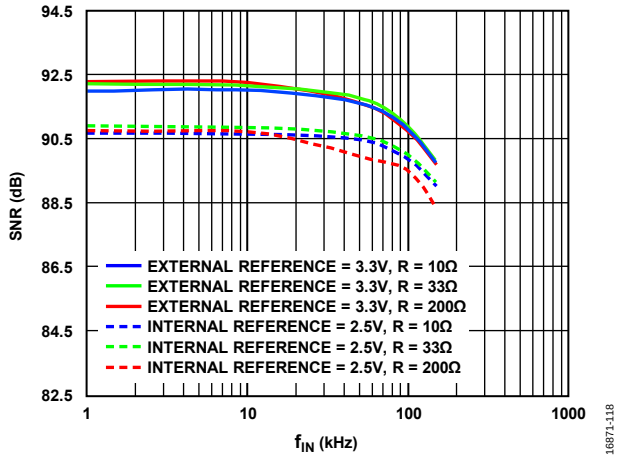


Figure 18. SNR vs. f_{IN} (R Means Resistance)

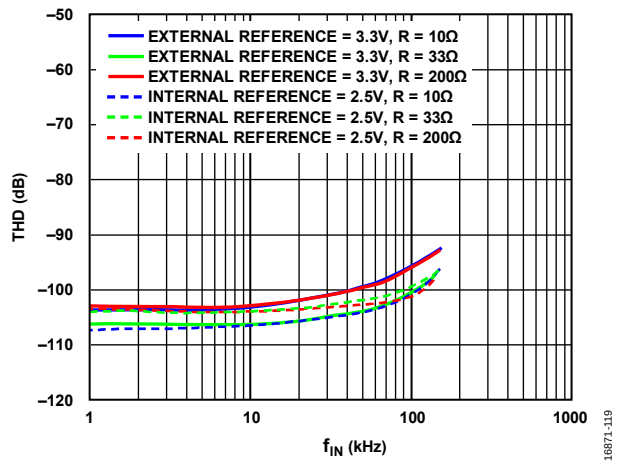


Figure 19. THD vs. f_{IN}

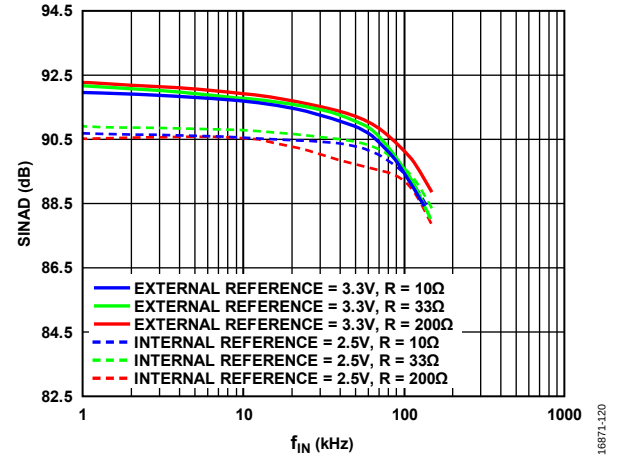


Figure 20. SINAD vs. f_{IN}

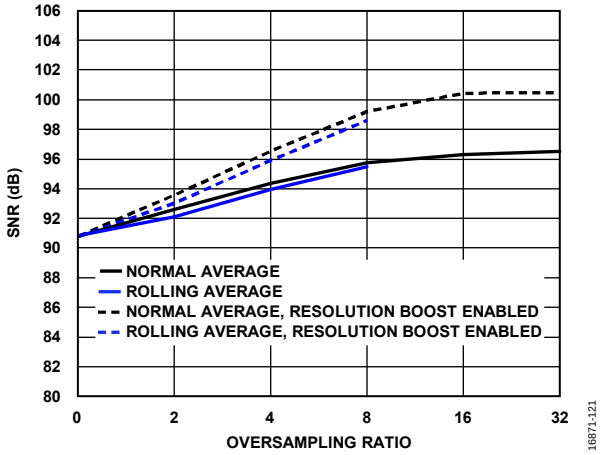


Figure 21. SNR vs. Oversampling Ratio

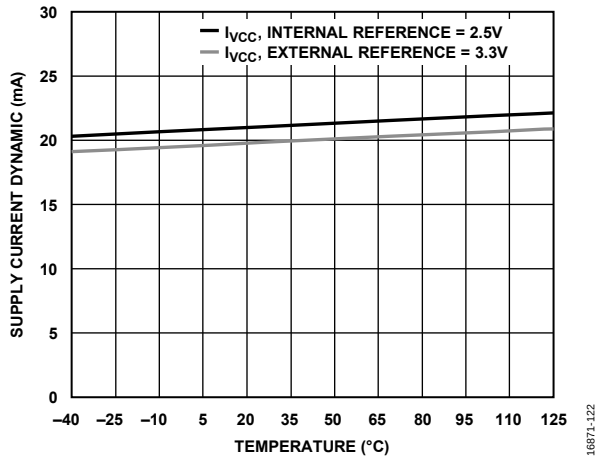


Figure 22. Supply Current Dynamic vs.Temperature

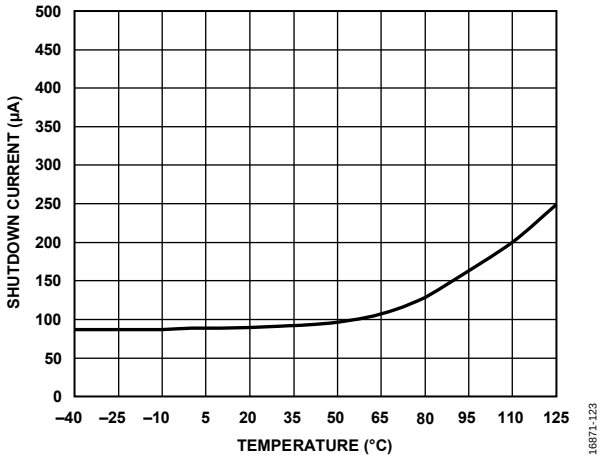


Figure 23. Shutdown Current vs. Temperature

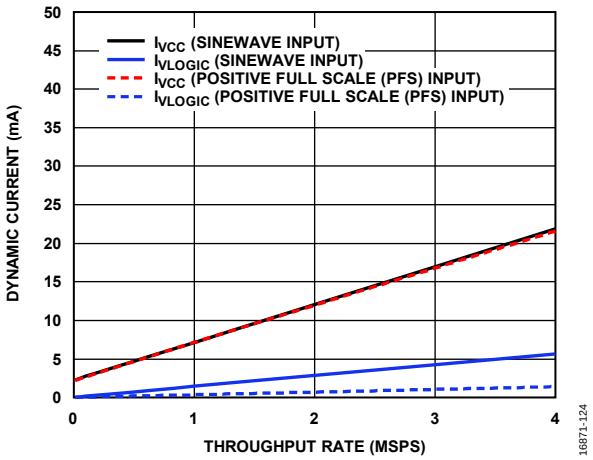


Figure 24. Dynamic Current at Different Input Signal vs. Throughput Rate

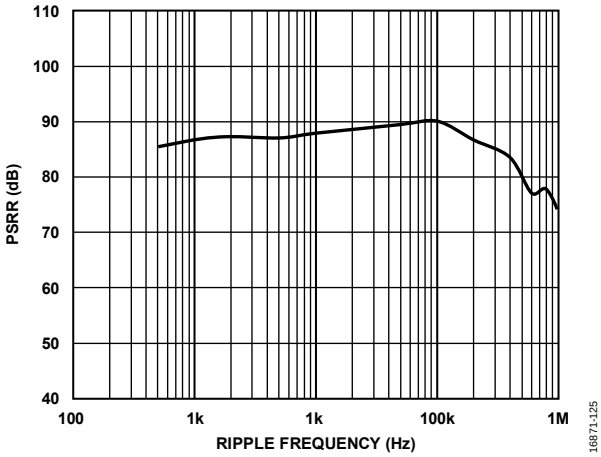


Figure 25. Power Supply Rejection Ratio (PSRR) vs. Ripple Frequency

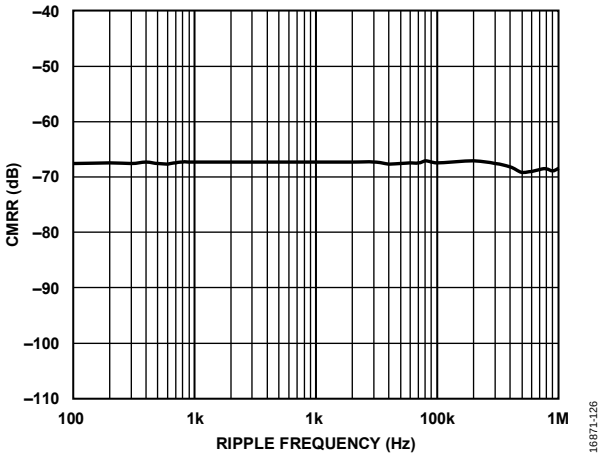


Figure 26. CMRR vs. Ripple Frequency

TERMINOLOGY

Differential Nonlinearity (DNL)
In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. DNL is often specified in terms of resolution for which no missing codes are guaranteed.

Integral Nonlinearity (INL)
INL is the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Gain Error
The first transition (from 100 … 000 to 100 … 001) occurs at a level ½ LSB above nominal negative full scale. The last transition (from 011 … 110 to 011 … 111) occurs for an analog voltage 1½ LSB below the nominal full scale. The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Gain Error Temperature Drift
The gain error drift is the gain error change due to a temperature change of 1°C.

Gain Error Match
Gain error match is the difference in negative full-scale error between the input channels and the difference in positive full-scale error between the input channels.

Zero Error
Zero error is the difference between the ideal midscale voltage, 0 V, and the actual voltage producing the midscale output code, 0 LSB.

Zero Error Drift
The zero error drift is the zero error change due to a temperature change of 1°C.

Zero Error Matching
Zero error matching is the difference in zero error between the input channels.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels (dB).

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in dB, between the rms amplitude of the input signal and the peak spurious signal.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in dB.

Signal-to-(Noise + Distortion) (SINAD)
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components that are less than the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in dB.

Analog Input Common-Mode Rejection Ratio (CMRR)
CMRR is the ratio of the power in the ADC output at the frequency, f, to the power of a 200 mV p-p sine wave applied to the common-mode voltage of $A_{IN}x+$ and $A_{IN}x-$ of frequency, f.

$$CMRR\ (dB) = 10log(P_{ADC_IN}/P_{ADC_OUT})$$

where:
P_{ADC_IN} is the common-mode power at the frequency, f, applied to the $A_{IN}x+$ and $A_{IN}x-$ inputs.
P_{ADC_OUT} is the power at the frequency, f, in the ADC output.

Aperture Delay
Aperture delay is the measure of the acquisition performance and is the time between the falling edge of the $\overline{CS}$ input and when the input signal is held for a conversion.

Aperture Delay Match
Aperture delay match is the difference of the aperture delay between ADC A and ADC B.

Aperture Jitter
Aperture jitter is the variation in aperture delay.

THEORY OF OPERATION

CIRCUIT INFORMATION

The AD7380/AD7381 are high speed, dual simultaneous sampling, fully differential 16-bit/14-bit, SAR ADCs. The AD7380/AD7381 operate from a 3.0 V to 3.6 V power supply and feature throughput rates up to 4 MSPS.

The AD7380/AD7381 contain two SAR ADCs and a serial interface with two separate data output pins. The device is housed in a 16-lead LFCSP, offering the user considerable space-saving advantages over alternative solutions.

Data is accessed from the device via the serial interface. The interface can operate with two or one serial outputs. The AD7380/AD7381 have an on-chip 2.5 V internal V_{REF}. If an external reference is desired, the internal reference can be disabled, and a reference value ranging from 2.5 V to 3.3 V can be supplied. If the internal reference is used elsewhere in the system, buffer the reference output. The differential analog input range for the AD7380/AD7381 is the common-mode voltage (V_{CM}) ± V_{REF}/2.

The AD7380/AD7381 feature an on-chip oversampling block to improve performance. Normal average and rolling average oversampling modes and power-down options that allow power saving between conversions are also available. Configuration of the device is implemented via the standard SPI (see the Interface section).

CONVERTER OPERATION

The AD7380/AD7381 have two SAR ADCs, each based around two capacitive digital-to-analog converters (DACs). Figure 27 and Figure 28 show simplified schematics of one of the ADCs in acquisition and conversion phases, respectively. The ADC comprises control logic, an SAR, and two capacitive DACs. In Figure 27 (the acquisition phase), SW3 is closed, SW1 and SW2 are in Position A, the comparator is held in a balanced condition, and the sampling capacitor (C_S) arrays can acquire the differential signal on the input.

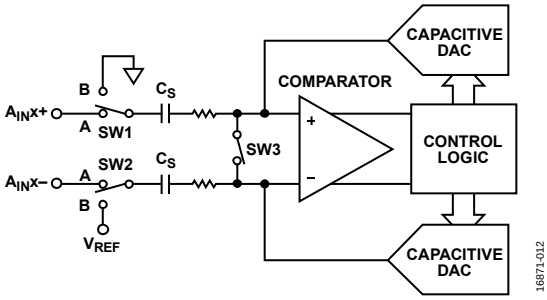


Figure 27. ADC Acquisition Phase

When the ADC starts a conversion (see Figure 28), SW3 opens and SW1 and SW2 move to Position B, causing the comparator to become unbalanced. Both inputs are disconnected when the conversion begins. The control logic and charge redistribution DACs are used to add and subtract fixed amounts of charge from the sampling capacitor arrays to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. The output impedances of the sources driving the A_{INX}+ and A_{INX}− pins must be matched. Otherwise, the two inputs have different settling times, resulting in errors.

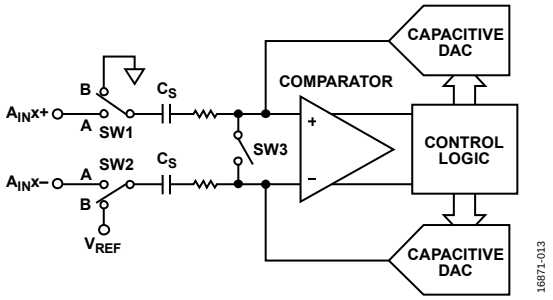


Figure 28. ADC Conversion Phase

ANALOG INPUT STRUCTURE

Figure 29 shows the equivalent circuit of the analog input structure of the AD7380/AD7381. The four diodes provide ESD protection for the analog inputs. Ensure that the analog input signals never exceed the supply rails by more than 300 mV. Exceeding the limit causes these diodes to become forward-biased and start conducting into the substrate. These diodes can conduct up to 10 mA without causing irreversible damage to the device.

The C1 capacitors in Figure 29 are typically 3 pF and are primarily attributed to pin capacitance. The R1 resistors are lumped components made up of the on resistance of the switches. The value of these resistors is typically about 200 Ω. The C2 capacitors are sampling capacitors of the ADC with a capacitance of 15 pF typically.

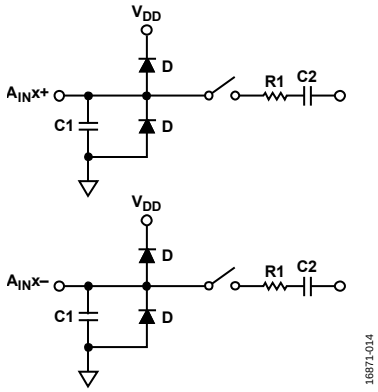


Figure 29. Equivalent Analog Input Circuit, Conversion Phase—Switches Open, Track Phase—Switches Closed

ADC TRANSFER FUNCTION

The AD7380/AD7381 can use a 2.5 V to 3.3 V V_{REF}. The AD7380/AD7381 convert the differential voltage of the analog inputs ($A_{IN}A+$, $A_{IN}A-$, $A_{IN}B+$, and $A_{IN}B-$) into a digital output.

The conversion result is MSB first, twos complement. The LSB size is $(2 \times V_{REF})/2^N$, where N is the ADC resolution. The ADC resolution is determined by the resolution of the device chosen, and if resolution boost mode is enabled. Table 8 outlines the LSB size expressed in milivolts for different resolutions and reference voltages options.

The ideal transfer characteristic for the AD7380/AD7381 is shown in Figure 30.

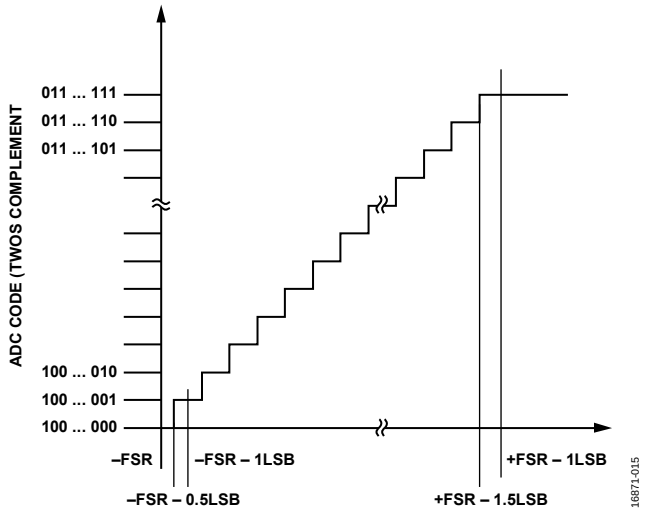


Figure 30. ADC Ideal Transfer Function (FSR = Full-Scale Range)

Table 8. LSB Size

Resolution	2.5 V Reference	3.3 V Reference	Unit
14-bit	305.2	402.8	µV
16-bit	76.3	100.7	µV
18-bit	19.1	25.2	µV

APPLICATIONS INFORMATION

Figure 31 shows an example of a typical application circuit for the AD7380/AD7381. Decouple the V_{CC}, V_{LOGIC}, REGCAP, and REFIO pins with suitable decoupling capacitors as shown.

The exposed pad is a ground reference point for circuitry on the device and must be connected to the board ground.

Place a differential RC filter on the analog inputs to ensure optimal performance is achieved. On a typical application, it is recommended that R = 33 Ω, C1 = 68 pF, and C2 = 330 pF. Figure 18 shows the SNR performance at different R values across the input frequency range.

The performance of the AD7380/AD7381 devices may be impacted by noise on the digital interface. This impact depends on the on-board layout and design. Keep a minimal distance between the digital line and the digital interface, or place a 100 Ω resistor in series and close to the SDOA pin and SDOB/$\overline{\text{ALERT}}$ pin to reduce noise from the digital interface coupling of the AD7380/AD7381.

The two differential channels of the AD7380/AD7381 can accept an input voltage range from 0 V to V_{REF} and has a wide common-mode range that allows the conversion of a variety of signals. These analog input pins can easily be driven with an amplifier.

Table 9 lists the recommended driver amplifiers that best fit and add value to the application.

The AD7380/AD7381 has an internal 2.5 V reference and can use an ultralow noise, high accuracy voltage reference as an external voltage source ranging from 2.5 V to 3.3 V such as the ADR4533 and ADR4525.

POWER SUPPLY

The typical application circuit in Figure 31 can be powered by a single 5 V (V+) voltage source that supplies the whole signal chain. The 5 V supply can come from a low noise, complementary metal-oxide semiconductor (CMOS) low dropout (LDO) regulator (ADP7105). The driver amplifier supply is provided by the+ 5 V (V+) and −2.5 V (V−), which is derived from the inverter, for example, the ADM660. The inverter then converts the +5 V to −5 V and supplies this voltage to the ADP7182 low noise voltage regulator to output the −2.5 V.

The two independent supplies of the AD7380/AD7381, V_{CC} and V_{LOGIC}, that supply the analog circuitry and digital interface, respectively, can be supplied by a low quiescent current LDO regulator such as the ADP166. The ADP166 is a suitable supply with a fixed output voltage range from 1.2 V to 3.3 V for typical V_{CC} and V_{LOGIC} levels. Decouple both the V_{CC} supply and the V_{LOGIC} supply separately with a 1 µF capacitor. Additionally, there is an internal LDO regulator that supplies the AD7380/AD7381. The on-chip regulator provides a 1.9 V supply for internal use on the device only. Decouple the REGCAP pin with a 1 µF capacitor connected to GND.

Power-Up

The AD7380/AD7381 are robust to power supply sequencing. V_{CC} and V_{LOGIC} can be applied in any sequence. After V_{CC} and V_{LOGIC} are applied, an external reference must be applied.

The AD7380/AD7381 require a $t_{POWERUP}$ time from applying V_{CC} and V_{LOGIC} until the ADC conversion results are stable. Applying $\overline{\text{CS}}$ pulses, or interfacing with the AD7380/AD7381 prior to the setup time elapsing, does not have a negative impact on ADC operation. Conversion results are not guaranteed to meet data sheet specifications during this time, however, and must be ignored.

Table 9. Signal Chain Components

Companion Parts	Part Name	Description	Typical Application
ADC Driver	ADA4896-2	1 nV/√Hz, rail to rail output amplifier	Precision, low noise, high frequency
	ADA4940-2	Ultralow power, full differential, low distortion	Precision, low density, low power
	ADA4807-2	1 mA, rail-to-rail output amplifier	Precision, low power, high frequency
External Reference	ADR4525	Ultralow noise, high accuracy 2.5 V voltage reference	2.5 V reference voltage
	ADR4533	Ultralow noise, high accuracy 3.3 V voltage reference	3.3 V reference voltage
LDO Regulator	ADP166	Low quiescent, 150 mA, LDO regulator	3.0 V to 3.6 V supply for V_{CC} and V_{LOGIC}
	ADP7104	Low noise, CMOS LDO regulator	5 V supply for driver amplifier
	ADP7182	Low noise line regulator	−2.5 V supply for driver amplifier

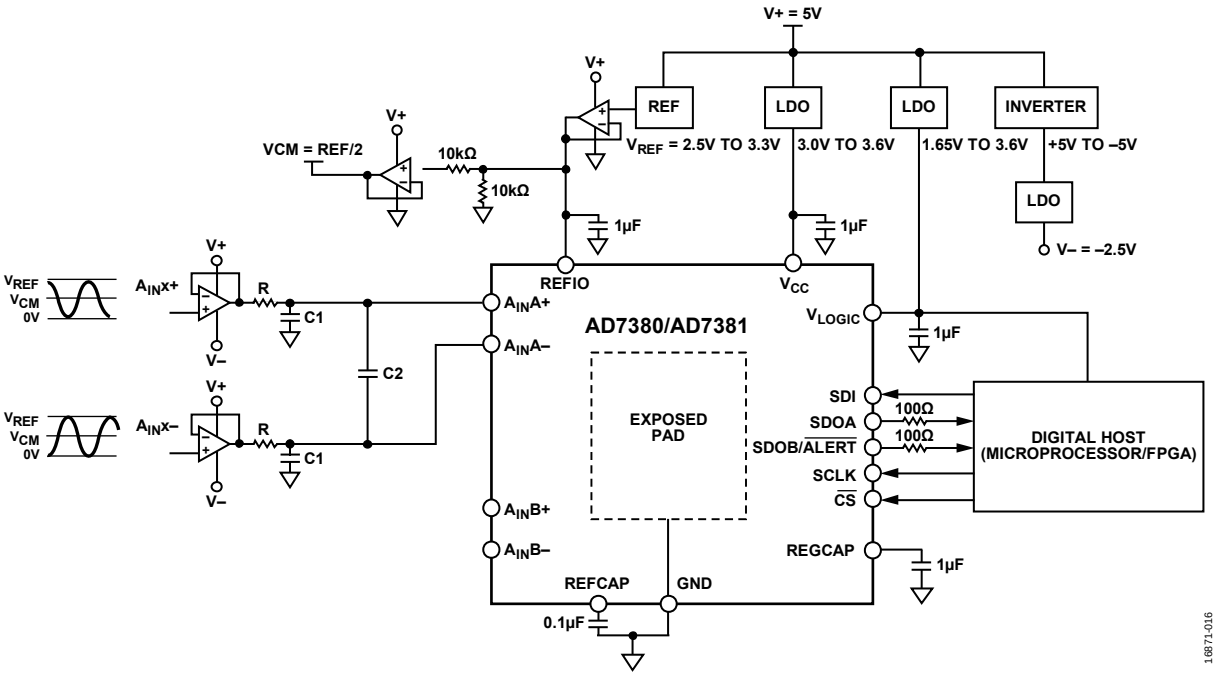


Figure 31. Typical Application Circuit

MODES OF OPERATION

The AD7380/AD7381 have several on-chip configuration registers for controlling the operational mode of the device.

OVERSAMPLING

Oversampling is a common method used in analog electronics to improve the accuracy of the ADC result. Multiple samples of the analog input are captured and averaged to reduce the noise component from quantization noise and thermal noise (kTC) of the ADC. The AD7380/AD7381 offer an oversampling function on-chip and have two user configurable oversampling modes, normal average and rolling average.

The oversampling functionality is configured by programming the OS_MODE bit and OSR bits in the CONFIGURATION1 register.

Normal Average Oversampling

Normal average oversampling mode can be used in applications where slower output data rates are allowable and where higher SNR or dynamic range is desirable. Normal average oversampling involves taking a number of samples, adding the samples together, and dividing the result by the number of samples taken. This result is then output from the device. The sample data is cleared after the process is completed.

Normal average oversampling mode is configured by setting the OS_MODE bit to Logic 0 and having a valid nonzero value in the OSR bits. Writing to the OSR bits has a two cycle latency before the register gets updated. The oversampling ratio of the digital filter is controlled using the oversampling bits, OSR, which provides the oversampling bit decoding to select the different oversample rates. The output result is decimated to 16-bit resolution for the AD7380 and 14-bit resolution for the AD7381. If additional resolution is required, configure the resolution boost bit in the CONFIGURATION1 register. See the Resolution Boost section for further details.

The number of samples, n, defined by the OSR bits are taken, added together, and the result is divided by n. The initial ADC conversion is initiated by the falling edge of $\overline{CS}$, and the AD7380/AD7381 control all subsequent samples in the oversampling sequence internally. The sampling rate of the additional n samples is at 3 MSPS for the AD7380 and 4 MSPS for AD7381 in normal average oversampling mode. The oversampled conversion result is ready for read back on the next serial interface access. After the technique is applied, the sample data used in the calculation is discarded. This process is repeated every time the application needs a new conversion result and initiates at the falling edge of $\overline{CS}$.

As the output data rate is reduced by the oversampling ratio, the serial peripheral interface (SPI) SCLK frequency required to transmit the data is also reduced accordingly.

Table 10. AD7380/AD7381 Normal Average Oversampling Performance Overview

Oversampling Ratio	AD7380					AD7381		
	SNR (dB typical)				Output Data Rate (kSPS Maximum)	SNR (dB typical)		Output Data Rate (kSPS Maximum)
	V_{REF} = 2.5 V		V_{REF} = 3.3 V					
	RES = 0	RES = 1	RES = 0	RES = 1		RES = 0	RES = 1	
Disabled	90.8	90.8	92.5	92.5	4000	85.2	85.2	4000
2	92.6	93.6	94.0	95.5	1500	84.7	88	2000
4	94.3	96.5	95.4	98.2	750	85.2	91.1	1000
8	95.8	99.2	96.3	100.5	375	85.5	93	500
16	96.3	100.4	96.8	102.0	187.5	85.7	94.6	250
32	96.5	100.5	97.0	102.8	93.75	85.9	95.6	125

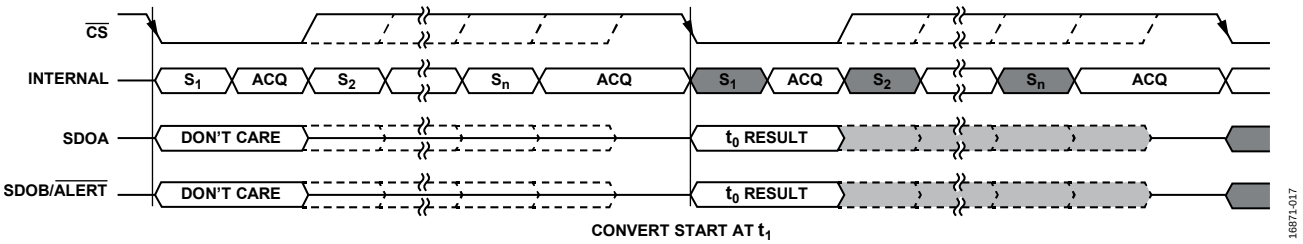


Figure 32. Normal Average Oversampling Operation

Rolling Average Oversampling

Rolling average oversampling mode can be used in applications where higher output data rates are required and where higher SNR or dynamic range is desirable. Rolling average oversampling involves taking a number of samples, adding the samples together, and dividing the result by the number of samples taken. This result is then output from the device. The sample data is not cleared after the process is completed. The rolling average oversampling mode uses a first in, first out (FIFO) buffer of the most recent samples in the averaging calculation, allowing the ADC throughput rate and output data rate to stay the same.

Rolling average oversampling mode is configured by setting the OS_MODE bit to Logic 1 and having a valid nonzero value in the OSR bits. The oversampling ratio of the digital filter is controlled using the oversampling bits, OSR (see Table 11). The output result is decimated to 16-bit resolution for the AD7380 and 14-bit result for the AD7381. If additional resolution is required, this resolution can be achieved by configuring the resolution boost bit in the CONFIGURATION1 register. See the Resolution Boost section for further details.

In rolling average oversampling mode, all ADC conversions are controlled and initiated by the falling edge of $\overline{CS}$. After a conversion is complete, the result is loaded into the FIFO. The FIFO length is 8, regardless of the oversampling ratio set. The FIFO is filled on the first conversion after a power-on reset, the first conversion after a software controlled hard or soft reset, or the first conversion after the REFSEL bit is toggled. A new conversion result is shifted into the FIFO on completion of every ADC conversion, regardless of the status of the OSR bits and the OS_MODE bit. This conversion allows a seamless transition from no oversampling to rolling average oversampling, or different rolling average oversampling ratios without waiting for the FIFO to fill.

The number of samples, n, defined by the OSR bits are taken from the FIFO, added together, and the result is divided by n. The time between $\overline{CS}$ falling edges is the cycle time which can be controlled by the user, depending on the desired data output rate.

Table 11. AD7380/AD7381 Rolling Averaging Oversampling Performance Overview

Oversampling Ratio	AD7380					AD7381		
	SNR (dB typical)				Output Data Rate (kSPS Maximum)	SNR (dB typical)		Output Data Rate (kSPS Maximum)
	V_{REF} = 2.5 V		V_{REF} = 3.3 V					
	RES = 0	RES = 1	RES = 0	RES = 1		RES = 0	RES = 1	
Disabled	91	91	92.5	92.5	4000	85	85	4000
2	92	93	93.2	94.5	4000	84.5	87.7	4000
4	94	96	94.8	97.2	4000	85	91	4000
8	95.5	98.6	95.9	99.6	4000	85.5	93	4000

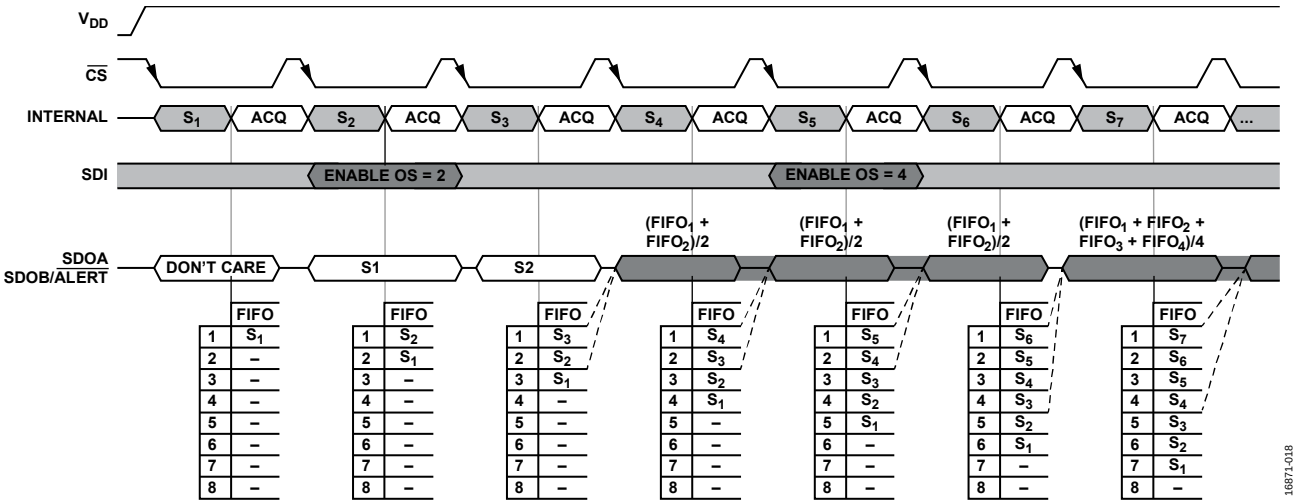


Figure 33. Rolling Average Oversampling Operation

RESOLUTION BOOST

The default conversion result output data size for the AD7380 is 16 bits and for the AD7381 is 14 bits. When the on-chip oversampling function is enabled, the performance of the ADC can exceed the 16-bit level for the AD7380 or the 14-bit level for the AD7381. To accommodate the performance boost achievable, enable an additional two bits of resolution. If the RES bit in the CONFIGURATION1 register is set to Logic 1 and the AD7380/AD7381 are in a valid oversampling mode, the conversion result size for the AD7380 is 18 bits and for the AD7381 is 16 bits. In this mode, 18 SCLK cycles are required to propagate the data for the AD7380 and 16 SCLK cycles are required for the AD7381.

ALERT

The alert functionality is an out of range indicator and can be used as an early indicator of an out of bounds conversion result. An alert event triggers when the conversion result value register exceeds the alert high limit value in the ALERT_HIGH_THRESHOLD register or falls below the alert low limit value in the ALERT_LOW_THRESHOLD register. The ALERT_HIGH_THRESHOLD register and the ALERT_LOW_THRESHOLD register are common to all ADCs. When setting the threshold limits, the alert high threshold must always be greater than the alert low threshold. Detailed alert information is accessible in the $\overline{\text{ALERT}}$ register.

The register contains two status bits per ADC, one corresponding to the high limit, and the other to the low limit. A logical OR of alert signals for all ADCs creates a common alert value. This value can be configured to drive out on the $\overline{\text{ALERT}}$ function of the SDOB/$\overline{\text{ALERT}}$ pin. The SDOB/$\overline{\text{ALERT}}$ pin is configured as $\overline{\text{ALERT}}$ by configuring the following bits in the CONFIGURATION1 register and the CONFIGURATION2 register:

- Set the SDO bit to 1.
- Set the ALERT_EN bit to 1.

In addition, set a valid value to the ALERT_HIGH_THRESHOLD register and the ALERT_LOW_THRESHOLD register.

The alert indication function is available in oversampling, both rolling average and normal average, and in nonoversampling modes.

The $\overline{\text{ALERT}}$ function of the SDOB/$\overline{\text{ALERT}}$ pin gets updated at the end of conversion. The alert indication status bits in the $\overline{\text{ALERT}}$ register get updated as well and must be read before the end of next conversion. The $\overline{\text{ALERT}}$ function of the SDOB/$\overline{\text{ALERT}}$ pin is cleared with a falling edge of $\overline{\text{CS}}$. Issuing a software reset also clears the alert status in the $\overline{\text{ALERT}}$ register.

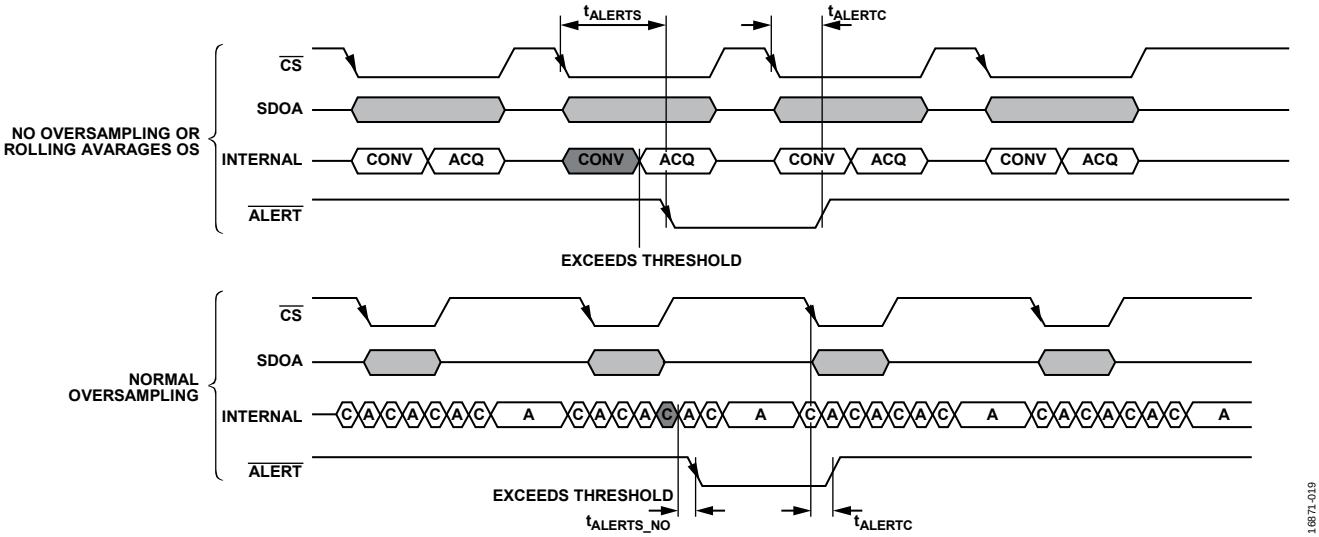


Figure 34. Alert Operation

POWER MODES

The AD7380/AD7381 have two power modes that can be set in the CONFIGURATION1 register, normal mode and shutdown mode. These modes of operation provide flexible power management options, allowing optimization of the power dissipation and throughput rate ratio for different application requirements.

Program the PMODE bit in the CONFIGURATION1 register to configure the power modes in the AD7380/AD7381. Set PMODE to Logic 0 for normal mode and Logic 1 for shutdown mode.

Normal Mode

Keep the AD7380/AD7381 in normal mode to achieve the fastest throughput rate. All blocks within the AD7380/AD7381 remain fully powered at all times, and an ADC conversion can be initiated by a falling edge of $\overline{CS}$, when required. When the AD7380/AD7381 are not converting, the devices are in static mode, and power consumption is automatically reduced. Additional current is required to perform a conversion. Therefore, power consumption on the AD7380/AD7381 scales with throughput.

Shutdown Mode

When slower throughput rates and lower power consumption are required, use shutdown mode by either powering down the ADC between each conversion or by performing a series of conversions at a high throughput rate and then powering down the ADC for a relatively long duration between these burst conversions. When the AD7380/AD7381 are in shutdown mode, all analog circuitry powers down, including the internal reference, if enabled. The serial interface remains active during shutdown mode to allow the AD7380/AD7381 to exit shutdown mode.

To enter shutdown mode, write to the PMODE bit in the CONFIGURATION1 register. The AD7380/AD7381 shuts down and current consumption reduces.

To exit shutdown mode and return to normal mode, set the PMODE bit in the CONFIGURATION1 register to Logic 0. All register configuration settings remain unchanged entering or leaving shutdown mode. After exiting shutdown mode, allow sufficient time for the circuitry to turn on before starting a conversion. If the internal reference is enabled, allow the reference to settle for accurate conversions to happen.

INTERNAL AND EXTERNAL REFERENCE

The AD7380/AD7381 have a 2.5 V internal reference. Alternatively, if a more accurate reference or higher dynamic range is required, an external reference can be supplied. An externally supplied reference can be in the range of 2.5 V to 3.3 V.

Reference selection, internal/external, is configured by the REFSEL bit in the CONFIGURATION1 register. If REFSEL is set to 0, the internal reference buffer is enabled. If an external reference is preferred, the REFSEL bit must be set to 1, and an external reference must be supplied to the REFIO pin.

SOFTWARE RESET

The AD7380/AD7381 have two reset modes, a soft reset and a hard reset. A reset is initiated by writing to the RESET bits, Bits[7:0], in the CONFIGURATION2 register.

A soft reset maintains the contents of the configurable registers but refreshes the interface and the ADC blocks. Any internal state machines are reinitialized, and the oversampling block and FIFO are flushed. The $\overline{ALERT}$ register is cleared. The reference and LDO remain powered.

A hard reset, in addition to the blocks reset by a soft reset, resets all user registers to the default status, resets the reference buffer, and resets the internal oscillator block.

DIAGNOSTIC SELF TEST

The AD7380/AD7381 run a diagnostic self test after a power-on reset (POR) or after a software hard reset to ensure correct configuration is loaded into the device.

The result of the self test is displayed in the SETUP_F bit in the $\overline{ALERT}$ register. If the SETUP_F bit is set to Logic 1, the diagnostic self test fails. If the test fails, perform a software hard reset to reset the AD7380/AD7381 registers to the default status.

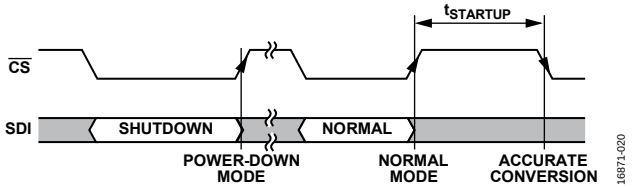


Figure 35. Shutdown Mode Operation

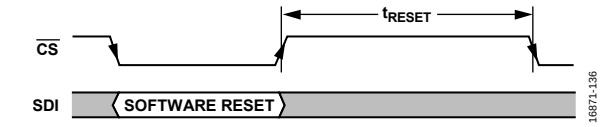


Figure 36. Software Reset Operation

INTERFACE

The interface to the AD7380/AD7381 is via the SPI. The interface consists of a $\overline{CS}$, SCLK, SDOA, SDOB/$\overline{ALERT}$, and SDI pins.

The $\overline{CS}$ signal frames a serial data transfer and initiates an ADC conversion process. The falling edge of $\overline{CS}$ puts the track-and-hold into hold mode, at which point, the analog input is sampled, and the bus is taken out of three-state.

The SCLK signal synchronizes data in and out of the device via the SDOA, SDOB, and SDI signals. A minimum of 16 SCLK cycles are required for a write to or read from a register. The minimum numbers of SCLK pulses for a conversion read is dependent on the resolution of the device and the configuration settings, see Table 12.

The ADC conversion operation is driven internally by an on-board oscillator and is independent of the SCLK signal.

The AD7380/AD7381 have two serial output signals, SDOA and SDOB. To achieve the highest throughput of the device, use both SDOA and SDOB, 2-wire mode, to read the conversion results. If a reduced throughput is required or oversampling is used, it is possible to use 1-wire mode, SDOA signal only, for reading conversion results. Programming the SDO bit in the CONFIGURATION2 register configures 2-wire or 1-wire mode.

Configuring the cyclic redundancy check (CRC) operation for SPI reads or SPI writes alters the operation of the interface. The relevant sections of this data sheet must be consulted to ensure correct operation.

READING CONVERSION RESULTS

The $\overline{CS}$ signal initiates the conversion process. A high to low transition on the $\overline{CS}$ signal initiates a simultaneous conversion of both ADCs, ADC A and ADC B. The AD7380/AD7381 have one cycle readback latency. Therefore, the conversion results are available on the next SPI access. Then, take the $\overline{CS}$ signal low, and the conversion result clocks out on the serial output pins. The next conversion also initiates at this point.

The conversion result shifts out of the device as a 16-bit result for the AD7380 and a 14-bit result for the AD7381. The MSB of the conversion result shifts out on the $\overline{CS}$ falling edge. The remaining data shifts out of the device under the control of the SCLK input. The data shifts out on the rising edge of the SCLK, and the data bits are valid on both the falling edge and the rising edge. After the final SCLK falling edge, take $\overline{CS}$ high again to return the SDOA and the SDOB/$\overline{ALERT}$ pins to a high impedance state.

The number of SCLK cycles to propagate the conversion results on the SDOA and the SDOB/$\overline{ALERT}$ pins is dependent on the serial mode of operation configured and if resolution boost mode is enabled, see Figure 37 and Table 12 for details. If CRC reading is enabled, this requires additional SCLK pulses to propagate the CRC information, see the CRC section for more details.

As the $\overline{CS}$ signal initiates a conversion, as well as framing the data, any data access must be completed within a single frame.

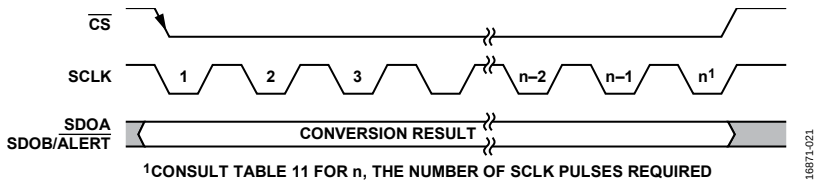


Figure 37. Reading Conversion Result

Table 12. Number of SCLKs, n, Required for Reading Conversion Results

Interface Configuration	Resolution Boost Mode	CRC Read	Number of SCLK Pulses	
			AD7380	AD7381
2-Wire	Disabled	Disabled	16	14
		Enabled	24	22
	Enabled	Disabled	18	16
		Enabled	26	24
1-Wire	Disabled	Disabled	32	28
		Enabled	40	36
	Enabled	Disabled	36	32
		Enabled	44	40

Serial 2-Wire Mode

Configure 2-wire mode by setting the SDO bit in the CONFIGURATION2 register to 0. In 2-wire mode, the conversion result for ADC A is output on the SDOA pin, and the conversion result for ADC B is output on the SDOB/$\overline{\text{ALERT}}$ pin (see Figure 38).

Serial 1-Wire Mode

In applications where slower throughput rates are allowed, or normal average oversampling is used, the serial interface can operate in 1-wire mode. In 1-wire mode, the conversion results from ADC A and ADC B are output on the serial output, SDOA. Additional SCLK cycles are required to propagate all data. The ADC A data is output first, followed by the ADC B conversion results (see Figure 39).

Resolution Boost Mode

The default resolution and output data size for the AD7380 is 16 bits and for the AD7381 is 14 bits. Enabling the on-chip oversampling function reduces noise and improves the device performance. To accommodate the performance boost achievable, enable an additional two bits of resolution in the conversion output data. If the RES bit in the CONFIGURATION1 register is set to Logic 1 and the AD7380/AD7381 are in a valid oversampling mode, the conversion result size for the AD7380 is 18 bit and for the AD7381 is 16 bit.

When the resolution boost mode is enabled, 18 SCLK cycles are required for the AD7380 and 16 SCLK cycles are required for the AD7381 to propagate the data.

LOW LATENCY READBACK

The interface on the AD7380/AD7381 has one cycle latency, as shown in Figure 40. For applications that operate at lower throughput rates, the latency of reading the conversion result can be reduced. When the conversion time elapses, $t_{CONVERT}$, a second $\overline{\text{CS}}$ pulse after the initial $\overline{\text{CS}}$ pulse that initiates the conversion can readback the conversion result. This operation is shown in Figure 40.

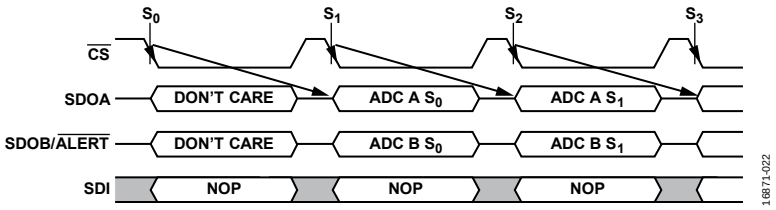


Figure 38. Reading Conversion Results for 2-Wire Mode

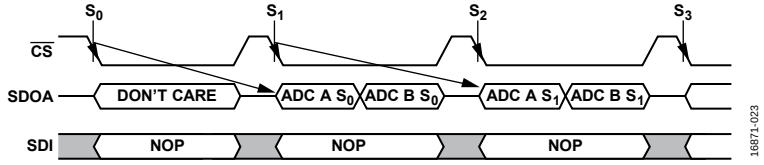


Figure 39. Read Conversion Results for 1-Wire Mode

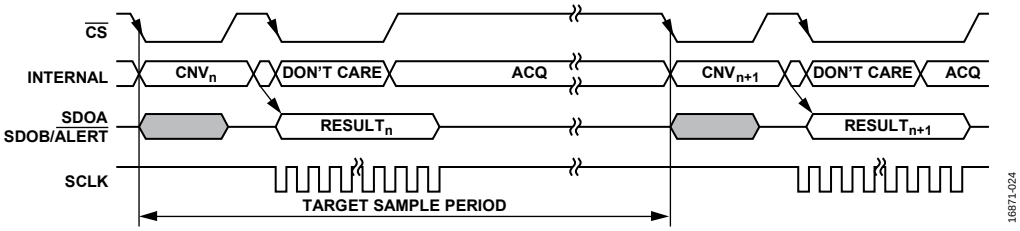


Figure 40. Low Throughput Low Latency

READING FROM DEVICE REGISTERS

All registers in the device can be read over the SPI. A register read is performed by issuing a register read command followed by an additional SPI command that can be either a valid command or no operation (NOP) command. The format for a read command is shown in Table 15. Bit D15 must be set to 0 to select a read command. Bits[D14:D12] contain the register address, and the subsequent twelve bits, Bits[D11:D0], are ignored.

WRITING TO DEVICE REGISTERS

All the read and write registers in the AD7380/AD7381 can be written to over the SPI. The length of an SPI write access is determined by the CRC write function. An SPI access is 16 bit if CRC write is disabled and is 24 bit when CRC write is enabled. The format for a write command is shown in Table 15. Bit D15 must be set to 1 to select a write command. Bits[D14:D12] contain the register address, and the subsequent twelve bits, Bits[D11:D0], contain the data to be written to the selected register.

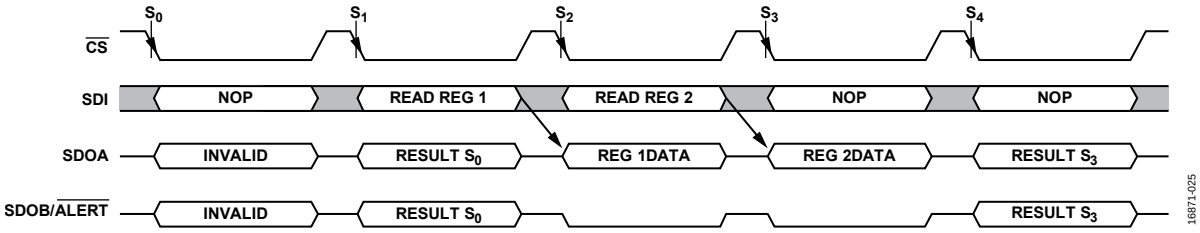


Figure 41. Register Read

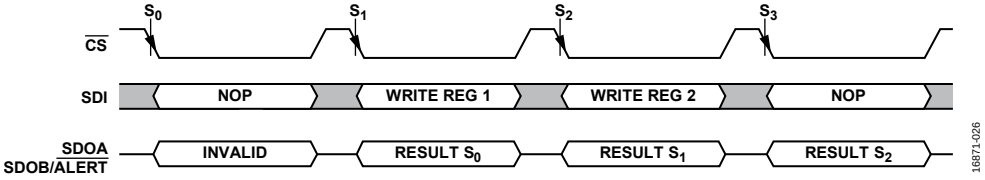


Figure 42. Register Write

CRC

The AD7380/AD7381 have CRC checksum modes that can be used to improve interface robustness by detecting errors in data transmissions. The CRC feature is independently selectable for SPI interface reads and SPI interface writes. For example, the CRC function for SPI writes can prevent unexpected changes to the device configuration but disabled on SPI reads, therefore maintaining a higher throughput rate. The CRC feature is controlled by the programming of the CRC_W and CRC_R bits in the CONFIGURATION1 register.

CRC Read

If enabled, a CRC is appended to the conversion result or register reads and consists of an 8-bit word. The CRC is calculated in the conversion result for ADC A and ADC B and is output on SDOA. A CRC is also calculated and appended to register read outputs.

The CRC read function can be used in 2-wire SPI mode, 1-wire SPI mode, and resolution boost mode.

CRC Write

To enable the CRC write function, the CRC_W bit in the CONFIGURATION1 register must be set to 1. To set the CRC_W bit to 1 to enable the CRC feature, the request frame must have a valid CRC appended to the frame.

After the CRC feature is enabled, all register write requests are ignored unless accompanied by a valid CRC command, requiring a valid CRC to both enable and disable the CRC write feature.

CRC Polynomial

For CRC checksum calculations, the following polynomial is always used: $x^8 + x^2 + x + 1$

To generate the checksum, the 16-bit data conversion result of the two channels are combined to produce 32-bit data. The 8 MSBs of the 32-bit data are inverted and then left shifted by eight bits to create a number ending in eight logic zeros. The polynomial is aligned such that the MSB is adjacent to the leftmost Logic 1 of the data. An exclusive or (XOR) function is applied to the data to produce a new, shorter number. The polynomial is again aligned such that the MSB is adjacent to the leftmost Logic 1 of the new result, and the procedure is repeated. This process repeats until the original data is reduced to a value less than the polynomial, which is the 8-bit checksum. The polynomial for this example is 100000111.

Let the original data of two channels be 0xAAAA and 0x5555, that is, 1010 1010 1010 1010 and 0101 0101 0101 0101. The data of the two channels is appended including eight zeros on the right, and then becomes 1010 1010 1010 1010 0101 0101 0101 0101 0000 0000.

Table 13 shows the CRC calculation of 16-bit two-channel data. In the final XOR operation, the reduced data is less than the polynomial. Therefore, the remainder is the CRC for the assumed data.

The same process is followed for the AD7381, but instead of dealing with 32-bit data (combined result of two channels), it is 28-bit data. For reading data such as the registers, CRC computation is based on a 16-bit register data, and the same process is performed as described for a 32-bit data.

Table 13. Example CRC Calculation for 2 16-Bit Data

Data	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**
Process Data	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
		1	0	0	0	0	0	1	1	1																														
				1 1	0 0	1 0	0 0	0 0	0 0	1 1	1 1	0 1																												
						1 1	0 0	0 0	0 0	0 0	0 0	1 1	1 1	0 1																										
														1 1	1 0	0 0	0 0	1 0	0 0	1 1	0 1	1 1																			
															1 1	0 0	0 0	1 0	0 0	0 0	1 1	0 1	0 1																		
																		1 1	0 0	0 0	0 0	1 0	1 0	1 1	0 1	1 1															
																						1 1	1 0	0 0	1 0	0 0	0 0	1 1	0 1	1 1											
																							1 1	0 0	1 0	0 0	0 0	0 0	1 1	0 1	0 1										
																									1 1	0 0	0 0	0 0	0 0	1 0	1 1	0 1	0 1								
																														1 1	0 0	0 0	1 0	0 0	0 0	1 1	0 1	1 1			
CRC																																	1	0	0	1	1	1	0	0

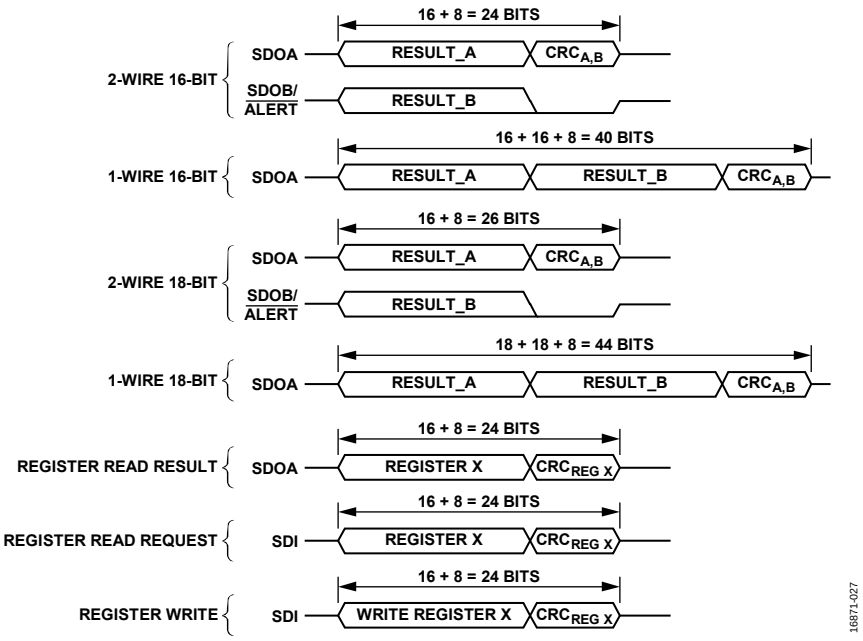


Figure 43. CRC Operation

REGISTERS

The AD7380/AD7381 have user programmable on-chip registers for configuring the device. Table 14 shows a complete overview of the registers available on the AD7380/AD7381. The registers are either read/write (R/W) or read only (R). Any read request to a write only register is ignored. Any write request to a read only register is ignored. Writes to any other register address are considered an NOP and are ignored. Any read request to a register address, other than those listed in Table 14, are considered an NOP, and the data transmitted in the next SPI frame are the conversion results.

Table 14. Register Summary

Hex. No.	Register Name	Bits	Bit 15 / Bit 7	Bit 14 / Bit 6	Bit 13 / Bit 5	Bit 12 / Bit 4	Bit 11 / Bit 3	Bit 10 / Bit 2	Bit 9 / Bit 1	Bit 8 / Bit 0	Reset	R/W
0x1	CONFIGURATION1	[15:8]	ADDRESSING				RESERVED		OS_MODE	OSR[2]	0x0000	R/W
		[7:0]	OSR[1:0]		CRC_W	CRC_R	ALERT_EN	RES	REFSEL	PMODE		
0x2	CONFIGURATION2	[15:8]	ADDRESSING				RESERVED			SDO	0x0000	R/W
		[7:0]	RESET									
0x3	$\overline{\text{ALERT}}$	[15:8]	ADDRESSING				RESERVED		CRCW_F	SETUP_F	0x0000	R
		[7:0]	RESERVED		AL_B_HIGH	AL_B_LOW	RESERVED		AL_A_HIGH	AL_A_LOW		
0x4	ALERT_LOW_THRESHOLD	[15:8]	ADDRESSING				ALERT_LOW[11:8]				0x0800	R/W
		[7:0]	ALERT_LOW[7:0]									
0x5	ALERT_HIGH_THRESHOLD	[15:8]	ADDRESSING				ALERT_HIGH[11:8]				0x07FF	R/W
		[7:0]	ALERT_HIGH[7:0]									

ADDRESSING REGISTERS

A serial register transfer on the AD7380/AD7381 consists of 16 SCLK cycles. The four MSBs written to the device are decoded to determine which register is addressed. The four MSBs consist of the register address (REGADDR), Bits[2:0], and the read/write bit (WR). The register address bits determine which on-chip register is selected. The read/write bit determines if the remaining 12 bits of data on the SDI input are loaded into the addressed register, if the addressed register is a valid write register. If the WR bit is 1, the bits load into the register addressed by the register select bits. If the WR bit is 0, the command is seen as a read request. The addressed register data is available to be read during the next read operation.

Table 15. Addressing Register Format

MSB LSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
WR	REGADDR[2:0]			DATA[11:0]											

Table 16. Bit Descriptions for Addressing Registers

Bit	Mnemonic	Description
D15	WR	If a 1 is written to this bit, Bits[D11:D0] of this register are written to the register specified by REGADDR, if it is a valid address. Alternatively, if a 0 is written, the next data sent out on the SDOA pin is a read from the designated register, if it is a valid address.
D14 to D12	REGADDR	When WR = 1, the contents of REGADDR determine the register for selection as outlined in Table 14. When WR = 0, and REGADDR contains a valid register address, the contents on the requested register are output on the SDOA pin during the next interface access. When WR = 0, and REGADDR contains 0x0, 0x6, or 0x7, the contents on the SDI line are ignored. The next interface access results in the conversion results being read back.
D11 to D0	DATA[11:0]	These bits are written into the corresponding register specified by the REGADDR bits when the WR bit is equal to 1 and the REGADDR bits contain a valid address.

CONFIGURATION1 REGISTER

Address: 0x1, Reset: 0x0000, Name: CONFIGURATION1

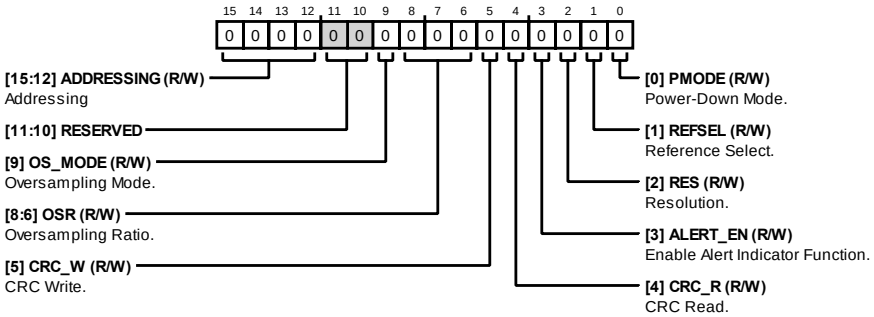


Table 17. Bit Descriptions for CONFIGURATION1

Bits	Bit Name	Description	Reset	Access
[15:12]	ADDRESSING	Addressing. Bits[15:12] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
[11:10]	RESERVED	Reserved.	0x0	R
9	OS_MODE	Oversampling Mode. Sets the oversampling mode of the ADC. 0: normal average. 1: rolling average.	0x0	R/W
[8:6]	OSR	Oversampling Ratio. Sets the oversampling ratio for all the ADCs in the relevant mode. Normal average mode supports oversampling ratios of ×2, ×4, ×8, ×16, and ×32. Rolling average mode supports oversampling ratios of ×2, ×4, and ×8. 000: disabled. 001: 2×. 010: 4×. 011: 8×. 100: 16×. 101: 32×. 110: disabled. 111: disabled.	0x0	R/W
5	CRC_W	CRC Write. Controls the CRC functionality for the SDI interface. When setting this bit from a 0 to a 1, the command must be followed by a valid CRC to set this configuration bit. If a valid CRC is not received, the entire frame is ignored. If the bit is set to 1, it requires a CRC to clear it to 0. 0: no CRC function. 1: CRC function.	0x0	R/W
4	CRC_R	CRC Read. Controls the CRC functionality for the SDOA and SDOB/$\overline{\text{ALERT}}$ interface. 0: no CRC function. 1: CRC function.	0x0	R/W
3	ALERT_EN	Enable Alert Indicator Function. This register functions when the SDO bit = 1. Otherwise, the ALERT_EN bit is ignored. 0: SDOB. 1: $\overline{\text{ALERT}}$.	0x0	R/W
2	RES	Resolution. Sets the size of the conversion result data. If OSR = 0, these bits are ignored, and the resolution is set to default resolution. 0: normal resolution. 1: 2-bit higher resolution.	0x0	R/W
1	REFSEL	Reference Select. Selects the ADC reference source. 0: selects internal reference. 1: selects external reference.	0x0	R/W
0	PMODE	Power-Down Mode. Sets the power modes. 0: normal mode. 1: power-down mode.	0x0	R/W

CONFIGURATION2 REGISTER

Address: 0x2, Reset: 0x0000, Name: CONFIGURATION2

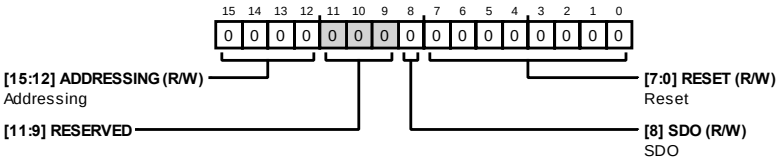


Table 18. Bit Descriptions for CONFIGURATION2

Bits	Bit Name	Description	Reset	Access
[15:12]	ADDRESSING	Addressing. Bits[15:12] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
[11:9]	RESERVED	Reserved.	0x0	R
8	SDO	SDO. Conversion results serial data output. 0: 2-wire, conversion data are output on both the SDOA and SDOB/$\overline{\text{ALERT}}$ pins. 1: 1-wire, conversion data are output on the SDOA pin only.	0x0	R/W
[7:0]	RESET	Reset. Set to 0x3C to perform a soft reset, which refreshes some block and register contents remain unchanged. Clears $\overline{\text{ALERT}}$ register and flushes any oversampling stored variables or active state machine. Set to 0xFF to perform a hard reset, which resets all possible blocks in the device. Register contents are set to defaults. All other values are ignored.	0x0	R/W

$\overline{\text{ALERT}}$ REGISTER

Address: 0x3, Reset: 0x0000, Name: $\overline{\text{ALERT}}$

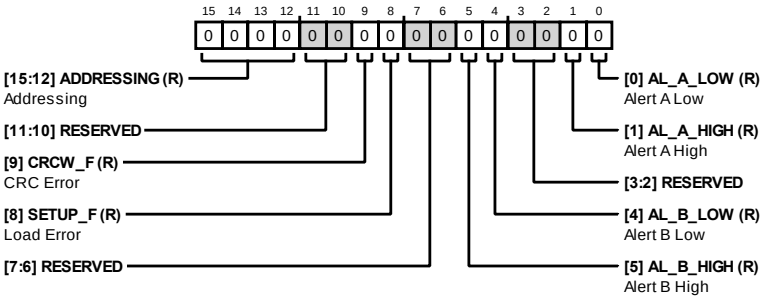


Table 19. Bit Descriptions for $\overline{\text{ALERT}}$

Bits	Bit Name	Description	Reset	Access
[15:12]	ADDRESSING	Addressing. Bits[15:12] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R
[11:10]	RESERVED	Reserved.	0x0	R
9	CRCW_F	CRC Error. Indicates that a register write command failed due to a CRC error. This fault bit is sticky and remains set until the register is read. 0: no CRC error. 1: CRC error.	0x0	R
8	SETUP_F	Load Error. The SETUP_F bit indicates that the device configuration data did not load correctly on startup. This bit does not clear on an $\overline{\text{ALERT}}$ register read. A hard reset via the CONFIGURATION2 register is required to clear this bit and restart the device setup again. 0: no setup error. 1: setup error.	0x0	R
[7:6]	RESERVED	Reserved.	0x0	R

Bits	Bit Name	Description	Reset	Access
5	AL_B_HIGH	Alert B High. The alert indication high bits indicate if a conversion result for the respective input channel exceeds the value set in the ALERT_HIGH_THRESHOLD register. This fault bit is sticky and remains set until the register is read. 0: no alert indication. 1: alert indication.	0x0	R
4	AL_B_LOW	Alert B Low. The alert indication low bits indicate if a conversion result for the respective input channel exceeds the value set in the ALERT_LOW_THRESHOLD register. This fault bit is sticky and remains set until the register is read. 0: no alert indication. 1: alert indication.	0x0	R
[3:2]	RESERVED	Reserved.	0x0	R
1	AL_A_HIGH	Alert A High. The alert indication high bits indicate if a conversion result for the respective input channel exceeds the value set in the ALERT_HIGH_THRESHOLD register. This fault bit is sticky and remains set until the register is read. 0: no alert indication. 1: alert indication.	0x0	R
0	AL_A_LOW	Alert A Low. The alert indication low bits indicate if a conversion result for the respective input channel exceeds the value set in the ALERT_LOW_THRESHOLD register. This fault bit is sticky and remains set until the register is read. 0: no alert indication. 1: alert indication.	0x0	R

ALERT_LOW_THRESHOLD REGISTER

Address: 0x4, Reset: 0x0800, Name: ALERT_LOW_THRESHOLD

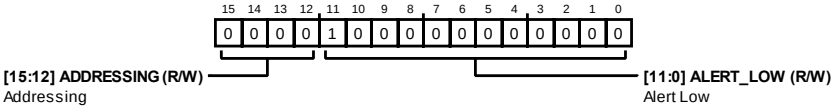


Table 20. Bit Descriptions for ALERT_LOW_THRESHOLD

Bits	Bit Name	Description	Reset	Access
[15:12]	ADDRESSING	Addressing. Bits[15:12] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
[11:0]	ALERT_LOW	Alert Low. Data Bits[D11:D0] are the MSBs of the 16-bit internal alert low register. The remaining 4 bits are fixed at 0x0, which sets an alert when the conversion result is below the ALERT_LOW_THRESHOLD and disables when the conversion result is above the ALERT_LOW_THRESHOLD.	0x800	R/W

ALERT_HIGH_THRESHOLD REGISTER

Address: 0x5, Reset: 0x07FF, Name: ALERT_HIGH_THRESHOLD

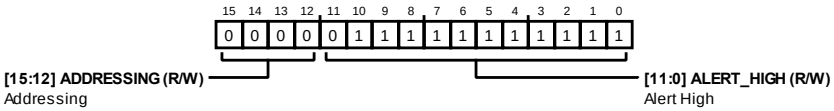


Table 21. Bit Descriptions for ALERT_HIGH_THRESHOLD

Bits	Bit Name	Description	Reset	Access
[15:12]	ADDRESSING	Addressing. Bits[15:12] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
[11:0]	ALERT_HIGH	Alert High. Data Bits[D11:D0] are the MSBs of the 16-bit internal ALERT_HIGH register. The remaining bits are fixed at 0xF, which sets an alert when the converter result is above the ALERT_HIGH_THRESHOLD and disables when the converter result is below the ALERT_HIGH_THRESHOLD.	0x7FF	R/W

OUTLINE DIMENSIONS

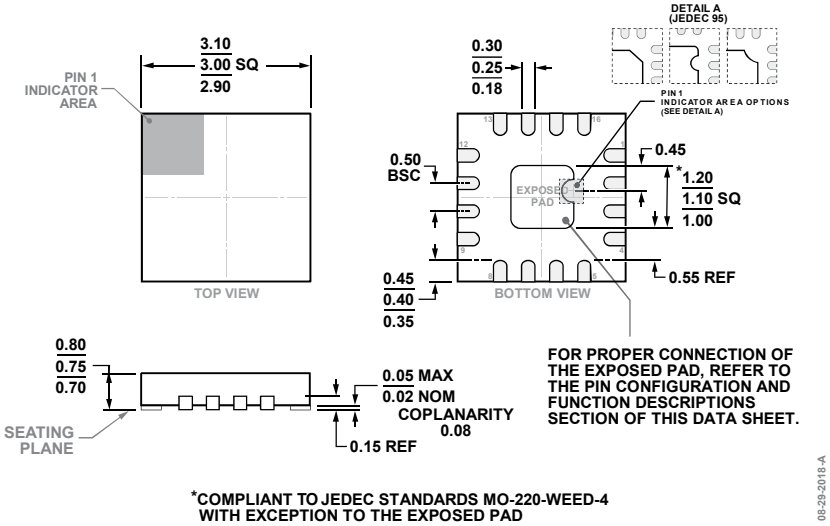


Figure 44. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-16-45)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Resolution (Bit)	Temperature Range	Package Description	Package Option	Marking Code
AD7380BCPZ-RL	16	−40°C to +125°C	16-Lead LFCSP	CP-16-45	C95
AD7380BCPZ-RL7	16	−40°C to +125°C	16-Lead LFCSP	CP-16-45	C95
AD7380BCPZ-R2	16	−40°C to +125°C	16-Lead LFCSP	CP-16-45	C95
AD7381BCPZ-RL	14	−40°C to +125°C	16-Lead LFCSP	CP-16-45	C93
AD7381BCPZ-RL7	14	−40°C to +125°C	16-Lead LFCSP	CP-16-45	C93
EVAL-AD7380FMCZ			AD7380 Evaluation Board		
EVAL-AD7381FMCZ			AD7381 Evaluation Board		

[1] Z = RoHS Compliant Part.
[2] The EVAL-AD7380FMCZ and the EVAL-AD7381FMCZ are compatible with the EVAL-SDP-CH1Z high speed controller board.

©2019 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
D16871-0-11/19(A)