

MC74HCT74A

Dual D Flip-Flop with Set and Reset with LSTTL Compatible Inputs

High-Performance Silicon-Gate CMOS

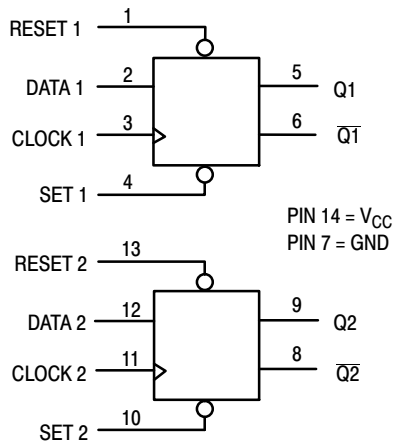
The MC74HCT74A is identical in pinout to the LS74. This device may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

This device consists of two D flip-flops with individual Set, Reset, and Clock inputs. Information at a D-input is transferred to the corresponding Q output on the next positive going edge of the clock input. Both Q and \bar{Q} outputs are available from each flip-flop. The Set and Reset inputs are asynchronous.

Features

- Output Drive Capability: 10 LSTTL Loads
- TTL NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μ A
- In Compliance With the JEDEC Standard No. 7.0 A Requirements
- Chip Complexity: 136 FETs or 34 Equivalent Gates
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

LOGIC DIAGRAM



Design Criteria	Value	Units
Internal Gate Count†	34	ea.
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	μ W
Speed Power Product	.0075	pJ

†Equivalent to a two-input NAND gate.



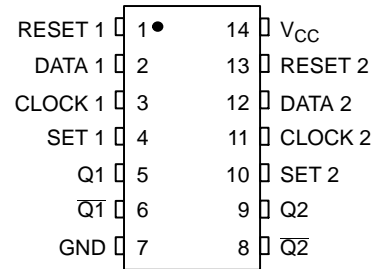
ON Semiconductor®

<http://onsemi.com>

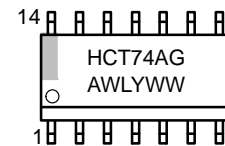


SOIC-14 NB
D SUFFIX
CASE 751A

PIN ASSIGNMENT



MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
Y, YY = Year
WW = Work Week
G = Pb-Free Package

FUNCTION TABLE

Inputs				Outputs	
Set	Reset	Clock	Data	Q	\bar{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	\nearrow	H	H	L
H	H	\nearrow	L	L	H
H	H	L	X	No Change	No Change
H	H	H	X	No Change	No Change
H	H	\searrow	X	No Change	No Change

*Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

MC74HCT74A

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air SOIC Package†	500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating: SOIC Package: -7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				-55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	4.5	2.0	2.0	2.0	V
			5.5	2.0	2.0	2.0	
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	4.5	0.8	0.8	0.8	V
			5.5	0.8	0.8	0.8	
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	4.5	4.4	4.4	4.4	V
			5.5	5.4	5.4	5.4	
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$	4.5	3.98	3.84	3.7	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	4.5	0.1	0.1	0.1	V
			5.5	0.1	0.1	0.1	
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$	4.5	0.26	0.33	0.4	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or } GND$	5.5	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or } GND$ $I_{out} = 0 \mu\text{A}$	5.5	2.0	20	80	μA
ΔI_{CC}	Additional Quiescent Supply Current	$V_{in} = 2.4 \text{ V, Any One Input}$ $V_{in} = V_{CC} \text{ or } GND, \text{ Other Inputs}$ $I_{out} = 0 \mu\text{A}$	5.5	≥ -55°C	25°C to 125°C		mA
				2.9	2.4		

MC74HCT74A

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0\text{ V} \pm 10\%$, $C_L = 50\text{ pF}$, Input $t_r = t_f = 6.0\text{ ns}$)

Symbol	Parameter	Guaranteed Limit			Unit
		-55 to 25°C	≤ 85°C	≤ 125°C	
f_{\max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	30	24	20	MHz
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Clock to Q or \bar{Q} (Figures 1 and 4)	24	30	36	ns
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Set or Reset to Q or \bar{Q} (Figures 2 and 4)	24	30	36	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	15	19	22	ns
C_{in}	Maximum Input Capacitance	10	10	10	pF

Symbol	Parameter	Typical @ 25°C, $V_{CC} = 5.0\text{ V}$		Unit
		32		
C_{PD}	Power Dissipation Capacitance (Per Enabled Output)*	32		pF

1. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

TIMING REQUIREMENTS ($V_{CC} = 5.0\text{ V} \pm 10\%$, $C_L = 50\text{ pF}$, Input $t_r = t_f = 6.0\text{ ns}$)

Symbol	Parameter	Fig.	Guaranteed Limit						Units
			-55 to 25°C		≤ 85°C		≤ 125°C		
			Min	Max	Min	Max	Min	Max	
t_{su}	Minimum Setup Time, Data to Clock	3	15		19		22		ns
t_h	Minimum Hold Time, Clock to Data	3	3		3		3		ns
t_{rec}	Minimum Recovery Time, Set or Reset Inactive to Clock	2	6		8		9		ns
t_w	Minimum Pulse Width, Clock	1	15		19		22		ns
t_w	Minimum Pulse Width, Set or Reset	2	15		19		22		ns
t_r , t_f	Maximum Input Rise and Fall Times	1		500		500		500	ns

ORDERING INFORMATION

Device	Package	Shipping†
MC74HCT74ADG	SOIC-14 NB (Pb-Free)	55 Units / Rail
MC74HCT74ADR2G	SOIC-14 NB (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MC74HCT74A

SWITCHING WAVEFORMS

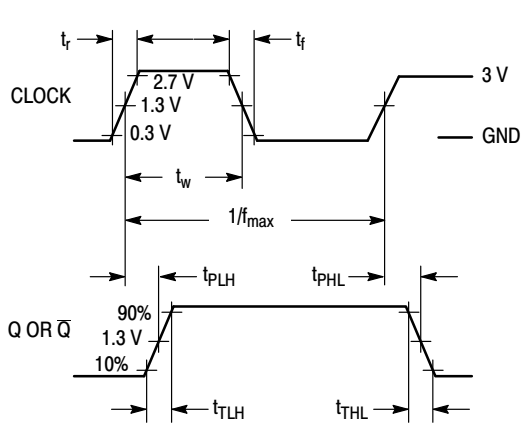


Figure 1.

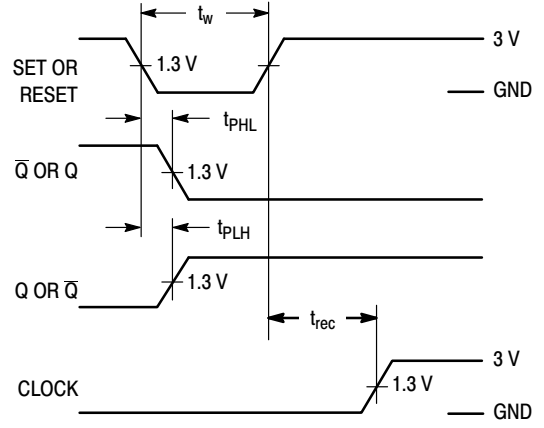


Figure 2.

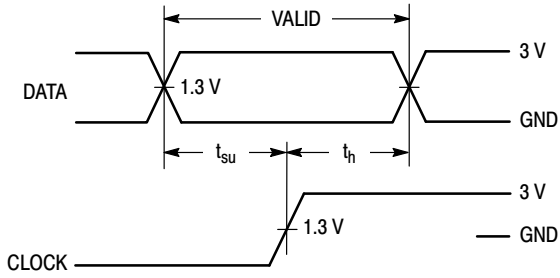
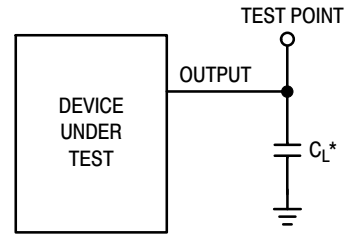


Figure 3.



*Includes all probe and jig capacitance

Figure 5.

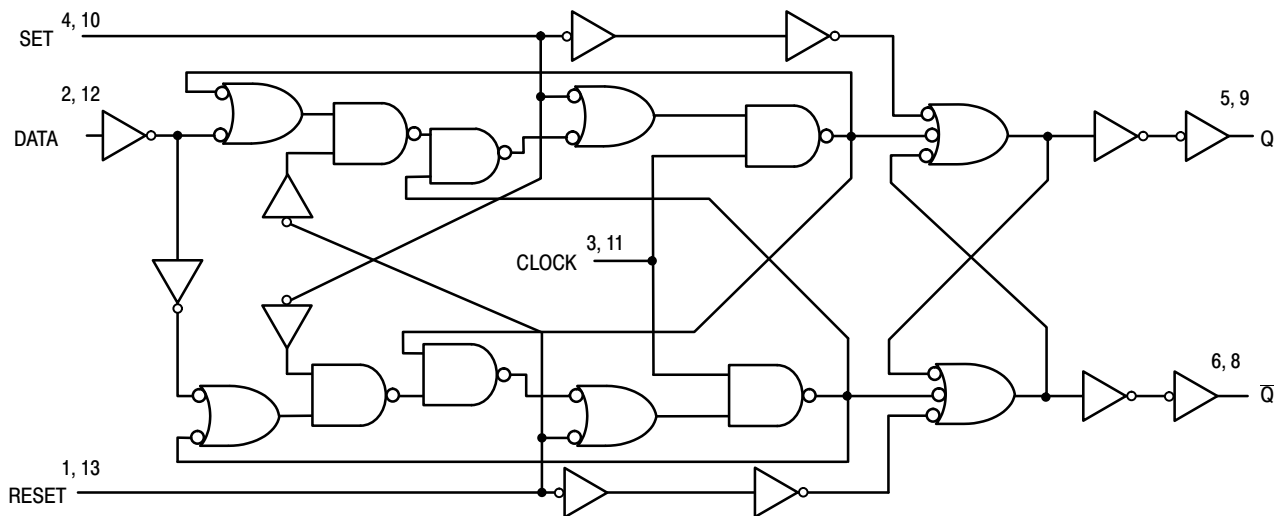
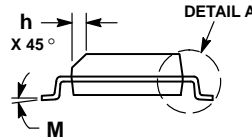
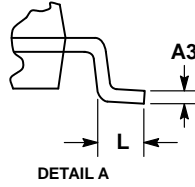
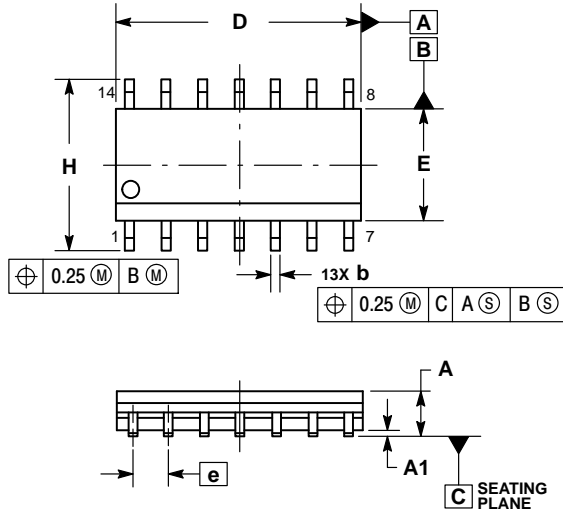


Figure 4. Expanded Logic Diagram

MC74HCT74A

PACKAGE DIMENSIONS

SOIC-14 NB
CASE 751A-03
ISSUE K

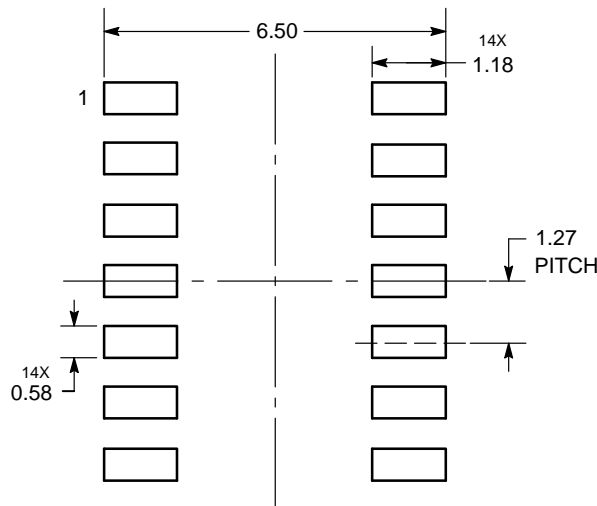


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and the are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local Sales Representative