TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

TB62785NG, TB62785FTG

7-SEGMENT DRIVERS WITH BUILT-IN DECODERS (COMMON ANODE CAPABILITY, MAXIMUM 4-DIGIT CONTROL)

The TB62785NG / TB62785FTG are multifunctional, compact, 7-egment LED display drivers.

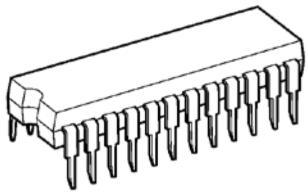
These ICs can directly drive 7-segment displays and individual LEDs, and can control either a 4-digit display with decimal points, or 32 individual LEDs.

These ICs can also be used with common-anode displays. Their outputs are constant current, the ampere levels at which are set using an external resistor.

A synchronous serial port connects the IC to the CPU.

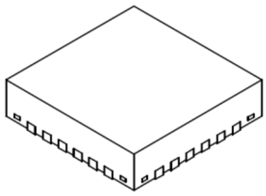
The different modes of control provided by this device including Duty Control Register Set, Digit Set, Decode Set and Standby Set, are all based on every 16-bit of serial data.

TB62785NG



SDIP24-P-300-1.78
Weight 1.22g (typ.)

TB62785FTG



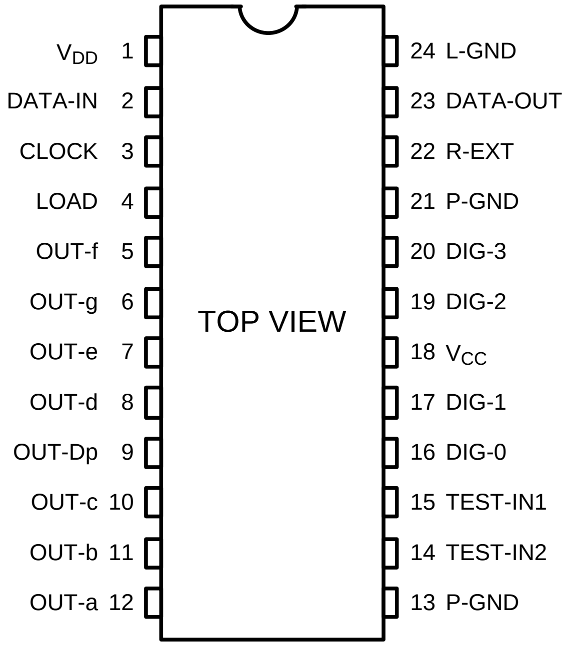
P-VQFN24-0404-0.50-001
Weight 0.037g (typ.)

FEATURES

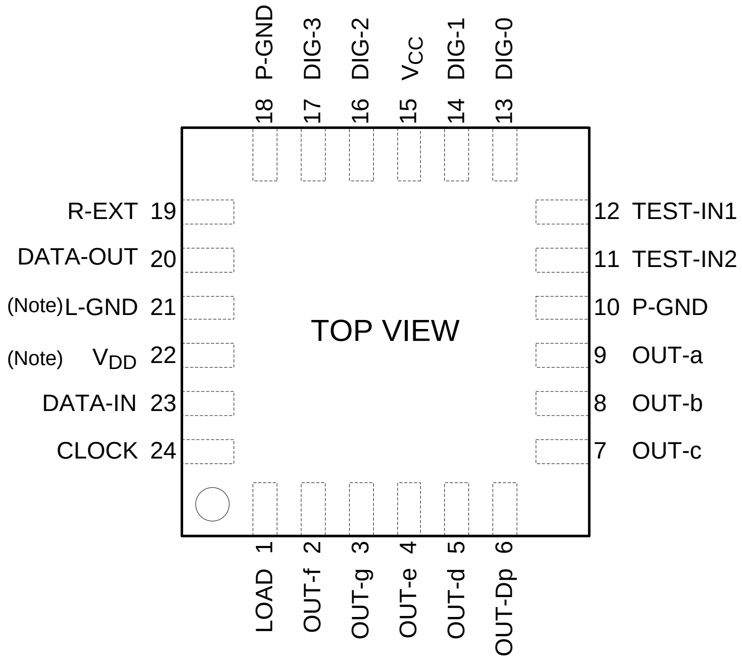
- Control circuit power supply
  : V_{DD} = 4.5 to 5.5 V
- Digit output rating
  : 17 V / -400 mA
- Decoder output rating
  : 17 V / 50 mA
- Built-in decoder
  : Decodes the numerals 0 to 9, certain alphabetic characters, and of course blanks code.
- Digit control function
  : Can scan digit outputs DIG-0 to DIG-3 when connected to the common anode pins of a 7-segment display.
- Maximum transmission frequency
  : f_{CLK} = 15 MHz
- Decoder outputs (OUT-a to OUT-Dp)
  Output current can be set up to a 40mA maximum using an external resistor.
- Constant current tolerance (Ta = 25°C, V_{DD} = 5.0 V)
  : Variation between bits = ±7%, variation between devices (including variation between bits) = ±15% at V_{CE} ≥ 0.7 V
- Package
  : TB62785NG SDIP24-P-300-1.78
  : TB62785FTG P-VQFN24-0404-0.50-001

PIN ASSIGNMENT (Top view)

< TB62785NG (SDIP24) >

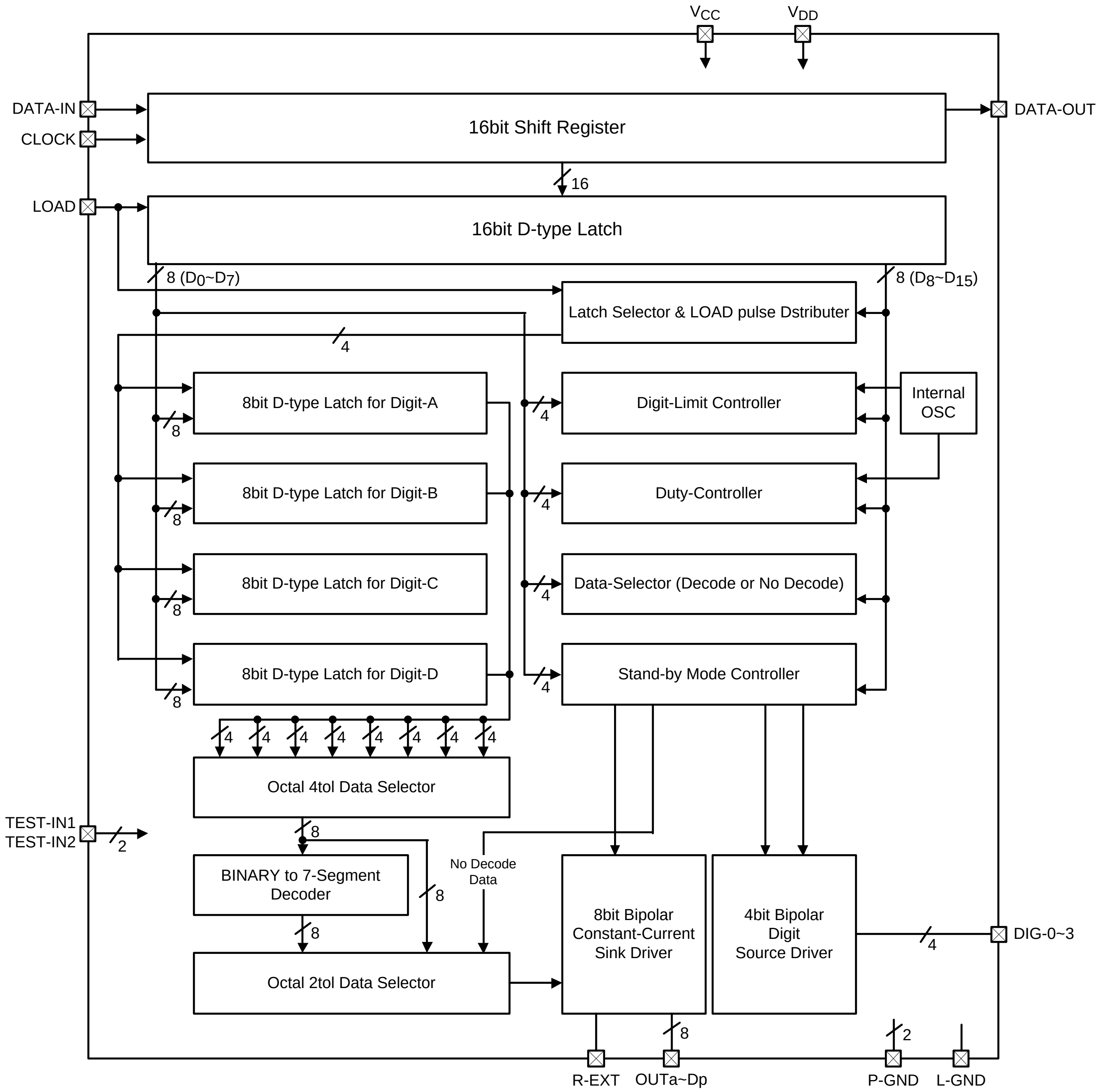


< TB62785FTG (VQFN24) >



*Note**:** VDD and L-GND are adjacent in TB62785FTG. (21pin / 22pin)
Please be careful.

BLOCK DIAGRAM



PIN FUNCTIONS

TB62785NG (SDIP24)

PIN NUMBER	I/O (Note)	PIN NAME	FUNCTION
1	P	V_{DD}	5 V power pin.
2	I	DATA-IN (DI)	Serial data input pin.
3	I	CLOCK (CK)	Clock input pin. The shift register shifts data on the clock's rising edge.
4	I	LOAD (LD)	Load signal input pin. The data in the D_8 to D_{15} are read on the rising edge and the load register is selected. And, the data of the D_0 to D_7 which corresponded each register on the falling edge.
5 to 12	O	OUT-a to OUT-Dp	Segment drive output pins. The a to Dp outputs correspond to the seven segments. These pins output constant sink current. Connect each of these pins to the corresponding LED's cathode.
13, 21	P	P-GND	Ground pins, There are two which can be used to ground the output OUT-a to OUT-Dp pins.
14	I	TEST-IN2	Product test pin. In normal use, be sure to connect to ground.
15	I	TEST-IN1	Product test pin. In normal use, be sure to connect to ground.
16, 17, 19, 20	O	DIG-0 to DIG-3	Digit output pins. Each of these pins can control one of the four seven-segment digits in a display. These pins output the V_{CC} pin voltage as a source current output. Connect these pins to the LED anodes.
18	P	V_{CC}	Power pin for digit output.
22	O	R-EXT	Current setting pin for the OUT-a to OUT-Dp pins. Connect a resistor between this pin and ground when setting the current.
23	O	DATA-OUT (DO)	Serial data output pin. Use when TB62785NG/ TB62785FTG device is used in cascade connections.
24	P	L-GND	Ground pin for logic and analog circuits.

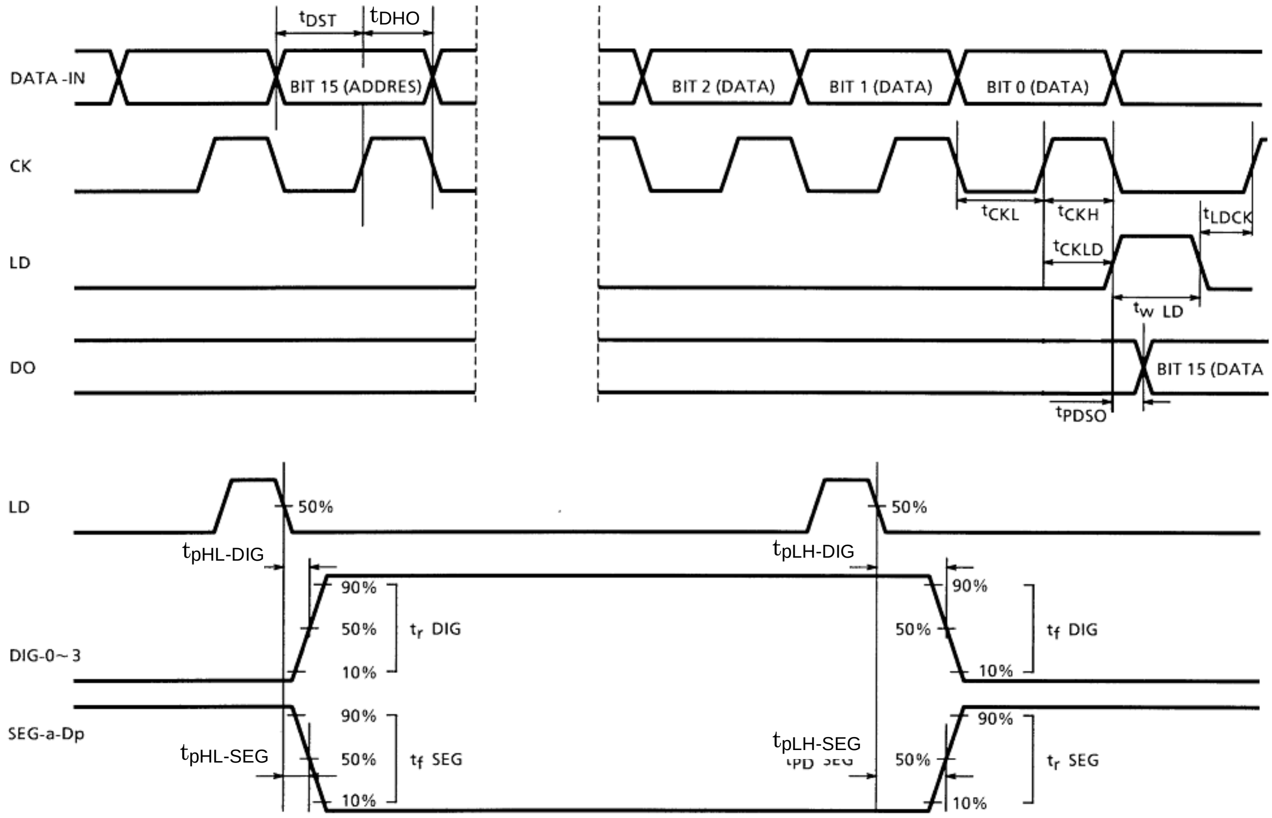
*Note Explanation of I/O**:** I = Input Terminal, O = Output Terminal, P = Power Supply

TB62785FTG (VQFN24)

PIN NUMBER	I/O (Note)	PIN NAME	FUNCTION
1	I	LOAD (LD)	Load signal input pin. The data in the D_8 to D_{15} are read on the rising edge and the load register is selected. And, the data of the D_0 to D_7 which corresponded each register on the falling edge.
2 to 9	O	OUT-a to D_p	Segment drive output pins. The A to Dp outputs correspond to the seven segments. These pins output constant sink current. Connect each of these pins to the corresponding LED's cathode.
10, 18	P	P-GND	Ground pins, There are two which can be used to ground the output OUT-a to OUT-Dp pins.
11	I	TEST-IN2	Product test pin. In normal use, be sure to connect to ground.
12	I	TEST-IN1	Product test pin. In normal use, be sure to connect to ground.
13, 14, 16, 17	O	DIG-0 to DIG-3	Digit output pins. Each of these pins can control one of the four seven-segment digits in a display. These pins output the V_{CC} pin voltage as a source current output. Connect these pins to the LED anodes.
15	P	V_{CC}	Power pin for digit output.
19	O	R-EXT	Current setting pin for the OUT-a to OUT-Dp pins. Connect a resistor between this pin and ground when setting the current.
20	O	DATA-OUT (DO)	Serial data output pin. Use when TB62785NG/TB62785FTG device is used in cascade connections.
21	P	L-GND	Ground pin for logic and analog circuits.
22	P	V_{DD}	5 V power pin.
23	I	DATA-IN (DI)	Serial data input pin.
24	I	CLOCK (CK)	Clock input pin. The shift register shifts data on the clock's rising edge.

*Note Explanation of I/O**:** I = Input Terminal, O = Output Terminal, P = Power Supply

TIMING DIAGRAM



DATA INPUT

- Transfer data to the DATA-IN pin on every 16-bit combining address (8bits) and data (8bits). After the 16th clock signal input following this data transfer input a load signal from the LD pin.
- Input the load signal using an Active High pulse. The register address is set on the rising edge of the load pulse. On the subsequent falling edge, the data are read as data of the mode of the register.

DESCRIPTION OF OPERATION

- Data input (DATA-IN, CLOCK, LOAD)

The data are input serially using the DATA-IN pin. The data input interface consists of a total of three inputs: DATA-IN, LOAD, and CLOCK.
Binary code stored in the 16-bit shift register offers control modes including duty Control Register Set, Digitset, Decode Set, and Standby Set,
The data are shifted on the rising edge of the clock, starting from the MSB. Cascade-connecting TB62785NG/TB62785FTG devices provides capability for controlling a larger number of digits.
The serial data in the 16-bit shift register are used as follows: the four bits D_{15} (MSB) to D_{12} select the IC operating mode (Table 1), while D_{11} to D_8 select the register corresponding to the operating mode (Table 2).
Bits D_7 to D_0 (LSB) of the 16-bit shift register are used for detail settings, such as number of digits in use, character settings in each digit, and light intensity.
The internal registers are loaded on the rising edge of the LOAD signal, which causes loading of data from an external source into the D_{15} (MSB) to D_8 bits of the shift register, operating mode and the corresponding register selection data. On the subsequent falling edge, the detail setting data of D_7 to D_0 (LSB) are loaded.
Normally LOAD is Low. After a serial transfer of 16bits, the input of a High-level pulse loads the data.
Note the following caution: Use the D_{15} to D_8 setting and the D_7 to D_0 detail data setting as a pair. If only the D_7 to D_0 data are input without setting D_{15} to D_8 an error condition may result, in which the device will not operate normally. If the current mode is set again by a new signal, the data for D_{15} to D_8 must also be re-input.

- Operating precautions

At power-on or after operation in Clear mode (in initial state), set the IC to Normal mode again. Otherwise, the IC will not drive the LED.
Operating the IC in Blank mode (all lights off) or in All On mode (all lights lit) does not affect the internal data. Setting the IC to Normal mode again continues the LED lighting in the state governed by the settings made immediately before mode change.
Normal mode (not Shut Down, Clear, Blank, or All On mode) continues the operations set in Load Register mode. In Normal mode, operations are governed by any new settings made in the Load Register, as soon as the changed setting values are loaded.

- Operating modes (Table 1.)

These ICs support the following five operating modes:

1. Blank : Forcibly turns OFF the constant-current output both for data and for digit setting. This mode is not affected by the values in bits D_{11} to D_0.

2. Normal Operate : Used for display operations after the settings of the digits are complete. This mode is not affected by the values in bits D_{11} to D_0.Note that setting this mode without making any other settings will cause display of the numeral 0.

3. Load Register : Used for the detail settings of the Duty Control Register, for setting Decode / No Decode, for inputting display data, and for setting the number of digits to drive. D_{11} to D_0 of the shift register are used for the detail settings of the digits currently being driven (Table 2).

4. All On : Forcibly turns ON the data-side constant-current output. This mode is not affected by D_{11} to D_0.
The initial setting is four digits. When the digits must be changed, use Load Register mode to set the number of digits to drive.

5. Standby : Used to set Standby state (in which internal data are not cleared) and to clear data (initialization). The settings in D_3 to D_0 of the shift register determine the choice between standby state or initialization.

Table 1 Operating mode settings

	REGISTER DATA								INITIAL SETTING
	D_{15}	D_{14}	D_{13}	D_{12}	D_{11} to D_8	D_7 to D_4	D_3 to D_0	HEX CODE	
BLANK (OUT-n & DIG-0 to 3 ALL-OFF)	0	0	0	0	-	-	-	0---H	*
NORMAL (OPERATION)	0	0	0	1	-	-	-	1---H	-
LOAD REGISTER (DUTY, DECODE, DIGIT & DATA)	0	0	1	0	X	X	X	2XXXH	-
ALL ON (OUTn ALL-ON)	0	0	1	1	-	-	-	3---H	-
STAND-BY	0	1	0	0	-	-	X	4--XH	-

X = Input H or L. "-" = Are not affected by the truth table.

- Load Register Selection modes (Table 2)

These modes select the register to provide the data to control the IC operation. The Load Register selection mode is determined by the settings of D_{15} to D_{12} and D_{11} to D_8 of the shift register.

1. Duty Register : The data in D_7 to D_0 of this register set the digit output duty cycle.
Duty settings can be made in 16 steps from 0 / 16 to 15 / 16.
(See Table 3)

2. Decode & Digit Register : Sets Decode / No Decode and the number of digits to drive. Decode can be set using D_7 to D_4.
The number of digits driven can be set using D_3 to D_0. Decode / No Decode and the number of digits driven are set simultaneously.

3. Data registers 0 to 3 : Set the display data corresponding to DIG0 to DIG3 respectively.
D_7 to D_0 of the shift register are used to set the display data.

Table 2 Load register selection

	REGISTER DATA							
	D_{15} to D_{12}	D_{11}	D_{10}	D_9	D_8	D_7 to D_4	D_3 to D_0	HEX CODE
LOAD DUTY REGISTER	2H	0	0	0	0	X	X	20XXH
LOAD DECODE & DIGIT REGISTER	2H	0	0	0	1	X	X	21XXH
LOAD DATA REGISTER 0	2H	0	0	1	0	X	X	22XXH
LOAD DATA REGISTER 1	2H	0	0	1	1	X	X	23XXH
LOAD DATA REGISTER 2	2H	0	1	0	0	X	X	24XXH
LOAD DATA REGISTER 3	2H	0	1	0	1	X	X	25XXH

X = Input H or L. "-" = Are not affected by the truth table.

DUTY CONTROL REGISTER SETTINGS

- Duty Control Register detail settings and operation (Table 3)

Writing 20H to D_{15} to D_8 and writing 0 to FH to D_3 to D_0 sets the duty cycle shown in the following table for the digit-side source driver output. The duty cycle can be set in 16 steps.
The initial setting is 15 / 16. After Data Clear, the setting is also 15 / 16.
The current settings continue until changed (by reset execution, or to the initial state, Data Clear state, or standby state).

Table 3 Duty control register settings

DUTY CYCLE	REGISTER DATA							INITIAL SETTING
	D_{15} to D_8	D_7 to D_4	D_3	D_2	D_1	D_0	HEX CODE	
0 / 16	20H	-	0	0	0	0	20X0H	-
1 / 16	20H	-	0	0	0	1	20X1H	-
2 / 16	20H	-	0	0	1	0	20X2H	-
3 / 16	20H	-	0	0	1	1	20X3H	-
4 / 16	20H	-	0	1	0	0	20X4H	-
5 / 16	20H	-	0	1	0	1	20X5H	-
6 / 16	20H	-	0	1	1	0	20X6H	-
7 / 16	20H	-	0	1	1	1	20X7H	-
8 / 16	20H	-	1	0	0	0	20X8H	-
9 / 16	20H	-	1	0	0	1	20X9H	-
10 / 16	20H	-	1	0	1	0	20XAH	-
11 / 16	20H	-	1	0	1	1	20XBH	-
12 / 16	20H	-	1	1	0	0	20XCH	-
13 / 16	20H	-	1	1	0	1	20XDH	-
14 / 16	20H	-	1	1	1	0	20XEH	-
15 / 16	20H	-	1	1	1	1	20XFH	*

X = Input H or L. "-" = Are not affected by the truth table.

DIGIT SETTINGS

- Setting the number of digits (Table 4)

Writing 21H to D_{15} to D_8 and at the same step writing 0H to 3H to D_3 to D_0 sets the number of digits to a maximum of four the display. The initial setting is four digits, and four will also be set by a Data Clear.
The current settings continue until changed (by reset execution, or to the initial state, Data Clear state, or standby state).
When changing the number of digits, also set D_7 to D_4.

Table 4 Digit settings

	REGISTER DATA							INITIAL SETTING
	D_{15} to D_8	D_7 to D_4	D_3	D_2	D_1	D_0	HEX CODE	
ACTIVATED DIG--0 ONLY	21H	X	0	0	0	0	21X0H	-
ACTIVATED DIG--0 to 1	21H	X	0	0	0	1	21X1H	-
ACTIVATED DIG--0 to 2	21H	X	0	0	1	0	21X2H	-
ACTIVATED DIG--0 to 3	21H	X	0	0	1	1	21X3H	*

X = Input H or L. "-" = Are not affected by the truth table.

DECODE SETTINGS

- Decode settings (Table 5)

The settings for Decode are the same as the settings for the number of digits, described under setting, above.
Writing 21H to D_{15} to D_8 and writing 0 to 1H to D_7 to D_4 set Decode mode.
When using this IC for controlling the lighting on individual LEDs used for a dot matrix rather than a 7-segment display, set to No Decode.
As Table 6 shows, D_0 in the data register is used to turn OUT-a ON and OFF ; D_1 turns OUT-b ON and OFF.
The initial setting is Decode mode, and Decode mode will also be set by a Data Clear.
The current settings continue until changed (by reset execution, or to the initial state, Data Clear state, or standby state).
Since D_3 to D_0 are also used for setting the number of digits, when changing the Decode setting, also set D_3 to D_0.

Table 5 Decode settings

	REGISTER DATA							INITIAL SETTING
	D_{15} to D_8	D_7	D_6	D_5	D_4	D_3 to D_0	HEX CODE	
PASS DECODER (NO DECODE)	21H	0	0	0	0	X	210XH	-
DECODE	21H	0	0	0	1	X	211XH	*

X = Input H or L. "-" = Are not affected by the truth table.

THE FOLLOWING TABLE SHOWS THE CORRESPONDENCE BETWEEN THE SERIAL DATA AND THE OUTPUT PINS WHEN NO DECODE IS SET

Table 6 Correspondence between serial data and output pins in no decode mode

REGISTER DATA	OUTPUT	INITIAL STATE	NOTE
D_0	OUT-a	L	Output is ON when data = H and OFF when data = L.
D_1	OUT-b	L	
D_2	OUT-c	L	
D_3	OUT-d	L	
D_4	OUT-e	L	
D_5	OUT-f	L	
D_6	OUT-g	L	
D_7	OUT-Dp	L	

STANDBY SETTINGS

- Standby mode settings and operation (Table 7)

Writing 4H to D_{15} to D_{12} and writing 0H to D_3 to D_0 sets Standby mode. Writing 4H to D_{15} to D_{12} and writing 1H to D_3 to D_0 sets All Data Clear mode.
Standby mode maintains the settings made immediately before this mode came in force, turns the output current OFF, and controls the bias current flowing in the internal circuits. All Data Clear resets all settings to their initial states.

Table 7 Standby settings

	REGISTER DATA						
	D_{15} to D_8	D_7 to D_4	D_3	D_2	D_1	D_0	HEX CODE
STANDBY (NO DATA CLEAR)	4-H	-	0	0	0	0	4XX0H
ALL DATA CLEAR	4-H	-	0	0	0	1	4XX1H

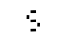
X = Input H or L. "-" Are not affected by the truth table.

LIST OF CHARACTER GENERATOR DECODING DATA

- Character generator decoding (Table 8)

  As the following table shows, the characters are decoded using combinations of the data in D_0 to D_3 and D_5 to D_4.
  In decoding, D_6 is used exclusively for setting decimal points.
  Spaces where (D_0, D_1, D_2, D_3) = (0000) and (D_5, D_4) = (01) are regarded as blank.

Table 8 List of character generator decoding data

		D_0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
		D_1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
		D_2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
		D_3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
D_5	D_4	HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	0																
0	1	1																

D_7	D_6	
X	0	Dp OFF
X	1	Dp ON

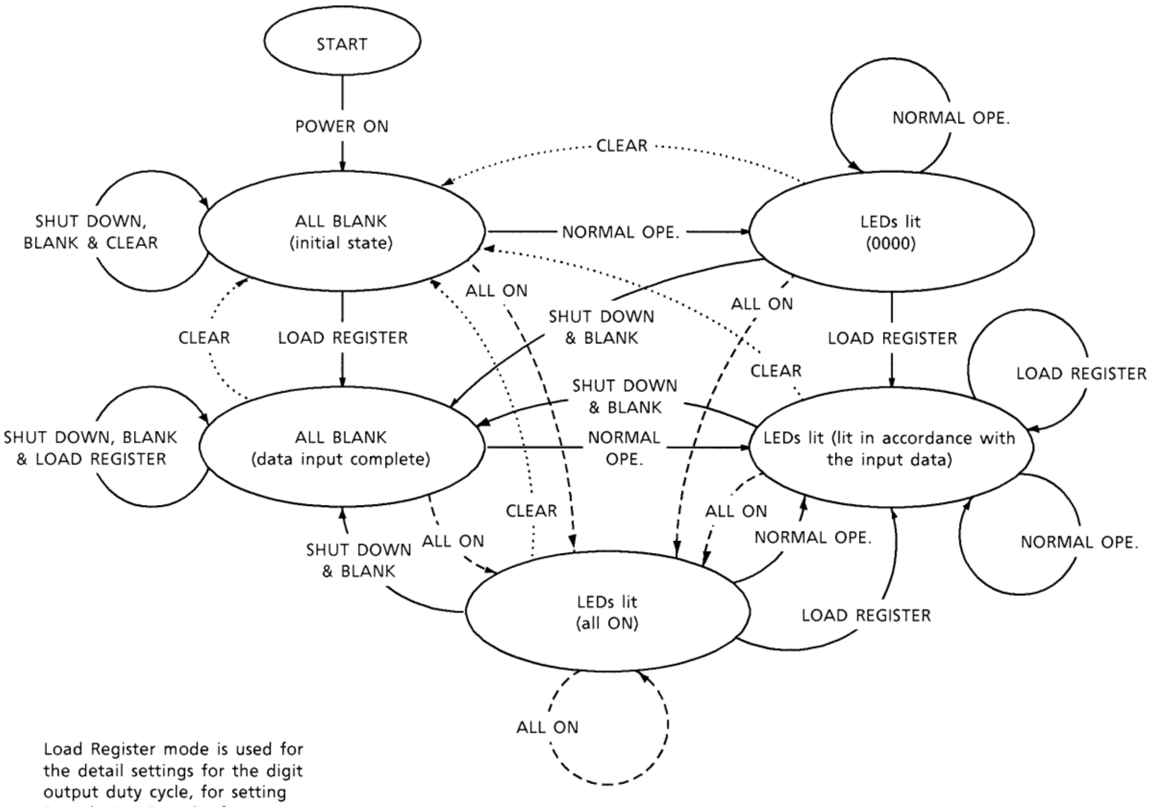
DATA INPUT
(Example 1: Displays and blinks characters a, b, c and d in digits 0, 1, 2 and 3 respectively.)

STEP	D15 to D12	D11 to D8	D7 to D4	D3 to D0	DIG-0 to 3	SEG -a, b, c, d, e, f, g	SEG -Dp	MODE	DISPLAY INDICATE
0	-	-	-	-	OFF	OFF	OFF	At power-on (= CLEAR MODE)	ALL BLANK
1	0010	0000	XXXX	1111	OFF	OFF	OFF	DUTY = 15 / 16	ALL BLANK
2	0010	0001	0001	0011	OFF	OFF	OFF	DECODE, 4DIG	ALL BLANK
3	0010	0010	X000	1010	OFF	OFF	OFF	DIG-0 = a	ALL BLANK
4	0010	0011	X000	1011	OFF	OFF	OFF	DIG-1 = b	ALL BLANK
5	0010	0100	X000	1100	OFF	OFF	OFF	DIG-2 = c	ALL BLANK
6	0010	0101	X000	1101	OFF	OFF	OFF	DIG-3 = d	ALL BLANK
7	0001	XXXX	XXXX	XXXX	ON	ON	OFF	NORMAL	a-b-c-d
8	0010	0000	XXXX	1000	ON	ON	OFF	DUTY = 8 / 16	a-b-c-d
9	0000	XXXX	XXXX	XXXX	OFF	OFF	OFF	BLANK	ALL BLANK
10	0001	XXXX	XXXX	XXXX	ON	ON	OFF	NORMAL	a-b-c-d
11	0000	XXXX	XXXX	XXXX	OFF	OFF	OFF	BLANK	ALL BLANK
12	0001	XXXX	XXXX	XXXX	ON	ON	OFF	NORMAL	a-b-c-d
13	0000	XXXX	XXXX	XXXX	OFF	OFF	OFF	BLANK	ALL BLANK
14	0001	XXXX	XXXX	XXXX	ON	ON	OFF	NORMAL	a-b-c-d
15	0100	XXXX	XXXX	0000	OFF	OFF	OFF	STAND-BY (SHUT DOWN)	ALL BLANK

DATA INPUT
(Example 2: Scroll-lights digits 0, 1, 2, 3 = a., b., c., d. (with decimal points))

STEP	D15 to D12	D11 to D8	D7 to D4	D3 to D0	DIG -0 to 3	SEG -a, b, c, d, e, f, g	SEG -Dp	MODE	DISPLAY INDICATE
0	-	-	-	-	OFF	OFF	OFF	At power-on (= CLEAR MODE)	ALL BLANK
1	0010	0000	XXXX	1111	OFF	OFF	OFF	DUTY = 15 / 16	ALL BLANK
2	0010	0001	0001	0011	OFF	OFF	OFF	DECODE, 4DIG	ALL BLANK
3	0010	0010	X100	1010	OFF	OFF	OFF	DIG-0 = a.	ALL BLANK
4	0010	0011	X001	0000	OFF	OFF	OFF	DIG-1 = blank	ALL BLANK
5	0010	0100	X001	0000	OFF	OFF	OFF	DIG-2 = blank	ALL BLANK
6	0010	0101	X001	0000	OFF	OFF	OFF	DIG-3 = blank	ALL BLANK
7	0001	XXXX	XXXX	XXXX	ON	ON	ON	NORMAL	a.---
8	0010	0010	X001	0000	OFF	ON	OFF	DIG-0 = blank	ALL BLANK
9	0010	0011	X100	1011	ON	ON	ON	DIG-1 = b.	-b.--
10	0010	0011	X001	0000	OFF	ON	OFF	DIG-1 = blank	ALL BLANK
11	0010	0100	X100	1100	ON	ON	ON	DIG-2 = c.	--c.-
12	0010	0100	X001	0000	OFF	ON	OFF	DIG-2 = blank	ALL BLANK
13	0010	0101	X100	1101	ON	ON	ON	DIG-3 = d.	---d.
14	0100	XXXX	XXXX	0000	OFF	OFF	OFF	STAND-BY (SHUT DOWN)	ALL BLANK

STATE TRANSITION DIAGRAM



Load Register mode is used for the detail settings for the digit output duty cycle, for setting Decode / No Decode, for inputting display data, and for setting the number of digits to use.

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage for Logic Circuits	V_{DD}	6.0	V
Supply Voltage	V_{CC}	17	V
DIG-0 to DIG-3 Output Current	I_{DIG}	-400	mA
OUT-a to Dp Output Current	I_{OUT}	50	mA
Output Current for Logic Block	I_{OH} / I_{OL}	±5	mA
Input Voltage	V_{IN}	-0.3 to VDD + 0.3 (Note 1)	V
Operating Frequency	f_{CK}	15.0 (Operation with 1IC)	MHz
Total Supply Current	I_{VDD}	400	mA
Power Dissipation	P_D	SDIP24: 1.78	W
		VQFN24: 2.4	
Operating Temperature	T_{opr}	-40 to 85	°C
Storage Temperature	T_{stg}	-55 to 150	°C

Note 1: However, do not exceed 6.0 V

ELECTRICAL CHARACTERISTICS
(Unless otherwise stated, V_{DD} = 5.0 V, V_{CC} = 5.0 V, R_{EXT} = 760 Ω, Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Operating Power Supply Current for Output Block	I_{CC1}	1	SET NORMAL OPE. MODE, R_{EXT} = 760 Ω @OUT-a to Dp ALL ON, Ta = 25°C	-	300	-	mA
	I_{CC2}	1	SET NORMAL OPE. MODE, R_{EXT} = 760 Ω @OUT-a to Dp ALL ON V_{CC} = 12 V, Ta = 25°C	-	320	-	
DIG-0 to DIG-3 Scan Frequency	f_{OSC}	2	NORMAL OPE. MODE, V_{DD} = 4.5 to 5.5 V	240	480	960	Hz
OUT-a to Dp Output Sink Current	I_{SEG}	3	NORMAL OPE. MODE, V_{CE} = 0.7 V, R_{EXT} = 760 Ω	29	34	40	mA
DIG-0 to 3 Output Leakage Current	I_{leak1}	4	ALL OFF MODE, V_{CC} = 17 V	-	-	-1	μA
OUT-a to Dp Output Leakage Current	I_{leak2}	4	ALL OFF MODE, V_{CC} = 17 V	-	-	1	μA
DIG-0 to 3 Output Voltage	V_{OUT}	5	NORMAL OPE. MODE, I_{DIG} = -320 mA	3.0	-	-	V

Logic block

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Static Power Supply Current for Logic Circuits	I_{DD1}	6	STANDBY MODE, Ta = 25°C	-	-	200	μA
	I_{DD2}	6	BLANK MODE, Ta = 25°C	-	-	12.5	mA
Operating Power Supply Current for Logic Circuits	I_{DD3}	6	NORMAL OPE. MODE, f_{CLK} = 10MHz, DATA-IN: OUT-a to Dp = ON, Ta = 25°C	-	-	20.5	mA
High Input Current for Logic Circuits	I_{IH}	-	DATA-IN, LOAD & CLOCK: V_{IN} = 5 V	-	-	1	μA
Low Input Current for Logic Circuits	I_{IL}	-	DATA-IN, LOAD & CLOCK: V_{IN} = 0 V	-	-	-1	μA
High Output Voltage for Logic Circuits	V_{OH1}	6	DATA-OUT, I_{OH} = -1.0 mA	4.6	-	-	V
	V_{OH2}	6	DATA-OUT, I_{OH} = -1.0 μA	-	V_{DD}	-	
Low Output Voltage for Logic Circuits	V_{OL1}	6	DATA-OUT, I_{OL} = 1.0 mA	-	-	0.4	V
	V_{OL2}	6	DATA-OUT, I_{OL} = 1.0 μA	-	0.1	-	
Clock Frequency	f_{CLK}	6	CASCADE CONNECTED, Ta = -40 to 85°C	-	-	10	MHz

SWITCHING CHARACTERISTICS
(Unless otherwise stated, V_{DD} = 5.0 V, V_{CC} = 5.0 V, Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Data Hold Time (D-IN-CLOCK)	t_{DHO}	-	-	-	10	-	ns
Data Setup Time (D-IN-CLOCK)	t_{DST}	-	-	-	20	-	ns
Serial Output Delay Time (CLOCK-D-OUT)	$t_{pHL\text{-}SO}$	-	C_L = 10 pF	-	25	-	ns
	$t_{pLH\text{-}SO}$		C_L = 10 pF	-	25	-	
High Clock Pulse Width	t_{CKH}	-	-	-	30	-	ns
Low Clock Pulse Width	t_{CKL}	-	-	-	30	-	ns
Load Pulse Width	t_{wLD}	-	-	-	100	-	ns
Load Clock Time (CLOCK-LOAD)	t_{CKLD}	-	-	-	50	-	ns
Clock Load Time (LOAD-CLOCK)	t_{LDCK}	-	-	-	50	-	ns
OUT-a to Dp Output Delay Time (LOAD(Internal EN)-OUTn)	$t_{pHL\text{-}SEG}$	-	C_L = 10 pF, Test mode	-	-	5.0	μs
	$t_{pLH\text{-}SEG}$		C_L = 10 pF, Test mode	-	-	5.0	
OUT-a to Dp Output Rise Time (OUTn)	t_r SEG	-	C_L = 10 pF	0.2	1.0	-	μs
OUT-a to Dp Output Fall Time (OUTn)	t_f SEG	-	C_L = 10 pF	0.2	1.0	-	μs
DIG-0 to DIG-3 Output Delay Time (LOAD(Internal EN)-DIGn)	$t_{pHL\text{-}DIG}$	-	C_L = 10 pF, Test mode	-	-	10.0	μs
	$t_{pLH\text{-}DIG}$		C_L = 10 pF, Test mode	-	-	10.0	
DIG-0 to DIG-3 Output Rise Time (DIGn)	t_r DIG	-	C_L = 10 pF	5	20	-	ns
DIG-0 to DIG-3 Output Fall Time (DIGn)	t_f DIG	-	C_L = 10 pF	50	150	-	ns

RECOMMENDED OPERATING CONDITIONS
(Unless otherwise stated, V_{DD} = 5.0 V, V_{CC} = 5.0 V, Ta = -40 to 85°C)

Output

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Supply Voltage for Output Block	V_{CC}	-	-	4.0	-	6.0	V
DIG-0 to DIG-3 Output Source Current	I_{DIG}	-	V_{OUT} = 3.0 V	-	-	-320	mA
OUT-a to OUT-Dp Output Sink Current	I_{SEG}	-	V_{CE} = 0.7 V	-	-	40	mA

Logic block

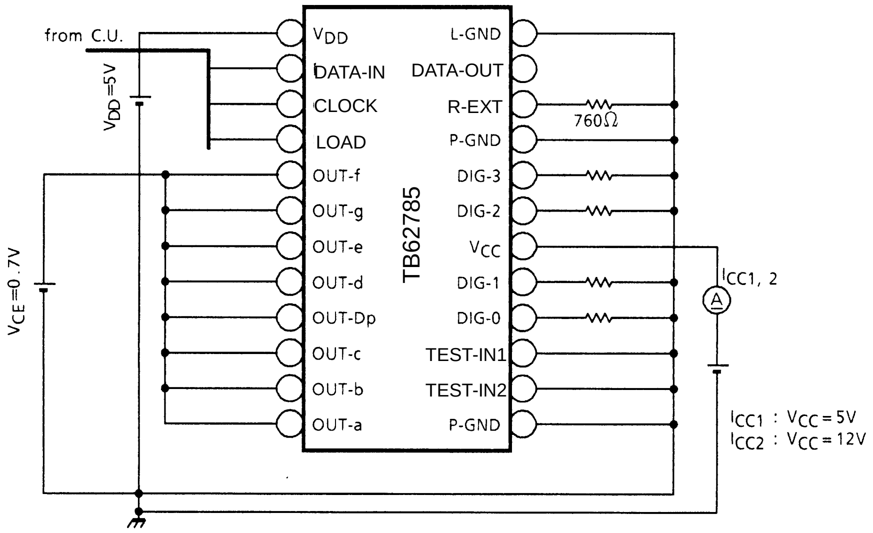
CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Supply Voltage for Logic Block	V_{DD}	-	-	4.5	-	5.5	V
High Input Current for Logic Circuits	I_{IH}	-	DATA-IN, LOAD & CLOCK, V_{IN} = V_{DD}	-	-	1	μA
Low Input Current for Logic Circuits	I_{IL}	-	DATA-IN, LOAD & CLOCK, V_{IN} = 0V	-	-	-1	μA
High Input Voltage for Logic Circuits	V_{IH}	-	-	0.7 V_{DD}	-	-	V
Low Input Voltage for Logic Circuits	V_{IL}	-	-	-	-	0.3 V_{DD}	V

SWITCHING CONDITIONS

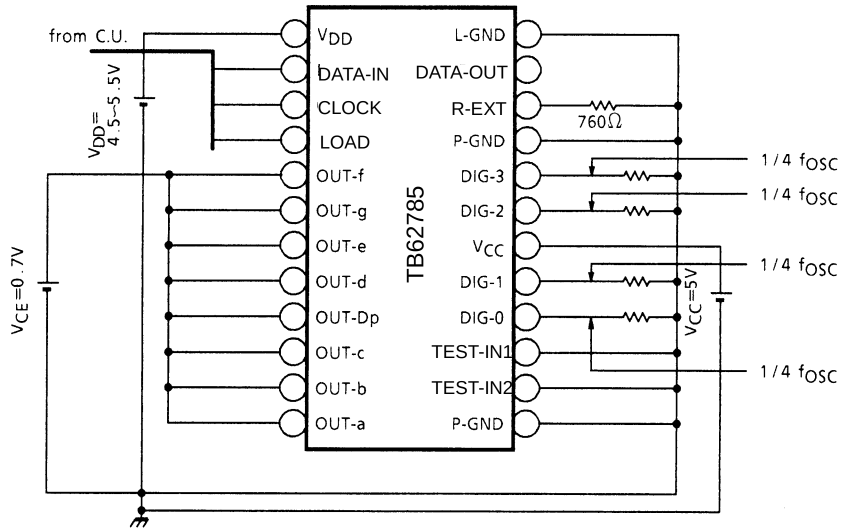
CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Data Hold Time (D-IN-CLOCK)	t_{DHO}	-	-	30	-	-	ns
Data Setup Time (D-IN-CLOCK)	t_{DST}	-	-	50	-	-	ns
Serial Output Delay Time (CLOCK-D-OUT)	t_{PDSO}	-	C_L = 10 pF	50	-	-	ns
High Clock Pulse Width	t_{CKH}	-	-	30	-	-	ns
Low Clock Pulse Width	t_{CKL}	-	-	30	-	-	ns
Load Pulse Width	t_{wLD}	-	-	150	-	-	ns
Load Clock Time (CLOCK-LOAD)	t_{CLKLD}	-	-	100	-	-	ns
Clock Load Time (LOAD-CLOCK)	t_{LDCLK}	-	-	100	-	-	ns

TEST CIRCUITS

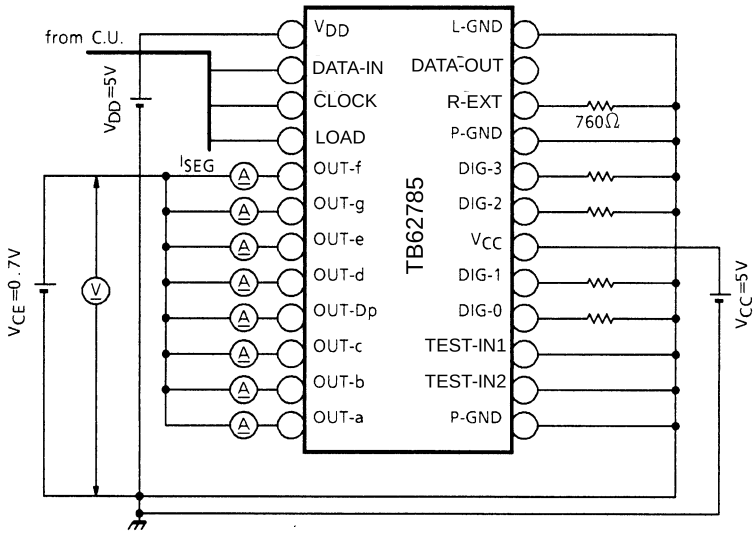
(1) I_{CC1}, I_{CC2}



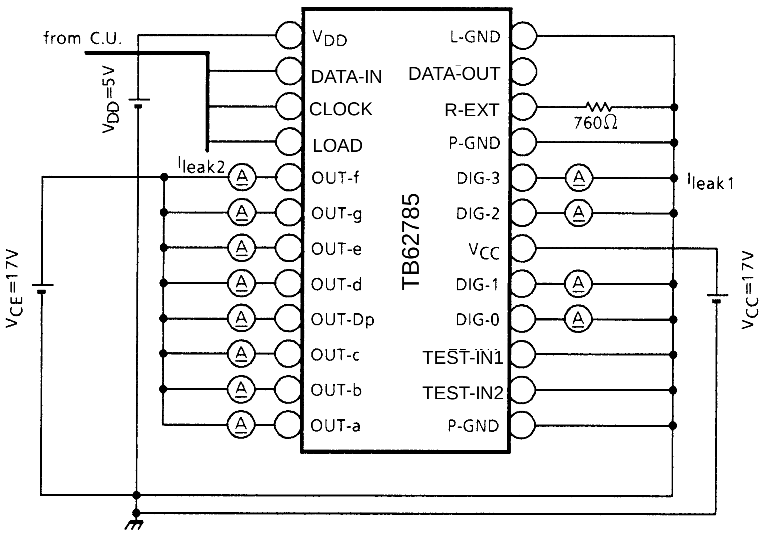
(2) fosc



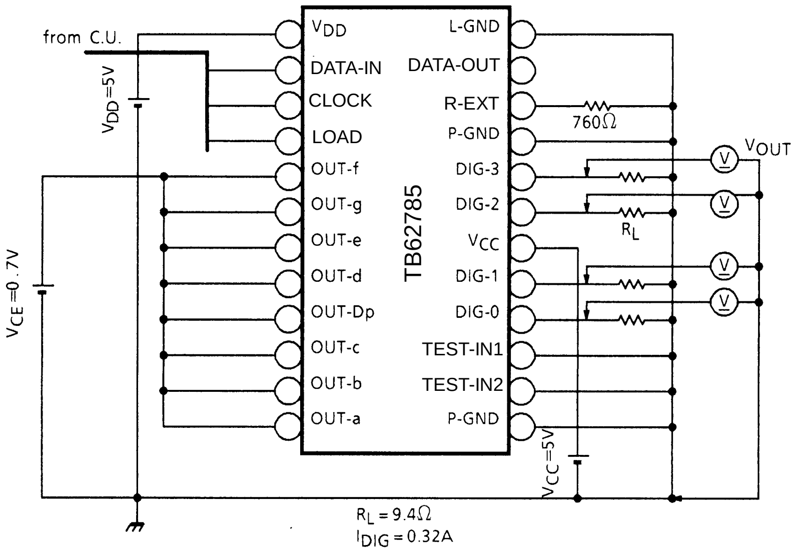
(3) ISEG



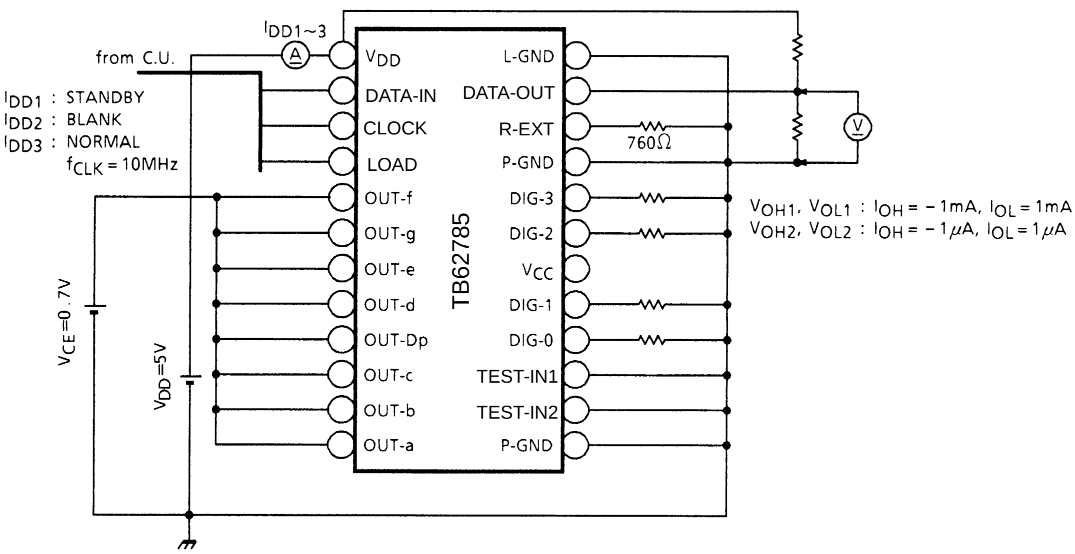
(4) Ileak1, Ileak2



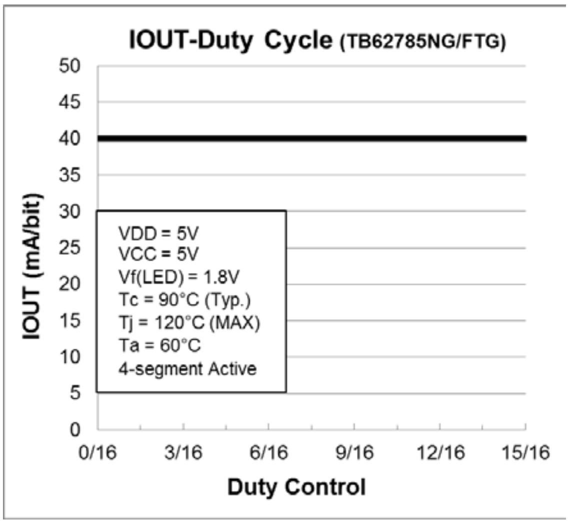
(5) VOUT

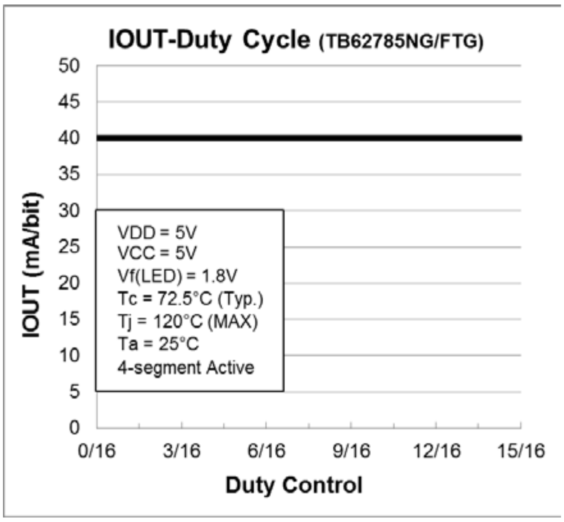


(6) IDD1, IDD2, IDD3, VOH1, VOH2, VOL1, VOL2, fCLK



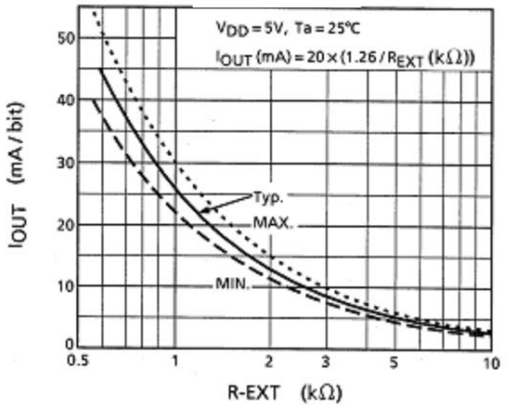
DUTY CYCLE SETTINGS AND OUTPUT CURRENT VALUES





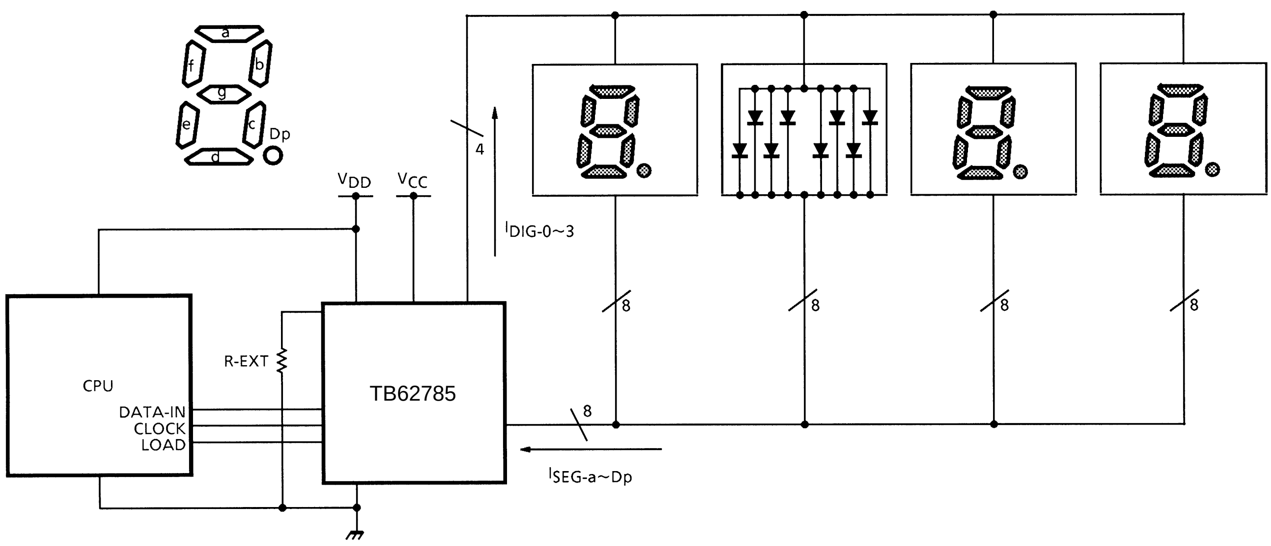
EXTERNAL RESISTANCE AND OUTPUT CURRENT VALUES

I_{OUT} - R-EXT



The following diagram shows application circuits.
Because operation may be unstable due to influences such as the electromagnetic induction of the wiring, the IC should be located as close as possible to the LED.
The L-GND and P-GND of the IC are connected to the substrate in the IC.
Take care to avoid a potential difference exceeding 0.4V at two pins.
When executing the pattern layout, Toshiba recommends not including inductance components in the GND or output pin lines, and not inserting capacitance components exceeding 50pF between the R-EXT and GND.

APPLICATION CIRCUIT EXAMPLE (Connection example)



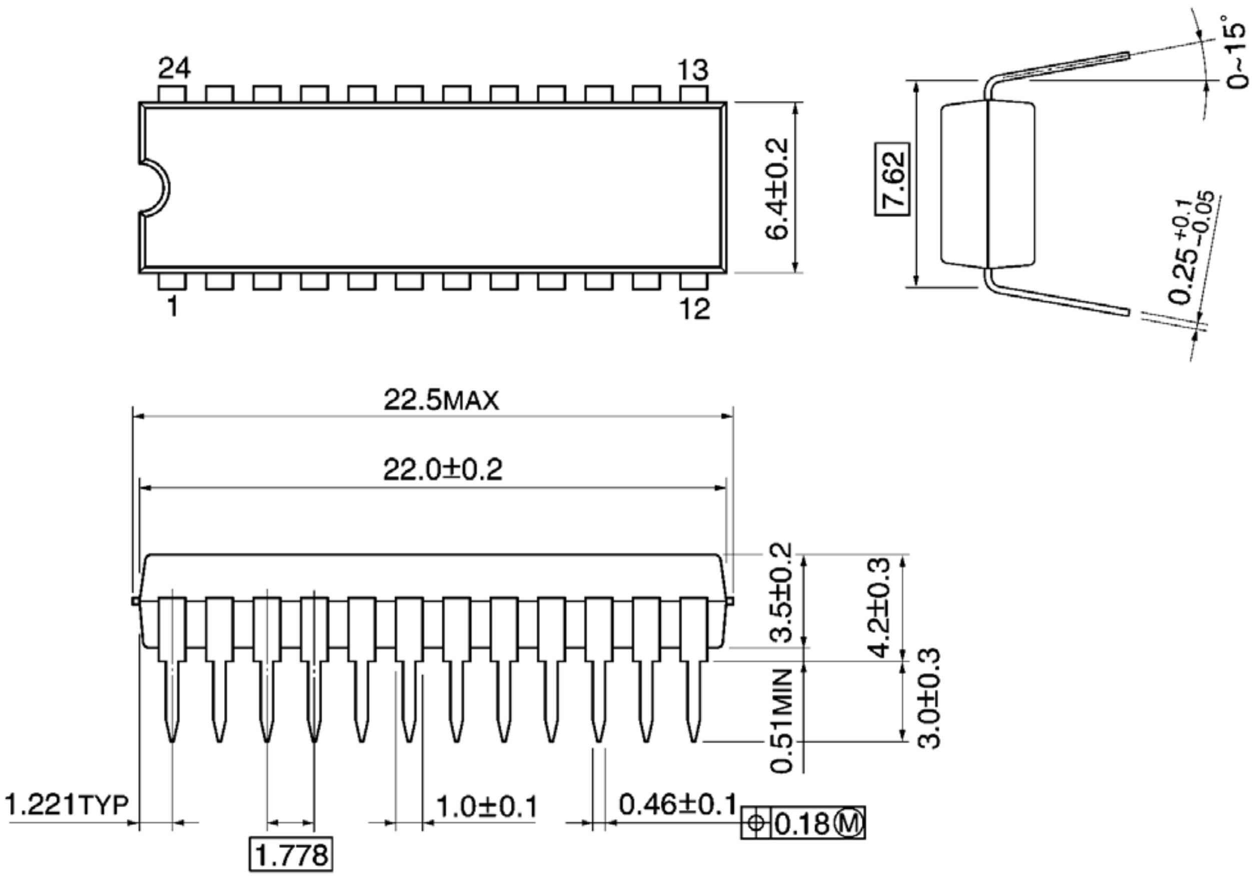
PRECAUTIONS for USING

Utmost care is necessary in the design of the output line, VCC (VDD) and (L-GND, P-GND) line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

Package Dimensions

SDIP24-P-300-1.78

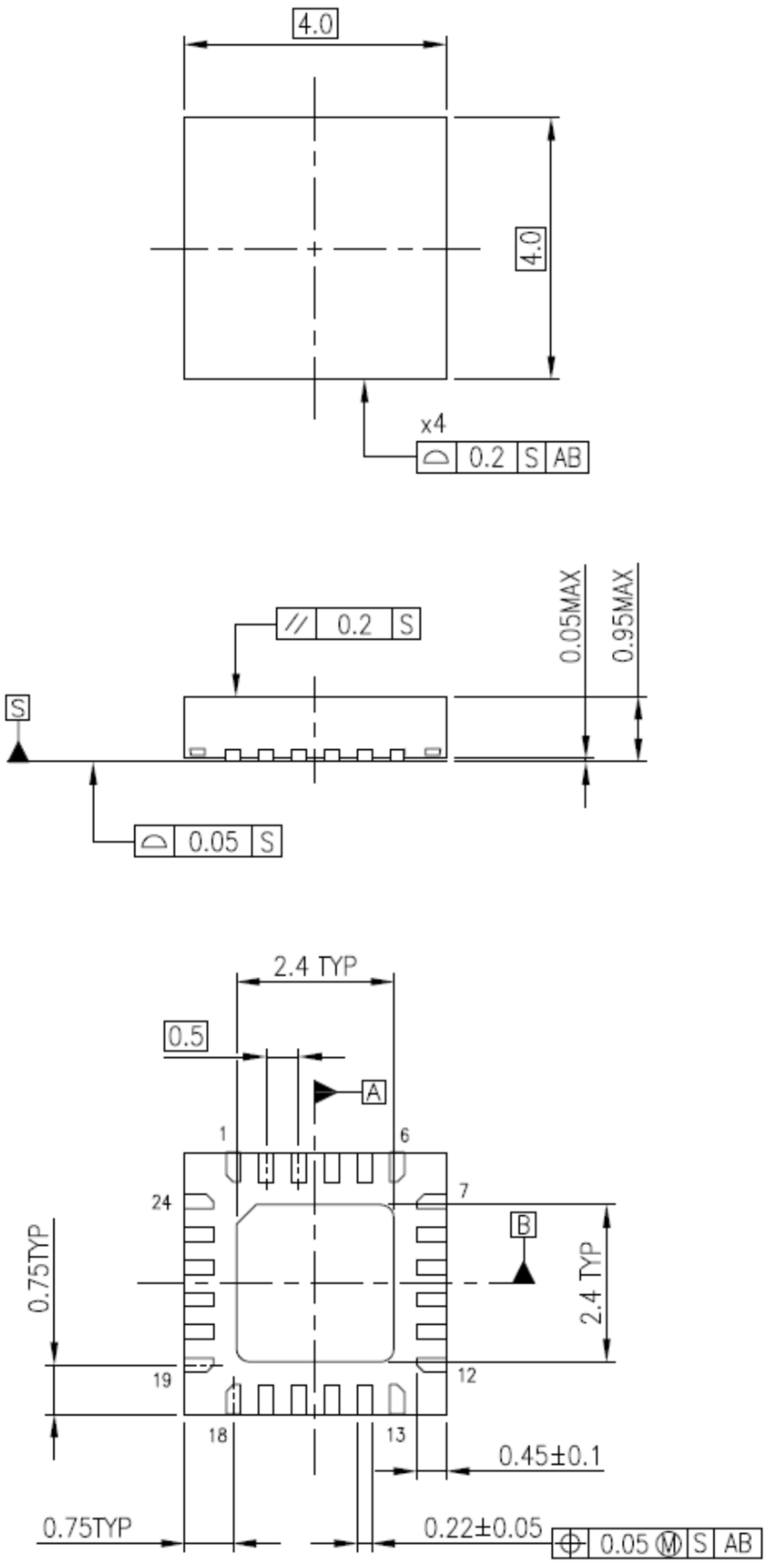
Unit: mm



Weight: 1.22 g (typ.)

P-VQFN24-0404-0.50-001

Unit: mm



Weight: 0.037 g (typ.)

Notes on Contents

1. Block Diagrams
Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits
The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts
Timing charts may be simplified for explanatory purposes.

4. Application Circuits
The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

5. Test Circuits
Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations
Notes on handling of ICs

[1] The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

[2] Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

[3] If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

[4] Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

[5] Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.
If there is a large amount of leakage current such as input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

Points to remember on handling of ICs

(1) Heat Radiation Design
In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_j) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(2) Back-EMF
When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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