

## Double channel high side driver for automotive applications

### Features

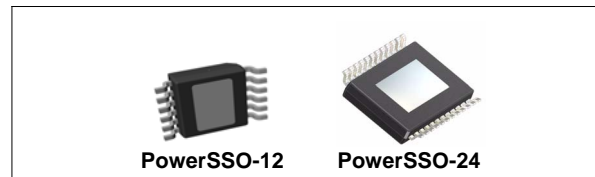
Max supply voltage	$V_{CC}$	41 V
Operating voltage range	$V_{CC}$	4.5 to 36 V
Max on-State resistance (per ch.)	$R_{ON}$	50 m $\Omega$
Current limitation (typ)	$I_{LIMH}$	18 A
Off-state supply current	$I_S$	2 $\mu$ A <sup>(1)</sup>

1. Typical value with all loads connected.

- Main
  - Inrush current active management by power limitation
  - Very low standby current
  - 3.0 V CMOS compatible input
  - Optimized electromagnetic emission
  - Very low electromagnetic susceptibility
  - In compliance with the 2002/95/EC European directive
- Diagnostic functions
  - Open drain status output
  - On-state open load detection
  - Off-state open load detection
  - Thermal shutdown indication
- Protections
  - Undervoltage shutdown
  - Overvoltage clamp
  - Output stuck to  $V_{CC}$  detection
  - Load current limitation
  - Self limiting of fast thermal transients
  - Protection against loss of ground and loss of  $V_{CC}$
  - Thermal shutdown

**Table 1. Device summary**

Package	Order code	
	Tube	Tape and reel
PowerSSO-12	VND5050J-E	VND5050JTR-E
PowerSSO-24	VND5050K-E	VND5050KTR-E



- Reverse battery protection (see [Figure 28](#))
- Electrostatic discharge protection

### Applications

- All types of resistive, inductive and capacitive loads

### Description

The VND5050K-E and VND5050J-E are monolithic devices made using STMicroelectronics VIPower M0-5 technology. they are intended for driving resistive or inductive loads with one side connected to ground. Active  $V_{CC}$  pin voltage clamp protects the devices against low energy spikes (see ISO7637 transient compatibility table). The devices detect open load condition both in on and off-state, when STAT\_DIS is left open or driven low. Output shorted to  $V_{CC}$  is detected in the off-state.

When STAT\_DIS is driven high, STATUS pin is in high impedance state.

Output current limitation protects the devices in overload condition. In case of long overload duration, the devices limit the dissipated power to a safe level up to thermal shutdown intervention. Thermal shutdown with automatic restart allows the devices to recover normal operation as soon as fault conditions disappear.

# Contents

<b>1</b>	<b>Block diagram and pin description</b>	<b>5</b>
<b>2</b>	<b>Electrical specifications</b>	<b>7</b>
2.1	Absolute maximum ratings	7
2.2	Thermal data	8
2.3	Electrical characteristics	8
2.4	Electrical characteristics curves	16
<b>3</b>	<b>Application information</b>	<b>20</b>
3.1	GND protection network against reverse battery	20
3.1.1	Solution 1: resistor in the ground line (RGND only)	20
3.1.2	Solution 2: a diode (DGND) in the ground line	21
3.2	Load dump protection	21
3.3	Microcontroller I/Os protection	21
3.4	Open-load detection in off-state	21
3.5	Maximum demagnetization energy (VCC = 13.5V)	23
<b>4</b>	<b>Package and PCB thermal data</b>	<b>24</b>
4.1	PowerSSO-12™ thermal data	24
4.2	PowerSSO-24™ thermal data	27
<b>5</b>	<b>Package and packing information</b>	<b>30</b>
5.1	ECOPACK® packages	30
5.2	PowerSSO-12™ package information	30
5.3	PowerSSO-24™ package information	32
5.4	PowerSSO-12™ packing information	34
5.5	PowerSSO-24™ packing information	35
<b>6</b>	<b>Revision history</b>	<b>36</b>

## List of tables

Table 2.	Pin function . . . . .	5
Table 3.	Suggested connections for unused and not connected pins . . . . .	6
Table 4.	Absolute maximum ratings . . . . .	7
Table 5.	Thermal data . . . . .	8
Table 6.	Power section . . . . .	8
Table 7.	Switching ( $V_{CC} = 13V$ ; $T_j = 25^{\circ}C$ ) . . . . .	9
Table 8.	Status pin ( $V_{SD}=0V$ ) . . . . .	9
Table 9.	Protections . . . . .	10
Table 10.	Openload detection . . . . .	10
Table 11.	Logic input . . . . .	10
Table 12.	Truth table . . . . .	12
Table 13.	Electrical transient requirements (part 1/3) . . . . .	13
Table 14.	Electrical transient requirements (part 2/3) . . . . .	13
Table 15.	Electrical transient requirements (part 3/3) . . . . .	14
Table 16.	PowerSSO-12™ thermal parameters . . . . .	26
Table 17.	PowerSSO-24™ thermal parameters . . . . .	29
Table 18.	PowerSSO-12™ mechanical data . . . . .	31
Table 19.	PowerSSO-24™ mechanical data . . . . .	32
Table 20.	Document revision history . . . . .	36

## List of figures

Figure 1.	Block diagram . . . . .	5
Figure 2.	Configuration diagram (top view) . . . . .	6
Figure 3.	Current and voltage conventions . . . . .	7
Figure 4.	Status timings . . . . .	11
Figure 5.	Switching characteristics . . . . .	12
Figure 6.	Output voltage drop limitation . . . . .	13
Figure 7.	Waveforms . . . . .	15
Figure 8.	Off-state output current . . . . .	16
Figure 9.	High level input current . . . . .	16
Figure 10.	Input clamp voltage . . . . .	16
Figure 11.	Input high level . . . . .	16
Figure 12.	Input low level . . . . .	16
Figure 13.	Input hysteresis voltage . . . . .	16
Figure 14.	Status low output voltage . . . . .	17
Figure 15.	On-state resistance vs $T_{case}$ . . . . .	17
Figure 16.	Status leakage current . . . . .	17
Figure 17.	On-state resistance vs $V_{CC}$ . . . . .	17
Figure 18.	Status clamp voltage . . . . .	17
Figure 19.	Openload on-state detection threshold . . . . .	17
Figure 20.	Openload off-state voltage detection threshold . . . . .	18
Figure 21.	$I_{LIM}$ vs $T_{case}$ . . . . .	18
Figure 22.	Turn-on voltage slope . . . . .	18
Figure 23.	Undervoltage shutdown . . . . .	18
Figure 24.	Turn-off voltage slope . . . . .	18
Figure 25.	STAT_DIS clamp voltage . . . . .	18
Figure 26.	High level STAT_DIS voltage . . . . .	19
Figure 27.	Low level STAT_DIS voltage . . . . .	19
Figure 28.	Application schematic . . . . .	20
Figure 29.	Open-load detection in off-state . . . . .	22
Figure 30.	Maximum turn-off current versus inductance (for each channel) . . . . .	23
Figure 31.	PowerSSO-12™ PC board . . . . .	24
Figure 32.	$R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel on) . . . . .	24
Figure 33.	PowerSSO-12™ thermal impedance junction ambient single pulse (one channel on) . . . . .	25
Figure 34.	Thermal fitting model of a double channel HSD in PowerSSO-12™ . . . . .	25
Figure 35.	PowerSSO-24™ PC board . . . . .	27
Figure 36.	$R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel on) . . . . .	27
Figure 37.	PowerSSO-24™ thermal impedance junction ambient single pulse (one channel on) . . . . .	28
Figure 38.	Thermal fitting model of a double channel HSD in PowerSSO-24™ . . . . .	28
Figure 39.	PowerSSO-12™ package dimensions . . . . .	30
Figure 40.	PowerSSO-24™ package dimensions . . . . .	32
Figure 41.	PowerSSO-12™ tube shipment (no suffix) . . . . .	34
Figure 42.	PowerSSO-12™ tape and reel shipment (suffix "TR") . . . . .	34
Figure 43.	PowerSSO-24™ tube shipment (no suffix) . . . . .	35
Figure 44.	PowerSSO-24™ tape and reel shipment (suffix "TR") . . . . .	35

# 1 Block diagram and pin description

Figure 1. Block diagram

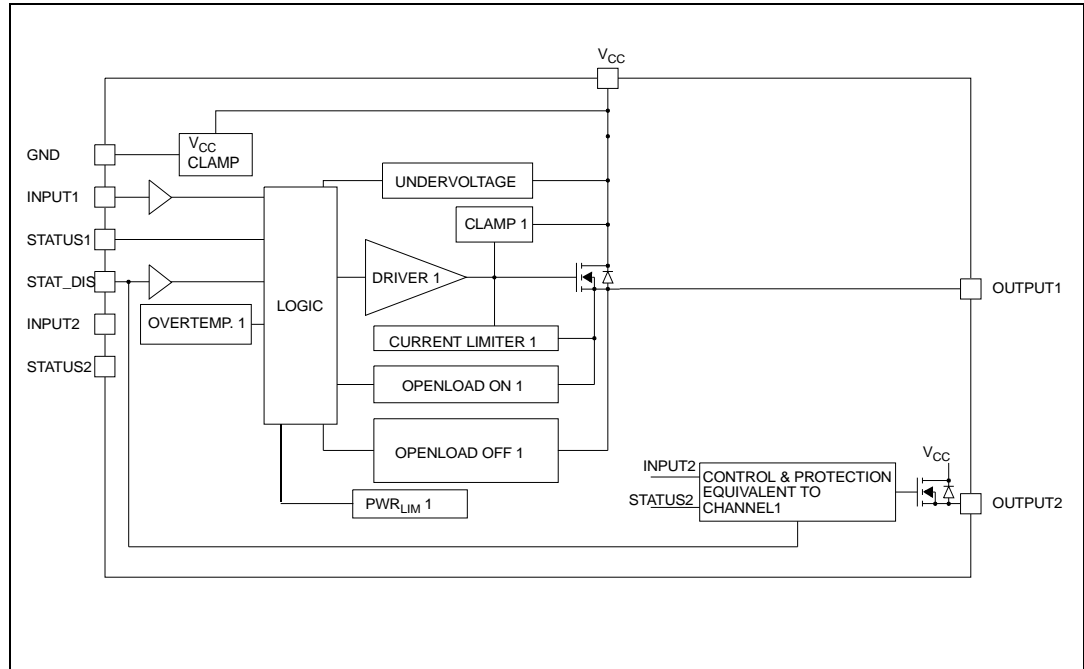


Table 2. Pin function

Name	Function
V <sub>CC</sub>	Battery connection.
OUTPUT <sub>n</sub>	Power output.
GND	Ground connection. Must be reverse battery protected by an external diode/resistor network.
INPUT <sub>n</sub>	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state.
STATUS <sub>n</sub>	Open drain digital diagnostic pin.
STAT_DIS	Active high CMOS compatible pin, to disable the STATUS pin.

Figure 2. Configuration diagram (top view)

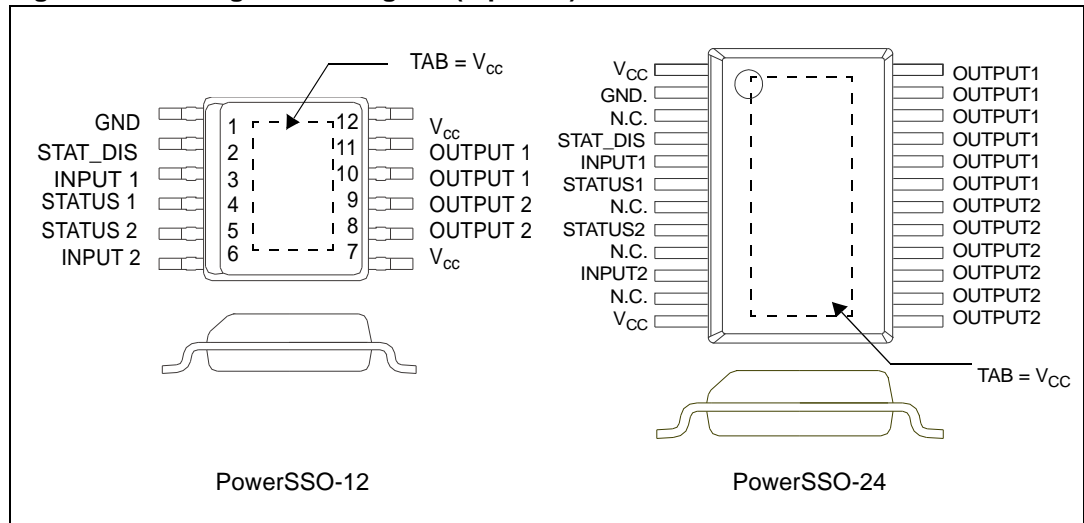


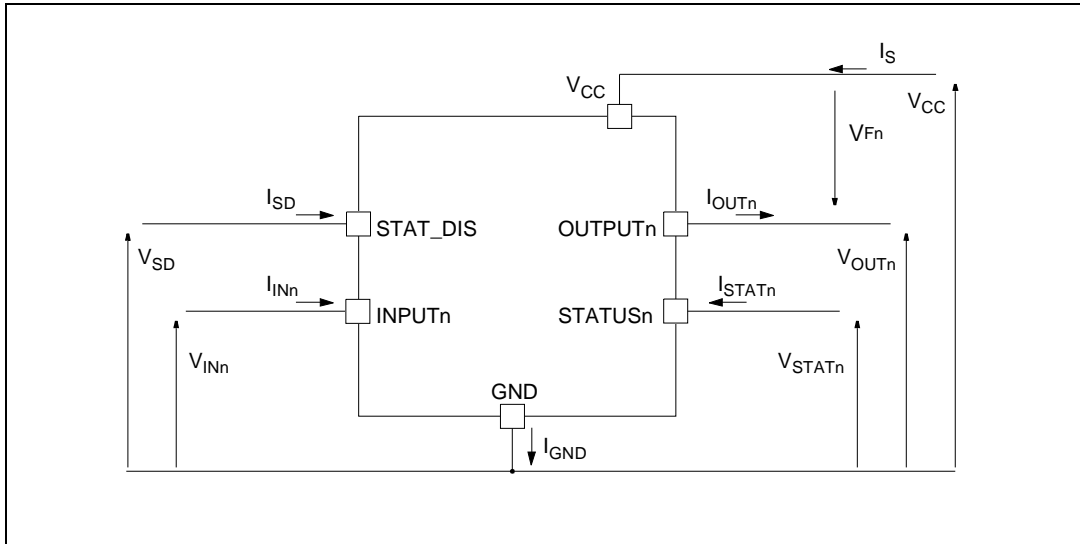
Table 3. Suggested connections for unused and not connected pins

Connection/pin	STATUS	N.C.	OUTPUT	INPUT	STAT_DIS
Floating	X	X	X	X	X
To ground	N.R. <sup>(1)</sup>	X	N.R.	Through 10KΩ resistor	Through 10KΩ resistor

1. Not recommended.

## 2 Electrical specifications

Figure 3. Current and voltage conventions



Note:  $V_{Fn} = V_{OUTn} - V_{CCn}$  during reverse battery condition.

### 2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{CC}$	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	0.3	V
$-I_{GND}$	DC reverse ground pin current	200	mA
$I_{OUT}$	DC output current	Internally limited	A
$-I_{OUT}$	Reverse dc output current	15	A
$I_{IN}$	DC input current	+10 / -1	mA
$I_{STAT}$	DC status current	+10 / -1	mA
$I_{STAT\_DIS}$	DC status disable current	+10 / -1	mA
$E_{MAX}$	Maximum switching energy ( $L=3mH$ ; $R_L=0\Omega$ ; $V_{bat}=13.5V$ ; $T_{jstart}=150^\circ C$ ; $I_{OUT} = I_{limL}(Typ.)$ )	104	mJ

**Table 4. Absolute maximum ratings (continued)**

Symbol	Parameter	Value	Unit
V <sub>ESD</sub>	Electrostatic discharge (Human Body Model: R=1.5KΩ; C=100pF)		
	– Input	4000	V
	– Status	4000	V
	– STAT_DIS	4000	V
	– Output	5000	V
	– V <sub>CC</sub>	5000	V
V <sub>ESD</sub>	Charge device model (CDM-AEC-Q100-011)	750	V
T <sub>j</sub>	Junction operating temperature	-40 to 150	°C
T <sub>stg</sub>	Storage temperature	- 55 to 150	°C

## 2.2 Thermal data

**Table 5. Thermal data**

Symbol	Parameter	Value		Unit
		PowerSSO-12	PowerSSO-24	
R <sub>thj-case</sub>	Thermal resistance junction case (max) (with one channel on)	2.8	2.8	°C/W
R <sub>thj-amb</sub>	Thermal resistance junction ambient (max)	See <a href="#">Figure 32</a>	See <a href="#">Figure 36</a>	°C/W

## 2.3 Electrical characteristics

8 V < V<sub>CC</sub> < 36 V; -40 °C < T<sub>j</sub> < 150 °C, unless otherwise specified.

**Table 6. Power section**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Operating supply voltage		4.5	13	36	V
V <sub>USD</sub>	Undervoltage shutdown			3.5	4.5	V
V <sub>USDhyst</sub>	Undervoltage shutdown hysteresis			0.5		V
R <sub>ON</sub>	On-state resistance <sup>(2)</sup>	I <sub>OUT</sub> =2A; T <sub>j</sub> =25°C I <sub>OUT</sub> =2A; T <sub>j</sub> =150°C I <sub>OUT</sub> =2A; V <sub>CC</sub> =5V; T <sub>j</sub> =25°C			50 100 65	mΩ mΩ mΩ
V <sub>clamp</sub>	Clamp voltage	I <sub>S</sub> =20mA	41	46	52	V
I <sub>S</sub>	Supply current	Off-state; V <sub>CC</sub> =13V; T <sub>j</sub> =25°C; V <sub>IN</sub> =V <sub>OUT</sub> =V <sub>SENSE</sub> =V <sub>CSD</sub> =0V On-state; V <sub>CC</sub> =13V; V <sub>IN</sub> =5V; I <sub>OUT</sub> =0A		2 <sup>(1)</sup> 3	5 <sup>(1)</sup> 6	μA mA



**Table 6. Power section (continued)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{L(off1)}$	Off-state output current <sup>(2)</sup>	$V_{IN}=V_{OUT}=0V$ ; $V_{CC}=13V$ ; $T_j=25^\circ C$	0	0.01	3	$\mu A$
		$V_{IN}=V_{OUT}=0V$ ; $V_{CC}=13V$ ; $T_j=125^\circ C$	0		5	
$I_{L(off2)}$	Off-state output current <sup>(2)</sup>	$V_{IN}=0V$ ; $V_{OUT}=4V$	-75		0	
$V_F$	Output - $V_{CC}$ diode voltage <sup>(2)</sup>	$-I_{OUT}=4A$ ; $T_j=150^\circ C$			0.7	V

1. PowerMOS leakage included.

2. For each channel.

**Table 7. Switching ( $V_{CC} = 13V$ ;  $T_j = 25^\circ C$ )**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 6.5\Omega$ (see <a href="#">Figure 5</a> )		20		$\mu s$
$t_{d(off)}$	Turn-off delay time	$R_L = 6.5\Omega$ (see <a href="#">Figure 5</a> )		40		$\mu s$
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	$R_L = 6.5\Omega$	See <a href="#">Figure 22</a>			V/ $\mu s$
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	$R_L = 6.5\Omega$	See <a href="#">Figure 24</a>			V/ $\mu s$
$W_{ON}$	Switching energy losses during $t_{won}$	$R_L = 6.5\Omega$ (see <a href="#">Figure 5</a> )		0.21		mJ
$W_{OFF}$	Switching energy losses during $t_{woff}$	$R_L = 6.5\Omega$ (see <a href="#">Figure 5</a> )		0.28		mJ

**Table 8. Status pin ( $V_{SD}=0V$ )**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{STAT}$	Status low output voltage	$I_{STAT} = 1.6 mA$ , $V_{SD}=0V$			0.5	V
$I_{LSTAT}$	Status leakage current	Normal operation or $V_{SD}=5V$ , $V_{STAT} = 5V$			10	$\mu A$
$C_{STAT}$	Status pin input capacitance	Normal operation or $V_{SD}=5V$ , $V_{STAT} = 5V$			100	pF
$V_{SCL}$	Status clamp voltage	$I_{STAT} = 1mA$	5.5		7	V
		$I_{STAT} = -1mA$		-0.7		V

**Table 9. Protections<sup>(1)</sup>**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{limH}$	DC short circuit current	$V_{CC}=13V$ $5V < V_{CC} < 36V$	12	18	24 24	A A
$I_{limL}$	Short circuit current during thermal cycling	$V_{CC}=13V$ $T_R < T_j < T_{TSD}$		7		A
$T_{TSD}$	Shutdown temperature		150	175	200	°C
$T_R$	Reset temperature		$T_{RS} + 1$	$T_{RS} + 5$		°C
$T_{RS}$	Thermal reset of STATUS		135			°C
$T_{HYST}$	Thermal hysteresis ( $T_{TSD} - T_R$ )			7		°C
$t_{SDL}$	Status delay in overload conditions	$T_j > T_{TSD}$ (see <a href="#">Figure 4</a> )			20	µs
$V_{DEMAG}$	Turn-off output voltage clamp	$I_{OUT}=2A$ ; $V_{IN}=0$ ; $L=6mH$	$V_{CC}-41$	$V_{CC}-46$	$V_{CC}-52$	V
$V_{ON}$	Output voltage drop limitation	$I_{OUT}=0.1A$ ; $T_j = -40°C \dots +150°C$ (see <a href="#">Figure 6</a> )		25		mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

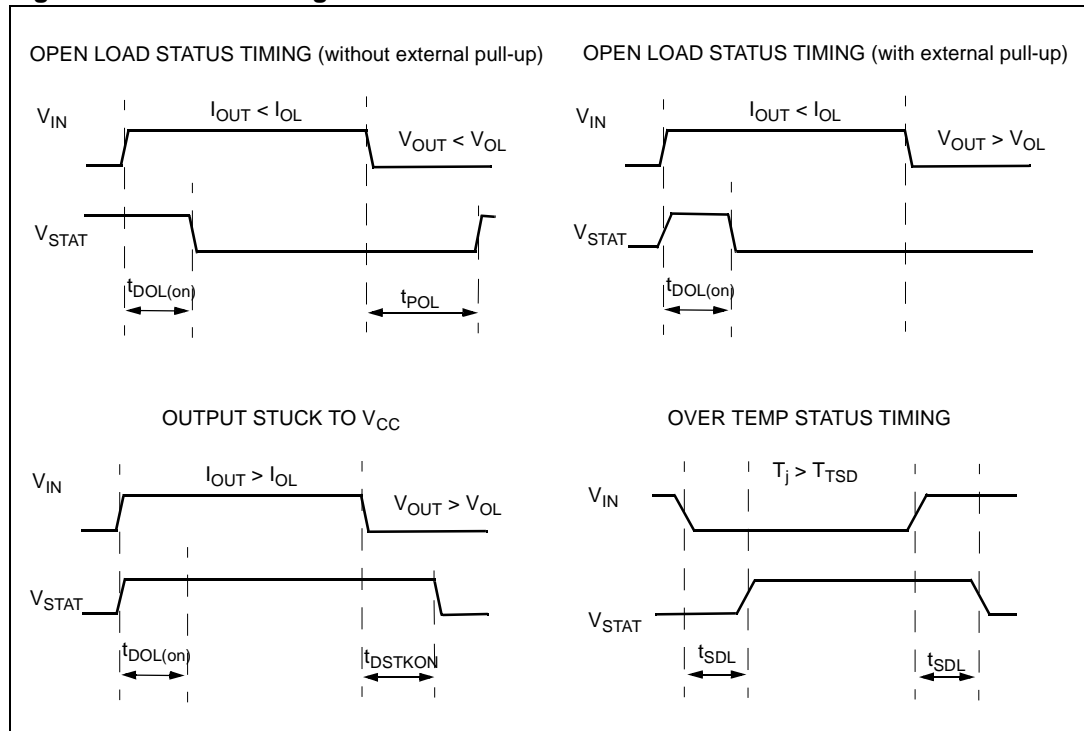
**Table 10. Openload detection**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{OL}$	Openload on-state detection threshold	$V_{IN} = 5V, 8V < V_{CC} < 18V$	10	See <a href="#">Figure 19</a>	70	mA
$t_{DOL(on)}$	Openload on-state detection delay	$I_{OUT} = 0A$ , $V_{CC}=13V$ (see <a href="#">Figure 4</a> )			200	µs
$t_{POL}$	Delay between INPUT falling edge and STATUS rising edge in Openload condition	$I_{OUT} = 0A$ (see <a href="#">Figure 4</a> )	200	500	1000	µs
$V_{OL}$	Openload off-state voltage detection threshold	$V_{IN} = 0V$ , $8V < V_{CC} < 16V$	2	See <a href="#">Figure 20</a>	4	V
$t_{DSTKON}$	Output short circuit to $V_{CC}$ detection delay at turn-off	(see <a href="#">Figure 4</a> )	180		$t_{POL}$	µs

**Table 11. Logic input**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IL}$	Input low level				0.9	V
$I_{IL}$	Low level input current	$V_{IN} = 0.9\text{ V}$	1			$\mu\text{A}$
$V_{IH}$	Input high level		2.1			V
$I_{IH}$	High level input current	$V_{IN} = 2.1\text{ V}$			10	$\mu\text{A}$
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
$V_{ICL}$	Input clamp voltage	$I_{IN} = 1\text{ mA}$ $I_{IN} = -1\text{ mA}$	5.5	-0.7	7	V V
$V_{SDL}$	STAT_DIS low level voltage				0.9	V
$I_{SDL}$	Low level STAT_DIS current	$V_{SD} = 0.9\text{ V}$	1			$\mu\text{A}$
$V_{SDH}$	STAT_DIS high level voltage		2.1			V
$I_{SDH}$	High level STAT_DIS current	$V_{SD} = 2.1\text{ V}$			10	$\mu\text{A}$
$V_{SD(hyst)}$	STAT_DIS hysteresis voltage		0.25			V
$V_{SDCL}$	STAT_DIS clamp voltage	$I_{SD} = 1\text{ mA}$ $I_{SD} = -1\text{ mA}$	5.5	-0.7	7	V V

**Figure 4. Status timings**



**Table 12. Truth table**

Conditions	Input	Output	Sense ( $V_{CSD}=0V$ ) <sup>(1)</sup>
Normal operation	L	L	H
	H	H	H
Current limitation	L	L	H
	H	X	H
Over temperature	L	L	H
	H	L	L
Undervoltage	L	L	X
	H	L	X
Output voltage > $V_{OL}$	L	H	L <sup>(2)</sup>
	H	H	H
Output current < $I_{OL}$	L	L	H <sup>(3)</sup>
	H	H	L

1. If the  $V_{CSD}$  is high, the SENSE output is at a high impedance, its potential depends on leakage currents and external circuit.
2. The STATUS pin is low with a delay equal to  $t_{DSTKON}$  after INPUT falling edge.
3. The STATUS pin becomes high with a delay equal to  $t_{POL}$  after INPUT falling edge.

**Figure 5. Switching characteristics**

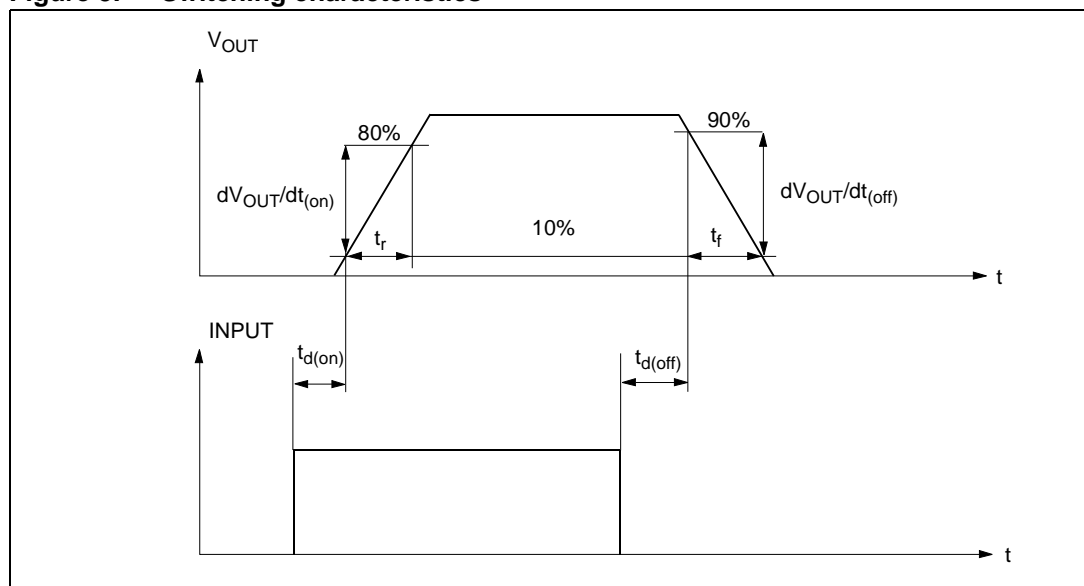


Figure 6. Output voltage drop limitation

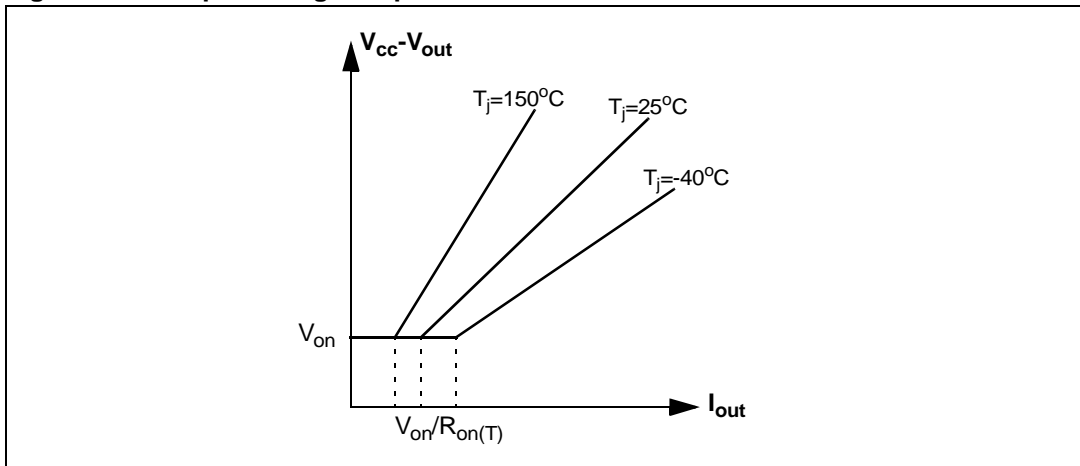


Table 13. Electrical transient requirements (part 1/3)

ISO 7637-2: 2004(E) test pulse	Test levels <sup>(1)</sup>		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and Impedance
	III	IV				
1	-75V	-100V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37V	+50V	5000 pulses	0.2 s	5 s	50 μs, 2 Ω
3a	-100V	-150V	1h	90 ms	100 ms	0.1 μs, 50 Ω
3b	+75V	+100V	1h	90 ms	100 ms	0.1 μs, 50 Ω
4	-6V	-7V	1 pulse			100 ms, 0.01 Ω
5b <sup>(2)</sup>	+65V	+87V	1 pulse			400 ms, 2 Ω

Table 14. Electrical transient requirements (part 2/3)

ISO 7637-2: 2004(E) test pulse	Test level results <sup>(1)</sup>	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b <sup>(2)</sup>	C	C

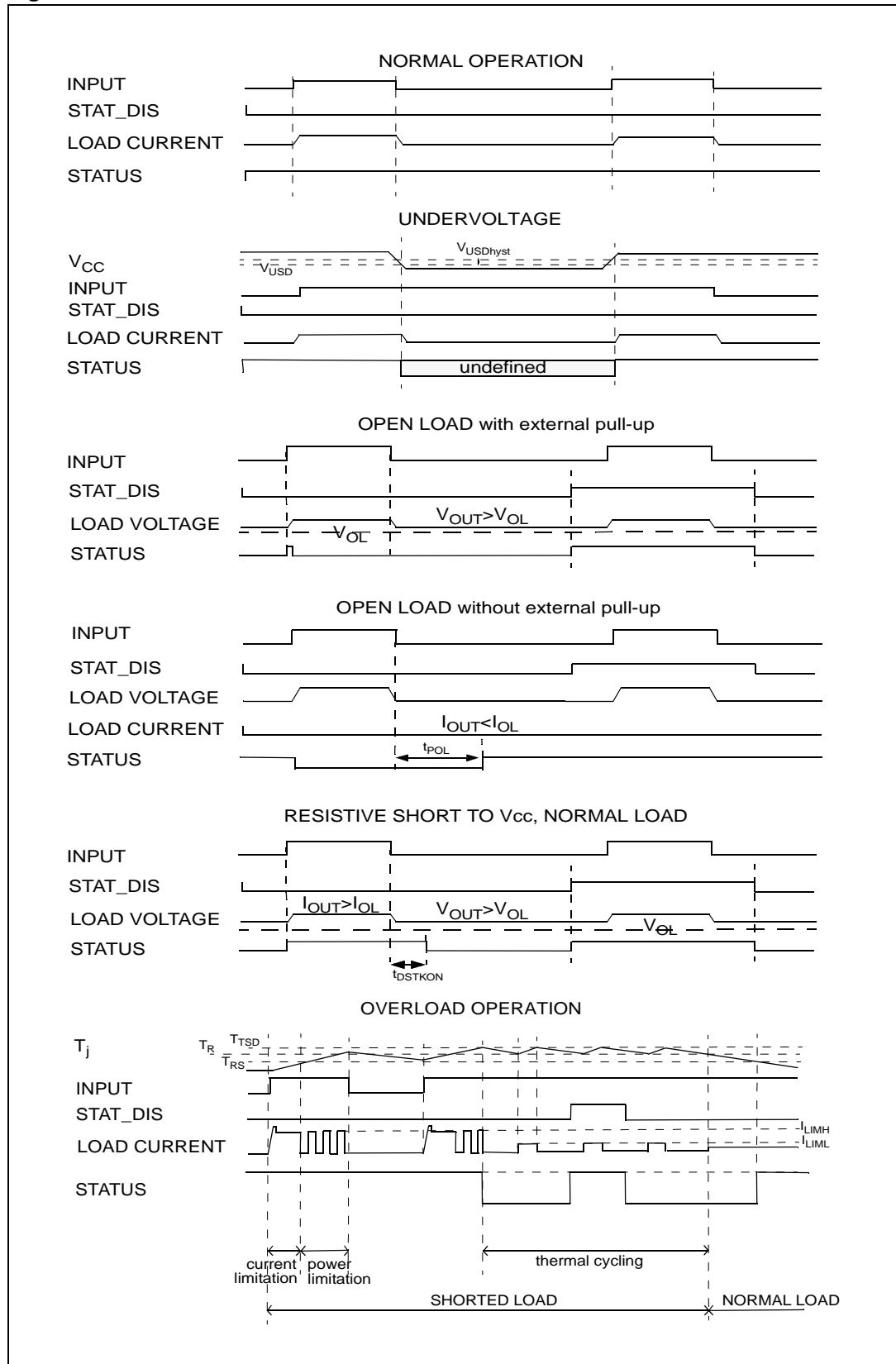
1. The above test levels must be considered referred to  $V_{cc} = 13.5\text{V}$  except for pulse 5b.

2. Valid in case of external load dump clamp: 40V maximum referred to ground.

**Table 15. Electrical transient requirements (part 3/3)**

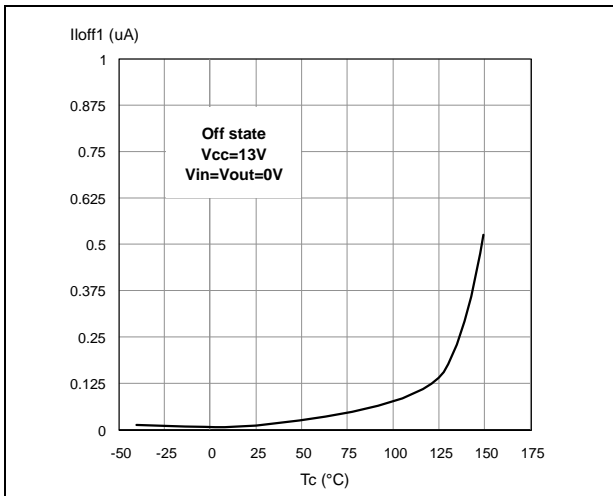
Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the

Figure 7. Waveforms

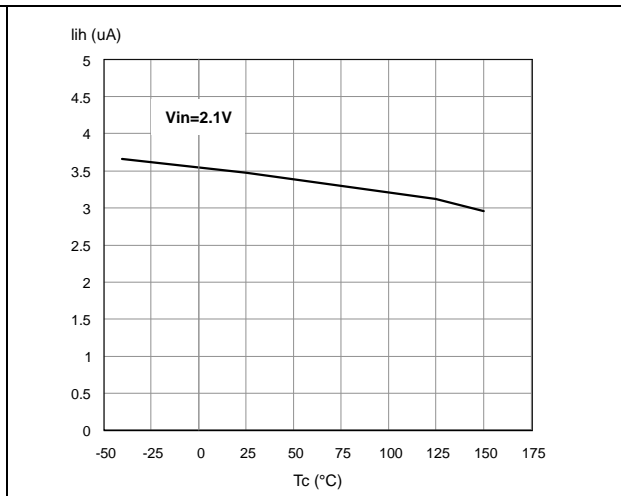


## 2.4 Electrical characteristics curves

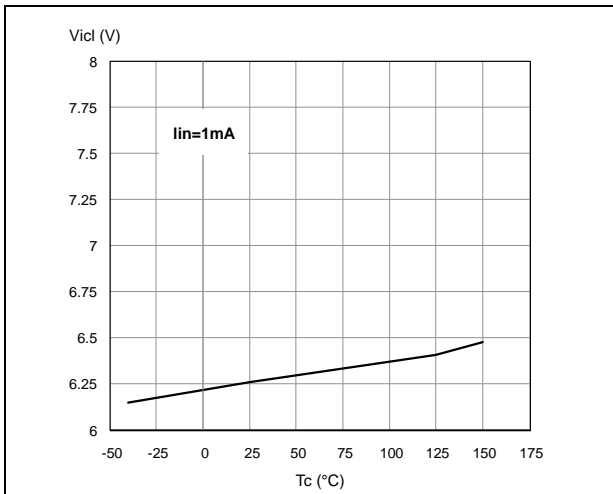
**Figure 8. Off-state output current**



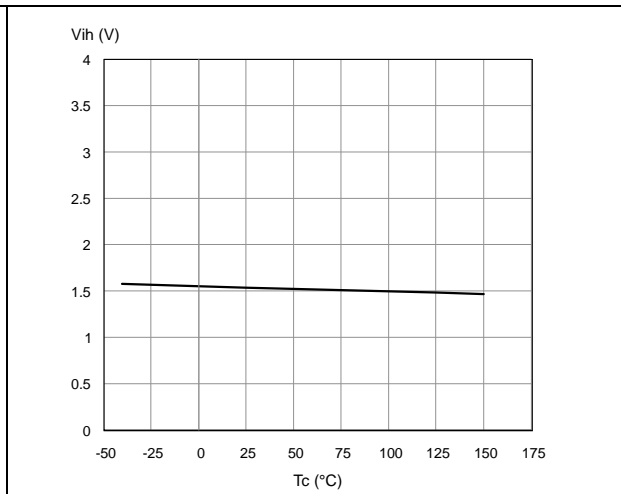
**Figure 9. High level input current**



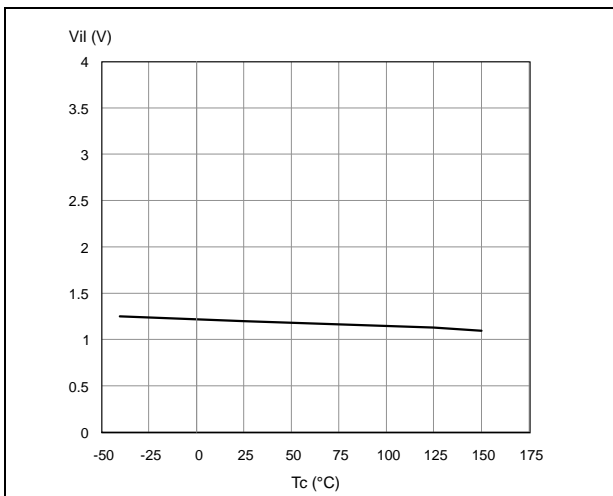
**Figure 10. Input clamp voltage**



**Figure 11. Input high level**



**Figure 12. Input low level**



**Figure 13. Input hysteresis voltage**

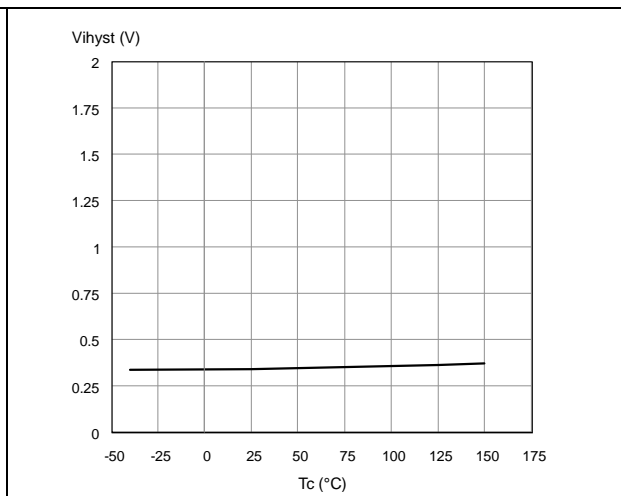




Figure 14. Status low output voltage

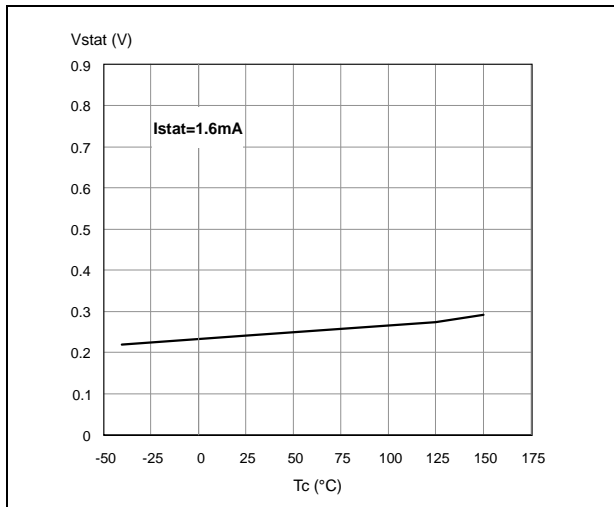


Figure 15. On-state resistance vs T<sub>case</sub>

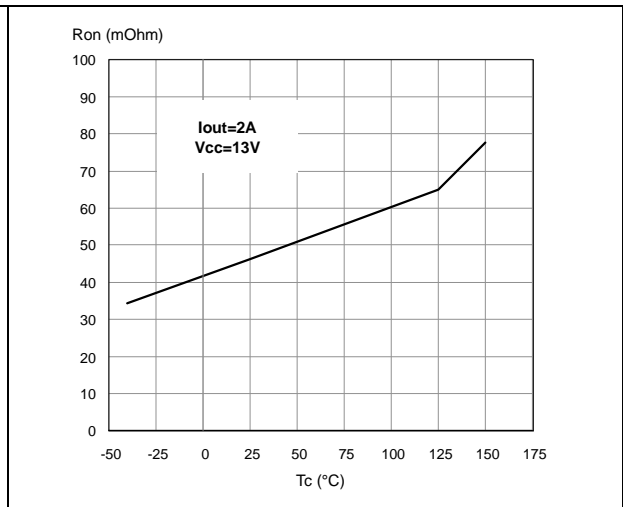


Figure 16. Status leakage current

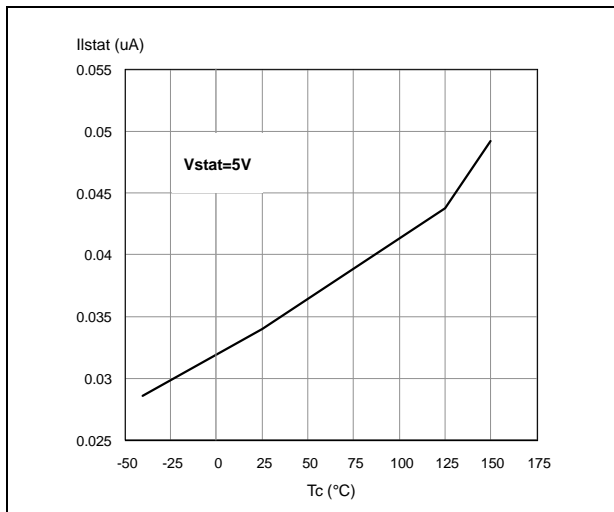


Figure 17. On-state resistance vs V<sub>CC</sub>

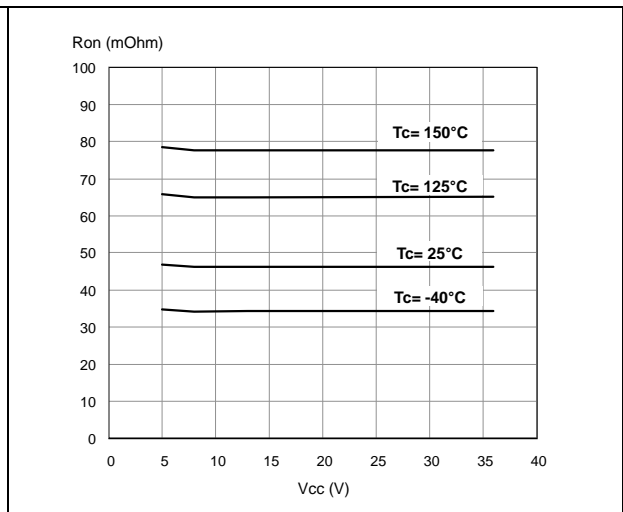


Figure 18. Status clamp voltage

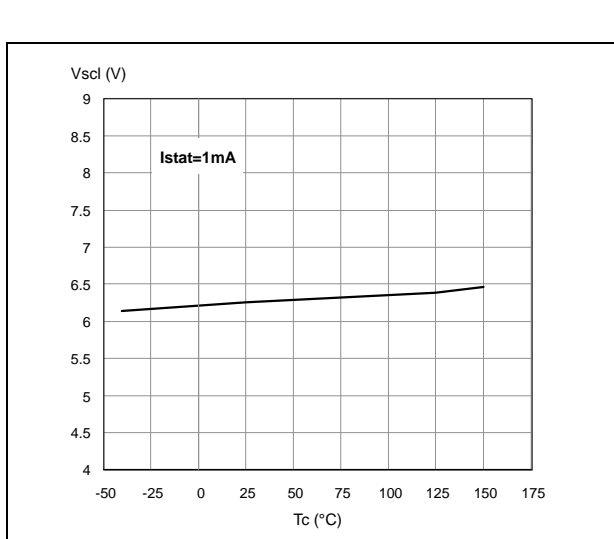
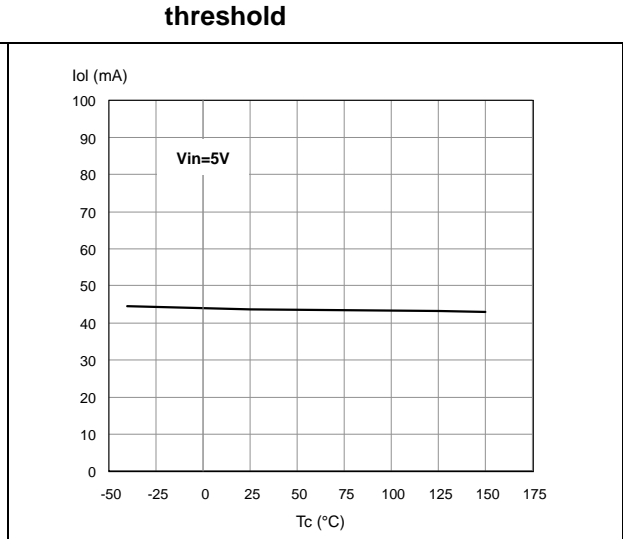
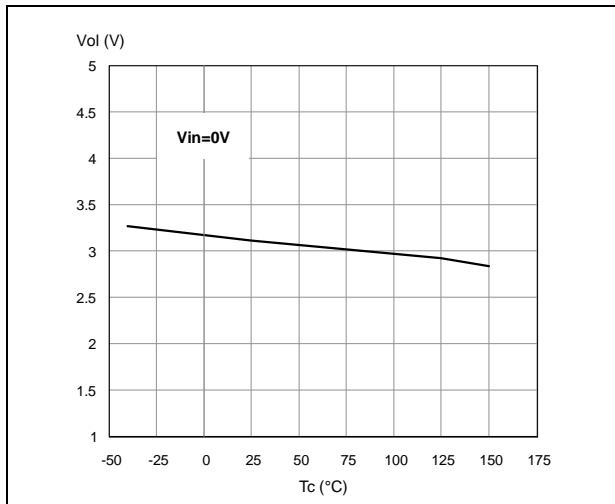


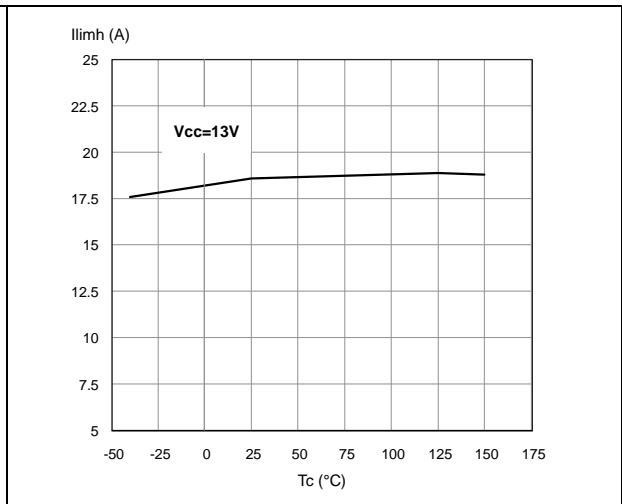
Figure 19. Openload on-state detection threshold



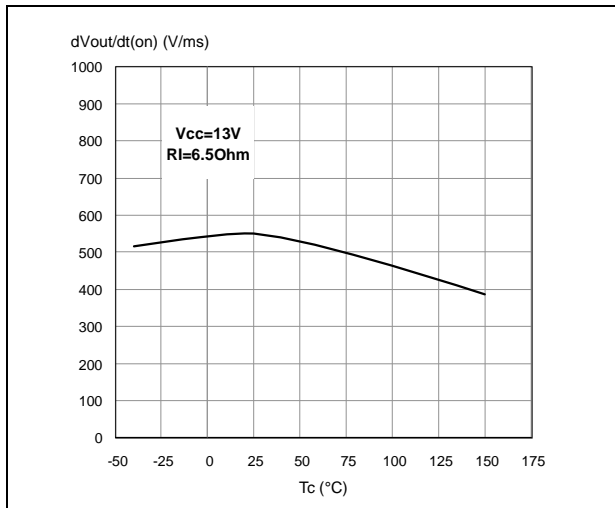
**Figure 20. Openload off-state voltage detection threshold**



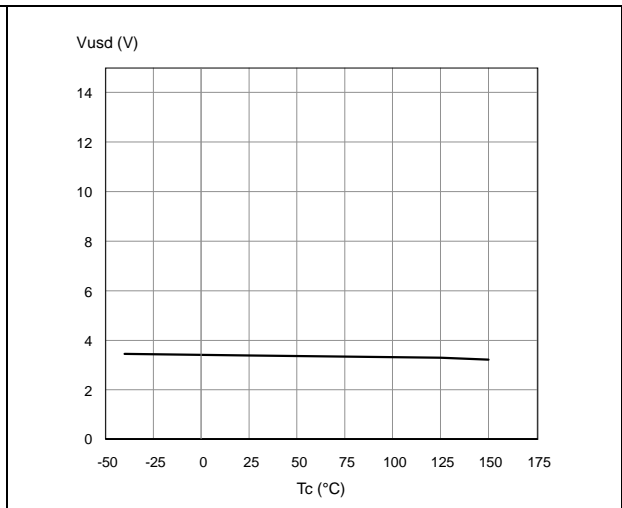
**Figure 21. I<sub>LIM</sub> vs T<sub>case</sub>**



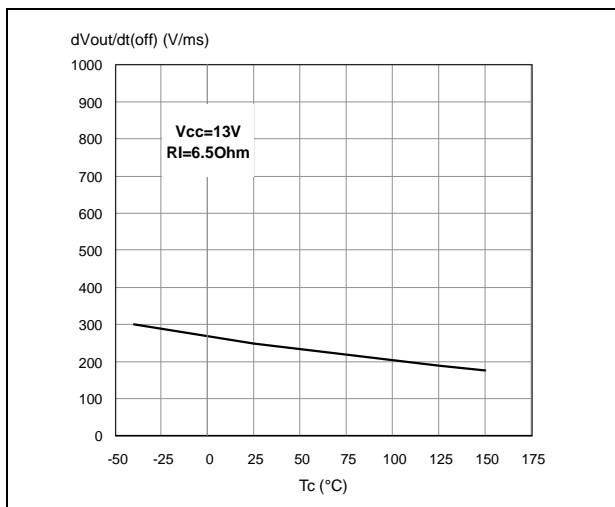
**Figure 22. Turn-on voltage slope**



**Figure 23. Undervoltage shutdown**



**Figure 24. Turn-off voltage slope**



**Figure 25. STAT\_DIS clamp voltage**

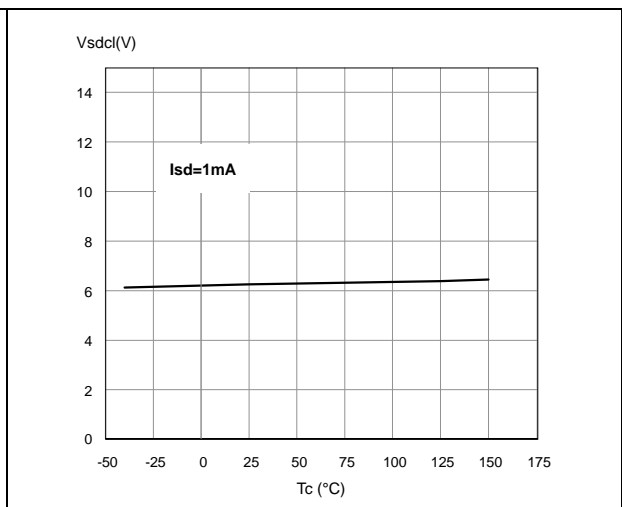


Figure 26. High level STAT\_DIS voltage

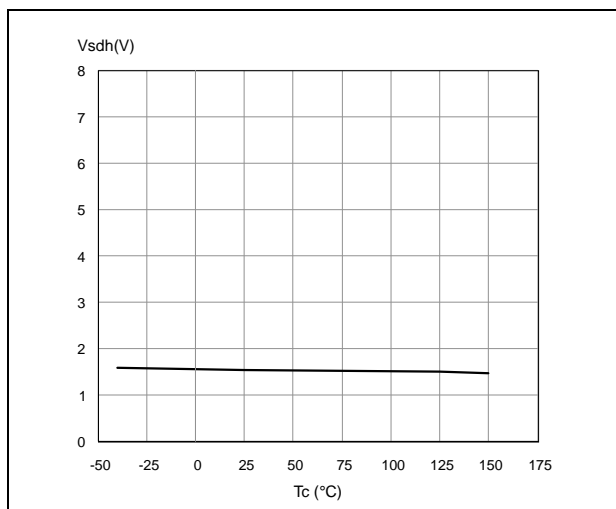
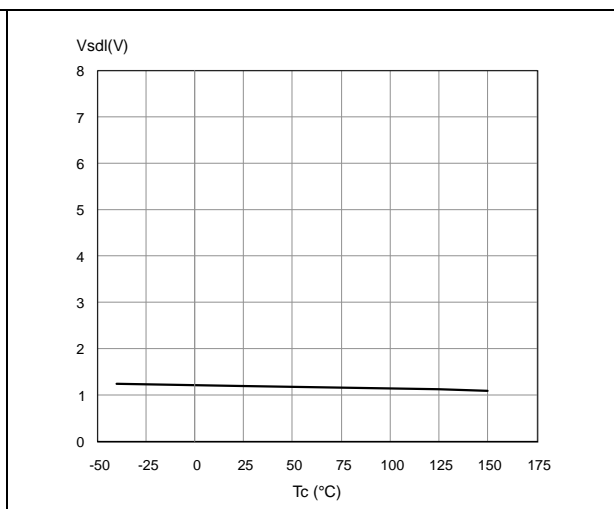
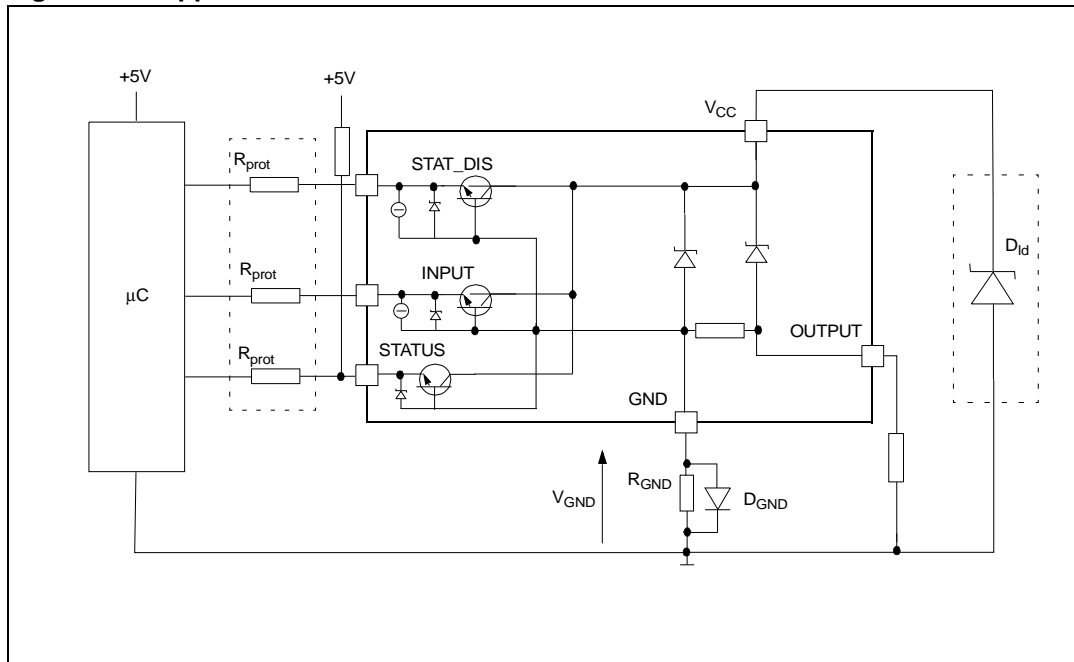


Figure 27. Low level STAT\_DIS voltage



### 3 Application information

Figure 28. Application schematic



Note: Channel 2 has the same internal circuit as channel 1.

### 3.1 GND protection network against reverse battery

#### 3.1.1 Solution 1: resistor in the ground line (R<sub>GND</sub> only)

This can be used with any type of load.

The following is an indication on how to dimension the R<sub>GND</sub> resistor.

1.  $R_{GND} \leq 600\text{mV} / (I_{S(on)max})$ .
2.  $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where  $-I_{GND}$  is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in R<sub>GND</sub> (when  $V_{CC} < 0$ : during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where  $I_{S(on)max}$  becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R<sub>GND</sub> will produce a shift ( $I_{S(on)max} * R_{GND}$ ) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R<sub>GND</sub>.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

### 3.1.2 Solution 2: a diode ( $D_{GND}$ ) in the ground line

A resistor ( $R_{GND}=1k\Omega$ ) should be inserted in parallel to  $D_{GND}$  if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift ( $\approx 600mV$ ) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

## 3.2 Load dump protection

$D_{ld}$  is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the  $V_{CC}$  max DC rating. The same applies if the device is subject to transients on the  $V_{CC}$  line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

## 3.3 Microcontroller I/Os protection

If a ground protection network is used and negative transients are present on the  $V_{CC}$  line, the control pins will be pulled negative. ST suggests to insert a resistor ( $R_{prot}$ ) in line to prevent the  $\mu C$  I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of  $\mu C$  and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of  $\mu C$  I/Os.

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For  $V_{CCpeak} = -100V$  and  $I_{latchup} \geq 20mA$ ;  $V_{OH\mu C} \geq 4.5V$

$$5k\Omega \leq R_{prot} \leq 180k\Omega$$

Recommended values:  $R_{prot} = 10k\Omega$ .

## 3.4 Open-load detection in off-state

Off-state open load detection requires an external pull-up resistor ( $R_{PU}$ ) connected between OUTPUT pin and a positive supply voltage ( $V_{PU}$ ) like the +5V line used to supply the microprocessor.

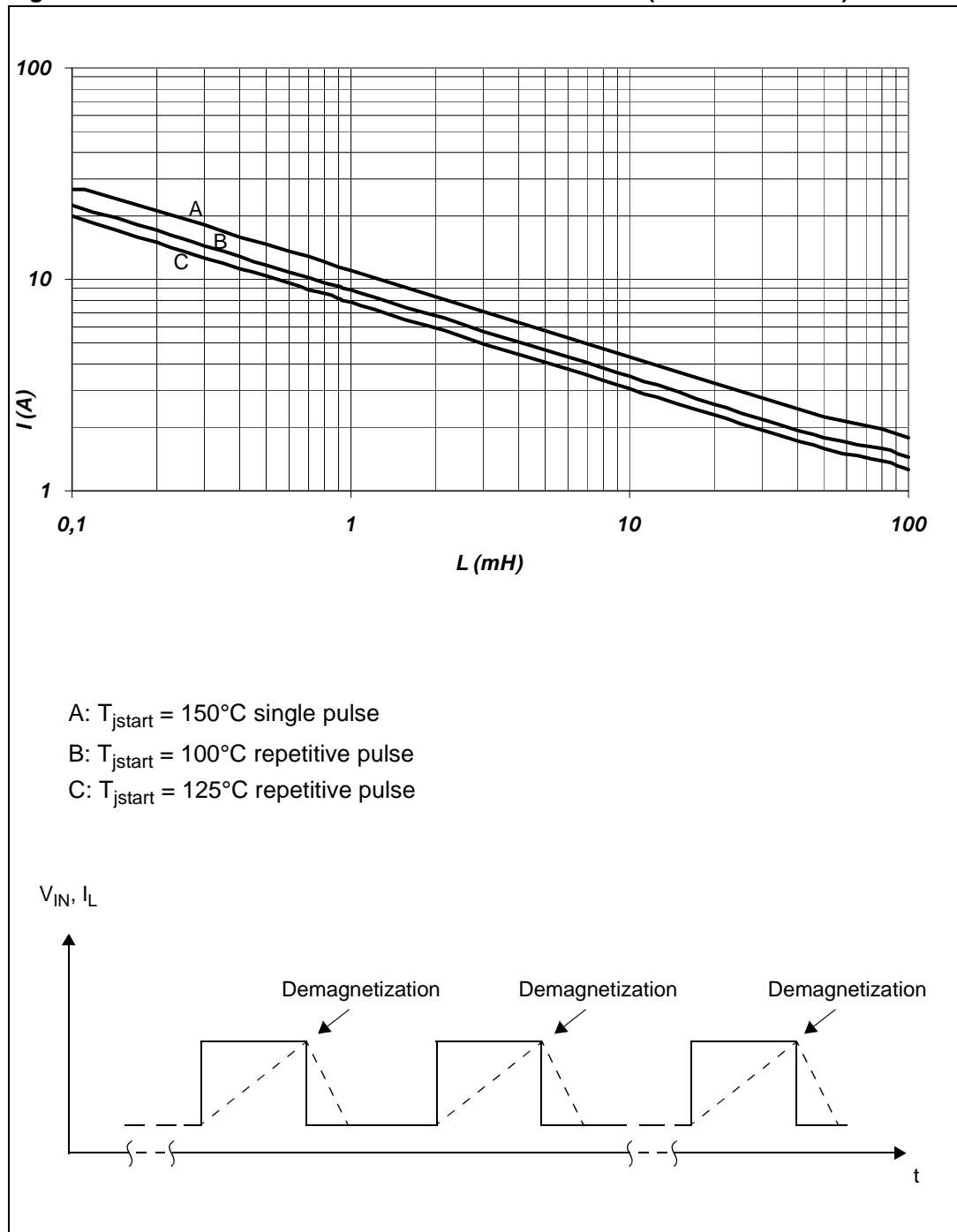
The external resistor has to be selected according to the following requirements:

- no false open load indication when load is connected: in this case we have to avoid  $V_{OUT}$  to be higher than  $V_{OLmin}$ ; this results in the following condition  $V_{OUT} = (V_{PU} / (R_L + R_{PU})) R_L < V_{OLmin}$ .
- no misdetection when load is disconnected: in this case the  $V_{OUT}$  has to be higher than  $V_{OLmax}$ ; this results in the following condition  $R_{PU} < (V_{PU} - V_{OLmax}) / I_{L(off2)}$ .



### 3.5 Maximum demagnetization energy ( $V_{CC} = 13.5V$ )

Figure 30. Maximum turn-off current versus inductance (for each channel)

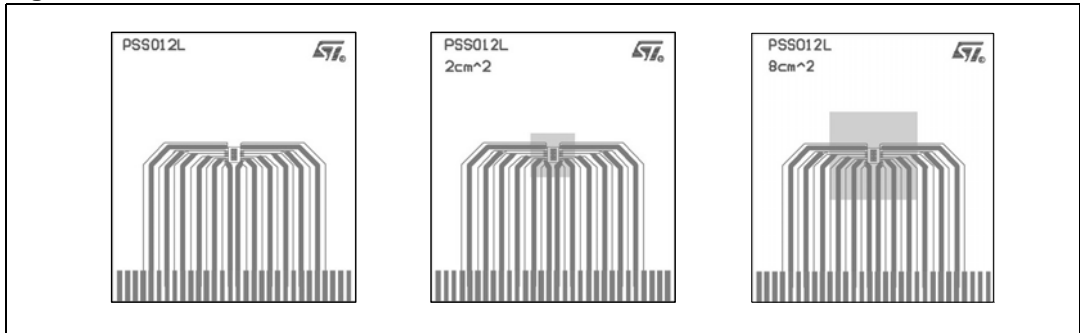


Note: Values are generated with  $R_L = 0\Omega$ . In case of repetitive pulses,  $T_{jstart}$  (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

## 4 Package and PCB thermal data

### 4.1 PowerSSO-12™ thermal data

Figure 31. PowerSSO-12™ PC board



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB: Double layer, Thermal Vias, FR4 area= 77mm x 86mm, PCB thickness=1.6mm, Cu thickness=70 $\mu$ m (front and back side), Copper areas: from minimum pad lay-out to 8cm<sup>2</sup>).

Figure 32.  $R_{thj-amb}$  vs PCB copper area in open box free air condition (one channel on)

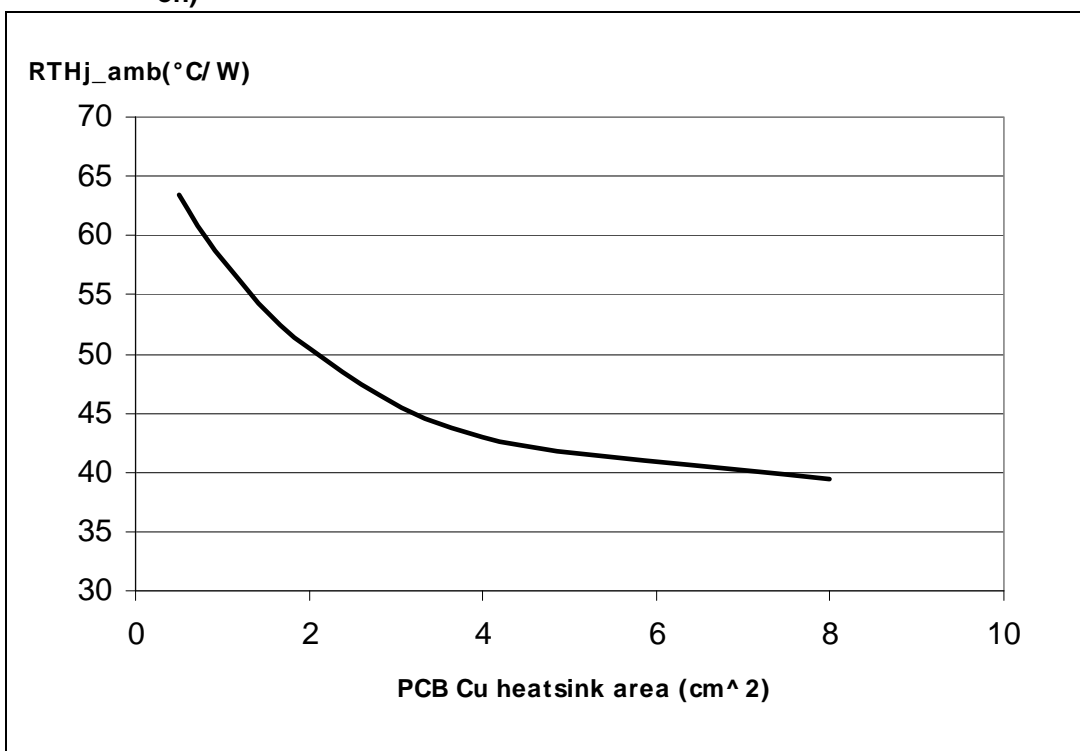
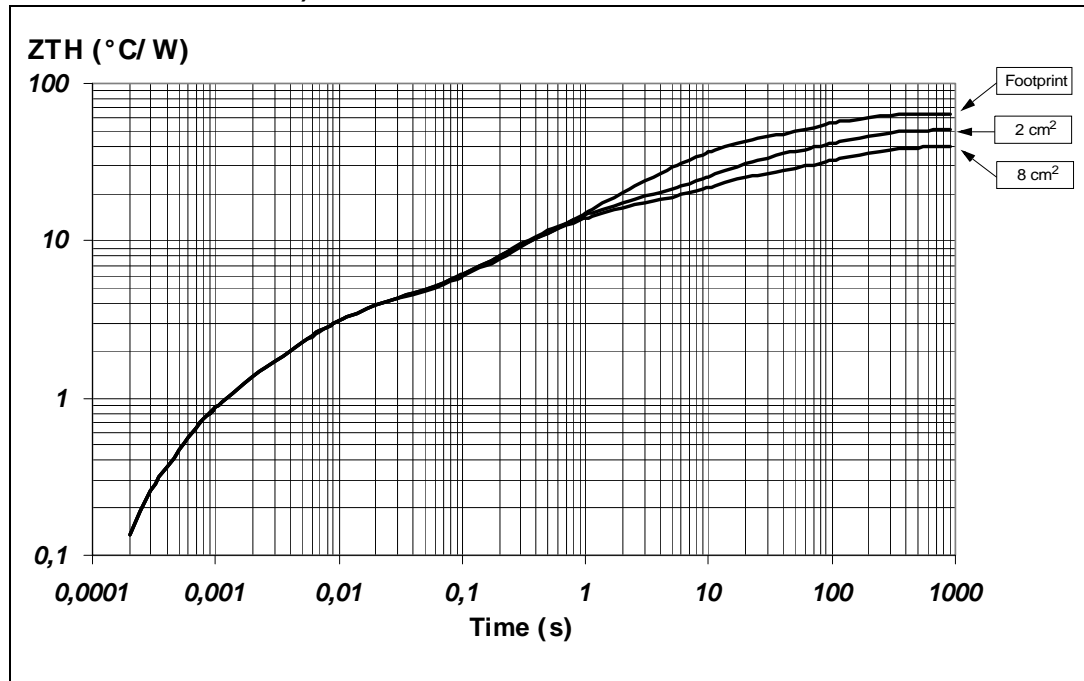




Figure 33. PowerSSO-12™ thermal impedance junction ambient single pulse (one channel on)

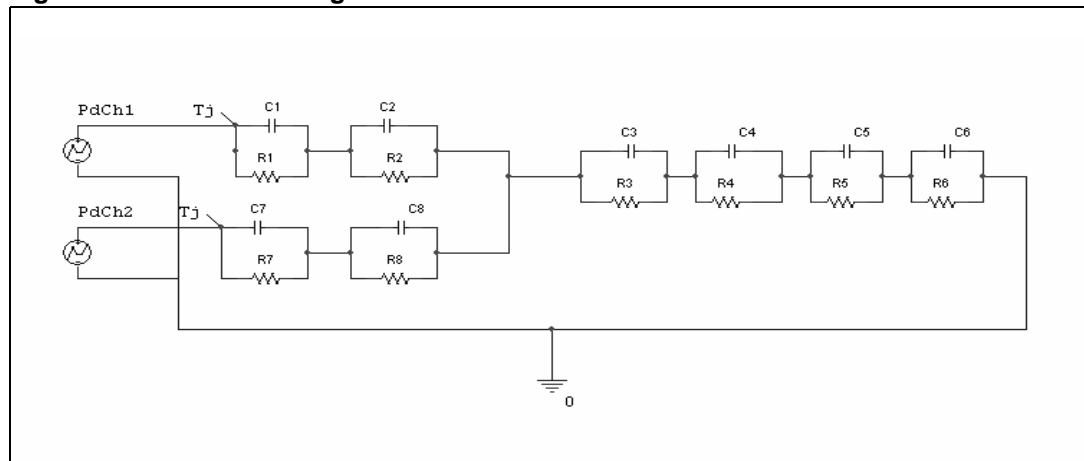


Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Figure 34. Thermal fitting model of a double channel HSD in PowerSSO-12™(a)



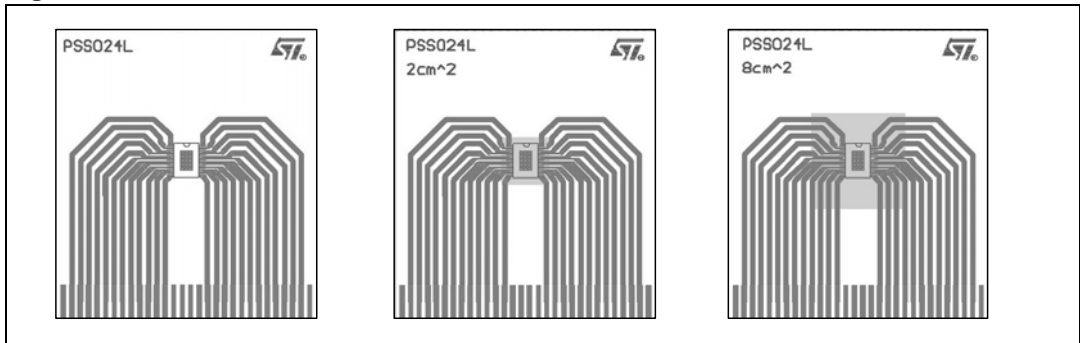
a. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 16. PowerSSO-12™ thermal parameters

Area/island (cm <sup>2</sup> )	Footprint	2	8
R1= R7 (°C/W)	0.7		
R2= R8 (°C/W)	2.8		
R3 (°C/W)	4		
R4 (°C/W)	8	8	7
R5 (°C/W)	22	15	10
R6 (°C/W)	26	20	15
C1= C7 (W.s/°C)	0.001		
C2= C8 (W.s/°C)	0.0025		
C3 (W.s/°C)	0.05		
C4 (W.s/°C)	0.2	0.1	0.1
C5 (W.s/°C)	0.27	0.8	1
C6 (W.s/°C)	3	6	9

## 4.2 PowerSSO-24™ thermal data

Figure 35. PowerSSO-24™ PC board



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB: Double layer, Thermal Vias, FR4 area= 77mm x 86mm, PCB thickness=1.6mm, Cu thickness=70μm (front and back side), Copper areas: from minimum pad lay-out to 8cm<sup>2</sup>).

Figure 36.  $R_{thj-amb}$  vs PCB copper area in open box free air condition (one channel on)

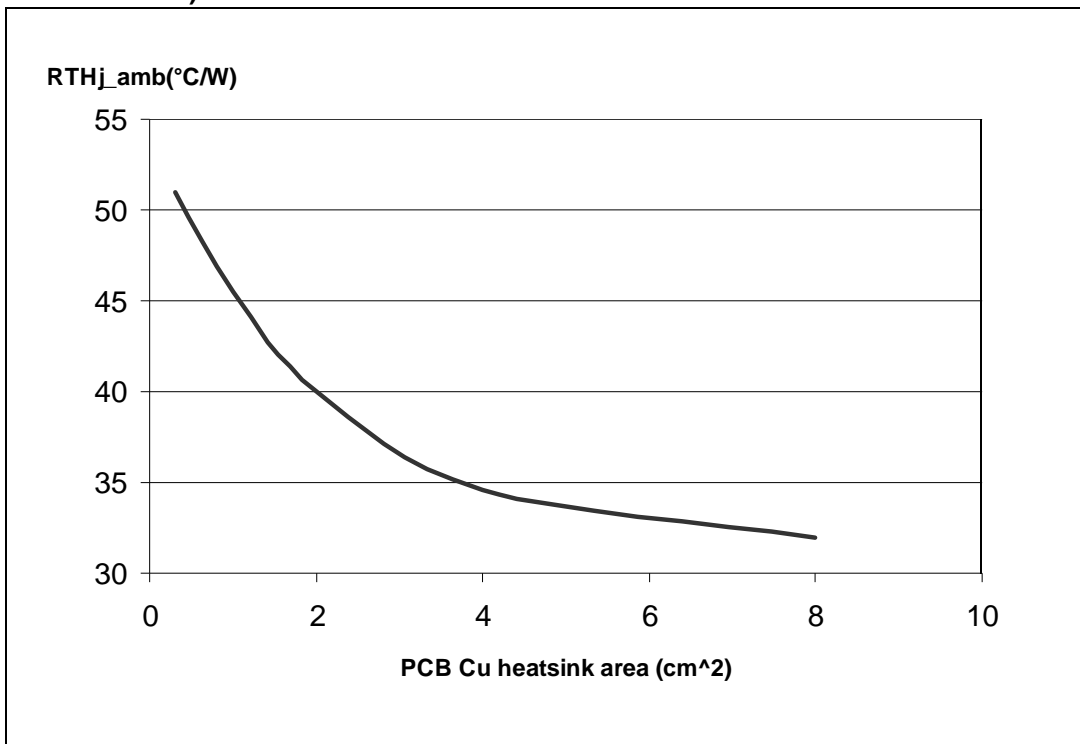
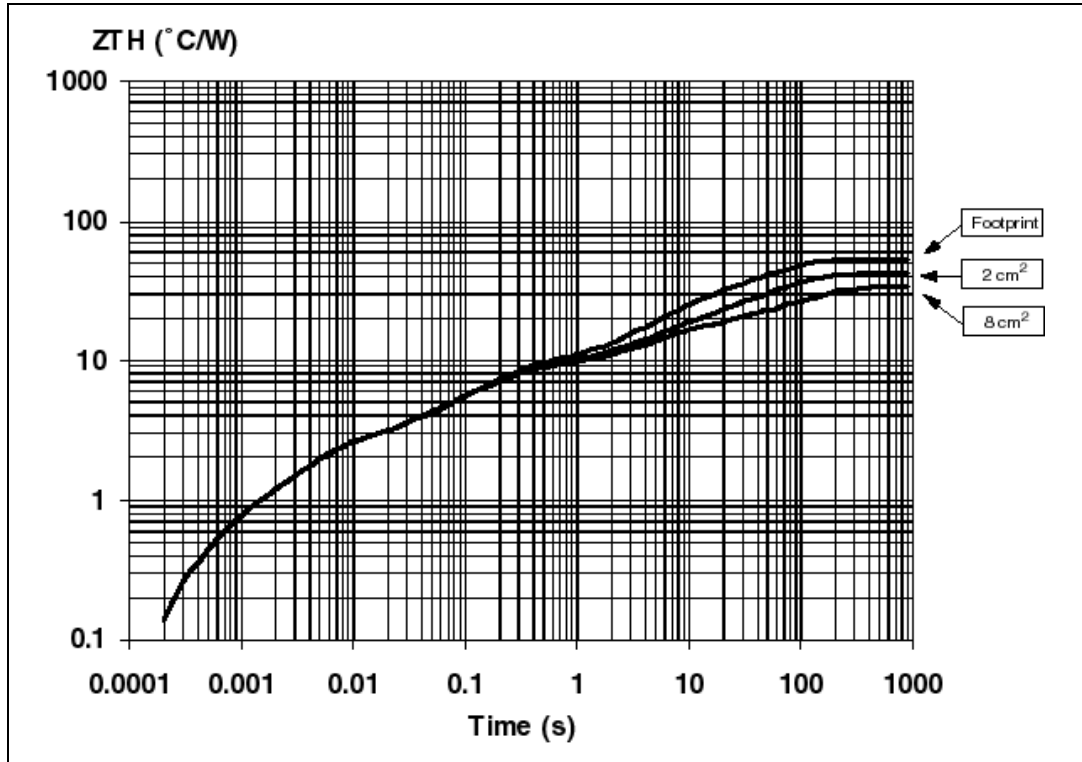


Figure 37. PowerSSO-24™ thermal impedance junction ambient single pulse (one channel on)

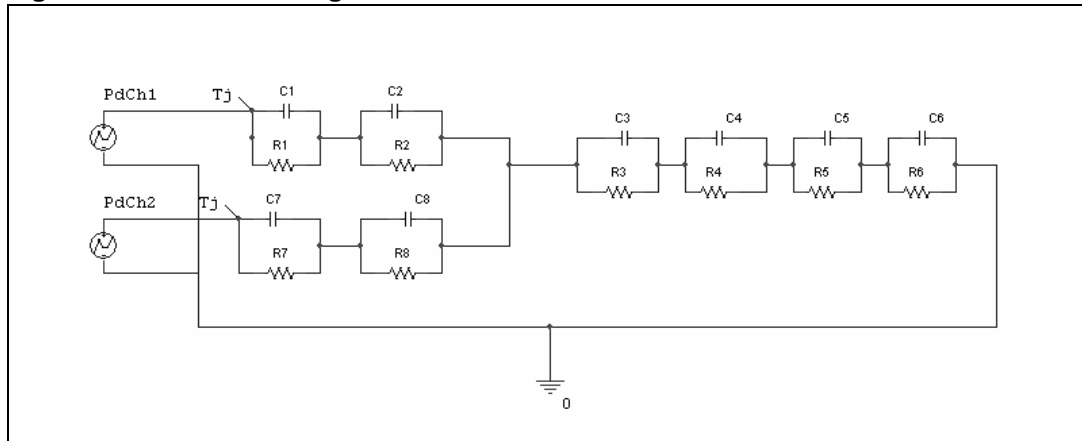


Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Figure 38. Thermal fitting model of a double channel HSD in PowerSSO-24™(b)



b. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 17. PowerSSO-24™ thermal parameters

Area/island (cm <sup>2</sup> )	Footprint	2	8
R1=R7 (°C/W)	0.4		
R2=R8 (°C/W)	2		
R3 (°C/W)	6		
R4 (°C/W)	7.7		
R5 (°C/W)	9	9	8
R6 (°C/W)	28	17	10
C1=C7 (W.s/°C)	0.001		
C2=C8 (W.s/°C)	0.0022		
C3 (W.s/°C)	0.025		
C4 (W.s/°C)	0.75		
C5 (W.s/°C)	1	4	9
C6 (W.s/°C)	2.2	5	17

## 5 Package and packing information

### 5.1 ECOPACK<sup>®</sup> packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com).

ECOPACK<sup>®</sup> is an ST trademark.

### 5.2 PowerSSO-12<sup>™</sup> package information

Figure 39. PowerSSO-12<sup>™</sup> package dimensions

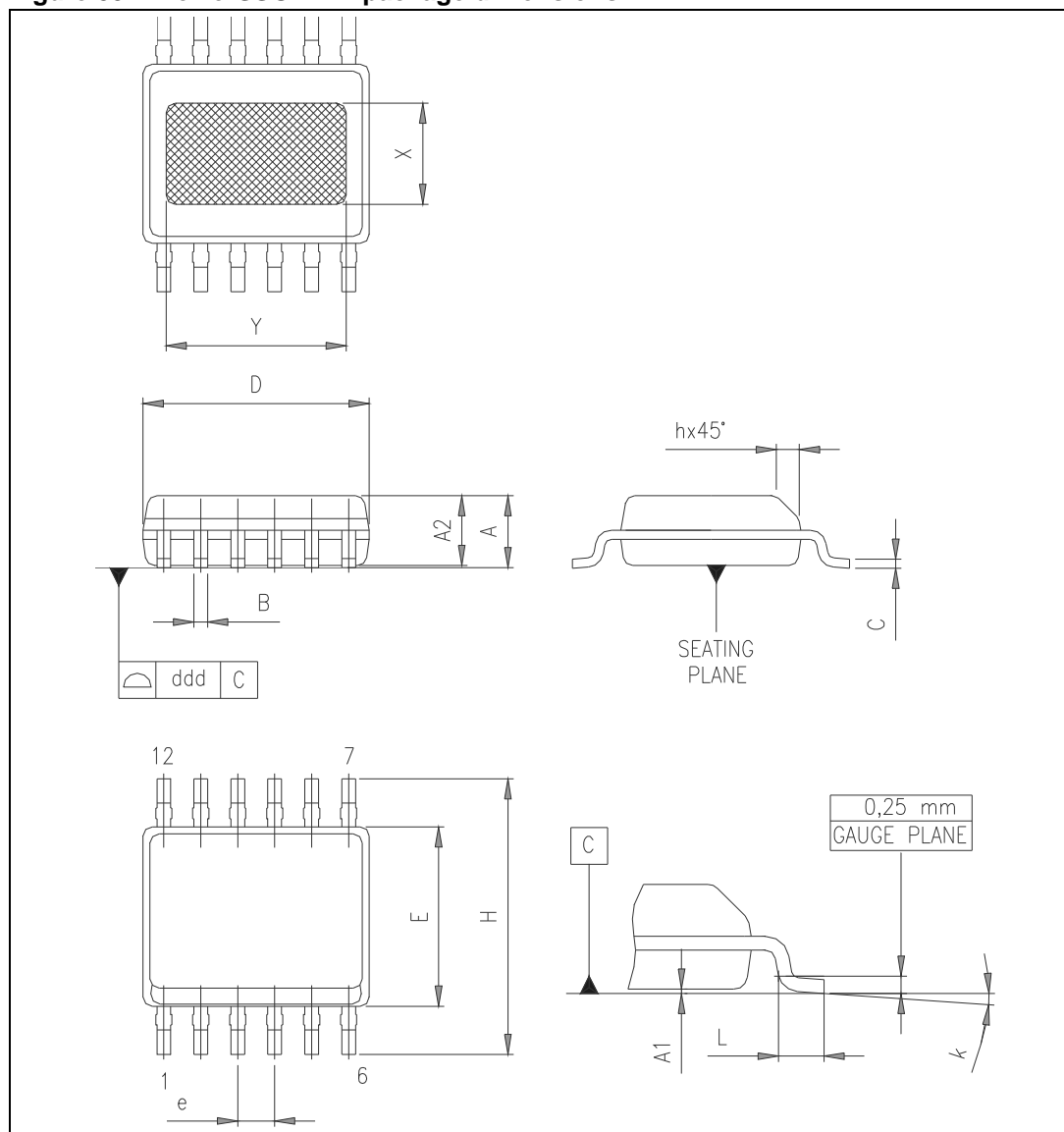


Table 18. PowerSSO-12™ mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	1.25		1.62
A1	0		0.1
A2	1.10		1.65
B	0.23		0.41
C	0.19		0.25
D	4.8		5.0
E	3.8		4.0
e		0.8	
H	5.8		6.2
h	0.25		0.5
L	0.4		1.27
k	0°		8°
X	1.9		2.5
Y	3.6		4.2
ddd			0.1

### 5.3 PowerSSO-24™ package information

Figure 40. PowerSSO-24™ package dimensions

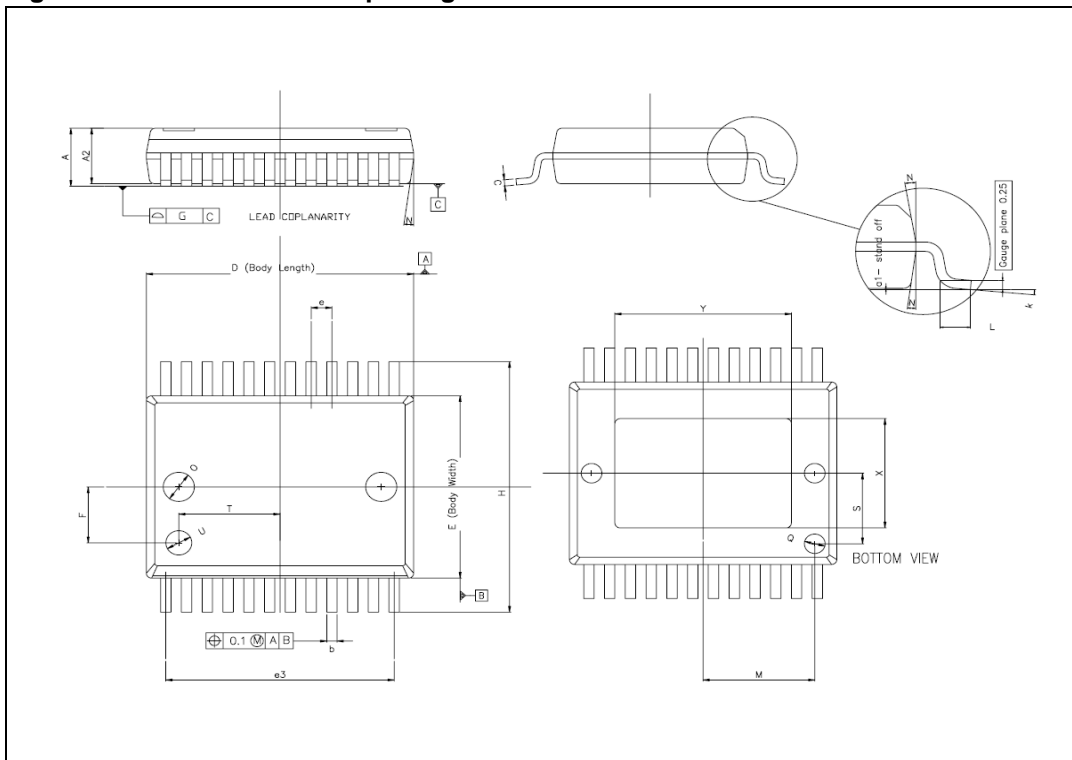


Table 19. PowerSSO-24™ mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A			2.45
A2	2.15		2.35
a1	0		0.1
b	0.33		0.51
c	0.23		0.32
D	10.10		10.50
E	7.4		7.6
e		0.8	
e3		8.8	
F		2.3	
G			0.1
H	10.1		10.5



Table 19. PowerSSO-24™ mechanical data (continued)

Symbol	Millimeters		
	Min.	Typ.	Max.
h			0.4
k	0deg		8deg
L	0.55		0.85
O		1.2	
Q		0.8	
S		2.9	
T		3.65	
U		1.0	
N			10deg
X	4.1		4.7
Y	6.5		7.1

### 5.4 PowerSSO-12™ packing information

Figure 41. PowerSSO-12™ tube shipment (no suffix)

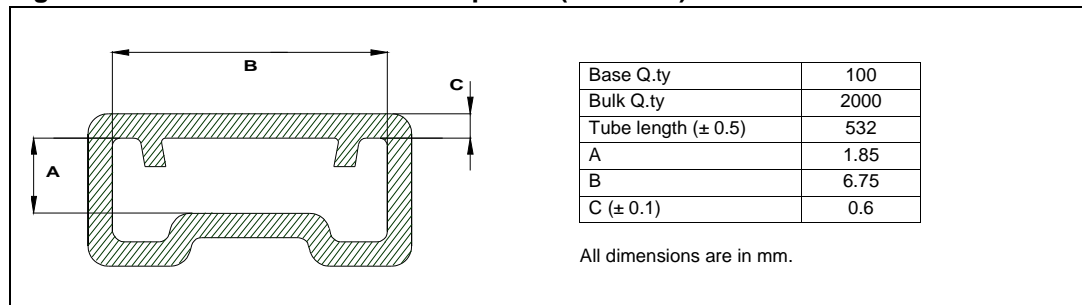
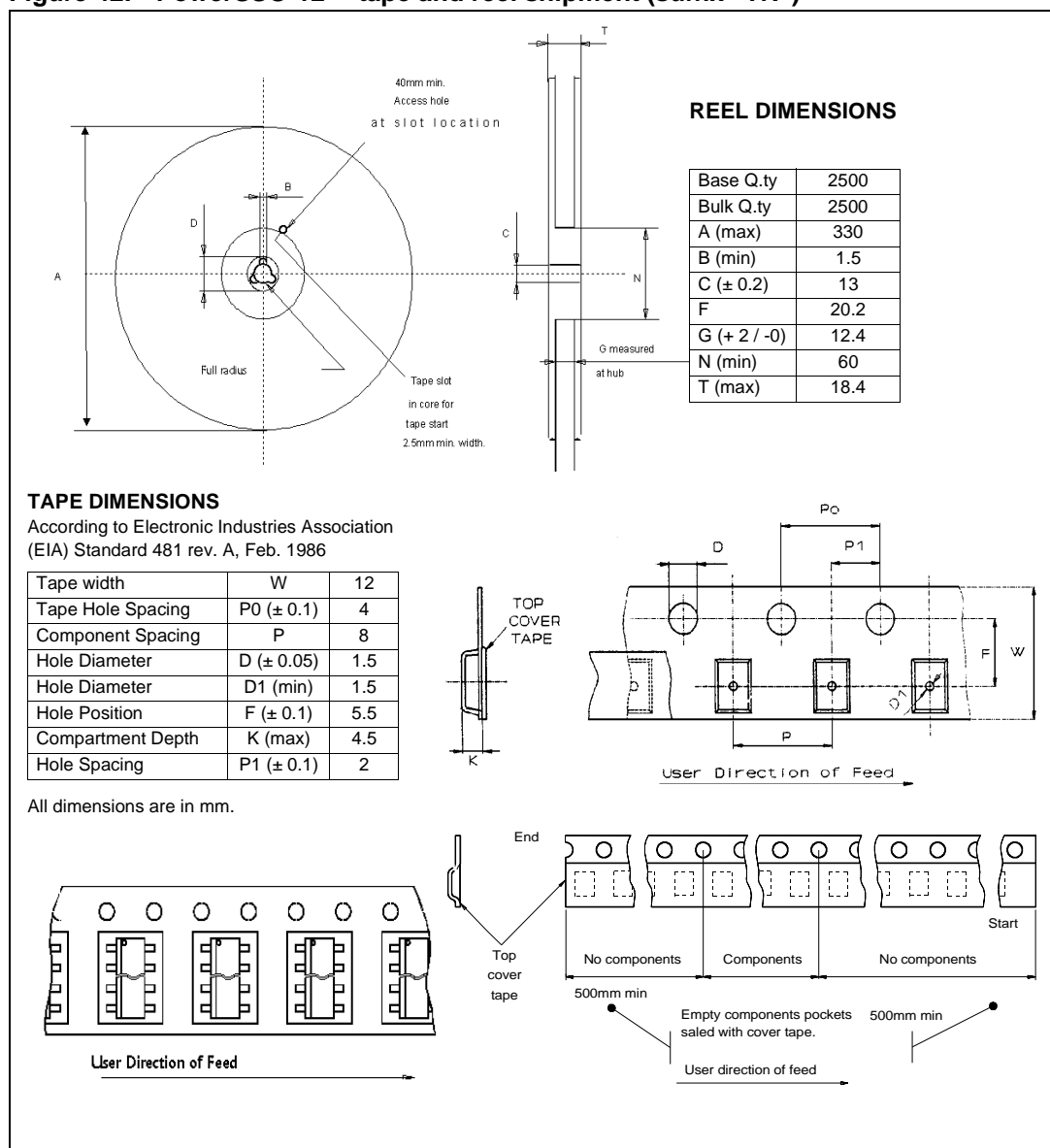


Figure 42. PowerSSO-12™ tape and reel shipment (suffix “TR”)



### 5.5 PowerSSO-24™ packing information

Figure 43. PowerSSO-24™ tube shipment (no suffix)

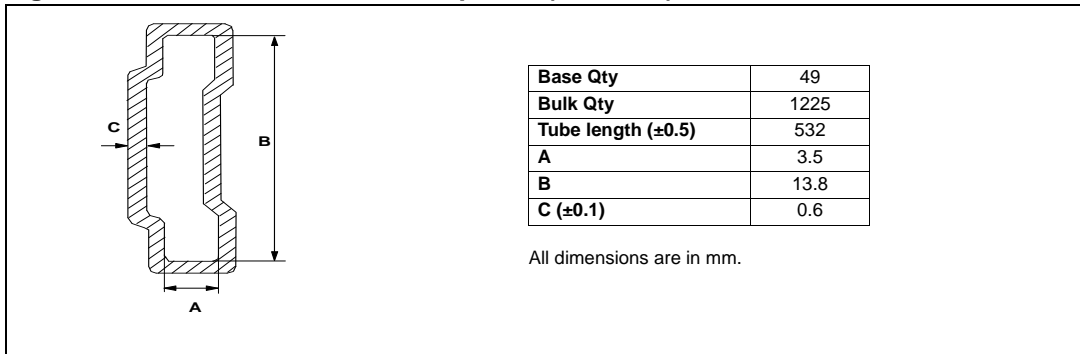
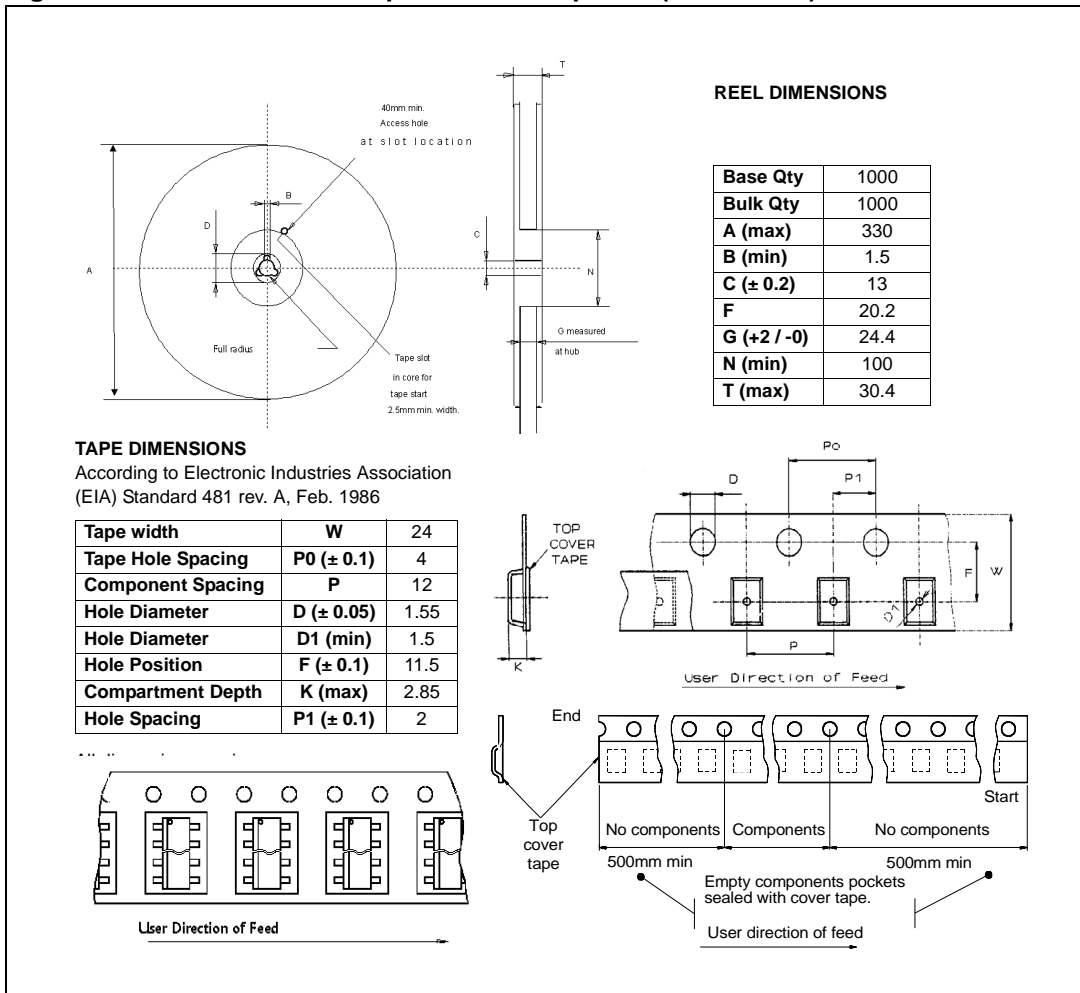


Figure 44. PowerSSO-24™ tape and reel shipment (suffix “TR”)



## 6 Revision history

**Table 20. Document revision history**

Date	Revision	Changes
30-Mar-2006	1	Initial release.
11-Jan-2007	2	Minor formatting changes. New disclaimer attached.
31-May-2007	3	Reformatted and restructured. Contents and lists of tables and figures added. <i>Section 3.5: Maximum demagnetization energy (VCC = 13.5V)</i> added. <i>Table 4: Absolute maximum ratings:</i> E <sub>MAX</sub> entries updated. <i>Table 13: Electrical transient requirements (part 1/3):</i> Test level values III and IV for test pulse 5b and notes updated <i>Figure 34: Thermal fitting model of a double channel HSD in PowerSSO-12™, Figure 38: Thermal fitting model of a double channel HSD in PowerSSO-24™:</i> added notes. Features table updated: I <sub>LIMH</sub> changed from 19 to 18A.
03-Dec-2007	4	Updated <i>Section 4.1: PowerSSO-12™ thermal data:</i> – Changed <i>Figure 32: R<sub>thj-amb</sub> vs PCB copper area in open box free air condition (one channel on).</i> – Changed <i>Figure 33: PowerSSO-12™ thermal impedance junction ambient single pulse (one channel on).</i> – Updated <i>Table 16: PowerSSO-12™ thermal parameters:</i> R3 value changed from 7 to 4 °C/W. R4 values changed from 10 /10 /10 to 8 /8 /7 °C/W.
17-Jun-2009	5	<i>Table 19: PowerSSO-24™ mechanical data:</i> – Deleted A (min) value – Changed A (max) value from 2.47 to 2.45 – Changed A2 (max) value from 2.40 to 2.35 – Changed a1 (max) value from 0.075 to 0.1 – Added F and k rows
22-Jul-2009	6	Updated <i>Figure 40: PowerSSO-24™ package dimensions.</i> Updated <i>Table 19: PowerSSO-24™ mechanical data:</i> – Deleted G1 row – Added O, Q, S, T and U rows.
23-Sep-2013	7	Updated Disclaimer.

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