FAN6248HC/HD/LC/LD

Advanced Synchronous Rectifier Controller for LLC Resonant Converter

The FAN6248 is an advanced synchronous rectifier (SR) controller that is optimized for LLC resonant converter topology with minimum external components. It has two driver stages for driving the SR MOSFETs which are rectifying the outputs of the secondary transformer windings. The two gate driver stages have their own sensing inputs and operate independently of each other. The adaptive parasitic inductance compensation function minimizes the body diode conduction maximizing the efficiency. The advanced control algorithm allows stable SR operation over entire load range. According to the operating frequency and turn-off threshold voltage, FAN6248 has four different versions − FAN6248HCMX, FAN6248HDMX, FAN6248LCMX, FAN6248LDMX.

Features

- Highly Integrated Self-contained Control of Synchronous Rectifier with a Minimum External Component Count
- Optimized for LLC Resonant Converter
- Anti Shoot-through Control for Reliable SR Operation
- Separate 100 V Rated Sense Inputs for Sensing the Drain and Source Voltage of each SR MOSFET
- Adaptive Parasitic Inductance Compensation to Minimize the Body Diode Conduction
- SR Current Inversion Detection under Light Load Condition
- Light Load Detection to Increase Dead Time Target
- Adaptive Minimum on Time for Noise Immunity
- Operating Voltage Range up to 30 V
- Low Start-up and Stand-by Current Consumption
- Operating Frequency Range from 25 kHz up to 700 kHz
- SOIC−8 Package
- High Driver Output Voltage of 10.5 V to Drive All MOSFET Brands to the Lowest R_{DS_ON}
- Low Operating Current in Green Mode (typ. 350 μA)
- These Devices are Pb−Free, Halogen Free and are RoHS Compliant

Applications

- High Power Density Laptop Adapter
- High Power Density Adapter
- Large Screen LCD−TV, PDP−TV, RP−TV Power
- High-efficiency Desktop and Server Power Supplies
- Networking and Telecom Power Supplies
- High Power LED Lighting

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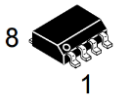
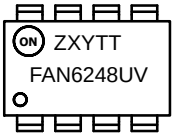


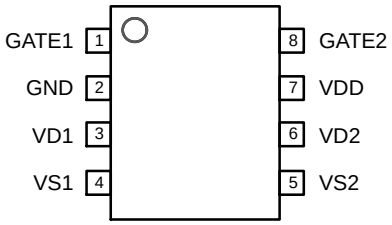
SOIC−8
CASE 751EB

MARKING DIAGRAM



U	= Frequency, H: High, L: Low
V	= V_{TH_OFF} Level, C or D
Z	= Assembly Plant Code
X	= Year Code
Y	= Two Week Code
TT	= Die Run Code

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

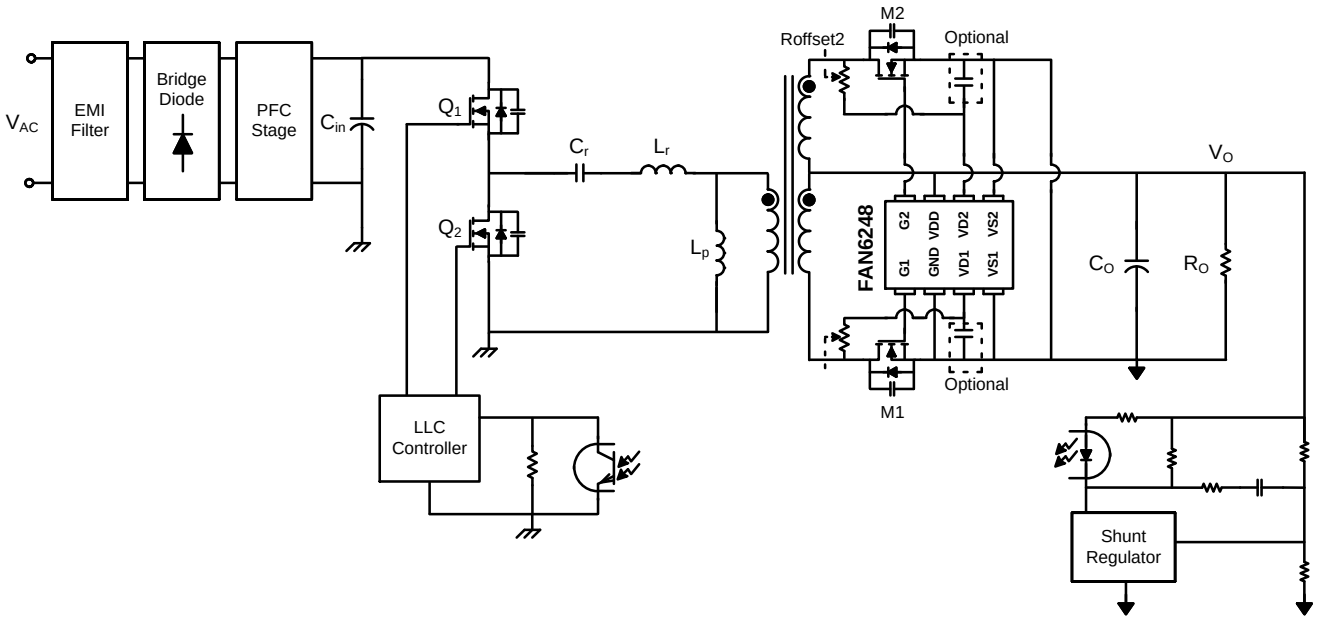


Figure 1. Typical Application Schematic of FAN6248

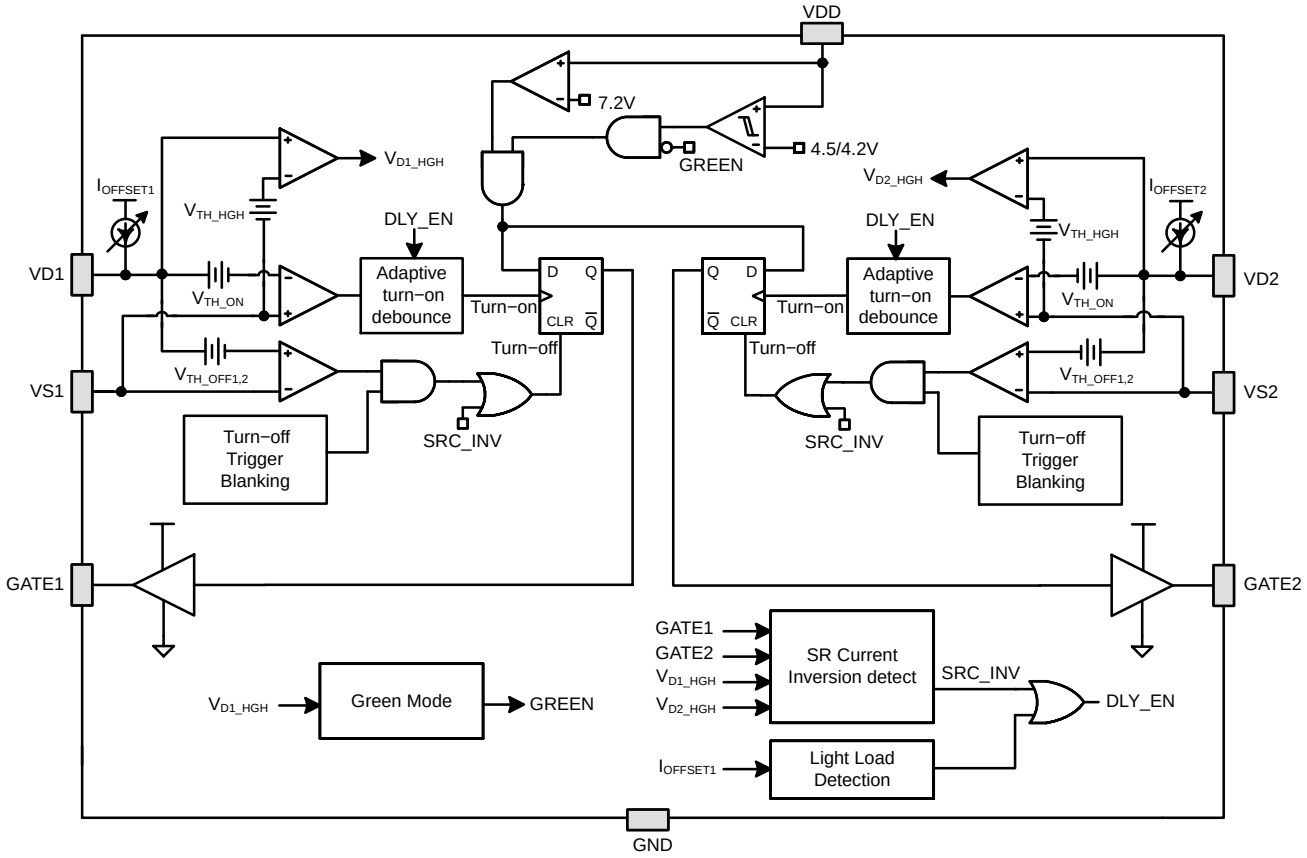


Figure 2. Internal Block Diagram of FAN6248

PIN DESCRIPTION

Pin Number	Pin Name	Description
1	GATE1	Gate drive output for SR1
2	GND	Ground
3	VD1	Synchronous rectifier drain sense input. A $I_{OFFSET1}$ current source flows out of the DRAIN pin such that an external series resistor can be used to adjust the synchronous rectifier turn-off threshold. The $I_{OFFSET1}$ current source is turned off when V_{DD} is under-voltage or when switching is disabled in green mode
4	VS1	Synchronous rectifier source sense input for SR1
5	VS2	Synchronous rectifier source sense input for SR2
6	VD2	Synchronous rectifier drain sense input. A $I_{OFFSET2}$ current source flows out of the DRAIN pin such that an external series resistor can be used to adjust the synchronous rectifier turn-off threshold. The $I_{OFFSET2}$ current source is turned off when V_{DD} is under-voltage or when switching is disabled in green mode
7	VDD	Supply Voltage
8	GATE2	Gate drive output for SR2

ORDERING AND SHIPPING INFORMATION

Ordering Code	Device Marking	V_{TH_OFF1} / V_{TH_OFF2}	Package	Shipping†
FAN6248HCMX	FAN6248HC	25 mV / 50 mV	SOIC−8	2500 / Tape & Reel
FAN6248HDMX	FAN6248HD	0 mV / 25 mV	SOIC−8	2500 / Tape & Reel
FAN6248LCMX	FAN6248LC	25 mV / 50 mV	SOIC−8	2500 / Tape & Reel
FAN6248LDMX	FAN6248LD	0 mV / 25 mV	SOIC−8	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{DD}	Power Supply Input Pin Voltage		−0.3	30	V
V_{D1}, V_{D2}	Drain Sense Input Pin Voltage		−1	100	V
V_{GATE1}, V_{GATE2}	Gate Drive Output Pin Voltage		−0.3	30	V
V_{S1}, V_{S2}	Source Sense Input Pin Voltage		−0.4	0.4	V
P_D	Power Dissipation (T_A = 25°C)			0.625	W
Θ_{JA}	Thermal Resistance (Junction-to-Ambient Thermal)			165	°C/W
T_J	Operating Junction Temperature		−40	150	°C
T_{STG}	Storage Temperature Range		−60	150	°C
T_L	Lead Temperature (Soldering) 10 Seconds			260	°C
ESD	Electrostatic Discharge Capability	Human Body Model, ANSI / ESDA / JEDEC JS−001−2012		4	kV
		Charged Device Model, JESD22−C101		1.75	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. All voltage values are with respect to the GND pin.

THERMAL CHARACTERISTICS

Symbol	Rating	Value	Unit
$R_{\psi JT}$	Thermal Characteristics	22	°C/W
$R_{\theta JA}$	Thermal Characteristics	165	°C/W

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{DD}	VDD Pin Supply Voltage to GND (Note 2)	0	27	V
V_{D1} ,V_{D2}	Drain Sense Input Pin Voltage	−0.7	100	V
V_{S1} V_{S2}	Source Sense Input Pin Voltage	−0.4	0.4	V
T_A	Operating Ambient Temperature (Note 3)	−40	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

2. Allowable operating supply voltage V_{DD} can be limited by the power dissipation of FAN6248 related to switching frequency, load capacitance and ambient temperature.
3. Allowable operating ambient temperature can be limited by the power dissipation of FAN6248 related to switching frequency, load capacitance on GATE pin and V_{DD}.

ELECTRICAL CHARACTERISTICS (V_{DD} = 12 V and T_J = −40°C to +125°C unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
INPUT VOLTAGE						
V_{DD_ON}	Turn-On Threshold	V_{DD} rising	4.2	4.5	4.7	V
V_{DD_OFF}	Turn-Off Threshold	V_{DD} falling	4.0	4.2	4.4	
$V_{DD\_GATE\_ON}$*	SR Gate Enable Threshold Voltage	V_{DD} rising		7.2		V
I_{DD_OP}	Operating Current	f_{SW} = 100 kHz, C_{GATE} = 3.3 nF	7	8.5	10	mA
$I_{DD\_SRARTUP}$		$V_{DD} = V_{DD\_ON} - 0.1$ V			200	μA
I_{DD_GREEN}	Operating Current in Green Mode	V_{DD} = 12 V (no switching)		350	500	μA
DRAIN VOLTAGE SENSING SECTION ($V_{D1} = V_{D2}$)						
V_{OSI}*	Comparator Input Offset Voltage		−1	0	1	mV
I_{OFFSET}*	$I_{OFFSET1}$ and $I_{OFFSET2}$	Maximum of adaptive offset current (15 steps, 9 μA resolution) $I_{OFFSET}=I_{OFFSET\_STEP15}$	112.5	135	157.5	μA
V_{TH_ON}	Turn-On Threshold	R_{DRAIN} = 0 Ω (includes comparator input offset voltage)	−290	−240	−190	mV
t_{ON_DLY}*	Turn on delay for de-bounce time when turn-on delay mode is disabled by detecting normal SR current	From V_{D1} falling below V_{TH_ON} to V_{GATE} rising above V_{G_HG} (With 50 mV overdrive), C_{GATE} = 0 nF		80		ns
$t_{ON\_DLY2\_H}$*	Turn on delay for de-bounce time when turn-on delay mode is enabled by detecting SR current inversion for HC and HD version	From V_{D1} falling below V_{TH_ON} to V_{GATE} rising above V_{G_HG} (With 50 mV overdrive), C_{GATE} = 0 nF		850		ns
$t_{ON\_DLY2\_L}$*	Turn on delay for de-bounce time when turn-on delay mode is enabled by detecting SR current inversion for LC and LD version	From V_{D1} falling below V_{TH_ON} to V_{GATE} rising above V_{G_HG} (With 50 mV overdrive), C_{GATE} = 0 nF		1100		ns
$V_{TH\_OFF1\_C}$*	First Level Turn-Off Threshold for HC and LC version	R_{DRAIN} = 0 Ω (includes comparator input offset voltage)		25		mV
$V_{TH\_OFF2\_C}$*	Second Level Turn-Off Threshold for HC and LC version	R_{DRAIN} = 0 Ω (includes comparator input offset voltage)		50		mV
$V_{TH\_OFF1\_D}$*	First Level Turn-Off Threshold for HD and LD version	R_{DRAIN} = 0 Ω (includes comparator input offset voltage)		0		mV
$V_{TH\_OFF2\_D}$*	Second Level Turn-Off Threshold for HD and LD version	R_{DRAIN} = 0 Ω (includes comparator input offset voltage)		25		mV
t_{OFF_DLY}*	Comparator Delay of V_{TH_OFF1}	From V_{D1} rising above V_{TH_OFF} to V_{GATE} falling below V_{G_LW} (With 10 mV overdrive), C_{GATE} = 0 nF		50		ns
V_{TH_HGH}	Drain Voltage High Detect Threshold	V_{D1} Rising	0.80	1	1.20	V
$t_{DB\_HGH\_H}$*	V_{TH_HGH} Detection Blanking Time for HC and HD version	From V_{D1} falling below V_{TH_ON}		540		ns
$t_{DB\_HGH\_L}$*	V_{TH_HGH} Detection Blanking Time for LC and LD version	From V_{D1} falling below V_{TH_ON}		1		μs
V_{OFF_FORCE}*	Forced Turn-off Threshold	$V_{D1} > V_{OFF\_FORCE} = V_{TH\_HGH\_EN}$		1		V
MINIMUM ON-TIME AND MAXIMUM ON-TIME						
K_{TON}*	Adaptive Minimum On Time Ratio	Ratio between t_{ON_MIN} and SR conduction time of previous switching cycle		25		%
$t_{ON\_MIN\_LH}$*	Minimum On-Time Lower Limit for HC and HD version	$t_{ON\_MIN\_LH} < t_{ON\_MIN} < t_{ON\_MIN\_UH}$		200		ns
$t_{ON\_MIN\_UH}$	Minimum On-Time Upper Limit for HC and HD version		0.96	1.2	1.44	μs

ELECTRICAL CHARACTERISTICS (V_{DD} = 12 V and T_J = −40°C to +125°C unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
MINIMUM ON-TIME AND MAXIMUM ON-TIME						
$t_{ON\_MIN\_LL}$*	Minimum On-Time Lower Limit for LC and LD version	$t_{ON\_MIN\_LL} < t_{ON\_MIN} < t_{ON\_MIN\_UL}$		0.4		μs
$t_{ON\_MIN\_UL}$	Minimum On-Time Upper Limit for LD and LD version		3.2	4	4.8	μs
$t_{SR\_CNDT\_H}$	Minimum SR Conduction Time to enable SR for HC and HD version	The duration from turn-on trigger to V_{DS} rising above V_{TH_HGH}	380	600	820	ns
$t_{SR\_CNDT\_L}$	Minimum SR Conduction Time to enable SR for LC and LD version	The duration from turn-on trigger to V_{DS} rising above V_{TH_HGH}	0.85	1.2	1.65	μs
$t_{SR\_MAX\_H}$*	Maximum SR Turn-on Time for HC and HD version			15		μs
$t_{SR\_MAX\_L}$*	Maximum SR Turn-on Time for LC and LD version			30		μs
REGULATED DEAD TIME						
t_{DEAD_H}*	Dead time regulation target for HC and HD version	From V_{GATE} falling below V_{G_LW} to V_{DS} rising above V_{TH_HGH}		280		ns
$t_{DEAD\_H\_LIGHT}$*	Dead time regulation target under light load condition for HC and HD version	From V_{GATE} falling below V_{G_LW} to V_{DS} rising above V_{TH_HGH}		320		ns
t_{DEAD_L}*	Dead time regulation target for LC and LD version	From V_{GATE} falling below V_{G_LW} to V_{DS} rising above V_{TH_HGH}		320		ns
$t_{DEAD\_L\_LIGHT}$*	Dead time regulation target under light load condition for LC and LD version	From V_{GATE} falling below V_{G_LW} to V_{DS} rising above V_{TH_HGH}		360		ns
t_{TSDT}*	Too small dead time threshold to speed up I_{OFFSET} change (Speed up 2 times)	From V_{GATE} falling below V_{G_LW} to V_{DS} rising above V_{TH_HGH}		50		ns
K_{INV}*	Adaptive SR current inversion detection time Ratio between T_{INV} and SR conduction time of previous switching cycle	$V_{GATE} > V_{G\_HG}$ and $V_{DS} > V_{TH\_OFF}$ $K_{INV} = 0.25 \times K_{TON}$		6.25		%
η_{INV_EXT}*	Normal switching cycles without capacitive current spike to exit SR current inversion detection state which has t_{ON_DLY2}			31		cycle
GREEN MODE CONTROL						
$t_{GRN\_ENT\_H}$	Non-Switching Period to Enter Green Mode for HC and HD version	Non switching cycles between burst switching bundles	60	80	100	μs
$t_{GRN\_ENT\_L}$	Non-Switching Period to Enter Green Mode for LC and LD version	Non switching cycles between burst switching bundles	120	160	200	μs
$t_{GRN\_ENT\_DBNC\_H}$	De-bounce time to Enter Green Mode for HC and HD version	De-bounce time after $t_{GRN.ENT\_H}$	130	180	230	μs
$t_{GRN\_ENT\_DBNC\_L}$	De-bounce time to Enter Green Mode for LC and LD version	De-bounce time after $t_{GRN\_ENT\_L}$	240	320	400	μs
$t_{GRN\_EXT\_H}$	Non-Switching Period to Exit Green for HC and HD version	Non switching cycles between burst switching bundles	30	40	50	μs
$t_{GRN\_EXT\_L}$	Non-Switching Period to Exit Green Mode for LC and LD version	Non switching cycles between burst switching bundles	60	80	100	μs
η_{CSW_EXT}	Continuous switching cycles to exit Green Mode for HC, HD, LC and LD version		4	7	10	cycle

ELECTRICAL CHARACTERISTICS (V_{DD} = 12 V and T_J = −40°C to +125°C unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
GREEN MODE CONTROL						
$t_{S\_NORMAL\_H}$	Switching period to be recognized as normal switching for HC and HD version		13	20	27	μs
$t_{S\_NORMAL\_L}$	Switching period to be recognized as normal switching for LC and LD version		27	40	53	μs
OUTPUT DRIVER SECTION						
V_{GATE_MAX}	Gate Clamping Voltage	12 V < V_{DD} < 25 V	9	10.5	12	V
V_{OL}	Output Voltage Low	V_{DD} = 12 V, V_{D1} = V_{D2} = 2 V, I_{GATE} = 50 mA			1.5	V
V_{OH}	Output Voltage High	V_{DD} = 12 V, I_{GATE} = −50 mA	7			V
I_{SOURCE}*	Peak Source Current for Turning On	V_{DD} = 12 V, V_{GATE} = 2 V		0.7		A
I_{SINK}*	Peak Sink Current for Turning Off	V_{DD} = 12 V, V_{GATE} = 7 V		1.4		A
t_R*	Rise Time	V_{DD} = 12 V, C_L = 3.3 nF, V_{GATE} = 2 V → 7 V		50		ns
t_F*	Fall Time	V_{DD} = 12 V, C_L = 3.3 nF, V_{GATE} = 7 V → 2 V		30		ns
V_{G_LW}*	Gate voltage considered as turned off for adaptive dead time control	Gate falling		4		V
V_{G_HG}*	Gate voltage considered as turned on for adaptive dead time control	Gate rising		6		V
SWITCHING FREQUENCY						
f_{MAX}*	Maximum Switching Frequency		700			kHz
f_{MIN}*	Minimum Switching Frequency				25	kHz

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
*Not tested but guaranteed by design

KEY DIFFERENT PARAMETERS FOR FAN6248 OPTIONS

Item	FAN6248HC	FAN6248HD	FAN6248LC	FAN6248LD
t_{ON_DLY2}	850 ns	850 ns	1100 ns	1100 ns
t_{DB_HGH}	540 ns	540 ns	1 μs	1 μs
$t_{ON\_MIN\_L}$	200 ns	200 ns	400 ns	400 ns
$t_{ON\_MIN\_U}$	1.2 μs	1.2 μs	4 μs	4 μs
t_{SR_CNDT}	0.6 μs	0.6 μs	1.2 μs	1.2 μs
t_{SR_MAX}	15 μs	15 μs	30 μs	30 μs
t_{DEAD}	280 ns	280 ns	320 ns	320 ns
t_{DEAD_LIGHT}	320 ns	320 ns	360 ns	360 ns
t_{GRN_ENT}	80 μs	80 μs	160 μs	160 μs
t_{GRN_EXT}	40 μs	40 μs	80 μs	80 μs
t_{S_NORMAL}	20 μs	20 μs	40 μs	40 μs

TYPICAL CHARACTERISTICS

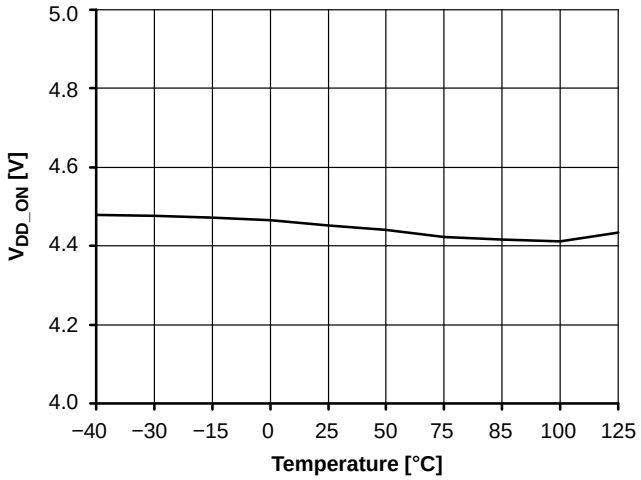


Figure 3. V_{DD_ON}

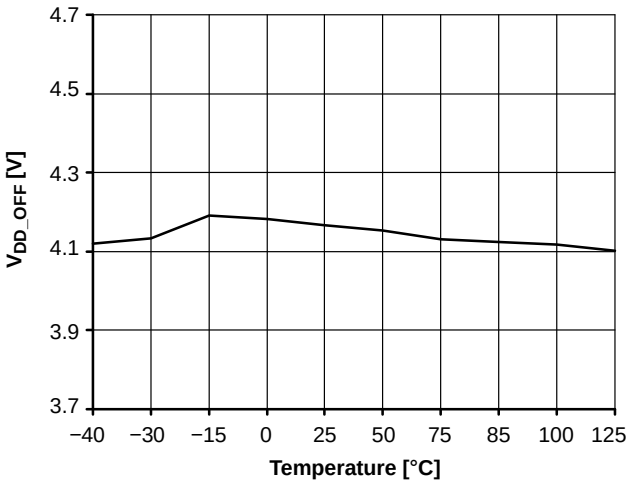


Figure 4. V_{DD_OFF}

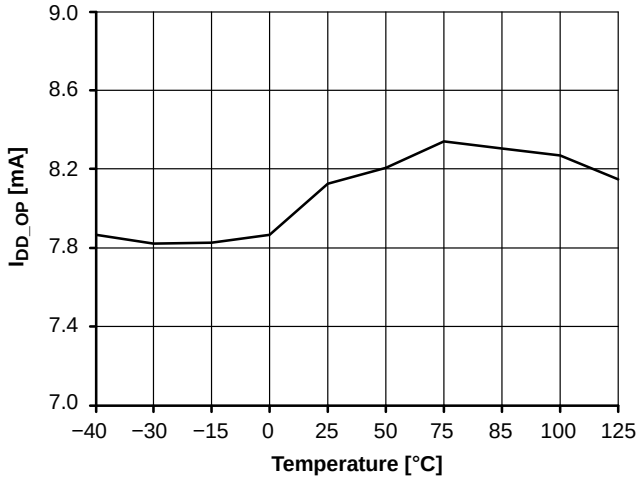


Figure 5. I_{DD_OP}

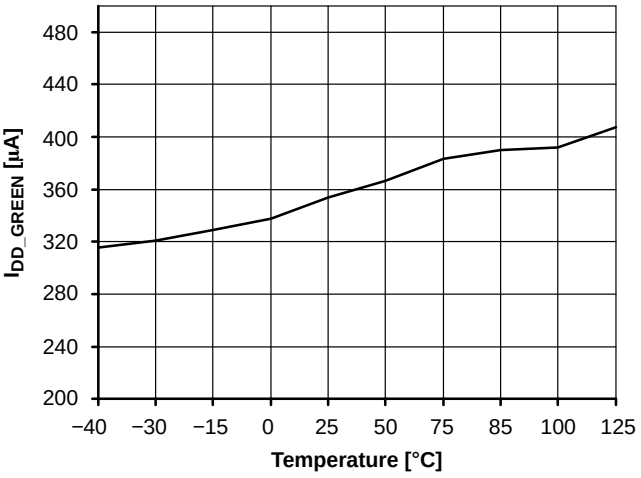


Figure 6. I_{DD_GREEN}

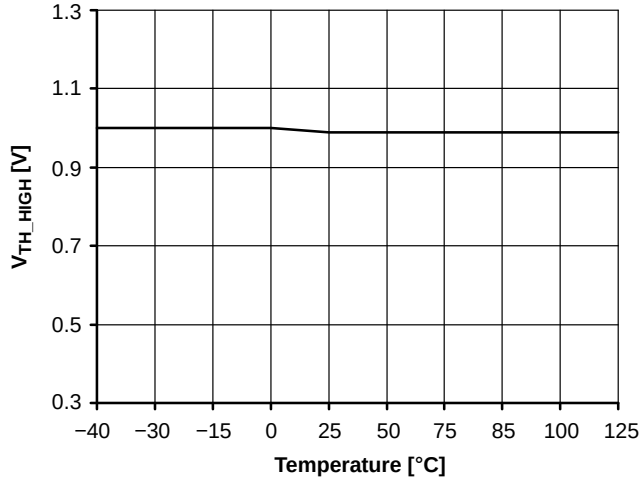


Figure 7. V_{TH_HIGH}

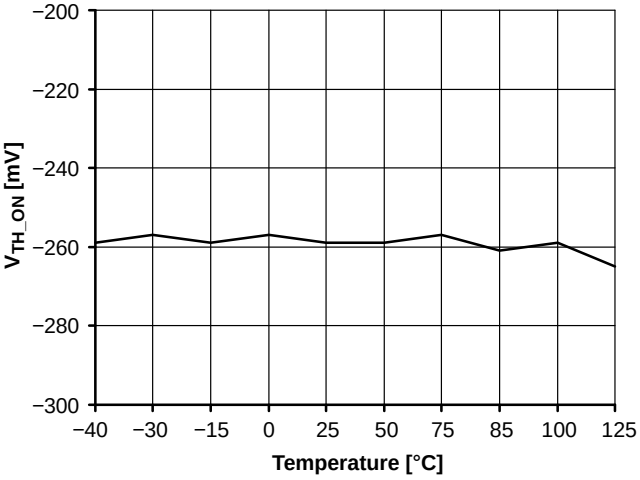


Figure 8. V_{TH_ON}

TYPICAL CHARACTERISTICS

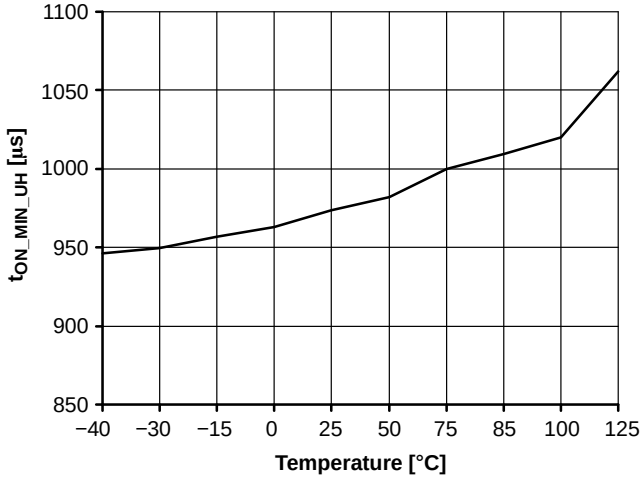


Figure 9. $t_{ON\_DLY2\_H}$

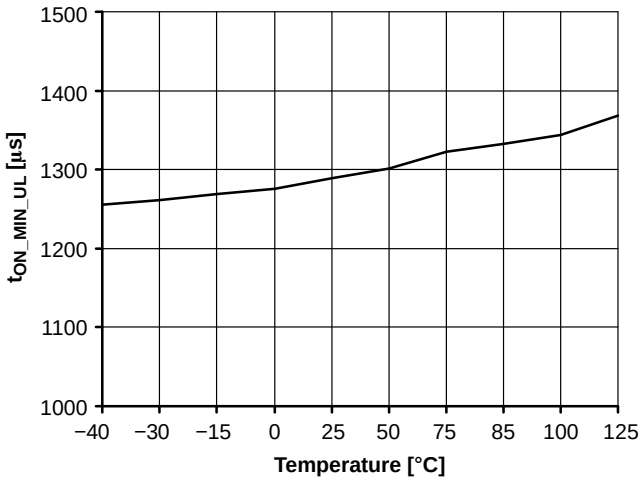


Figure 10. $t_{ON\_DLY2\_L}$

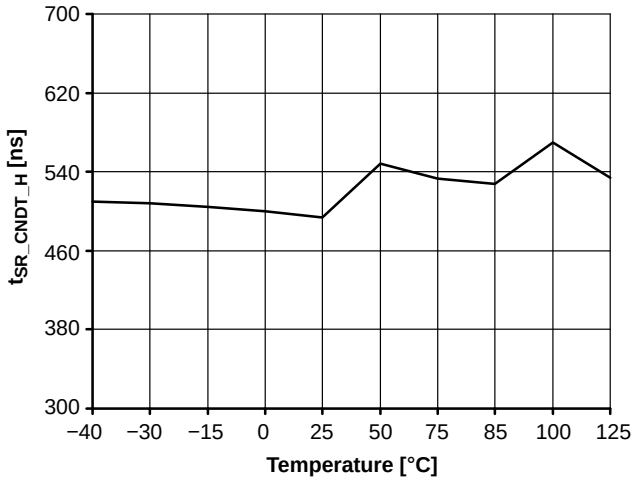


Figure 11. $t_{SR\_CNDT\_H}$

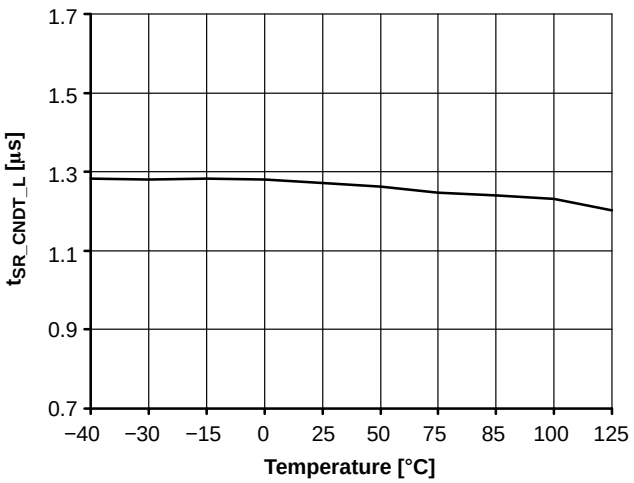


Figure 12. $t_{SR\_CNDT\_L}$

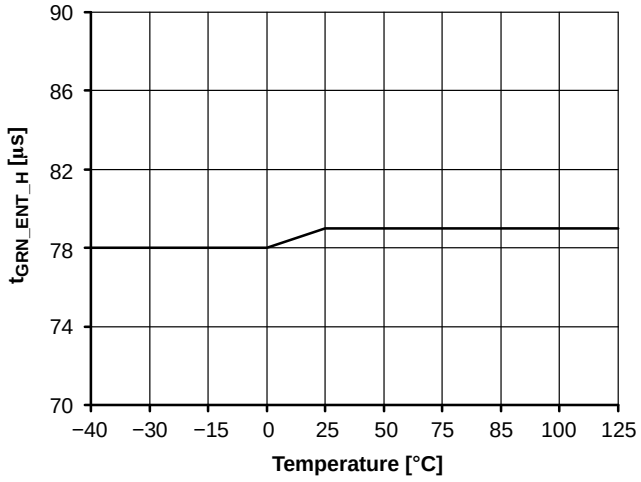


Figure 13. $t_{GRN\_ENT\_H}$

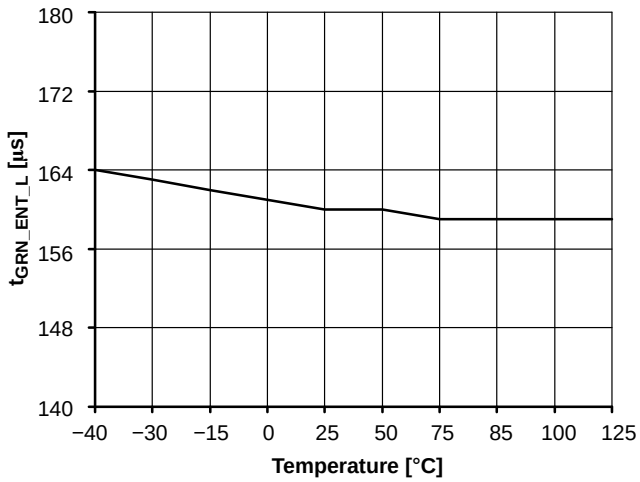


Figure 14. $t_{GRN\_ENT\_L}$

TYPICAL CHARACTERISTICS

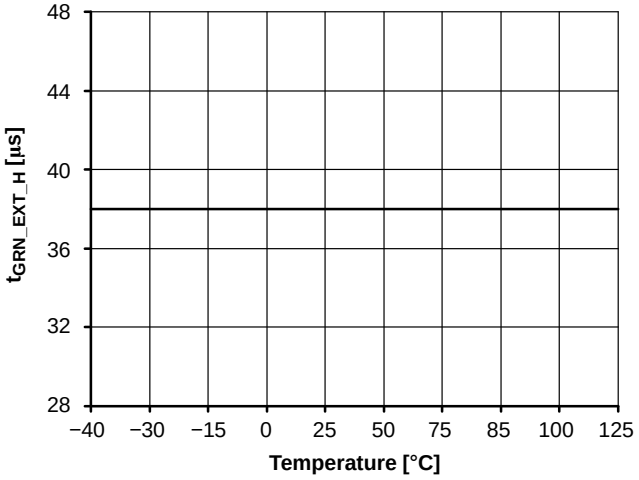


Figure 15. $t_{GRN\_EXT\_H}$

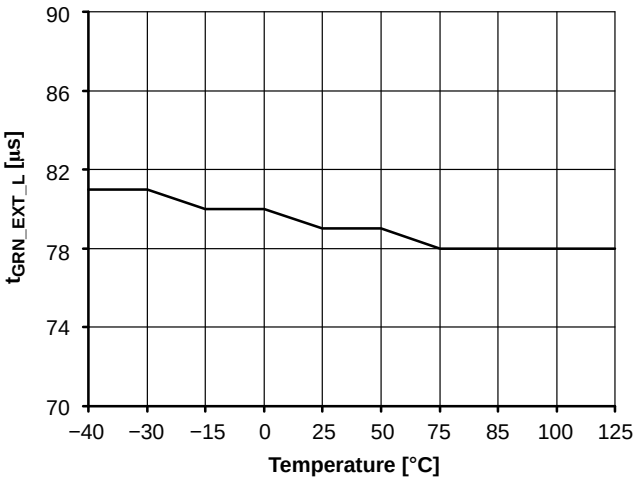


Figure 16. $t_{GRN\_EXT\_L}$

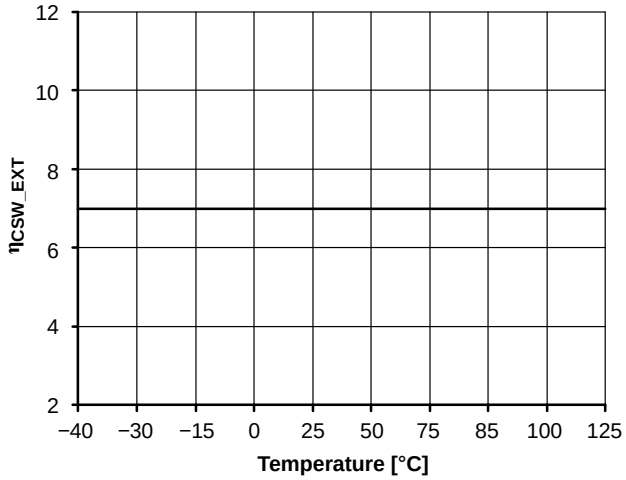


Figure 17. η_{CSW_EXT}

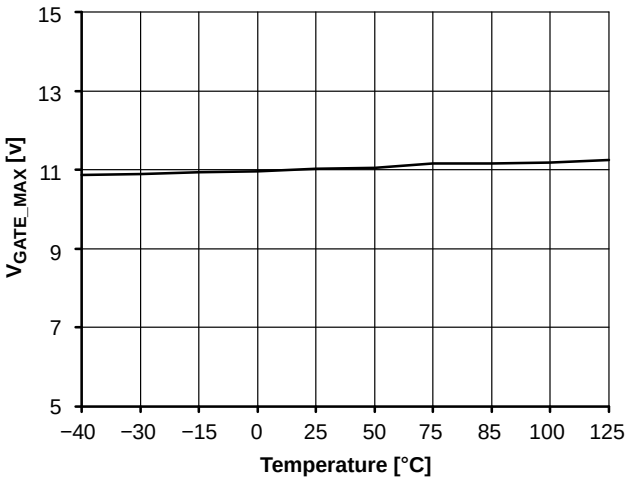


Figure 18. V_{GATE_MAX}

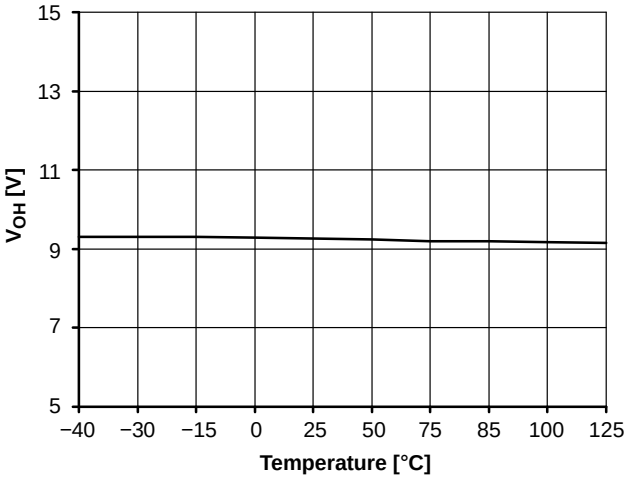


Figure 19. V_{OH}

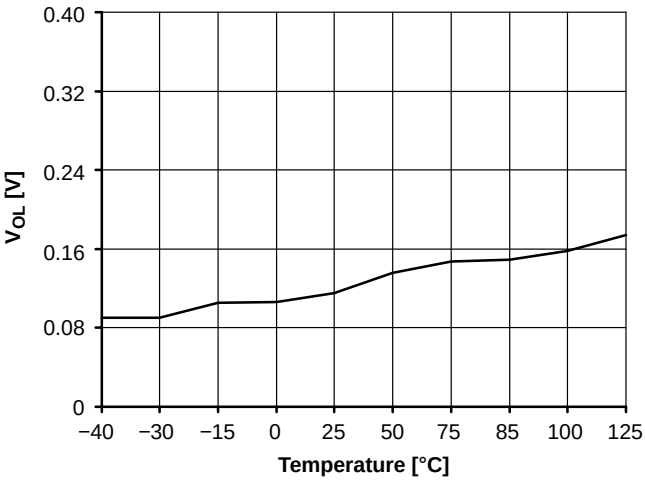


Figure 20. V_{OL}

APPLICATION INFORMATION

Basic Operation Principle

FAN6248 controls the SR MOSFET based on the instantaneous drain-to-source voltage sensed across *DRAIN* and *SOURCE* pins. Before SR gate is turned on, SR body diode operates as the conventional diode rectifier. Once the body diode starts conducting, the drain-to-source voltage drops below the turn-on threshold voltage V_{TH_ON} which triggers the turn-on of the SR gate. Then the drain-to-source voltage is determined by the product of turn-on resistance R_{ds_on} of SR MOSFET and instantaneous SR current. When the drain-to-source voltage reaches the turn-off threshold voltage V_{TH_OFF} as SR MOSFET current decreases to near zero, FAN6248 turns off the gate. If a SR dead time is larger or smaller than the dead time regulation target t_{DEAD}, FAN6248 adaptively changes internal offset voltage to compensate the dead time. In addition, to prevent cross conduction SR operation, FAN6248 has 200 ns of turn-on blocking time just after alternating SR gate is turned off.

SR Turn-off Algorithm

Since a SR turn-off method determines SR conduction time and stable SR operation, the SR turn-off method is one of important feature of SR controllers. The SR turn-off method can be classified into two methods. The first method uses present information by an instantaneous drain voltage. This method is widely used and easy to realize, and can prevent late turn-off. However, it may show premature turn-off by parasitic stray inductances caused by PCB pattern and lead frame of SR MOSFET. The second method predicts SR conduction time by using previous cycle drain voltage information. Since it can prevent the premature turn-off, it is good for the system with constant operating frequency and turn-on time. However, in case of the frequency varying system, it may lead late turn-off so that negative current can flow in the secondary side.

To achieve both advantages, FAN6248 adopts mixed type control method as shown in Figure 21. Basically the instantaneous drain voltage V_{Drain} is compared with V_{TH_OFF} to turn off SR gate. Then, the offset voltage V_{offset}, which is determined by the product R_{offset} and I_{offset}, is added to V_{Drain} in order to compensate the stray inductance effect and maintain 280 ns of t_{DEAD} regardless of parasitic inductances. R_{offset} is an external resistor in Figure 1 and I_{offset} is an internal modulation current in Figure 2. Therefore, FAN6248 can show robust operation with minimum dead time.

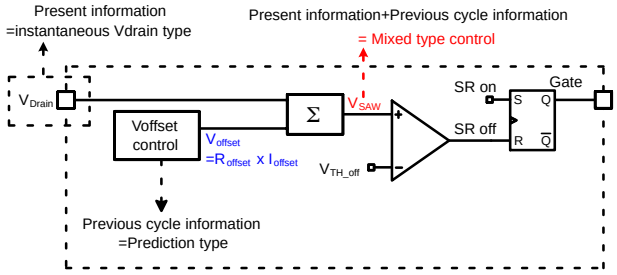


Figure 21. SR Turn-off Algorithm

Adaptive Dead Time Control

The stray inductances of the lead frame of SR MOSFET and PCB pattern induce positive voltage offset across drain-to-source voltage when SR current decreases. This makes drain-to-source voltage of SR MOSFET larger than the product of R_{ds_on} and instantaneous SR current, which results in premature turn-off of SR gate. Since the induced offset voltage changes as load condition changes, the dead time also changes with load variation. To compensate the induced offset voltage, FAN6248 has a adaptive virtual turn-off threshold voltage as shown in Figure 22 with a combination of variable internal turn-off threshold voltages V_{TH_OFF1} and V_{TH_OFF2} (2 steps) and modulated offset voltage V_{offset} (16 steps). The virtual turn-off threshold voltage can be expressed as:

$$\text{Virtual } V_{TH\_OFF} = V_{TH\_OFF} - V_{offset} \qquad \text{(eq. 1)}$$

In FAN6248HC(D) version, if a dead time T_{DEAD} is larger than 280 ns of t_{DEAD_H}, as shown in Figure 23, V_{offset} is decreased by one step in next switching cycle. As a result, the dead time is decreased by increase of virtual V_{TH_OFF}, and becomes close to t_{DEAD_H}, as shown in Figure 24. If the dead time is smaller than t_{DEAD_H}, the dead time is increased by the virtual V_{TH_OFF} decrease. Thus, the dead time is maintained at around t_{DEAD_H} regardless of parasitic inductances.

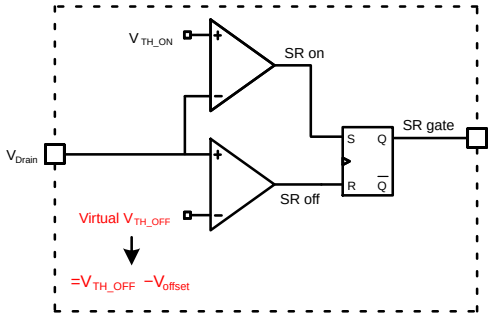


Figure 22. Virtual V_{TH_OFF}

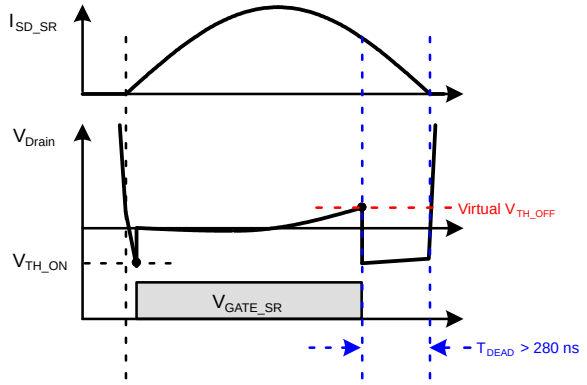


Figure 23. Premature SR Gate Turn-off ($T_{DEAD} > t_{DEAD\_H}$)

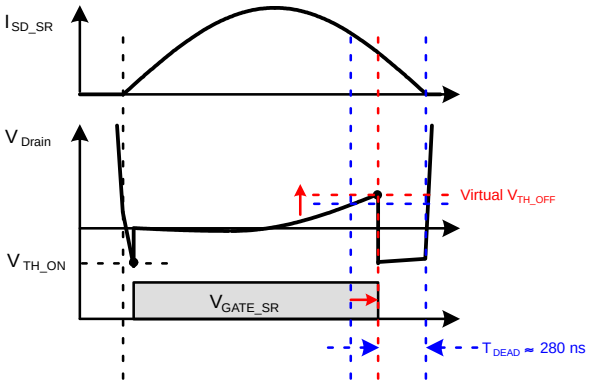


Figure 24. Dead Time Control to Maintain $T_{DEAD} \approx t_{DEAD\_H}$

Minimum Turn-on Time

When SR gate is turned on, there may be severe oscillation in drain-to-source voltage of SR MOSFET, which results in several mis-triggering turn-off as shown in Figure 25. To provide stable SR control without mis-trigger, it is desirable to have large turn-off blanking time (= minimum turn-on time) until the drain voltage oscillation attenuates. However, too large blanking time results in problems at light load condition where the SR conduction time is shorter than the minimum turn-on time. To solve this issue, FAN6248 has adaptive minimum turn-on time where the turn-off blanking time changes in accordance with the SR conduction time T_{SRCOND} measured in previous switching cycle. The SR conduction time is measured by the time from SR gate rising edge to the instant when drain sensing voltage V_{DS_SR} is higher than V_{TH_HGH}. From the previous cycle T_{SRCOND} measurement result, the minimum turn-on time is defined by 25% of T_{SRCOND}.

Capacitive Current Spike Detection

At heavy load condition, the body diode of SR MOSFET in LLC resonant converter starts conducting right after the primary side switching transition takes place. However, when the resonance capacitor voltage amplitude is not large enough at light load condition, the voltage across the magnetizing inductance of the transformer is smaller than the reflected output voltage. Thus, the secondary side SR body diode conduction is delayed until the magnetizing inductor voltage builds up to the reflected output voltage. However, the primary side switching transition can cause capacitive current spike and turn on the body diode of SR MOSFET for a short time as shown in Figure 26, which induces SR mis-trigger signal. Finally, the SR mis-trigger makes inversion current in the secondary side. If a proper algorithm is not provided to prevent the mis-trigger by the capacitive current spike, severe SR current inversion can happen.

To prevent the SR mis-trigger, FAN6248 has a capacitive current spike detection method. When SR current inversion occurs by the mis-trigger signal, the drain sensing voltage of SR MOSFET becomes positive. In this condition, if V_{DS_SR} is higher than V_{TH_OFF} for ($T_{SRCOND} \times K_{INV}$), SR current inversion is detected. After then, FAN6248 turns off SR immediately and increases turn-on delay to t_{ON_DLY2} next cycle.

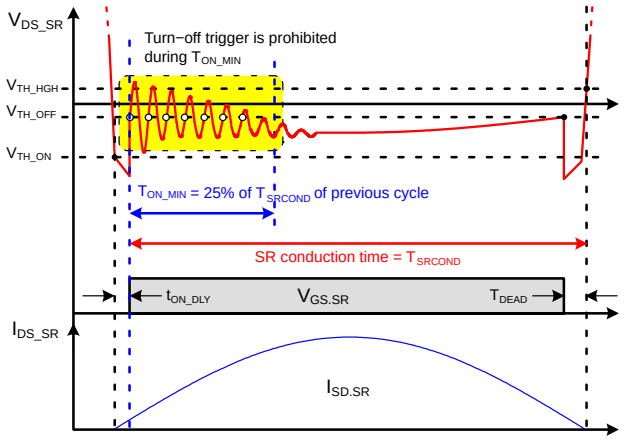


Figure 25. Minimum Turn-on Time

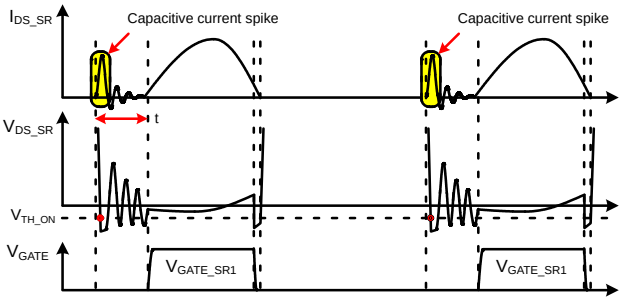


Figure 26. Capacitive Current Spike at Light Load Condition

As a result, SR mis-trigger is prevented. To exit the SR current inversion detection mode, seven consecutive switching cycles without capacitive current spike are required.

Light Load Detection (LLD)

To guarantee stable operation under light load condition, FAN6248 adopts a light load detection function. The modulation current I_{OFFSET} is mainly used for the adaptive dead time control. When the output load is heavy, I_{OFFSET_STEP} declines due to large di/dt in the secondary side current to maintain 280 ns of t_{DEAD} in FAN6248HC(D). On the contrary, I_{OFFSET_STEP} increases at light load condition by small di/dt of SR current. FAN6248 can detect light load condition by using this I_{OFFSET_STEP} as shown in Figure 27. When SR turn-off threshold voltage is V_{TH_OFF1} and the modulation current is higher than I_{OFFEST_STEP8}, the light load detection is triggered. In this mode, dead time target becomes to 320 ns of t_{DEAD_LIGHT} in FAN6248HC(D) and 360 ns in FAN6248LC(D) version.

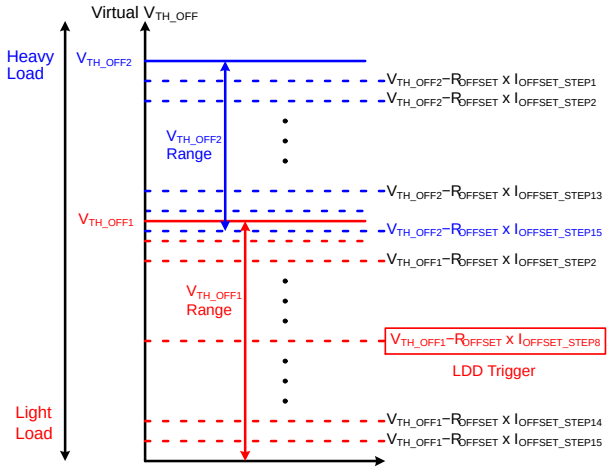


Figure 27. Light Load Detection

Green Mode

When the power supply system operates at very light load condition, FAN6248 disables SR operation and enters into green mode operation. Once FAN6248 is in the green mode, all the major blocks are disabled to minimize the operating current. When V_{DS_SR} has no switching operation longer than t_{GRN_ENT} during the burst mode of the primary side LLC controller, the green mode is enabled after $t_{GRN\_ENT\_DBNC}$ of debounce time. After then, FAN6248 exits the green mode when the non−switching time in the burst mode is less than $t_{GRN\_EXT\_H}$ or 7 consecutive switching cycles are detected as shown in Figure 28.

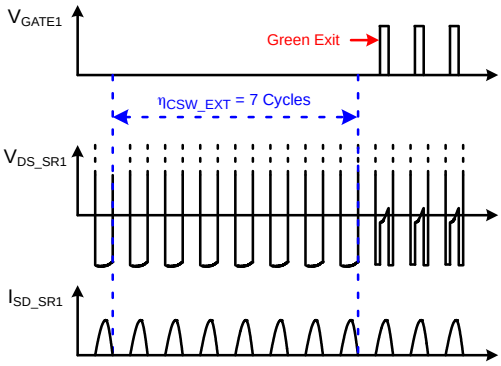
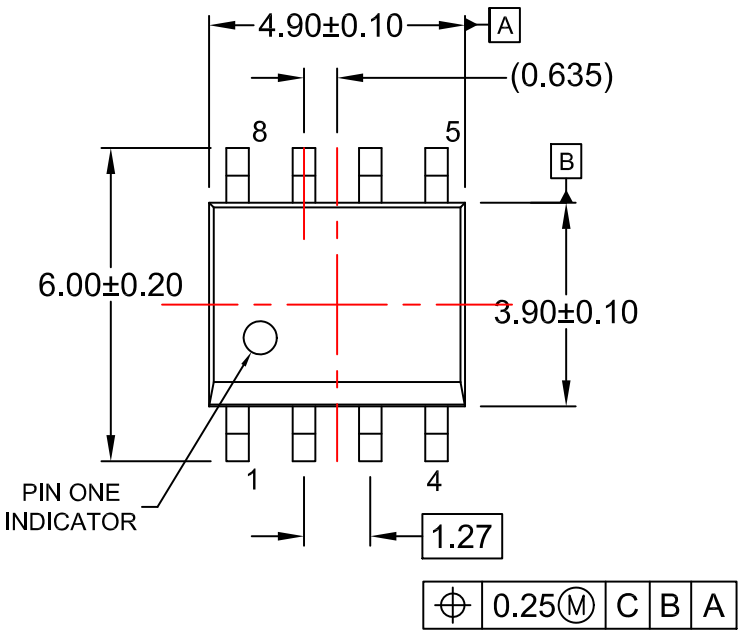
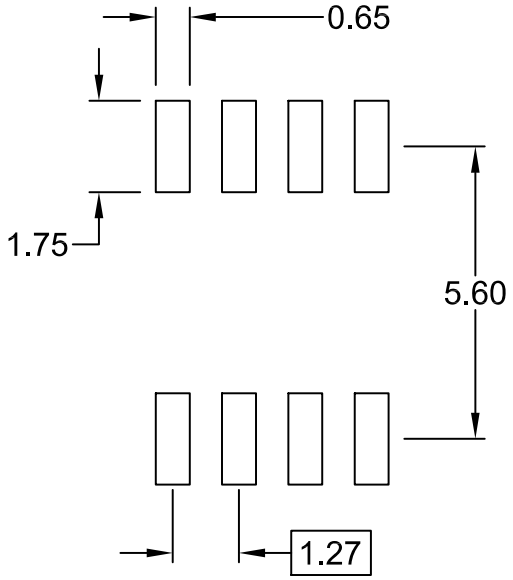


Figure 28. Green Mode Exit

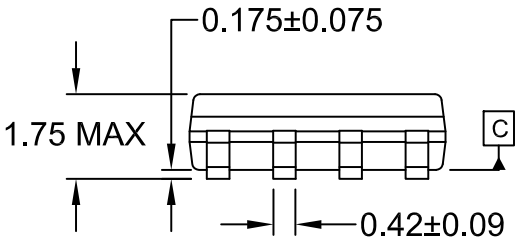
PACKAGE DIMENSIONS

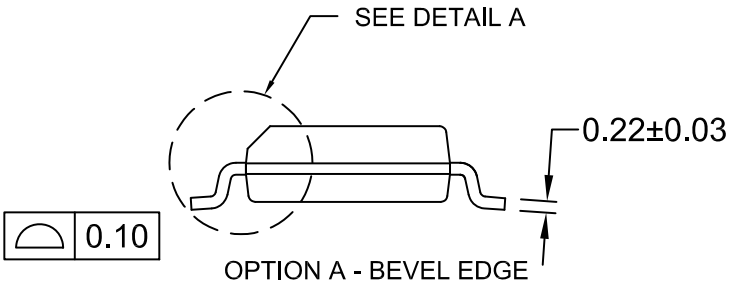
SOIC8
CASE 751EB
ISSUE A



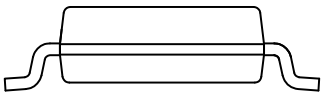


LAND PATTERN RECOMMENDATION

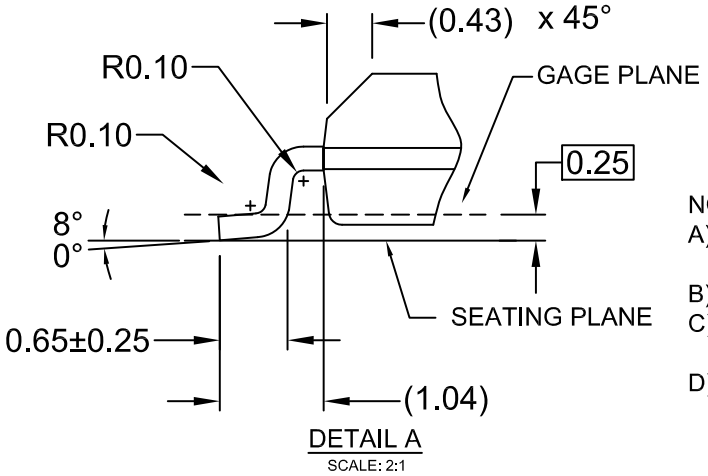




OPTION A - BEVEL EDGE



OPTION B - NO BEVEL EDGE



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