N-Channel Power MOSFET

600V, 18A, 0.19Ω

FEATURES

- Super-Junction technology
- High performance, small $R_{DS(ON)}$*Q_g figure of merit (FOM)
- High ruggedness performance
- 100% UIS tested
- High commutation performance
- Pb-free plating
- Compliant to RoHS Directive 2011/65/EU and in accordance to WEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

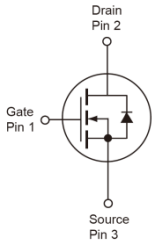
KEY PERFORMANCE PARAMETERS		
PARAMETER	**VALUE**	**UNIT**
V_{DS}	600	V
$R_{DS(on)}$ (max)	0.19	Ω
Q_g	31	nC

Pb-Free RoHS COMPLIANT HALOGEN FREE

APPLICATION

- Power Supply
- AC/DC LED Lighting

ITO-220



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage		V_{DS}	600	V
Gate-Source Voltage		V_{GS}	±30	V
Continuous Drain Current (Note 1)	T_C = 25°C	I_D	18	A
	T_C = 100°C		10.8	A
Pulsed Drain Current (Note 2)		I_{DM}	54	A
Total Power Dissipation @ T_C = 25°C		P_{DTOT}	33.8	W
Single Pulsed Avalanche Energy (Note 3)		E_{AS}	212.9	mJ
Single Pulsed Avalanche Current (Note 3)		I_{AS}	2.6	A
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	°C

THERMAL PERFORMANCE			
PARAMETER	**SYMBOL**	**LIMIT**	**UNIT**
Junction to Case Thermal Resistance	$R_{\Theta JC}$	3.7	°C/W
Junction to Ambient Thermal Resistance	$R_{\Theta JA}$	62	°C/W

Notes: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JA}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design. $R_{\Theta JA}$ shown below for single device operation on FR-4 PCB with minimum recommended footprint in still air.

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Static (Note 4)						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	BV_{DSS}	600	--	--	V
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	$V_{GS(TH)}$	2.0	3.0	4.0	V
Gate Body Leakage	V_{GS} = ±30V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V_{DS} = 600V, V_{GS} = 0V	I_{DSS}	--	--	1	μA
Drain-Source On-State Resistance	V_{GS} = 10V, I_D = 6A	$R_{DS(on)}$	--	0.17	0.19	Ω
Dynamic (Note 5)						
Total Gate Charge	V_{DS} = 380V, I_D = 18A, V_{GS} = 10V	Q_g	--	31	--	nC
Gate-Source Charge		Q_{gs}	--	8	--	
Gate-Drain Charge		Q_{gd}	--	12.6	--	
Input Capacitance	V_{DS} = 100V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	1273	--	pF
Output Capacitance		C_{oss}	--	92	--	
Gate Resistance	F = 1MHz, open drain	R_g	--	3.1	--	Ω
Switching (Note 6)						
Turn-On Delay Time	V_{DD} = 380V, R_{GEN} = 25Ω, I_D = 18A, V_{GS} = 10V,	$t_{d(on)}$	--	36	--	ns
Turn-On Rise Time		t_r	--	21	--	
Turn-Off Delay Time		$t_{d(off)}$	--	95	--	
Turn-Off Fall Time		t_f	--	21	--	
Source-Drain Diode (Note 4)						
Forward On Voltage	I_S = 18A, V_{GS} = 0V	V_{SD}	--	--	1.4	V
Reverse Recovery Time	V_R=100V, I_S = 18A dI$_F$/dt = 100A/μs	t_{rr}	--	359.4	--	ns
Reverse Recovery Charge		Q_{rr}	--	4.54	--	μC

Notes:

1. Current limited by package.
2. Pulse width limited by the maximum junction temperature.
3. L = 63mH, I_{AS} = 2.6A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
4. Pulse test: PW ≤ 300μs, duty cycle ≤ 2%.
5. For DESIGN AID ONLY, not subject to production testing.
6. Switching time is essentially independent of operating temperature.

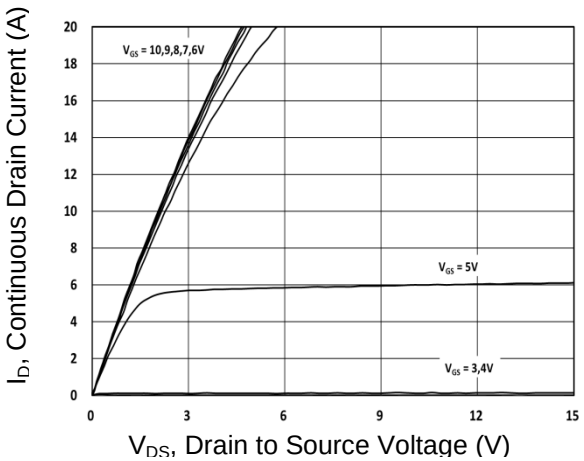
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM60NB190CI C0G	ITO-220	50pcs / Tube

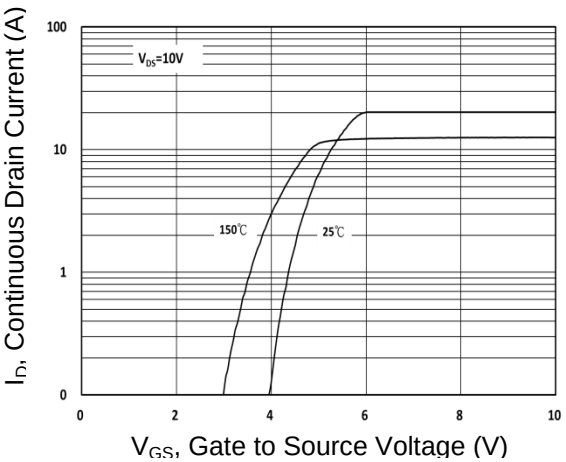
CHARACTERISTICS CURVES

(T_C = 25°C unless otherwise noted)

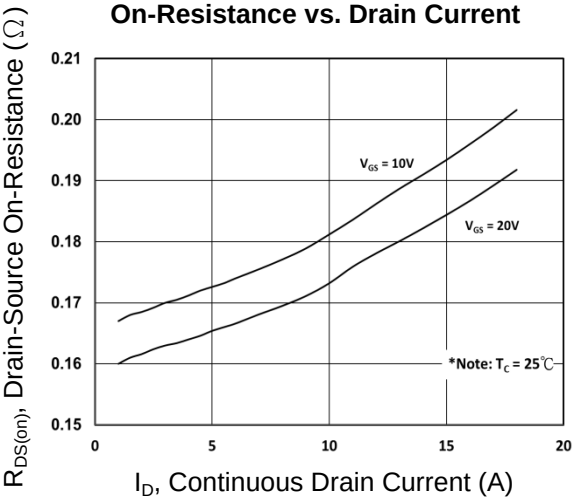
Output Characteristics



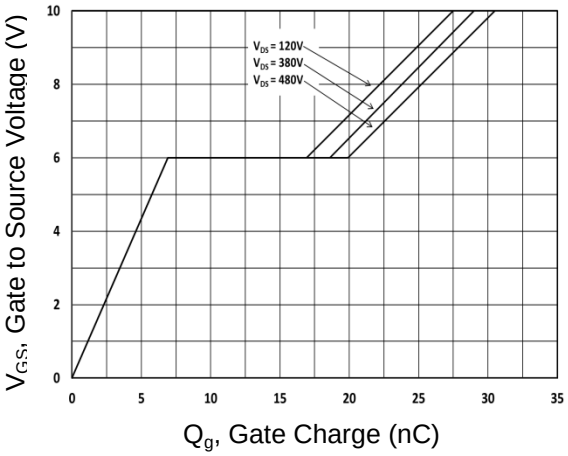
Transfer Characteristics



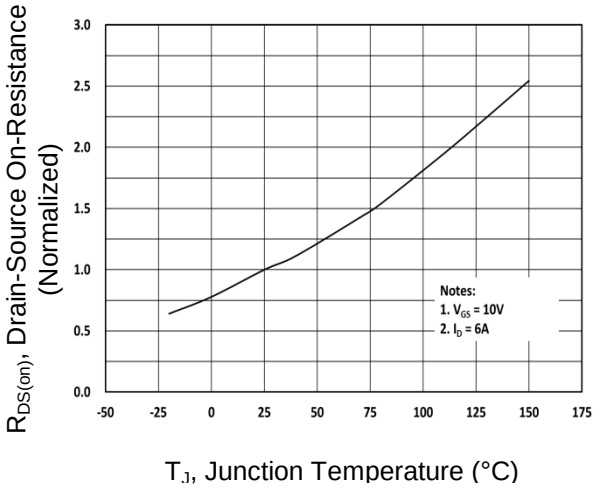
On-Resistance vs. Drain Current



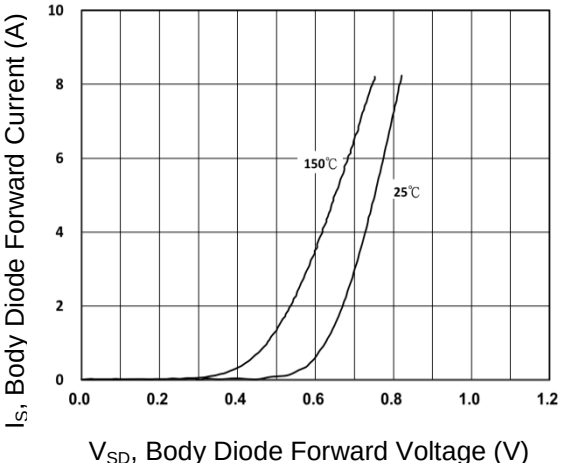
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



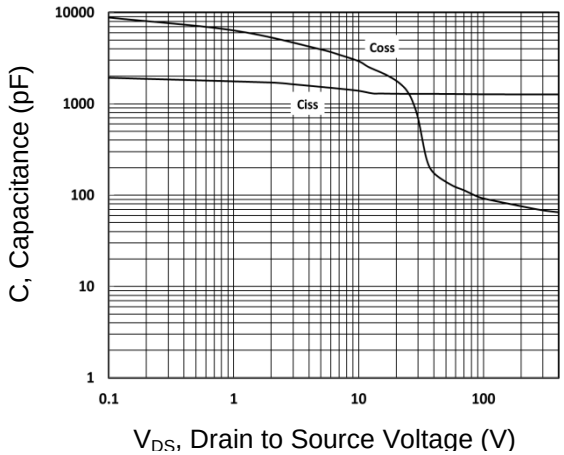
Source-Drain Diode Forward Current vs. Voltage



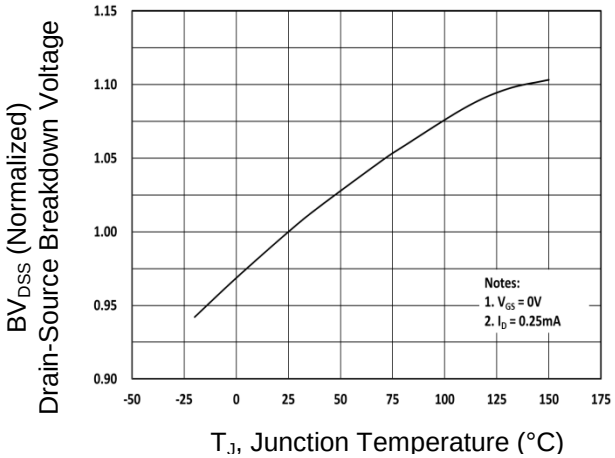
CHARACTERISTICS CURVES

(T_C = 25°C unless otherwise noted)

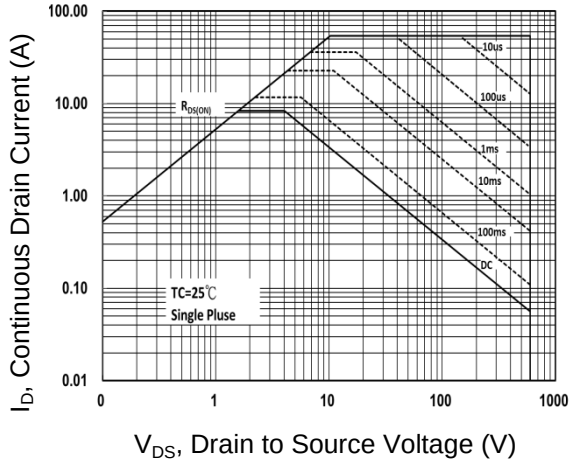
Capacitance vs. Drain-Source Voltage



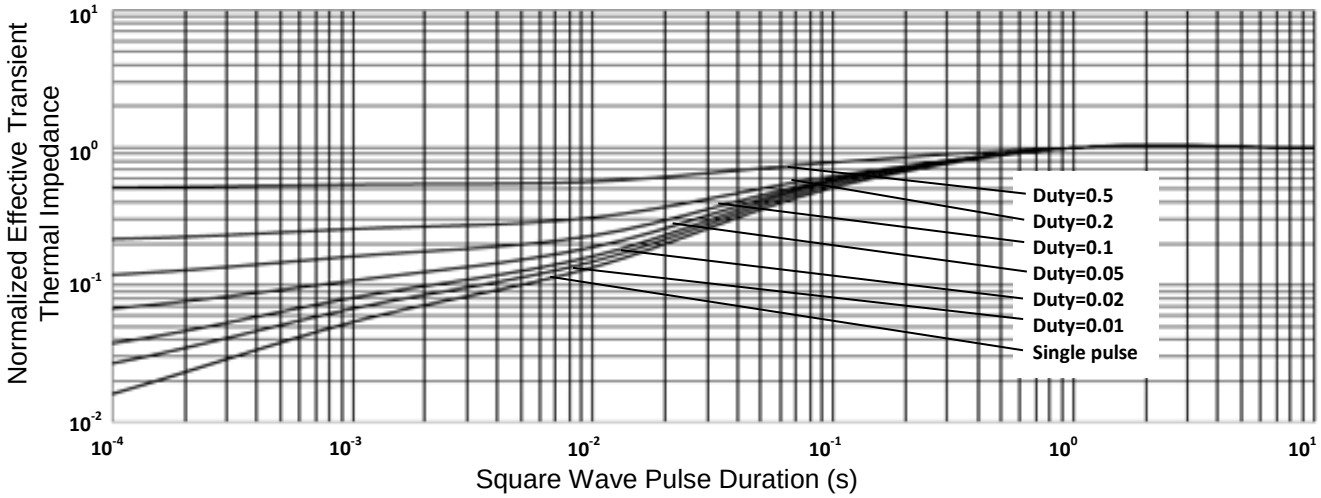
BV_{DSS} vs. Junction Temperature



Maximum Safe Operating Area (ITO-220)

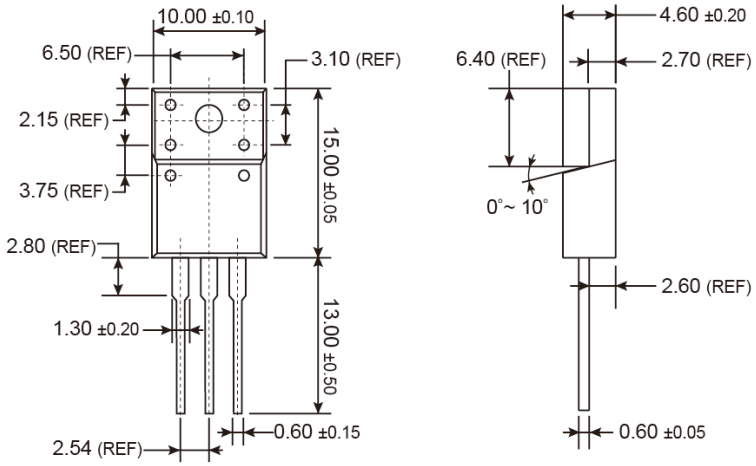


Normalized Thermal Transient Impedance, Junction-to-Case (ITO-220)



PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

ITO-220



MARKING DIAGRAM

G = Halogen Free
Y = Year Code
WW = Week Code (01~52)
F = Factory Code

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