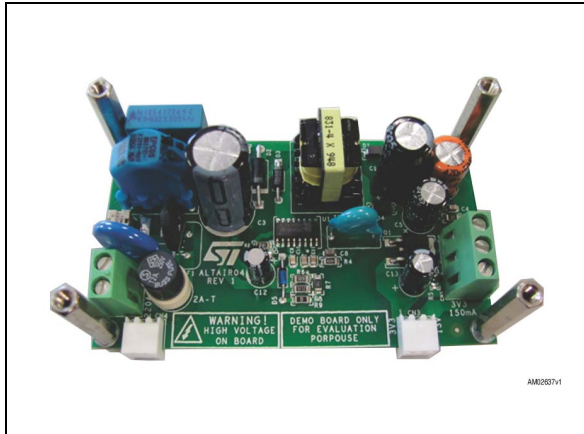


Double output SMPS for power line applications using the ALTAIR04-900 primary controller

Data brief



The STEVAL-ISA133V1 demonstration board uses the new ALTAIR04-900, a quasi-resonant (QR) current-mode controller IC specifically designed for QR ZVS (zero voltage switching at switch turn-on) flyback converters, which combines a high-performance low-voltage PWM controller chip and a typical 16 $R_{DS(on)}$, 900 V, avalanche-rugged power MOSFET in the same package.

The device is capable of providing constant output voltage regulation using primary-sensing constant voltage loop (CV loop). This eliminates the need for the optocoupler and the secondary voltage reference while maintaining very accurate regulation.

Also, using the primary constant current loop, it is possible to set the maximum deliverable output current without using secondary components or current sensor.

The board implements several protection features that considerably increase end-product safety and reliability: auxiliary winding disconnection (or brownout) detection, shorted secondary rectifier detection, and transformer saturation protection, all of which are auto-restart mode.

Features

- Universal input mains range: 90 264 V_{ac} - frequency 45 65 Hz
- Double output voltage: 13V @ 0.55 A and 3.3 V @ 100 mA peak power
- Optoless constant-voltage/constant-current output regulation
- Meets power line communication system specifications with the ST7580
- Average efficiency: > 70%
- EMI: in accordance with EN55022-Class-B

Description

The STEVAL-ISA133V1 demonstration board implements a 7.5 W double output wide range mains adapter with constant-voltage/constant-current, designed as an innovative AC-DC adapter to supply a complete power line communication system based on the ST7580.

The power supply provides a 13 V output voltage to supply the power line modem (PLM) and the analog circuitry, and a post-regulated 3.3 volts to supply digital circuitry and an optional external microcontroller.

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Figure 1. STEVAL-ISA133V1 schematic diagram

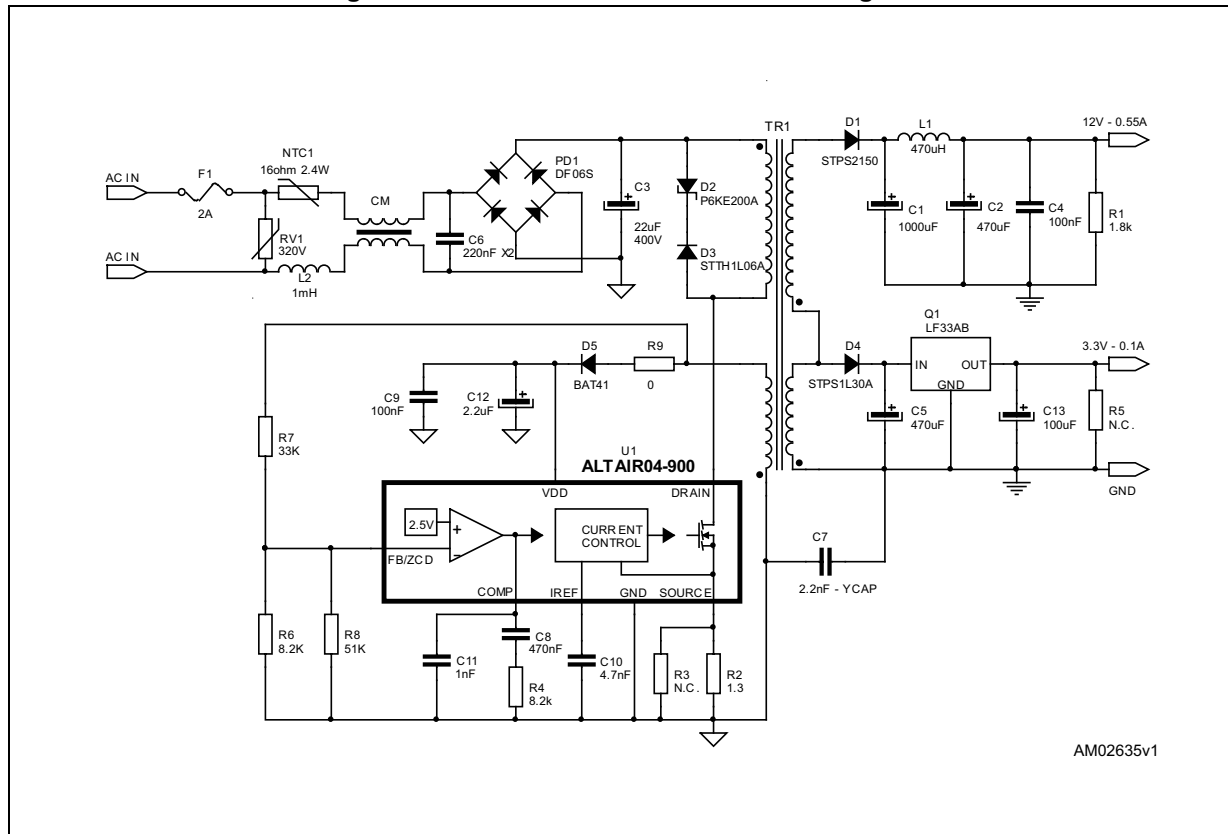


Figure 2. Output voltage with 3V3 @ 40 mA

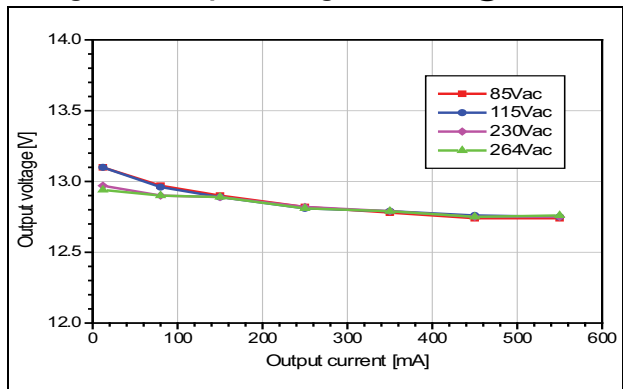
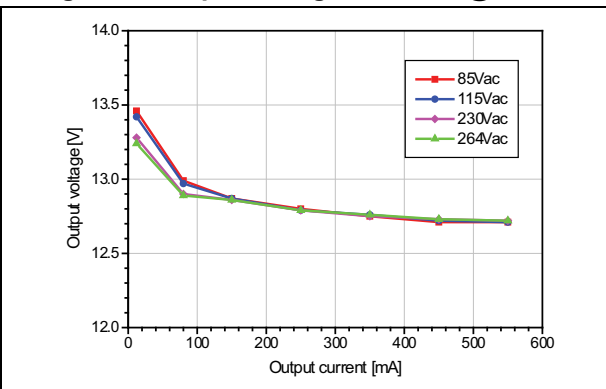


Figure 3. Output voltage with 3V3 @ 80 mA



2 Revision history

Table 1. Document revision history

Date	Revision	Changes
16-Apr-2013	1	Initial release.

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