

N-Channel Power MOSFET

900V, 4A, 4.0Ω

FEATURES

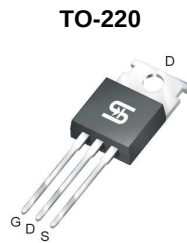
- Low $R_{DS(ON)}$ 4Ω (Max.)
- Low gate charge typical @ 25nC (Typ.)
- Improve dV/dt capability

APPLICATION

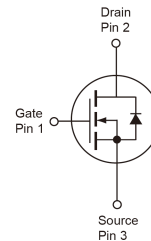
- High efficiency switch mode power Supply
- Lighting

KEY PERFORMANCE PARAMETERS

PARAMETER	VALUE	UNIT
V_{DS}	900	V
$R_{DS(on)}$ (max)	4	Ω
Q_g	25	nC



ITO-220


Notes: Moisture sensitivity level: level 3. Per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER		SYMBOL	TO-220	ITO-220	UNIT
Drain-Source Voltage		V _{DS}	900		V
Gate-Source Voltage		V _{GS}	±30		V
Continuous Drain Current ^(Note 1)	T _C = 25°C	I _D	4	4*	A
	T _C = 100°C		2.2	2.2*	
Pulsed Drain Current ^(Note 2)		I _{DM}	16	16 *	A
Total Power Dissipation @ T _C = 25°C		P _{DTOT}	123	38.7	W
Single Pulsed Avalanche Energy ^(Note 3)		E _{AS}	474		mJ
Single Pulsed Avalanche Current ^(Note 3)		I _{AS}	4		A
Repetitive Avalanche Energy ^(Note 2)		E _{AR}	12.3		mJ
Peak Diode Recovery ^(Note 7)		dV/dt	4.5		V
Operating Junction and Storage Temperature Range		T _J , T _{STG}	- 55 to +150		°C

THERMAL PERFORMANCE

PARAMETER	SYMBOL	TO-220	ITO-220	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	1.01	3.23	°C/W
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	62.5		°C/W

Notes: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 PCB in still air.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static ^(Note 4)						
Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA	BV _{DSS}	900	--	--	V
Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	V _{GS(TH)}	2	--	4	V
Gate Body Leakage	V _{GS} = ±30V, V _{DS} = 0V	I _{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V _{DS} = 900V, V _{GS} = 0V	I _{DSS}	--	--	10	μA
Drain-Source On-State Resistance	V _{GS} = 10V, I _D = 2.0A	R _{DS(on)}	--	3.2	4.0	Ω
Forward Transconductance	V _{DS} = 30V, I _D = 2.0A	g _{fs}	--	6	--	S
Dynamic ^(Note 5)						
Total Gate Charge	V _{DS} = 720V, I _D = 4.0A, V _{GS} = 10V	Q _g	--	25	--	nC
Gate-Source Charge		Q _{gs}	--	4.8	--	
Gate-Drain Charge		Q _{gd}	--	10.2	--	
Input Capacitance	V _{DS} = 25V, V _{GS} = 0V, f = 1.0MHz	C _{iss}	--	955	--	pF
Output Capacitance		C _{oss}	--	80	--	
Gate Resistance	F = 1MHz, open drain	R _g	--	--	4	Ω
Switching ^(Note 6)						
Turn-On Delay Time	V _{DD} = 450V, R _{GEN} = 25Ω, I _D = 4.0A, V _{GS} = 10V,	t _{d(on)}	--	49	--	ns
Turn-On Rise Time		t _r	--	38	--	
Turn-Off Delay Time		t _{d(off)}	--	146	--	
Turn-Off Fall Time		t _f	--	50	--	
Source-Drain Diode ^(Note 4)						
Forward On Voltage	I _S = 4.0A, V _{GS} = 0V	V _{SD}	--	--	1.5	V
Reverse Recovery Time	V _{GS} = 0V, I _S = 4A dI _F /dt = 100A/μs	t _{rr}	--	487	--	ns
Reverse Recovery Charge		Q _{rr}	--	2.8	--	μC

Notes:

1. Current limited by package.
2. Pulse width limited by the maximum junction temperature.
3. $L = 56mH, I_{AS} = 4.0A, V_{DD} = 50V, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$.
4. Pulse test: $PW \leq 300\mu s$, duty cycle $\leq 2\%$.
5. For DESIGN AID ONLY, not subject to production testing.
6. Switching time is essentially independent of operating temperature.
7. $I_{SD} \leq 4A, dI/dt \leq 200A/\mu s, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$.

ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM4N90CZ C0G	TO-220	50pcs / Tube
TSM4N90CI C0G	ITO-220	50pcs / Tube

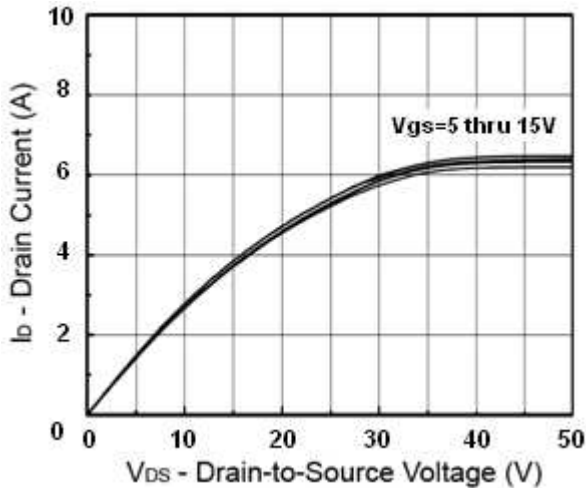
Note:

1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
2. Halogen-free according to IEC 61249-2-21 definition

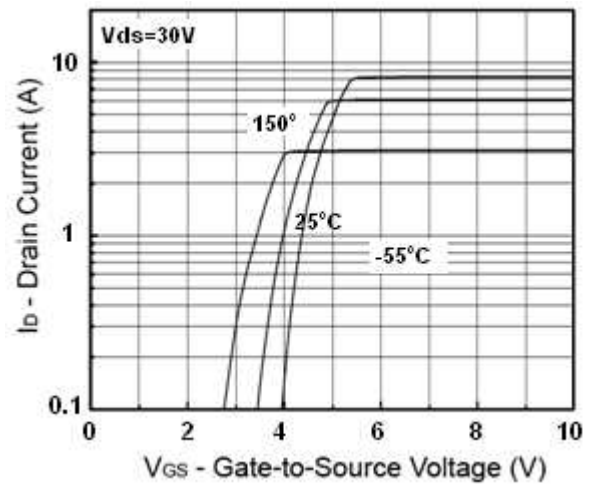
CHARACTERISTICS CURVES

($T_C = 25^\circ\text{C}$ unless otherwise noted)

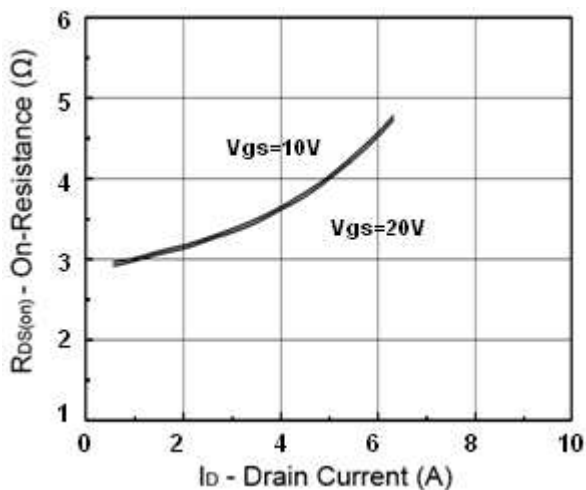
Output Characteristics



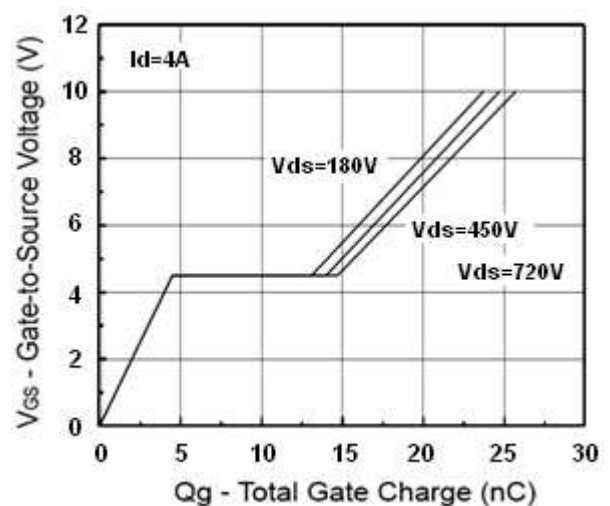
Transfer Characteristics



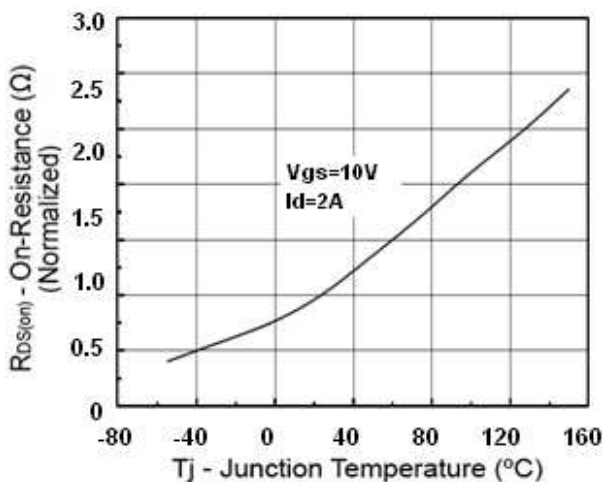
On-Resistance vs. Drain Current



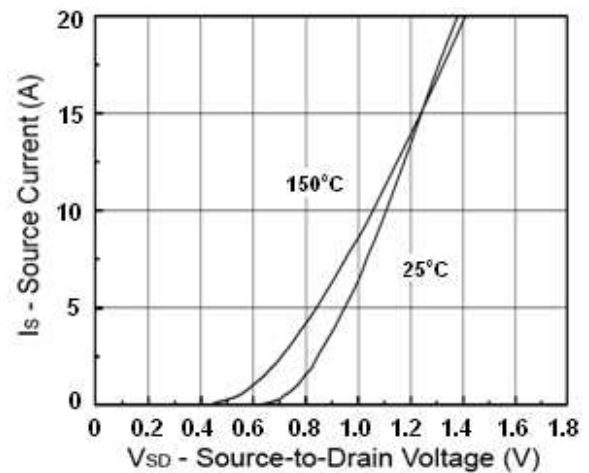
Gate Charge



On-Resistance vs. Junction Temperature



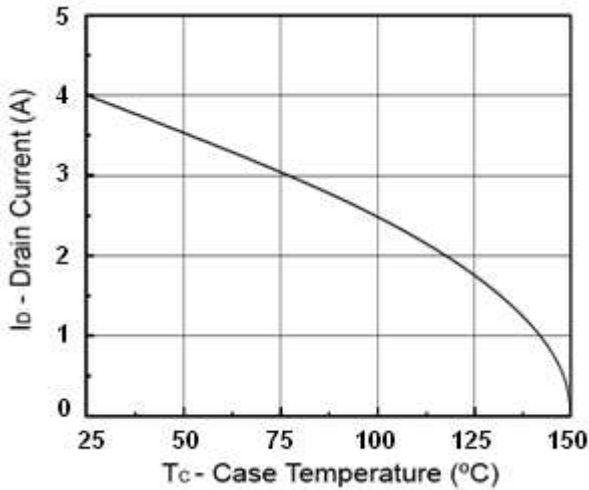
Source-Drain Diode Forward Voltage



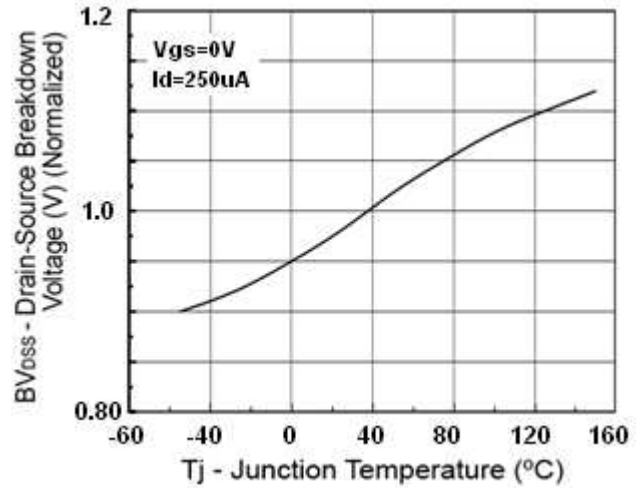
CHARACTERISTICS CURVES

($T_c = 25^\circ\text{C}$ unless otherwise noted)

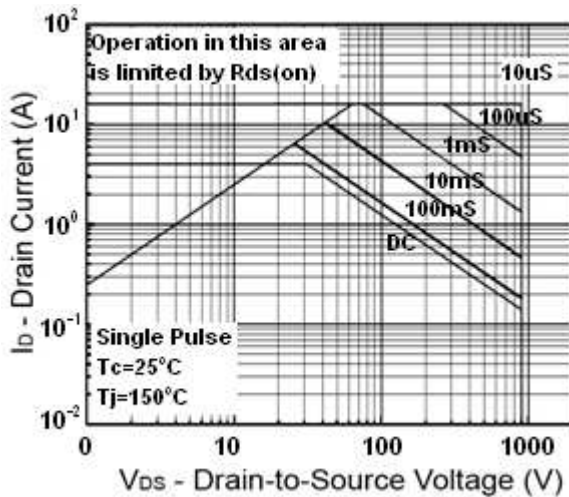
Drain Current vs. Case Temperature



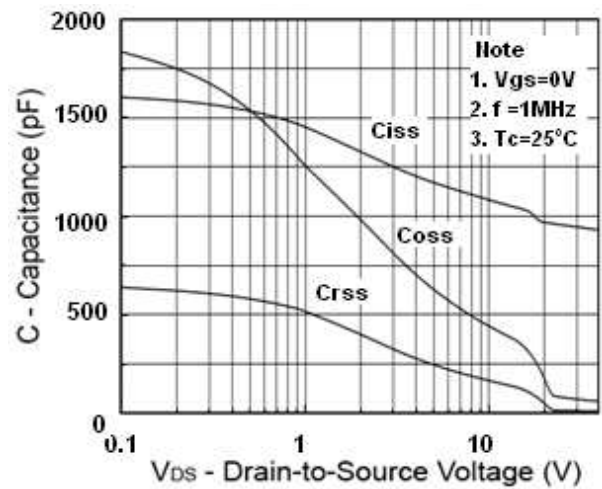
BV_{DSS} vs. Junction Temperature



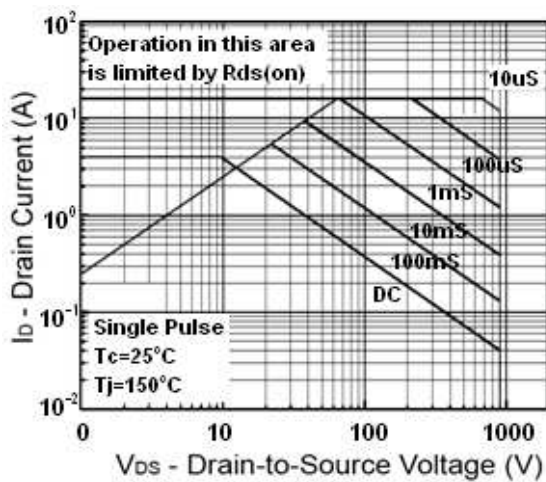
Maximum Safe Operating Area



Capacitance vs. Drain-Source Voltage



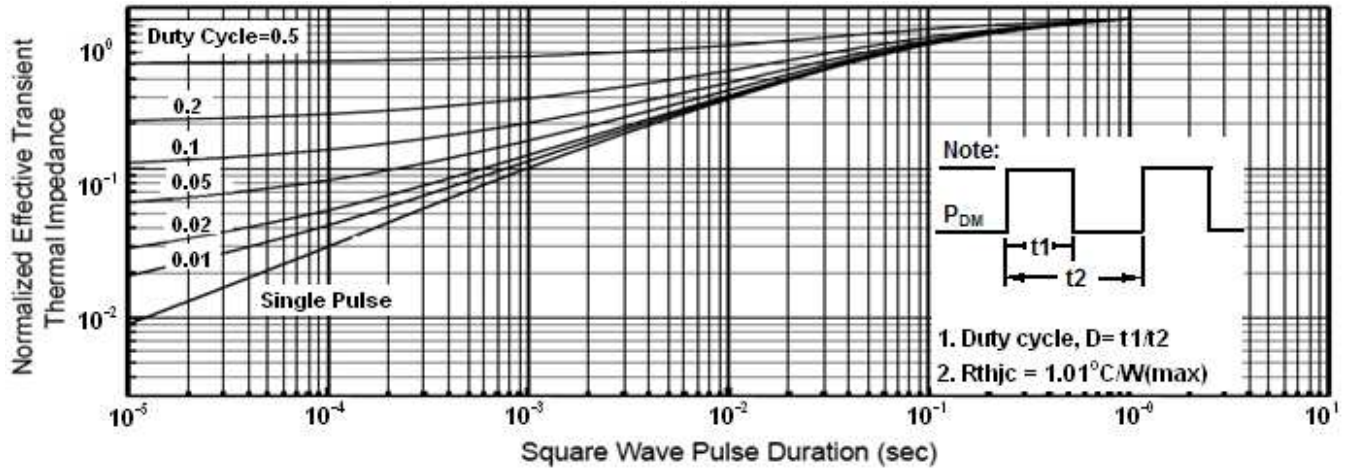
Maximum Safe Operating Area (ITO-220)



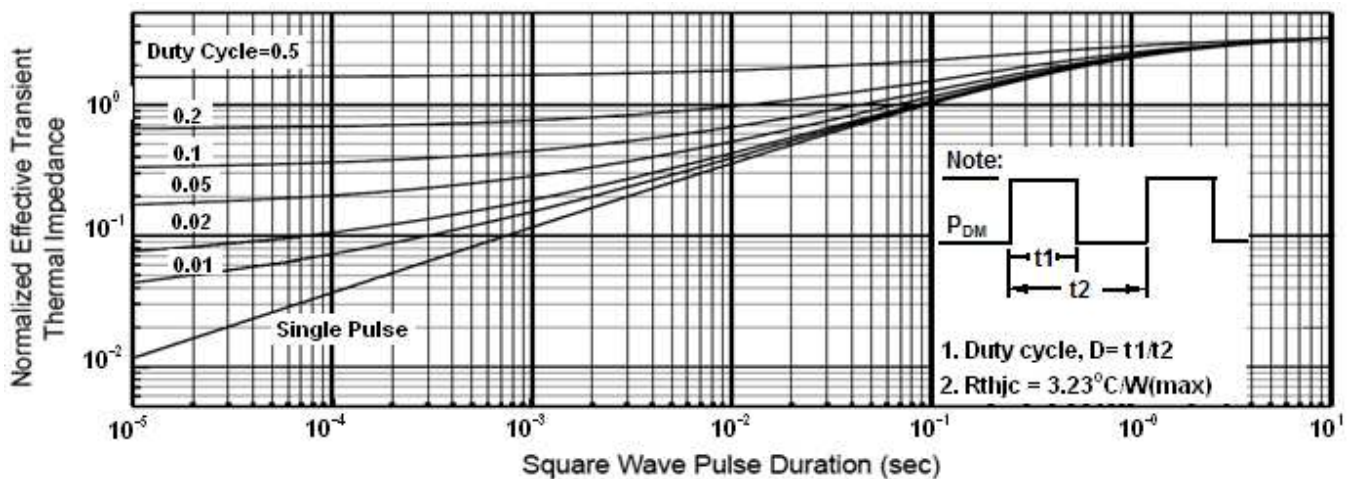
CHARACTERISTICS CURVES

($T_c = 25^\circ\text{C}$ unless otherwise noted)

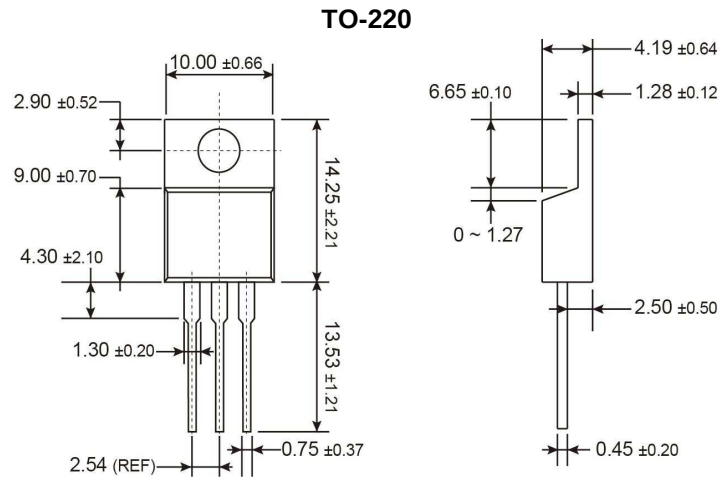
Normalized Thermal Transient Impedance, Junction-to-Ambient (TO-220)



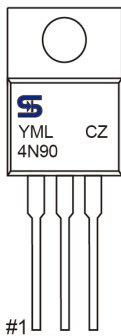
Normalized Thermal Transient Impedance, Junction-to-Ambient (ITO-220)



PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

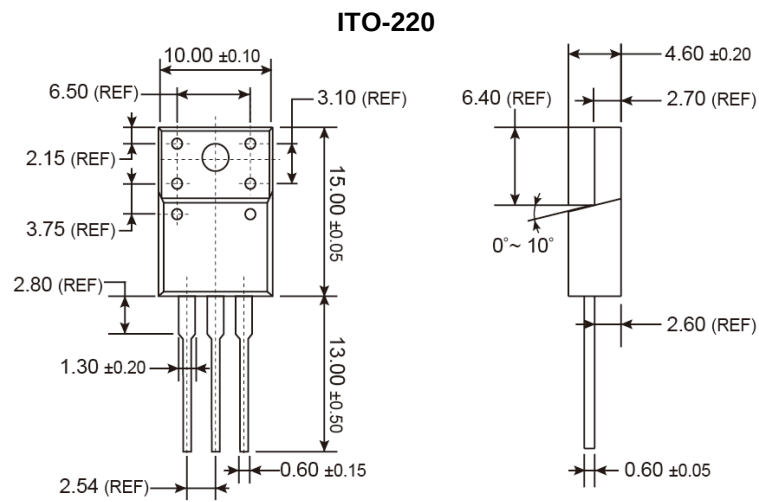


MARKING DIAGRAM

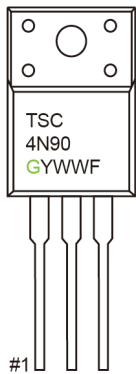


Y = Year Code
M = Month Code for Halogen Free Product
O =Jan **P** =Feb **Q** =Mar **R** =Apr
S =May **T** =Jun **U** =Jul **V** =Aug
W =Sep **X** =Oct **Y** =Nov **Z** =Dec
L = Lot Code (1~9, A~Z)

PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)



MARKING DIAGRAM



- G** = Halogen Free
- Y** = Year Code
- WW** = Week Code (01~52)
- F** = Factory Code

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