X9313

Digitally Controlled Potentiometer (XDCP™) Linear, 32 Taps, 3 Wire Interface, Terminal Voltages ± VCC

FN8177
Rev 7.00
October 7, 2015

The Intersil X9313 is a digitally controlled potentiometer (XDCP). The device consists of a resistor array, wiper switches, a control section, and nonvolatile memory. The wiper position is controlled by a 3-wire interface.

The potentiometer is implemented by a resistor array composed of 31 resistive elements and a wiper switching network. Between each element and at either end are tap points accessible to the wiper terminal. The position of the wiper element is controlled by the $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$ inputs. The position of the wiper can be stored in nonvolatile memory and then be recalled upon a subsequent power-up operation.

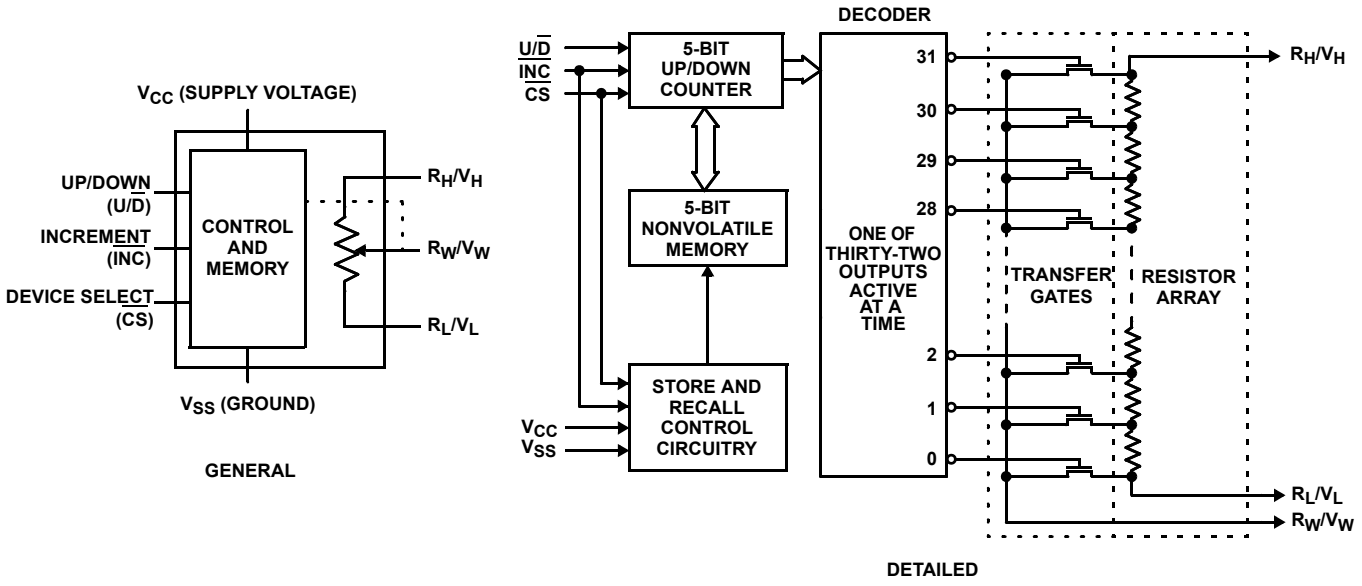
The device can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications including:

- Control
- Parameter adjustments
- Signal processing

Features

- Solid-state potentiometer
- 3-wire serial interface
- 32 wiper tap points
  - Wiper position stored in nonvolatile memory and recalled on power-up
- 31 resistive elements
  - Temperature compensated
  - End-to-end resistance range ±20%
  - Terminal voltages, $-V_{CC}$ to $+V_{CC}$
- Low power CMOS
  - V_{CC} = 3V or 5V
  - Active current, 3mA max.
  - Standby current, 500µA max.
- High reliability
  - Endurance, 100,000 data changes per bit
  - Register data retention, 100 years
- R_{TOTAL} values = 1kΩ, 10kΩ, 50kΩ
- Packages
  - 8 Ld SOIC, 8 Ld MSOP and 8 Ld PDIP
- Pb-free available (RoHS compliant)

Block Diagram



Ordering Information

PART NUMBER	PART MARKING	V_{CC} RANGE (V)	R_{TOTAL} (kΩ)	TEMPERATURE RANGE (°C)	PACKAGE	PKG. DWG. #
X9313UMIZ* (Note)	DDB	4.5 to 5.5	50	-40 to +85	8 Ld MSOP (Pb-free)	M8.118
X9313USZ* (Note)	X9313U Z			0 to +70	8 Ld SOIC (Pb-free)	M8.15
X9313USIZ* (Note)	X9313U ZI			-40 to +85	8 Ld SOIC (Pb-free)	M8.15
X9313WMZ* (Note)	DDF		10	0 to +70	8 Ld MSOP (Pb-free)	M8.118
X9313WMIZ* (Note)	DDE			-40 to +85	8 Ld MSOP (Pb-free)	M8.118
X9313WPIZ	X9313WP ZI			-40 to +85	8 Ld PDIP*** (Pb-free)	MDP0031
X9313WSZ* (Note)	X9313W Z			0 to +70	8 Ld SOIC (Pb-free)	M8.15
X9313WSIZ* (Note)	X9313WS ZI			-40 to +85	8 Ld SOIC (Pb-free)	M8.15
X9313ZMZ* (Note)	DDJ		1	0 to +70	8 Ld MSOP (Pb-free)	M8.118
X9313ZMIZ* (Note)	DDH			-40 to +85	8 Ld MSOP (Pb-free)	M8.118
X9313ZSZ* (Note)	X9313 Z			0 to +70	8 Ld SOIC (Pb-free)	M8.15
X9313ZSIZ* (Note)	X9313ZS ZI			-40 to +85	8 Ld SOIC (Pb-free)	M8.15
X9313UMZ* (Note)	DDC	3 to 5.5	50	0 to +70	8 Ld MSOP	M8.118
X9313UMZ-3* (Note)	DDD	3 to 5.5	50	0 to +70	8 Ld MSOP	M8.118
X9313UMIZ-3* (Note)	13UEZ			-40 to +85	8 Ld MSOP (Pb-free)	M8.118
X9313USZ-3* (Note)	X9313U ZD			0 to +70	8 Ld SOIC (Pb-free)	M8.15
X9313WMZ-3* (Note)	DDG		10	0 to +70	8 Ld MSOP (Pb-free)	M8.118
X9313WMIZ-3* (Note)	13WEZ			-40 to +85	8 Ld MSOP (Pb-free)	M8.118
X9313WSZ-3* (Note)	X9313W ZD			0 to +70	8 Ld SOIC (Pb-free)	M8.15
X9313ZMZ-3* (Note)	DDK		1	0 to +70	8 Ld MSOP (Pb-free)	M8.118
X9313ZMIZ-3* (Note)	13ZEZ			-40 to +85	8 Ld MSOP (Pb-free)	M8.118
X9313ZSZ-3* (Note)	X9313Z ZD			0 to +70	8 Ld SOIC (Pb-free)	M8.15
X9313ZSIZ-3* (Note)	X9313Z ZE			-40 to +85	8 Ld SOIC (Pb-free)	M8.15

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

*Add “T1” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
**Add "T2" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
***Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

Pin Descriptions

RH/VH and RL/VL

The high (RH/VH) and low (RL/VL) terminals of the X9313 are equivalent to the fixed terminals of a mechanical potentiometer. The terminology of RL/VL and RH/VH references the relative position of the terminal in relation to wiper movement direction selected by the U/$\overline{D}$ input and not the voltage potential on the terminal.

RW/VW

RW/VW is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs. The wiper terminal series resistance is typically 40Ω at V_{CC} = 5V.

Up/Down (U/$\overline{D}$)

The U/$\overline{D}$ input controls the direction of the wiper movement and whether the counter is incremented or decremented.

Increment ($\overline{INC}$)

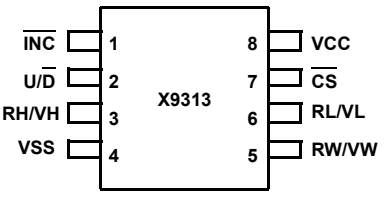
The $\overline{INC}$ input is negative-edge triggered. Toggling $\overline{INC}$ will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the U/$\overline{D}$ input.

Chip Select ($\overline{CS}$)

The device is selected when the $\overline{CS}$ input is LOW. The current counter value is stored in nonvolatile memory when $\overline{CS}$ is returned HIGH while the $\overline{INC}$ input is also HIGH. After the store operation is complete, the X9313 will be placed in the low power standby mode until the device is selected once again.

Pinouts

X9313
(8 LD PDIP, 8 LD SOIC)
TOP VIEW



X9313
(8 LD MSOP)
TOP VIEW

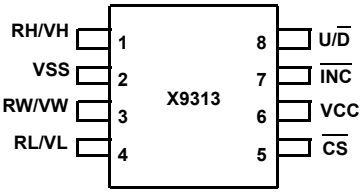


TABLE 1. PIN NAMES

SYMBOL	DESCRIPTION
RH/VH	High terminal
RW/VW	Wiper terminal
RL/VL	Low terminal
VSS	Ground
VCC	Supply voltage
U/$\overline{D}$	Up/Down control input
INC	Increment control input
CS	Chip Select control input

Principles of Operation

There are three sections of the X9313: the input control, counter and decode section; the nonvolatile memory; and the resistor array. The input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. Under the proper conditions, the contents of the counter can be stored in nonvolatile memory and retained for future use. The resistor array is comprised of 31 individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

The electronic switches on the device operate in a “make before break” mode when the wiper changes tap positions. If the wiper is moved several positions, multiple taps are connected to the wiper for t_{IW} (INC to V_W change). The R_{TOTAL} value for the device can temporarily be reduced by a significant amount if the wiper is moved several positions.

When the device is powered-down, the last wiper position stored will be maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the wiper is set to the value last stored.

Instructions and Programming

The $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$ inputs control the movement of the wiper along the resistor array. With $\overline{CS}$ set LOW the device is selected and enabled to respond to the U/$\overline{D}$ and $\overline{INC}$ inputs. HIGH to LOW transitions on $\overline{INC}$ will increment or decrement (depending on the state of the U/$\overline{D}$ input) a seven bit counter. The output of this counter is decoded to select one of thirty-two wiper positions along the resistive array.

The value of the counter is stored in nonvolatile memory whenever $\overline{CS}$ transitions HIGH while the $\overline{INC}$ input is also HIGH.

The system may select the X9313, move the wiper and deselect the device without having to store the latest wiper position in nonvolatile memory. After the wiper movement is performed as previously described and once the new position is reached, the system must keep $\overline{INC}$ LOW while taking $\overline{CS}$ HIGH. The new wiper position will be maintained until changed by the system or until a power-up/down cycle recalled the previously stored data.

This procedure allows the system to always power-up to a preset value stored in nonvolatile memory; then during system operation, minor adjustments could be made. The adjustments might be based on user preference, system parameter changes due to temperature drift, etc.

The state of U/$\overline{D}$ may be changed while $\overline{CS}$ remains LOW. This allows the host system to enable the device and then move the wiper up and down until the proper trim is attained.

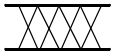
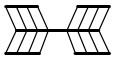
TABLE 2. MODE SELECTION

$\overline{CS}$	$\overline{INC}$	U/$\overline{D}$	MODE
L	↘	H	Wiper up
L	↘	L	Wiper down
↗	H	X	Store wiper position
H	X	X	Standby current
↗	L	X	No store, return to standby

TABLE 2. MODE SELECTION

$\overline{CS}$	$\overline{INC}$	U/$\overline{D}$	MODE
	L	H	Wiper up (not recommended)
	L	L	Wiper down (not recommended)

Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don’t Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Absolute Maximum Ratings

Temperature Under Bias . . . . . -65°C to +135°C
Storage Temperature . . . . . -65°C to +150°C
Voltage on $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$, and
V_{CC} with Respect to V_{SS} . . . . . -1V to +7V
Voltage on V_H, V_L, V_W
with respect to V_{SS} . . . . . -6V to +7V
$\Delta V = |V_H - V_L|$:
X9313Z 4V
X9313W, X9313U 10V
I_W (10s) . . . . . .±8.8mA
ESD Rating
Human Body Model 2.0kV
Machine Model 200V

Recommended Operating Conditions

Temperature:
Commercial . . . . . 0°C to +70°C
Industrial . . . . . -40°C to +85°C
Supply Voltage (VCC):
X9313 . . . . . .5V ±10%
X9313-3 . . . . . 3V to 5.5V
Max Wiper current . . . . . .±4.4mA
Power rating:
$R_{TOTAL} \geq 10k\Omega$ 10mW
R_{TOTAL} 1kΩ 16mW
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp
Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Potentiometer Characteristics

Over recommended operating conditions, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
	End-to-end Resistance Tolerance				±20	%
V_{VH}	V_H Terminal Voltage		$-V_{CC}$		$+V_{CC}$	V
V_{VL}	V_L Terminal Voltage		$-V_{CC}$		$+V_{CC}$	V
R_W	Wiper Resistance	$I_W = (V_H - V_L)/R_{TOTAL}$, V_{CC} = 5V		40	100	Ω
I_W	Wiper Current				±4.4	mA
	Noise (Note 5)	Ref: 1kHz		-120		dBV
	Resolution			3		%
	Absolute Linearity (Note 1)	$R_{W(n)(actual)} - R_{W(n)(expected)}$			±1	MI (Note 3)
	Relative Linearity (Note 2)	$R_{W(n+1)} - (R_{W(n)}+MI)$			±0.2	MI (Note 3)
	R_{TOTAL} Temperature Coefficient (Note 5)			±300		ppm/°C
	Ratiometric Temperature Coefficient (Note 5)			±20		ppm/°C
$C_H/C_L/C_W$ (Note 5)	Potentiometer Capacitances	See Circuit #3		10/10/25		pF

NOTES:

1. Absolute linearity is utilized to determine actual wiper voltage versus expected voltage = $(V_{W(n)(actual)} - V_{W(n)(expected)})$ = ±1 MI maximum.
2. Relative linearity is a measure of the error in step size between taps = $R_{W(n+1)} - (R_{W(n)} + MI)$ = ±0.2 MI.
3. 1 MI = minimum increment = $R_{TOT}/31$.

DC Electrical Specifications

Over recommended operating conditions, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS/NOTES	LIMITS			UNIT
			MIN	TYP (Note 4)	MAX	
I_{SB}	V_{CC} Active Current	$\overline{CS}$ = V_{IL}, U/$\overline{D}$ = V_{IL} or V_{IH} and $\overline{INC}$ = 0.42/2.4V @ max t_{CYC}		1	3	mA
	Standby Supply Current	$\overline{CS}$ = V_{CC} - 0.3V, U/$\overline{D}$ and $\overline{INC}$ = V_{SS} or V_{CC} - 0.3V		200	500	µA
I_{LI}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input Leakage Current	V_{IN} = V_{SS} to V_{CC}			±10	µA
V_{IH}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input HIGH Current		2			V
V_{IL}	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input LOW Current				+0.8	V
C_{IN} (Note 5)	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ Input Capacitance	V_{CC} = 5V, V_{IN} = V_{SS}, T_A = +25°C, f = 1MHz		10		pF

Endurance and Data Retention

PARAMETER	MIN	UNIT
Minimum endurance	100,000	Data changes per bit per register
Data retention	100	Years

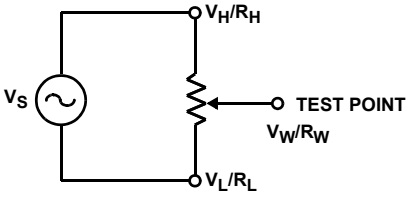


FIGURE 1. TEST CIRCUIT #1

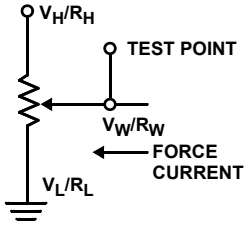


FIGURE 2. TEST CIRCUIT #2

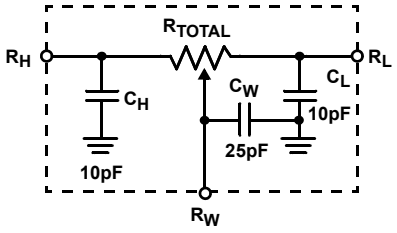


FIGURE 3. CIRCUIT #3 SPICE MACRO MODEL

AC Electrical Specifications Over recommended operating conditions, unless otherwise stated.

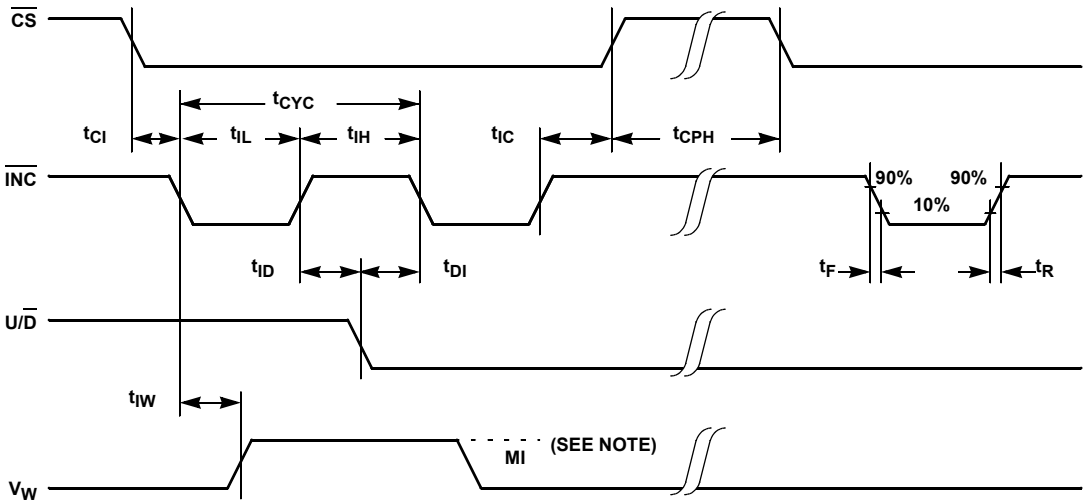
SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	TYP (Note 4)	MAX	
t_{CI}	$\overline{CS}$ to $\overline{INC}$ Setup	100			ns
t_{ID}	$\overline{INC}$ HIGH to U/$\overline{D}$ Change	100			ns
t_{DI}	U/$\overline{D}$ to $\overline{INC}$ Setup	2.9			µs
t_{IL}	$\overline{INC}$ LOW Period	1			µs
t_{IH}	$\overline{INC}$ HIGH Period	1			µs
t_{IC}	$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	1			µs
t_{CPH}	$\overline{CS}$ Deselect Time (STORE)	20			ms
t_{CPH}	$\overline{CS}$ Deselect Time (NO STORE)	100			ns
t_{IW}	$\overline{INC}$ to V_W Change		5		µs
t_{CYC}	$\overline{INC}$ Cycle Time	2			µs
t_R, t_F (Note 5)	$\overline{INC}$ Input Rise and Fall Time			500	µs
t_{PU} (Note 5)	Power-up to Wiper Stable		10		µs
t_R V_{CC} (Note 5)	V_{CC} Power-up Rate	0.2		50	V/ms
t_{WR} (Note 5)	Store Cycle		10		ms

NOTES:

4. Typical values are for T_A = +25°C and nominal supply voltage.
5. This parameter is not 100% tested.

Power-Up and Power-Down Requirements

The recommended power-up sequence is to apply V_{CC}/V_{SS} first, then the potentiometer voltages. During power-up, the data sheet parameters for the DCP do not fully apply until 1ms after V_{CC} reaches its final value. The V_{CC} ramp specification is always in effect. In order to prevent unwanted tap position changes, or an inadvertent store, bring the $\overline{CS}$ and $\overline{INC}$ high before or concurrently with the VCC pin on power-up.



NOTE: MI IN THE AC TIMING DIAGRAM REFERS TO THE MINIMUM INCREMENTAL CHANGE IN THE V_W OUTPUT DUE TO A CHANGE IN THE WIPER POSITION.

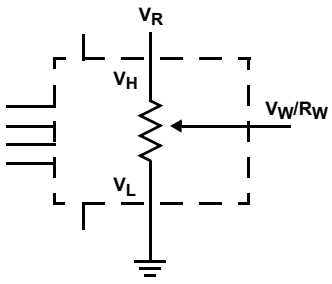
FIGURE 4. AC TIMING DIAGRAM

Applications Information

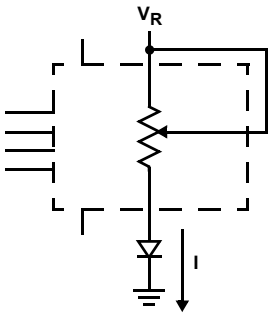
Electronic digitally controlled potentiometers (XDCP) provide three powerful application advantages:

1. The variability and reliability of a solid-state potentiometer.
2. The flexibility of computer-based digital controls.
3. The retentivity of nonvolatile memory used for the storage of multiple potentiometer settings or data.

Basic Configurations of Electronic Potentiometers



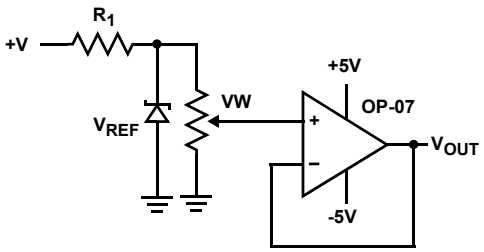
THREE-TERMINAL POTENTIOMETER;
VARIABLE VOLTAGE DIVIDER



TWO-TERMINAL VARIABLE RESISTOR;
VARIABLE CURRENT

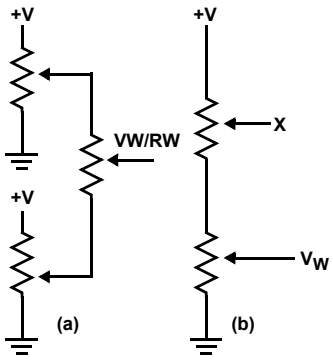
Basic Circuits

BUFFERED REFERENCE VOLTAGE

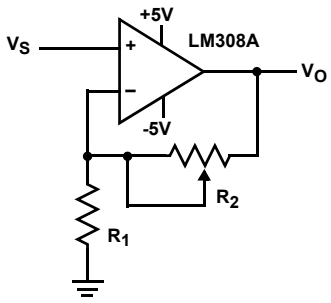


$V_{OUT} = V_W/R_W$

CASCADING TECHNIQUES

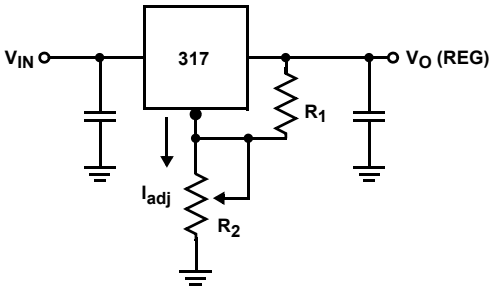


NONINVERTING AMPLIFIER



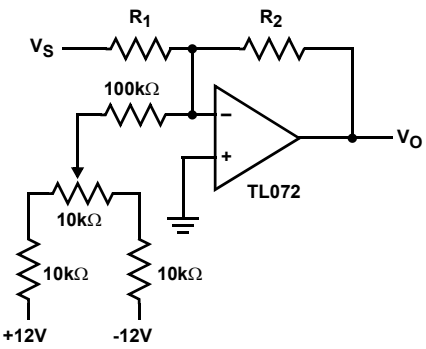
$V_O = (1 + R_2/R_1)V_S$

VOLTAGE REGULATOR

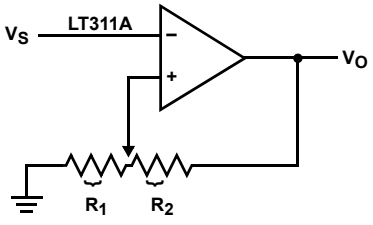


V_O (REG) = 1.25V (1 + R_2/R_1) + I_{ADJ} R_2

OFFSET VOLTAGE ADJUSTMENT



COMPARATOR WITH HYSTERESIS



$V_{UL} = [R_1/(R_1 + R_2)]$ V_O(max)
$V_{LL} = [R_1/(R_1 + R_2)]$ V_O(min)

(FOR ADDITIONAL CIRCUITS SEE AN115)

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
October 7, 2015	FN8177.7	Added Revision History beginning with Rev 7. Added About Intersil Verbiage. Updated Ordering Information on page 2. DC Electrical Spec Table on page 6 - changed I_{CC} for Parameter V_{CC} Active Current to I_{SB} Updated POD M8.118 to most current revision with changes as follows: Corrected lead width dimension in side view 1 from "0.25 - 0.036" to "0.25 - 0.36" Updated to new intersil format by adding land pattern and moving dimensions from table onto drawing. Updated POD M8.15 to most current revision with changes as follows: Changed Note 1 "1982" to "1994" Changed in Typical Recommended Land Pattern the following: 2.41(0.095) to 2.20(0.087) 0.76 (0.030) to 0.60(0.023) 0.200 to 5.20(0.205) Updated to new POD format by removing table and moving dimensions onto drawing and adding land pattern.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

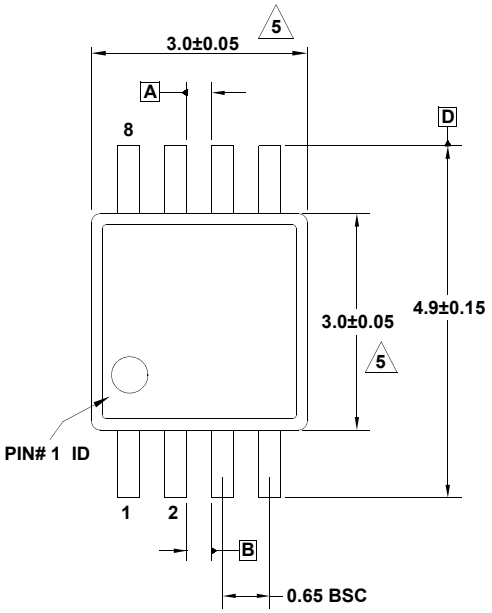
Reliability reports are also available from our website at www.intersil.com/support

Package Outline Drawing

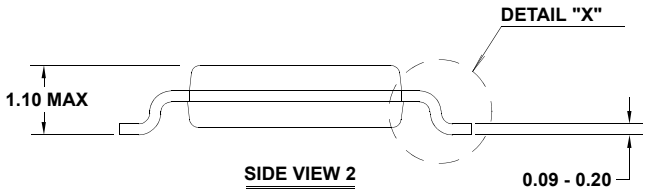
M8.118

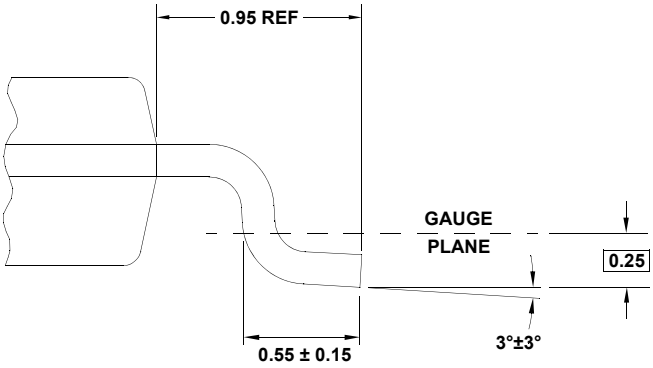
8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

Rev 4, 7/11

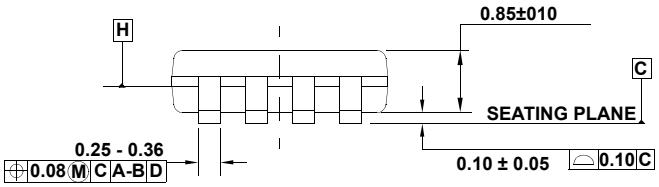


TOP VIEW

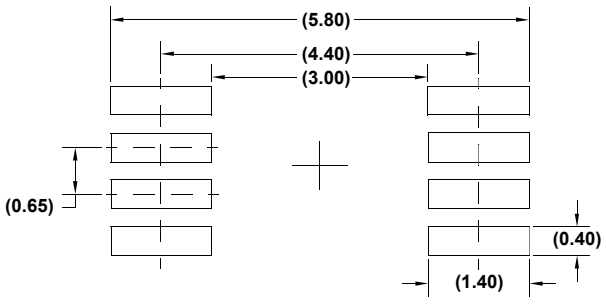




DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

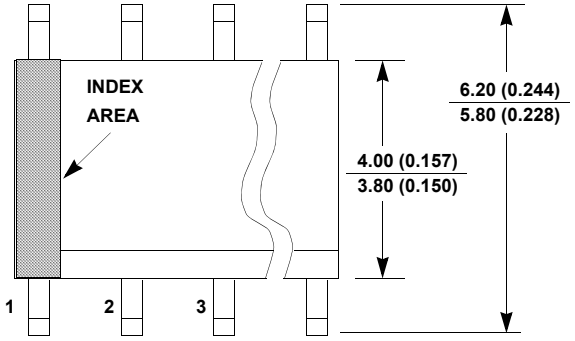
1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.

Package Outline Drawing

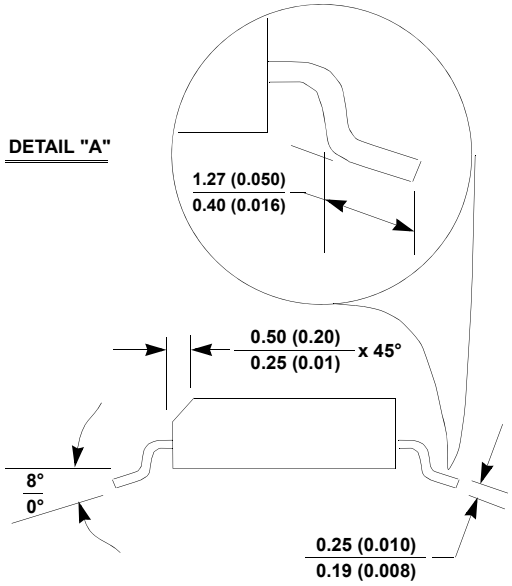
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

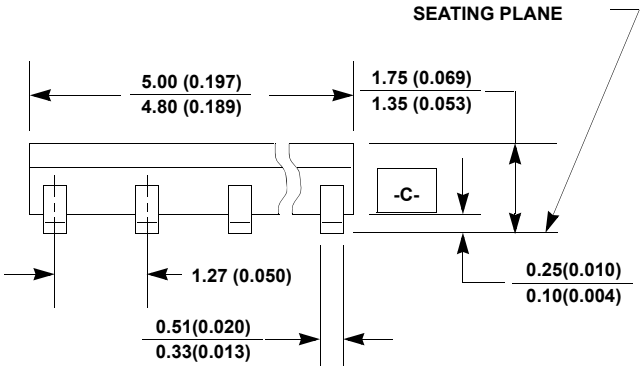
Rev 4, 1/12



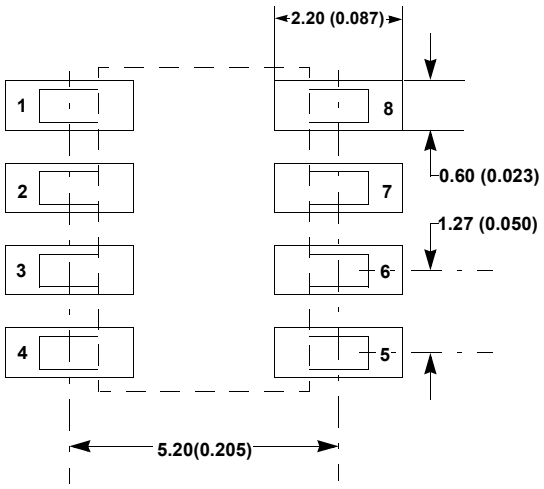
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"

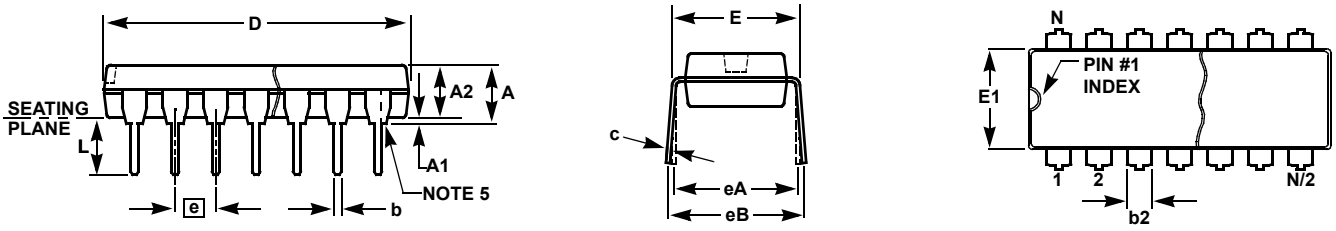


TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

Plastic Dual-In-Line Packages (PDIP)



MDP0031

PLASTIC DUAL-IN-LINE PACKAGE

SYMBOL	INCHES					TOLERANCE	NOTES
	PDIP8	PDIP14	PDIP16	PDIP18	PDIP20		
A	0.210	0.210	0.210	0.210	0.210	MAX	
A1	0.015	0.015	0.015	0.015	0.015	MIN	
A2	0.130	0.130	0.130	0.130	0.130	±0.005	
b	0.018	0.018	0.018	0.018	0.018	±0.002	
b2	0.060	0.060	0.060	0.060	0.060	+0.010/-0.015	
c	0.010	0.010	0.010	0.010	0.010	+0.004/-0.002	
D	0.375	0.750	0.750	0.890	1.020	±0.010	1
E	0.310	0.310	0.310	0.310	0.310	+0.015/-0.010	
E1	0.250	0.250	0.250	0.250	0.250	±0.005	2
e	0.100	0.100	0.100	0.100	0.100	Basic	
eA	0.300	0.300	0.300	0.300	0.300	Basic	
eB	0.345	0.345	0.345	0.345	0.345	±0.025	
L	0.125	0.125	0.125	0.125	0.125	±0.010	
N	8	14	16	18	20	Reference	

Rev. C 2/07

NOTES:

1. Plastic or metal protrusions of 0.010” maximum per side are not included.
2. Plastic interlead protrusions of 0.010” maximum per side are not included.
3. Dimensions E and eA are measured with the leads constrained perpendicular to the seating plane.
4. Dimension eB is measured with the lead tips unconstrained.
5. 8 and 16 lead packages have half end-leads as shown.