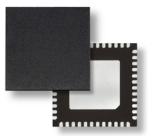
# Multi-output DC/DC regulator for low-power LS1 communication processors

**VR5100**

**POWER MANAGEMENT**



**EP SUFFIX**
**98ASA00719D**
**48 QFN 7.0 X 7.0**

The VR5100 is a high performance, highly integrated, multi-output, DC/DC regulator solution, with integrated power MOSFETs, ideally suited for the LS1 family of communications processors. Integrating three buck converters, six linear regulators, RTC supply and a coin-cell charger, the VR5100 can provide power for a complete system, including communications processors, memory, and system peripherals.

**Features:**

- Three adjustable high efficiency buck regulators: 3.8 A, 1.25 A, 1.5 A
  - Selectable modes: PWM, PFM, APS
- 5.0 V, 600 mA boost regulator with PFM or Auto mode
- Six adjustable general purpose linear regulators
- Input voltage range: 2.8 V to 4.5 V
- OTP (One Time Programmable) memory for device configuration
  - Programmable start-up sequence and timing
  - Selectable output voltage, frequency, soft start
- $I^2C$ control
- Always ON RTC supply and Coin cell charger
- DDR reference voltage
- -40 °C to +125 °C operating junction temperature

**Applications:**

- Network attached storage (NAS)
- Value IOT gateway
- Mobile NAS
- Industrial control
- Home/Factory automation

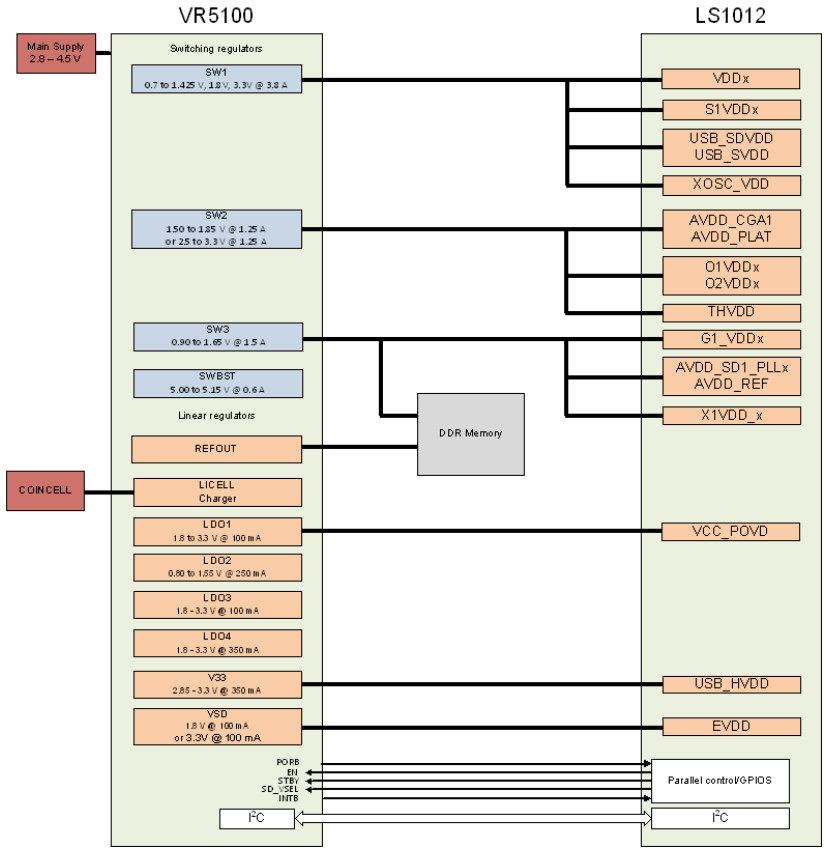



**Figure 1. VR5100 simplified application diagram**

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

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# 1 Orderable parts

The VR5100 is available with pre-programmed OTP memory configurations. The devices are identified using the program codes from Table 1. Details of the OTP programming for each device can be found in Table 37.

**Table 1. Orderable part variations**

| Part Number | Temperature ($T_A$) | Package | Programming Options | Notes |
|---|---|---|---|---|
| MC34VR5100A0EP | -40 °C to 105 °C (For use in Industrial applications) | 48 QFN 7.0 mm x 7.0 mm | 0 - Not programmed | (1) |
| MC34VR5100A1EP | | | 1 (LS1012 with DDR3L) | |
| MC34VR5100A2EP | | | 2 (LX2160 with DDR4) | |

Notes
1. For tape and reel, add an R2 suffix to the part number.

# 2 Internal block diagram

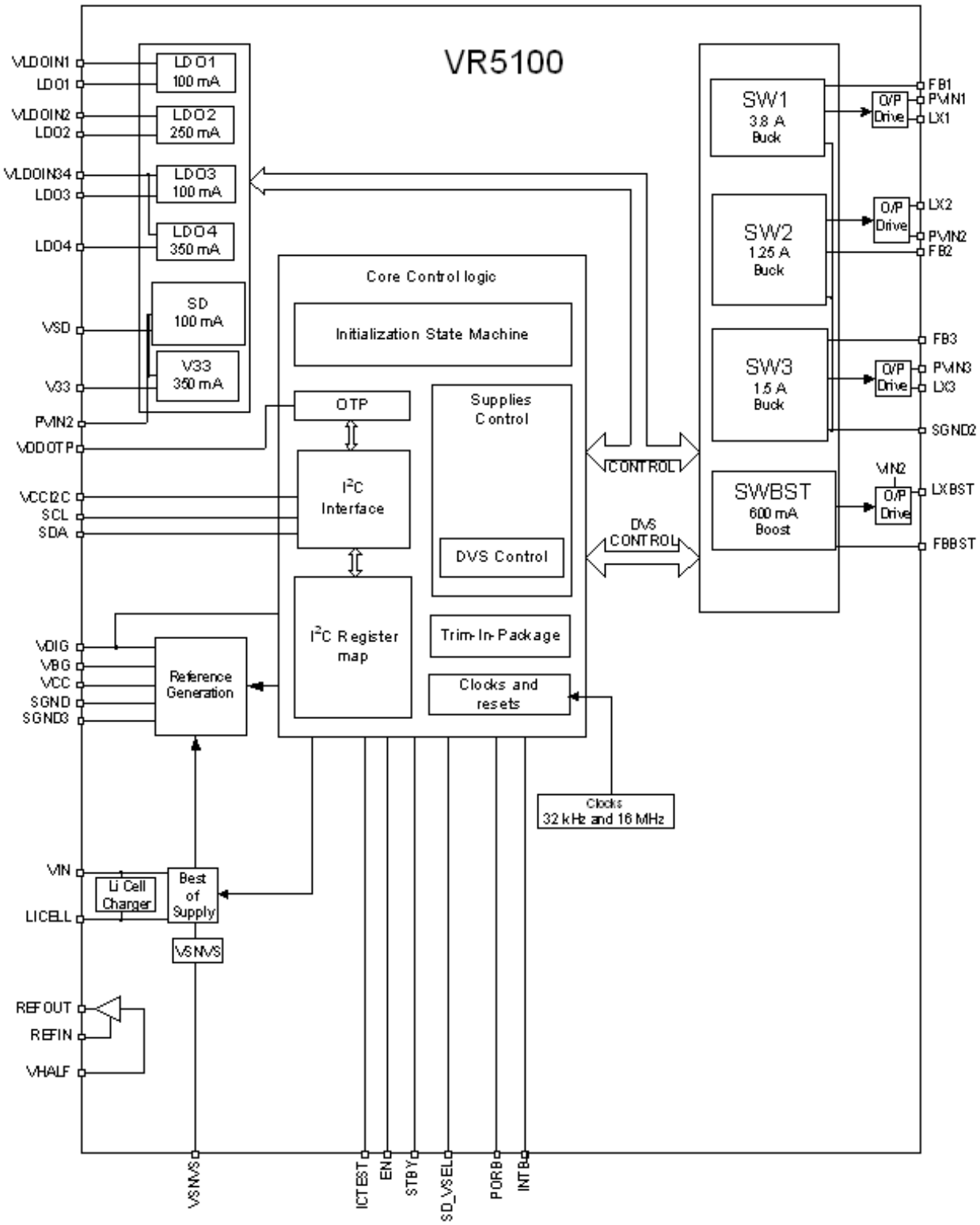



**Figure 2. VR5100 simplified internal block diagram**

# 3 Pin connections

## 3.1 Pinout diagram

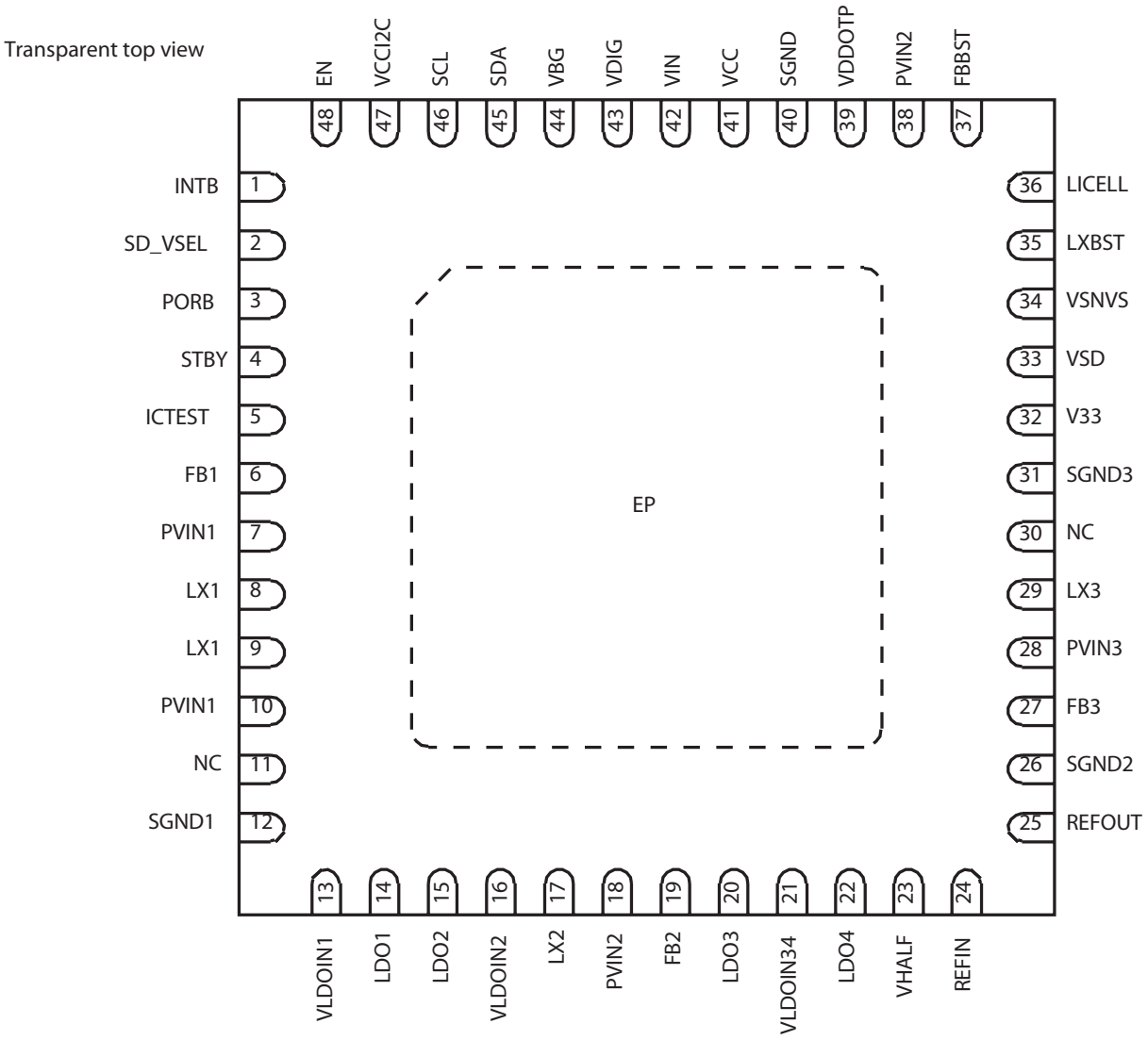



**Figure 3. Pinout diagram**

## 3.2 Pin definitions

**Table 2. Pin definitions**

| Pin number | Pin name | Pin function | Type | Definition |
|---|---|---|---|---|
| - | EP | GND | GND | Expose pad. Functions as ground return for buck and boost regulators. Tie this pad to the inner and external ground planes through vias to allow effective thermal dissipation |
| 1 | INTB | O | Digital | Open drain interrupt signal to processor |
| 2 | SD_VSEL | I/O | Digital | Input from LS1 processor to select SD regulator voltage • SD_VSEL=0, SD = 3.3 V • SD_VSEL= 1, VSD = 1.8 V |
| 3 | PORB | O | Digital | Open drain reset output to processor |
| 4 | STBY | I | Digital | Standby input signal from processor |
| 5 | ICTEST | I | Digital and Analog | Reserved pin. Connect to GND in application |
| 6 | FB1 | I | Analog | SW1 output voltage feedback pin. Route this trace separately from the high current path and terminate at the output capacitance or near the load, if possible for best regulation |
| 7 | PVIN1 | I | Analog | Input to SW1 regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible |
| 8, 9 | LX1 | O | Analog | Switcher 1 switch node connection. Connect to SW1 inductor |
| 10 | PVIN1 | I | Analog | Input to SW1 regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible |
| 11, 30 | NC | — | — | Leave this pin floating |
| 12 | SGND1 | GND | GND | Ground reference for SW1. Connect to GND. Keep away from high current ground return paths |
| 13 | VLDOIN1 | I | Analog | LDO1 input supply. Bypass with a 1.0 µF decoupling capacitor as close to the pin as possible |
| 14 | LDO1 | O | Analog | LDO1 regulator output. Bypass with a 2.2 µF ceramic output capacitor |
| 15 | LDO2 | O | Analog | LDO2 regulator output. Bypass with a 4.7 µF ceramic output capacitor |
| 16 | VLDOIN2 | I | Analog | LDO2 input supply. Bypass with a 1.0 µF decoupling capacitor as close to the pin as possible |
| 17 | LX2 (2) | O | Analog | Switcher 2 switch node connection.Connect to SW2 inductor |
| 18 | PVIN2 (2) | I | Analog | Input to SW2 regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible |
| 19 | FB2 (2) | I | Analog | SW2 output voltage feedback pin. Route this trace separately from the high current path and terminate at the output capacitor or near the load, if possible for best regulation |
| 20 | LDO3 | O | Analog | LDO3 regulator output. Bypass with a 2.2 µF ceramic output capacitor |
| 21 | VLDOIN34 | I | Analog | LDO3 and LDO4 input supply. Bypass with a 1.0 µF decoupling capacitor as close to the pin as possible |
| 22 | LDO4 | O | Analog | LDO4 regulator output. Bypass with a 2.2 µF ceramic output capacitor |
| 23 | VHALF | I | Analog | Half supply reference for REFOUT. Bypass with 0.1 µF to ground. |
| 24 | REFIN | I | Analog | REFOUT regulator input. Connect a 0.1 µF capacitor between REFIN and VHALF pin. Ensure there is at least 1.0 µF net capacitance from REFIN to ground |
| 25 | REFOUT | O | Analog | REFOUT regulator output. Bypass with 1.0 µF to ground |
| 26 | SGND2 | GND | GND | Reference ground for SW2 and SW3 regulators. Connect to GND. Keep away from high current ground return paths |
| 27 | FB3 (2) | I | Analog | SW3 output voltage feedback pin. Route this trace separately from the high current path and terminate at the output capacitor or near the load, if possible for best regulation |
| 28 | PVIN3 (2) | I | Analog | Input to SW3 regulator. Bypass with at least a 4.7 µF ceramic capacitor and a 0.1 µF decoupling capacitor as close to the pin as possible |
| 29 | LX3 (2) | O | Analog | Switcher 3 switch node connection. Connect the SW3 inductor |

**Table 2. Pin definitions (continued)**

| | | | | |
|---|---|---|---|---|
| 31 | SGND3 | GND | GND | Connect to GND. |
| 32 | V33 | O | Analog | V33 regulator output. Bypass with a 4.7 µF ceramic output capacitor |
| 33 | VSD | O | Analog | Output of VSD regulator. Bypass with a 2.2 µF ceramic output capacitor. |
| 34 | VSNVS | O | Analog | VSNVS regulator/switch output. Bypass with 0.47 µF capacitor to ground. |
| 35 | LXBST (2) | I/O | Analog | SWBST switch node connection. Connect to SWBST inductor and anode of Schottky diode |
| 36 | LICELL | I/O | Analog | Coin cell supply input/output. Bypass with 0.1 µF capacitor. Connect to optional coin cell |
| 37 | FBBST (2) | I | Analog | SWBST output voltage feedback pin. Route this trace separately from the high current path and terminate at the output capacitor |
| 38 | PVIN2 | I | Analog | Input to SD, V33 regulators and SWBST control circuitry. Connect to VIN rail and bypass with 10 µF capacitor |
| 39 | VDDOTP | I | Digital & Analog | Supply to program OTP fuses. Connect VDDOTP to GND during normal application |
| 40 | SGND | GND | GND | Ground reference for IC core circuitry. Connect to ground. Keep away from high current ground return paths |
| 41 | VCC | O | Analog | Internal analog core supply. Bypass with 1 µF capacitor to ground |
| 42 | VIN | I | Analog | Main IC supply. Bypass with 1.0 µF capacitor to ground. Connect to system input supply. |
| 43 | VDIG | O | Analog | Internal digital core supply. Bypass with 1.0 µF capacitor to ground |
| 44 | VBG | O | Analog | Main band gap reference. Bypass with 220 nF capacitor to ground |
| 45 | SDA | I/O | Digital | $I^2C$ data line (open drain). Pull up to VCCI2C with a 4.7 kΩ resistor |
| 46 | SCL | I | Digital | $I^2C$ clock. Pull up to VCCI2C with a 4.7 kΩ resistor |
| 47 | VCCI2C | I | Analog | Supply for $I^2C$ bus. Bypass with 0.1 µF ceramic capacitor. Connect to 1.7 to 3.6 V supply. Ensure VCCI2C is always lesser than or equal to VIN |
| 48 | EN | I | Digital | Power ON/OFF input from processor |

Notes

2. Unused switching regulators should be connected as follows: Pins SWxLX and SWxFB should be unconnected and Pin SWxIN should be connected to VIN with a 0.1 µF bypass capacitor.

# 4 General product characteristics

## 4.1 Absolute maximum ratings

**Table 3. Absolute maximum voltage ratings**

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause malfunction or permanent damage to the device. The detailed maximum voltage rating per pin can be found in the pin list section.

| Symbol | Description | Value | Unit | Notes |
|---|---|---|---|---|
| **Electrical ratings** | | | | |
| ICTEST, LXBST | – | -0.3 to 7.5 | V | |
| VIN, PVIN2, VLDOIN1, PVIN1, PVIN2, PVIN3, LX1, LX2, LX3 | – | -0.3 to 4.8 | V | |
| VDDOTP | OTP programming input supply voltage | -0.3 to 10.0 | V | (3) |
| FBBST | Boost switcher feedback | -0.3 to 5.5 | V | |
| INTB, SD_VSEL, PORB, STBY, FB1, FB2, FB3, LDO1, VLDOIN2, VLDOIN34, LDO3, LDO4, VHALF, REFIN, REFOUT, V33, VSD, VSNVS, LICELL, VCC, SDA, SCL, VCCI2C, EN | – | -0.3 to 3.6 | V | |
| LDO2 | LDO2 linear regulator output | -0.3 to 2.5 | V | |
| VDIG | Digital core supply voltage output | -0.3 to 1.65 | V | |
| VBG | Bandgap reference voltage output | -0.3 to 1.5 | V | |
| $V_{ESD}$ | ESD ratings<br>• Human body model<br>• Charge device model | <br>±2000<br>±500 | V | (4) |

Notes

3. 10 V Maximum voltage rating during OTP fuse programming. 7.5 V Maximum DC voltage rated otherwise.
4. ESD testing is performed in accordance with the Human Body Model (HBM) ($C_{ZAP}$ = 100 pF, $R_{ZAP}$ = 1500 Ω), and the Charge device model (CDM), Robotic ($C_{ZAP}$ = 4.0 pF).

# 4.2 Thermal characteristics

**Table 4. Thermal ratings**

| Symbol | Description (Rating) | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| **Thermal ratings** | | | | | |
| $T_A$ | Ambient operating temperature range<br>• Industrial version | -40 | 105 | °C | |
| $T_J$ | Operating junction temperature range | -40 | 125 | °C | (5) |
| $T_{ST}$ | Storage temperature range | -65 | 150 | °C | |
| $T_{PPRT}$ | Peak package reflow temperature | – | (7) | °C | (6) (7) |
| **QFN48 thermal resistance and package dissipation ratings** | | | | | |
| $R_{\theta JA}$ | Junction to ambient, natural convection<br>• Four layer board (2s2p)<br>• Eight layer board (2s6p) | <br>–<br>– | <br>24<br>15 | °C/W | (8) (9) (10) |
| $R_{\theta JB}$ | Junction to board | – | 11 | °C/W | (11) |
| $R_{\Theta JCBOTTOM}$ | Junction to case bottom | – | 1.4 | °C/W | (12) |
| $\Psi JT$ | Junction to package top<br>• Natural convection | – | 1.3 | °C/W | (13) |

Notes

5. Do not operate beyond 125 °C for extended periods of time. Operation above 150 °C may cause permanent damage to the IC. See Thermal Protection Thresholds for thermal protection features.
6. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.
7. NXP's package reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For peak package reflow temperature and moisture sensitivity levels (MSL), go to www.nxp.com, search by part number (remove prefixes/suffixes) and enter the core ID to view all orderable parts, and review parametrics.
8. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
9. The Board uses the JEDEC specifications for thermal testing (and simulation) JESD51-7 and JESD51-5.
10. Per JEDEC JESD51-6 with the board horizontal.
11. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
12. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
13. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters ($\Psi JT$) are not available, the thermal characterization parameter is written as Psi-JT.

# 4.3 Current consumption

The current consumption of the individual blocks is described in detail in the following table.

**Table 5. Current consumption summary**

$T_A$= -40 °C to 105 °C, $V_{IN}$ = 3.6 V, $V_{CCI2C}$ = 1.7 V to 3.6 V, $L_{ICELL}$ = 1.8 V to 3.3 V, $V_{SNVS}$ = 3.0 V, typical external component values, unless otherwise noted. Typical values are characterized at VIN = 3.6 V, $V_{CCI2C}$ = 3.3 V, $L_{ICELL}$ = 3.0 V, $V_{SNVS}$ = 3.0 V and 25 °C, unless otherwise noted.

| Mode | VR5100 Conditions | System Conditions | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| Coin Cell | VSNVS from LICELL, All other blocks off, VIN = 0.0 V | No load on VSNVS | 4.0 | 7.0 | µA | (14) (15) |
| Off | VSNVS from VIN or LICELL<br>Wake-up from EN active<br>32 kHz RC on<br>All other blocks off<br>VIN ≥ UVDET | No load on VSNVS, PMIC able to wake-up | 16 | 25 | µA | (14) (15) |
| Sleep LPSR | VSNVS from VIN<br>Wake-up from EN active<br>Trimmed reference active<br>SW3 PFM. All other regulators off.<br>Trimmed 16 MHz RC off<br>32 kHz RC on<br>REFOUT disabled | No load on any of the regulators | 130 (14)<br>200 (17) | 220 (14) | µA | (16) |
| | LDO1 & LDO3 activated in addition to SW3 | No load on any of the regulators | 170 (14)<br>260 (17) | 248 (14) | µA | (16) |
| Standby | VSNVS from either VIN or LICELL<br>SW1 in PFM<br>SW2 in PFM<br>SW3 in PFM<br>SWBST off<br>Trimmed 16 MHz RC enabled<br>Trimmed reference active<br>LDO1-4 enabled<br>V33 enabled<br>VSD enabled<br>REFOUT enabled | No load on any of the regulators | 297 | 450 | µA | (16) |
| ON | VSNVS from VIN<br>SW1 in APS<br>SW2 in APS<br>SW3 in APS<br>SWBST off<br>Trimmed 16 MHz RC enabled<br>Trimmed reference active<br>LDO1-4 enabled<br>V33 enabled<br>VSD enabled<br>REFOUT enabled | No load on any of the regulators | 1.2 | | mA | |

Notes

14. At 25 °C only
15. When $V_{IN}$ is below the UVDET threshold, in the range of 1.8 V ≤ $V_{IN}$ < 2.65 V, the quiescent current increases by 50 µA, typically.
16. For PFM operation, headroom should be 300 mV or greater.
17. At 105 °C only

# 4.4 Electrical characteristics

**Table 6. Static electrical characteristics – SW1**

All parameters are specified at $T_A$ = -40 °C to 105 °C, $V_{IN}$ = $V_{PVIN1}$ = 3.6 V, $V_{SW1}$ = 1.2 V, $I_{SW1}$ = 100 mA, typical external component values, $f_{SW1}$ = 2.0 MHz, unless otherwise noted. Typical values are characterized at $V_{IN}$ = $V_{PVIN1}$ = 3.6 V, $V_{SW1}$ = 1.2 V, $I_{SW1}$ = 100 mA, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **Switch mode supply SW1** | | | | | | |
| $V_{PVIN1}$ | Operating input voltage | 2.8 | – | 4.5 | V | (18) |
| $V_{SW1}$ | Nominal output voltage | – | Table 46 | – | V | |
| $V_{SW1ACC}$ | Output voltage accuracy<br>• PWM, APS, 2.8 V < $V_{PVIN1}$ < 4.5 V, 0 < $I_{SW1}$ < 3.8 A<br>0.7 V ≤ $V_{SW1}$ ≤ 1.2 V<br>• PFM, APS, 2.8 V < $V_{PVIN1}$ < 4.5 V, 0 < $I_{SW1}$ < 3.8 A<br>1.225 V < $V_{SW1}$ < 1.425 V<br>• PFM, steady state, 2.8 V < $V_{PVIN1}$ < 4.5 V, 0 < $I_{SW1}$ < 150 mA<br>1.8 V ≤ $V_{SW1}$ ≤ 1.425 V<br>• PWM, APS, 2.8 V < $V_{PVIN1}$ < 4.5 V, 0 < $I_{SW1}$ < 2.75A<br>1.8 V < $V_{SW1}$ < 3.3 V<br>• PFM, steady state, 2.8 V < $V_{PVIN1}$ < 4.5 V, 0 < $I_{SW1}$ < 150 mA<br>1.8 V ≤ $V_{SW1}$ ≤ 3.3 V | -25<br><br>-25<br><br>-45<br><br>-6.0<br><br>-6.0 | – | 25<br><br>35<br><br>45<br><br>6.0<br><br>6.0 | mV<br><br>mV<br><br>mV<br><br>%<br><br>% | |
| $I_{SW1}$ | Rated output load current,<br>• 2.8 V ≤ $V_{PVIN1}$ ≤ 4.5 V, 0.7 V < $V_{SW1}$ < 1.425 V, 1.8V, 3.3V | 3800 | – | – | mA | |
| $I_{SW1Q}$ | Quiescent current<br>• PFM Mode<br>• APS Mode | <br>–<br>– | <br>22<br>300 | <br>–<br>– | µA | |
| $I_{SW1LIM}$ | Current limiter peak current detection , current through inductor<br>• SW1ILIM = 0<br>• SW1ILIM = 1 | <br>4<br>2.6 | <br>5.5<br>4.0 | <br>8.0<br>5.4 | A | |
| $\Delta V_{SW1}$ | Output ripple | – | 5.0 | – | mV | |
| $R_{SW1DIS}$ | Discharge resistance | – | 600 | – | Ω | |
| **Switch mode supply SW1** | | | | | | |
| $V_{SW1OSH}$ | Start-up overshoot, $I_{SW1}$ = 0 mA, DVS clk = 25 mV/4 µs, $V_{IN}$ = $V_{PVIN1}$ = 4.5 V, $V_{SW1}$ = 1.425 V | – | – | 66 | mV | |
| $t_{ONSW1}$ | Turn-on time, enable to 90% of end value, $I_{SW1}$ = 0 mA, DVS clk = 25 mV/4 µs, $V_{IN}$ = $V_{PVIN1}$ = 4.5 V, $V_{SW1}$ = 1.425 V | – | – | 500 | µs | |

Notes

18. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any VR5100 regulator, or external system supply.

**Table 7. Static electrical characteristics – SW2**

All parameters are specified at $T_A$ = -40 °C to 105 °C, $V_{IN}$ = $V_{PVIN2}$ = 3.6 V, $V_{SW2}$ = 3.15 V, $I_{SW2}$ = 100 mA, typical external component values, $f_{SW2}$ = 2.0 MHz, unless otherwise noted. Typical values are characterized at $V_{IN}$ = $V_{PVIN2}$ = 3.6 V, $V_{SW2}$ = 3.15 V, $I_{SW2}$ = 100 mA, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **Switch mode supply SW2** | | | | | | |
| $V_{PVIN2}$ | Operating input voltage | 2.8 | – | 4.5 | V | (19) |
| $V_{SW2}$ | Nominal output voltage | – | Table 48 | – | V | |
| $V_{SW2ACC}$ | Output voltage accuracy<br>• PWM, APS, 2.8 V ≤ $V_{PVIN2}$ ≤ 4.5 V, 0 ≤ $I_{SW2}$ ≤ 1.25 A<br>• 1.50 V ≤ $V_{SW2}$ ≤ 1.85 V<br>• 2.5 V ≤ $V_{SW2}$ ≤ 3.3 V<br>• PFM, 2.8 V ≤ $V_{PVIN2}$ ≤ 4.5 V, 0 ≤ $I_{SW2}$ ≤ 50 mA<br>• 1.50 V ≤ $V_{SW2}$ ≤ 1.85 V<br>• 2.5 V ≤ $V_{SW2}$ ≤ 3.3 V | <br><br>-3.0%<br>-6.0%<br><br>-6.0%<br>-6.0% | <br><br>–<br>–<br><br>–<br>– | <br><br>3.0%<br>6.0%<br><br>6.0%<br>6.0% | % | |
| $I_{SW2}$ | Rated output load current,<br>2.8 V < $V_{PVIN2}$ < 4.5 V, 1.50 V < $V_{SW2}$ < 1.85 V, 2.5 V < $V_{SW2}$ < 3.3 V | 1250 | – | – | mA | (20) |
| $I_{SW2Q}$ | Quiescent current<br>• PFM mode<br>• APS mode (Low output voltage settings)<br>• APS mode (High output voltage settings, SW2_HI=1) | <br>–<br>–<br>– | <br>23<br>145<br>305 | <br>–<br>–<br>– | µA | |
| $I_{SW2LIM}$ | Current limiter peak current detection, current through inductor<br>• SW2ILIM = 0<br>• SW2ILIM = 1 | <br>1.625<br>1.235 | <br>2.5<br>1.9 | <br>3.375<br>2.565 | A | |
| $\Delta V_{SW2}$ | Output ripple | – | 5.0 | – | mV | |
| $R_{ONSW2P}$ | SW2 P-MOSFET $R_{DS(on)}$ at $V_{IN}$ = $V_{PVIN2}$ = 3.3 V | – | 215 | 245 | mΩ | |
| $R_{ONSW2N}$ | SW2 N-MOSFET $R_{DS(on)}$ at $V_{IN}$ = $V_{PVIN2}$ = 3.3 V | – | 258 | 326 | mΩ | |
| $I_{SW2PQ}$ | SW2 P-MOSFET leakage current, $V_{IN}$ = $V_{PVIN2}$ = 4.5 V | – | – | 10.5 | µA | |
| $I_{SW2NQ}$ | SW2 N-MOSFET leakage current, $V_{IN}$ = $V_{PVIN2}$ = 4.5 V | – | – | 3.0 | µA | |
| $R_{SW2DIS}$ | Discharge resistance during OFF mode | – | 600 | – | Ω | |
| $V_{SW2OSH}$ | Start-up overshoot, $I_{SW2}$ = 0.0 mA, DVS clk = 25 mV/4 µs,<br>$V_{IN}$ = $V_{PVIN2}$ = 4.5 V | – | – | 66 | mV | |
| $t_{ONSW2}$ | Turn-on time, enable to 90% of end value, $I_{SW2}$ = 0.0 mA,<br>DVS clk = 25 mV/4 µs, $V_{IN}$ = $V_{PVIN2}$ = 4.5 V | – | – | 500 | µs | |

Notes

19. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any VR5100 regulator, or external system supply.
20. The higher output voltages available depend on the voltage drop in the conduction path as given by the following equation: ($V_{PVIN2}$ - $V_{SW2}$) = $I_{SW2}$* (DCR of Inductor + $R_{ONSW2P}$ + PCB trace resistance).

**Table 8. Static electrical characteristics – SW3**

All parameters are specified at $T_A$ = -40 °C to 105 °C, $V_{IN}$ = $V_{PVIN3}$ = 3.6 V, $V_{SW3}$ = 1.5 V, $I_{SW3}$ = 100 mA, typical external component values, $f_{SW3}$ = 2.0 MHz. Typical values are characterized at $V_{IN}$ = $V_{PVIN3}$ = 3.6 V, $V_{SW3}$ = 1.5 V, $I_{SW3}$ = 100 mA, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **Switch mode supply SW3** | | | | | | |
| $V_{PVIN3}$ | Operating input voltage | 2.8 | – | 4.5 | V | (21) |
| $V_{SW3}$ | Nominal output voltage | – | Table 50 | – | V | |
| $V_{SW3ACC}$ | Output voltage accuracy<br>• PWM, APS, 2.8 V < $V_{PVIN3}$ < 4.5 V, 0 < $I_{SW3}$ < 1.5 A, 0.9 V < $V_{SW3}$ < 1.65 V<br>• PFM, steady state (2.8 V < $V_{PVIN3}$ < 4.5 V, 0 < $I_{SW3}$ < 50 mA), 0.9 V < $V_{SW3}$ < 1.65 V | -3.0%<br>-6.0% | –<br>– | 3.0%<br>6.0% | % | |
| $I_{SW3}$ | Rated output load current, 2.8 V < $V_{PVIN3}$ < 4.5 V, 0.9 V < $V_{SW3}$ < 1.65 V, PWM, APS mode | 1500 | – | – | mA | (22) |
| $I_{SW3Q}$ | Quiescent current<br>• PFM Mode<br>• APS Mode | –<br>– | 50<br>150 | –<br>– | µA | |
| $I_{SW3LIM}$ | Current limiter peak current detection, current through inductor<br>• SW3ILIM = 0<br>• SW3ILIM = 1 | 1.95<br>1.45 | 3.0<br>2.25 | 4.05<br>3.05 | A | |
| $\Delta V_{SW3}$ | Output ripple | – | 5.0 | – | mV | |
| $R_{ONSW3P}$ | SW3 P-MOSFET $R_{DS(on)}$at $V_{IN}$ = $V_{SW3IN}$ = 3.3 V | – | 205 | 235 | mΩ | |
| $R_{ONSW3N}$ | SW3 N-MOSFET $R_{DS(on)}$ at $V_{IN}$ = $V_{SW3IN}$ = 3.3 V | – | 250 | 315 | mΩ | |
| $I_{SW3PQ}$ | SW3 P-MOSFET leakage current, $V_{IN}$ = $V_{SW3IN}$ = 4.5 V | – | – | 12 | µA | |
| $I_{SW3NQ}$ | SW3 N-MOSFET leakage current, $V_{IN}$ = $V_{SW3IN}$ = 4.5 V | – | – | 4.0 | µA | |
| $R_{SW3DIS}$ | Discharge resistance during Off mode | – | 600 | – | Ω | |
| $V_{SW3OSH}$ | Start-up overshoot, $I_{SW3}$ = 0.0 mA, DVS clk = 25 mV/4 µs, $V_{IN}$ = $V_{PVIN3}$ = 4.5 V | – | – | 66 | mV | |
| $t_{ONSW3}$ | Turn-on time, enable to 90% of end value, $I_{SW3}$ = 0 mA, DVS clk = 25 mV/4 µs, $V_{IN}$ = $V_{PVIN3}$ = 4.5 V | – | – | 500 | µs | |

Notes

21. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any VR5100 regulator, or external system supply.
22. The higher output voltages available depend on the voltage drop in the conduction path as given by the following equation: ($V_{SW3IN}$ - $V_{SW3}$) = $I_{SW3}$* (DCR of Inductor +$R_{ONSW3P}$ + PCB trace resistance).

**Table 9. Static electrical characteristics - SWBST**

All parameters are specified at $T_A$ = -40 °C to 105 °C, $V_{IN}$ = $V_{SWBSTIN}$ = 3.6 V, $V_{SWBST}$ = 5.0 V, $I_{SWBST}$ = 100 mA, typical external component values, $f_{SWBST}$ = 2.0 MHz, otherwise noted. Typical values are characterized at $V_{IN}$ = $V_{SWBSTIN}$ = 3.6 V, $V_{SWBST}$ = 5.0 V, $I_{SWBST}$ = 100 mA, and 25 °C, unless otherwise noted.

| Symbol | Parameters | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **Switch mode supply SWBST** | | | | | | |
| $V_{SWBSTIN}$ | Input voltage range | 2.8 | – | 4.5 | V | (23) |
| $V_{SWBST}$ | Nominal output voltage | – | Table 52 | – | V | |
| $I_{SWBST}$ | Continuous load current<br>• 2.8 V ≤ $V_{IN}$ ≤ 3.0 V<br>• 3.0 V ≤ $V_{IN}$ ≤ 4.5 V | <br>500<br>600 | <br>–<br>– | <br>–<br>– | mA | |
| $V_{SWBSTACC}$ | Output voltage accuracy, 2.8 V ≤ $V_{IN}$ ≤ 4.5 V, 0 < $I_{SWBST}$ < $I_{SWBSTMAX}$ | -4.0 | – | 3.0 | % | |
| $I_{SWBSTQ}$ | Quiescent current (auto mode) | – | 222 | 289 | µA | |
| $\Delta V_{SWBST}$ | Output ripple, 2.8 V ≤ $V_{IN}$ ≤ 4.5 V, 0 < $I_{SWBST}$ < $I_{SWBSTMAX}$, excluding reverse recovery of Schottky diode | – | – | 120 | mVp-p | |
| $I_{SWBSTLIM}$ | Peak Current Limit | 1400 | 2200 | 3200 | mA | (24) |
| $R_{DSONBST}$ | MOSFET on resistance | – | 206 | 306 | mΩ | |
| $I_{SWBSTHSQ}$ | NMOS Off leakage, $V_{SWBST}$ = 4.5 V, SWBSTMODE [1:0] = 00 | – | 1.0 | 5.0 | µA | |
| $V_{SWBSTOSH}$ | Start-up overshoot, $I_{SWBST}$ = 0.0 mA | – | – | 500 | mV | |
| $t_{ONSWBST}$ | Turn-on time, enable to 90% of VSWBST, ISWBST = 0.0 mA | – | – | 2.0 | ms | |

Notes

23. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any VR5100 regulator, or external system supply.
24. Only in Auto and APS modes.

**Table 10. Static electrical characteristics - VSNVS**

All parameters are specified at $T_A$ = -40 °C to 105 °C, $V_{IN}$ = 3.6 V, $V_{SNVS}$ = 3.0 V, $I_{SNVS}$ = 5.0 µA, typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN}$ = 3.6 V, $V_{SNVS}$ = 3.0 V, $I_{SNVS}$ = 5.0 µA, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **VSNVS** | | | | | | |
| $V_{IN}$ | Operating input voltage<br>• Valid coin cell range<br>• Valid $V_{IN}$ | <br>1.8<br>2.25 | <br>-<br>– | <br>3.3<br>4.5 | V | |
| $I_{SNVS}$ | Operating load current, $V_{INMIN}$ < $V_{IN}$ < $V_{INMAX}$ | 1.0 | – | 1000 | µA | |
| $V_{SNVS}$ | Output voltage<br>• 5.0 µA < $I_{SNVS}$ < 1000 µA (OFF), 3.20 V < $V_{IN}$ < 4.5 V<br>• 5.0 µA < $I_{SNVS}$ < 1000 µA (ON), 3.20 V < $V_{IN}$ < 4.5 V<br>• 5.0 µA < $I_{SNVS}$ < 1000 µA (Coin Cell mode), 2.84 V < $V_{COIN}$ < 3.3 V | <br>-5.0%<br>-5.0%<br>$V_{COIN}$-0.10 | <br>3.0<br>3.0 | <br>7.0%<br>5.0%<br>$V_{COIN}$ | V | |
| $V_{SNVSDROP}$ | Dropout voltage, 2.85 V < $V_{IN}$ < 2.9 V, 1.0 µA < $I_{SNVS}$ < 1000 µA | – | – | 110 | mV | |
| $I_{SNVSLIM}$ | Current limit, $V_{IN}$ > $V_{TH1}$ | 1100 | – | 6750 | µA | |
| **VSNVS DC, SWITCH** | | | | | | |
| $V_{LICELL}$ | Operating input voltage, valid coin cell range | 1.8 | – | 3.3 | V | |
| $I_{SNVS}$ | Operating load current | 1.0 | – | 1000 | µA | |
| $R_{DSONSNVS}$ | Internal switch $R_{DS(on)}$ | – | – | 100 | Ω | |

**Table 11. Dynamic electrical characteristics - VSNVS**

All parameters are specified at $T_A$ = -40 °C to 105 °C, $V_{IN}$ = 3.6 V, $V_{SNVS}$ = 3.0 V, $I_{SNVS}$ = 5.0 μA, typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN}$ = 3.6 V, $V_{SNVS}$ = 3.0 V, $I_{SNVS}$ = 5.0 μA, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **VSNVS** | | | | | | |
| $V_{SNVSTON}$ | Turn-on time (load capacitor, 0.47 μF), from $V_{IN}$ = $V_{TH1}$ to 90% of $V_{SNVS}$, $V_{COIN}$ = 0.0 V, $I_{SNVS}$ = 5.0 μA | – | – | 24 | ms | (25),(26) |
| $V_{SNVSOSH}$ | Start-up overshoot, $I_{SNVS}$ = 5.0 μA | – | 40 | 70 | mV | |
| $V_{SNVSLOTR}$ | Transient load response, 3.2 < $V_{IN}$ ≤ 4.5 V, $I_{SNVS}$ = 100 to 1000 μA | 2.8 | – | – | V | |
| $V_{TL1}$ | $V_{IN}$ falling threshold ($V_{IN}$ powered to coin cell powered) | 2.45 | 2.70 | 3.05 | V | |
| $V_{TH1}$ | $V_{IN}$ Rising Threshold (coin cell powered to $V_{IN}$ powered) | 2.5 | 2.75 | 3.10 | V | |
| $V_{HYST1}$ | $V_{IN}$ threshold hysteresis for $V_{TH1}$-$V_{TL1}$ | 5.0 | - | - | mV | |
| $V_{SNVSCROSS}$ | Output voltage during crossover, $V_{COIN}$ > 2.9 V, Switch to LDO: $V_{IN}$ > $V_{TH1}$, $I_{SNVS}$ = 100 μA, LDO to Switch: $V_{IN}$ < $V_{TL1}$, $I_{SNVS}$ = 100 μA | 2.45 | - | - | V | |

Notes

25. The start-up of $V_{SNVS}$ is not monotonic. It first rises to 1.0 V and then settles to 3.0 V.
26. From coin cell insertion to VSNVS = 1.0 V, the delay time is typically 400 ms.

**Table 12. Static electrical characteristics - LDO1**

All parameters are specified at $T_A$ = -40 °C to 105 °C, $V_{IN}$ = 3.6 V, $V_{LDOIN1}$ = 3.6 V, $V_{LDO1}$ = 3.3 V, $I_{LDO1}$ = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN}$ = 3.6 V, $V_{LDOIN1}$ = 3.6 V, $V_{LDO1}$ = 3.3 V, $I_{LDO1}$ = 10 mA, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **LDO1 linear regulator** | | | | | | |
| $V_{LDOIN1}$ | Operating input voltage<br>• 1.8 V ≤ $V_{LDO1NOM}$ ≤ 2.5 V<br>• 2.6 V ≤ $V_{LDO1NOM}$ ≤ 3.3 V | 2.8<br>$V_{LDO1NOM}$ +0.250 | –<br>– | 4.5<br>4.5 | V | (27) |
| $V_{LDO1NOM}$ | Nominal output voltage | – | Table 55 | – | V | |
| $I_{LDO1}$ | Rated output load current | 100 | – | – | mA | |
| $V_{LDO1TOL}$ | Output voltage tolerance, $V_{LDO1INMIN}$ < $V_{LDOIN1}$ < 4.5 V, 0.0 mA < $I_{LDO1}$ < 100 mA, LDO1 = 1.8 V to 3.3 V | -3.0 | – | 3.0 | % | |
| $I_{LDO1Q}$ | Quiescent current, no load, change in $I_{VIN,}$ when LDO1 enabled | – | 13 | – | μA | |
| $I_{LDO1LIM}$ | Current limit, $I_{LDO1}$ when $V_{LDO1}$ is forced to $V_{LDO1NOM}$/2 | 122 | 167 | 280 | mA | |

Notes

27. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any VR5100 regulator, or external system supply.

**Table 13. Dynamic electrical characteristics - LDO1**

All parameters are specified at $T_A$ = -40 °C to 105 °C, $V_{IN}$ = 3.6 V, $V_{LDOIN1}$ = 3.6 V, $V_{LDO1}$ = 3.3 V, $I_{LDO1}$ = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN}$ = 3.6 V, $V_{LDOIN1}$ = 3.6 V, $V_{LDO1}$ = 3.3 V, $I_{LDO1}$ = 10 mA, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **LDO1 linear regulator** | | | | | | |
| $PSRR_{LDO1}$ | PSRR, $I_{LDO1}$ = 75 mA, 20 Hz to 20 kHz<br>• LDO1 = 1.8 V to 3.3 V, $V_{LDOIN1}$ = $V_{LDO1INMIN}$ + 100 mV<br>• LDO1 = 1.8 V to 3.3 V, $V_{LDOIN1}$ = $V_{LDO1NOM}$ + 1.0 V | <br>35<br>52 | <br>40<br>60 | <br>–<br>– | dB | |
| $NOISE_{LDO1}$ | Output noise density, $V_{LDOIN1}$ = $V_{LDO1INMIN}$, $I_{LDO1}$ = 75 mA<br>• 100 Hz to <1.0 kHz<br>• 1.0 kHz to <10 kHz<br>• 10 kHz to 1.0 MHz | <br>–<br>–<br>– | <br>-114<br>-129<br>-135 | <br>-102<br>-123<br>-130 | dBV/ √Hz | |
| $t_{ONLDO1}$ | Turn-On time, enable to 90% of end value, $V_{LDOIN1}$ = $V_{LDO1INMIN}$ to 4.5 V, $I_{LDO1}$ = 0.0 mA, all output voltage settings | 60 | – | 500 | µs | |
| $t_{OFFLDO1}$ | Turn-Off time, disable to 10% of initial value, $V_{LDOIN1}$ = $V_{LDO1INMIN}$, $I_{LDO1}$ = 0.0 mA | – | – | 10 | ms | |
| $LDO1_{OSHT}$ | Start-up overshoot, $V_{LDOIN1}$ = $V_{LDO1INMIN}$ to 4.5 V, $I_{LDO1}$ = 0.0 mA | – | 1.0 | 2.0 | % | |

**Table 14. Static electrical characteristics - LDO2**

All parameters are specified at $T_A$ = -40 °C to 105 °C, $V_{IN}$ = 3.6 V, $V_{LDOIN2}$ = 3.0 V, $V_{LDO2}$ = 1.55 V, $I_{LDO2}$ = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN}$ = 3.6 V, $V_{LDOIN2}$ = 3.0 V, $V_{LDO2}$ = 1.55 V, $I_{LDO2}$ = 10 mA and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **LDO2 linear regulator** | | | | | | |
| $V_{LDOIN2}$ | Operating Input Voltage | 1.75 | – | 3.40 | V | |
| $V_{LDO2NOM}$ | Nominal output voltage | – | Table 56 | – | V | |
| $I_{LDO2}$ | Rated output load current | 250 | – | – | mA | |
| $V_{LDO2TOL}$ | Output voltage tolerance, 1.75 V < $V_{LDOIN2}$ < 3.40 V, 0.0 mA < $I_{LDO2}$ < 250 mA, LDO2 = 0.8 V to 1.55 V | -3.0 | – | 3.0 | % | |
| $I_{LDO2Q}$ | Quiescent current, no load, change in $I_{VIN}$ and $I_{VLDOIN2}$, when $V_{LDO2}$ enabled | – | 16 | – | µA | |
| $I_{LDO2LIM}$ | Current limit, $I_{LDO2}$ when $V_{LDO2}$ is forced to $V_{LDO2NOM}$/2 | 333 | 417 | 612 | mA | |

**Table 15. Dynamic electrical characteristics - LDO2**

All parameters are specified at $T_A$ = -40 °C to 105 °C, $V_{IN}$ = 3.6 V, $V_{LDOIN2}$ = 3.0 V, $V_{LDO2}$ = 1.55 V, $I_{LDO2}$ = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN}$ = 3.6 V, $V_{LDOIN2}$ = 3.0 V, $V_{LDO2}$ = 1.55 V, $I_{LDO2}$ = 10 mA and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **LDO2 linear regulator** | | | | | | |
| $PSRR_{LDO2}$ | PSRR, $I_{LDO2}$ = 187.5 mA, 20 Hz to 20 kHz<br>• LDO2 = 0.8 V to 1.55 V<br>• LDO2 = 1.1 V to 1.55 V | <br>50<br>37 | <br>60<br>45 | <br>–<br>– | dB | |
| $NOISE_{LDO2}$ | Output noise density, $V_{LDOIN2}$ = 1.75 V, $I_{LDO2}$ = 187.5 mA<br>• 100 Hz to <1.0 kHz<br>• 1.0 kHz to <10 kHz<br>• 10 kHz to 1.0 MHz | <br>–<br>–<br>– | <br>-108<br>-118<br>-124 | <br>-100<br>-108<br>-112 | dBV/√Hz | |
| $t_{ONLDO2}$ | Turn-on time, enable to 90% of end value, $V_{LDO2IN}$ = 1.75 V to 3.4 V, $I_{LDO2}$ = 0.0 mA | 60 | – | 500 | µs | |
| $t_{OFFLDO2}$ | Turn-Off time, disable to 10% of initial value, $V_{LDO2IN}$ = 1.75 V, $I_{LDO2}$ = 0.0 mA | – | – | 10 | ms | |
| $LDO2_{OSHT}$ | Start-up overshoot, $V_{LDO2IN}$ = 1.75 V to 3.4 V, $I_{LDO2}$ = 0.0 mA | – | 1.0 | 2.0 | % | |

**Table 16. Static electrical characteristics – VSD**

All parameters are specified at $T_A$ = -40 °C to 105 °C, $V_{IN}$ = 3.6 V, V18 = 1.85 V, $I_{VSD}$ = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN}$ = 3.6 V, V18 = 1.85 V, $I_{VSD}$ = 10 mA, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **V18 linear regulator** | | | | | | |
| $V_{PVIN2}$ | Operating input voltage | 2.8 | – | 4.5 | V | (28) |
| $V_{VSD}$ | Nominal output voltage | – | Table | – | V | |
| $I_{VSD}$ | Rated output load current | 100 | – | – | mA | |
| $V_{VSD}$ | Output voltage accuracy, 2.8 V < $V_{IN}$ < 4.5 V, 0.0 mA < $I_{VSD}$ < 100 mA | -3.0 | – | 3.0 | % | |
| $I_{VSD}$ | Quiescent current, no load, change in $I_{VIN}$ and $I_{PVIN2}$, When $V_{18}$ enabled | – | 13 | – | µA | |
| $I_{VSDLIM}$ | Current limit, $I_{VSD}$ when $V_{VSD}$ is forced to $V_{VSDNOM}$/2 | 122 | 167 | 280 | mA | |

Notes

28. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any VR5100 regulator, or external system supply.

**Table 17. Dynamic Electrical Characteristics - VSD**

All parameters are specified at $T_A$ = -40 °C to 105 °C, $V_{IN}$ = 3.6 V, V18 = 1.85 V, $I_{VSD}$ = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN}$ = 3.6 V, V18 = 1.85 V, $I_{VSD}$ = 10 mA, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **V18 LINEAR REGULATOR** | | | | | | |
| $PSRR_{VSD}$ | PSRR, $I_{VSD}$ = 75 mA, 20 Hz to 20 kHz<br>• V18, $V_{IN}$ = $V_{VSDNOM}$ + 1.0 V | <br>52 | <br>60 | <br>– | dB | |
| $NOISE_{VSD}$ | Output Noise Density, $V_{IN}$ = 2.8V, $I_{VSD}$ = 75 mA<br>• 100 Hz – <1.0 kHz<br>• 1.0 kHz – <10 kHz<br>• 10 kHz – 1.0 MHz | <br>–<br>–<br>– | <br>-114<br>-129<br>-135 | <br>-102<br>-123<br>-130 | dBV/√Hz | |

**Table 17. Dynamic Electrical Characteristics - VSD(continued)**

All parameters are specified at $T_A$ = -40 °C to 105 °C, $V_{IN}$ = 3.6 V, V18 = 1.85 V, $I_{VSD}$ = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN}$ = 3.6 V, V18 = 1.85 V, $I_{VSD}$ = 10 mA, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **V18 linear regulator (Continued)** | | | | | | |
| $t_{ONVSD}$ | Turn-on time, enable to 90% of end value, $V_{IN}$ = 2.8 V to 4.5 V, $I_{VSD}$ = 0.0 mA | 60 | – | 500 | µs | |
| $t_{OFFVSD}$ | Turn-off time, disable to 10% of initial value, $V_{IN}$ = 2.8 V, $I_{VSD}$ = 0.0 mA | – | – | 10 | ms | |
| $VSD_{OSHT}$ | Start-up overshoot, $V_{IN}$ = 2.8 V to 4.5 V, $I_{VSD}$ = 0.0 mA | – | 1.0 | 2.0 | % | |

**Table 18. Static Electrical Characteristics – V33**

All parameters are specified at $T_A$ = -40 °C to 105 °C, $V_{IN}$ = 3.6 V, $V_{33}$ = 3.3 V, $I_{V33}$ = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN}$ = 3.6 V, $V_{33}$ = 3.3 V, $I_{V33}$ = 10 mA, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **V33 linear regulator** | | | | | | |
| $V_{IN}$ | Operating input voltage, 2.9 V ≤ $V_{33NOM}$ ≤ 3.6 V | 2.8 | – | 4.5 | V | (29), (30) |
| $V_{33NOM}$ | Nominal output voltage | – | Table 57 | – | V | |
| $I_{V33}$ | Rated output load current | 350 | – | – | mA | |
| $V_{33TOL}$ | Output voltage tolerance, 2.8 V < $V_{IN}$ < 4.5 V, 0.0 mA < $I_{V33}$ < 350 mA, $V_{33}$[1:0] = 00 to 11 | -3.0 | – | 3.0 | % | |
| $I_{V33Q}$ | Quiescent current, no load, change in $I_{VIN}$, When $V_{33}$ enabled | – | 13 | – | µA | |
| $I_{V33LIM}$ | Current limit, $I_{V33}$ when $V_{33}$ is forced to $V_{33NOM}$/2 | 435 | 584.5 | 950 | mA | |

Notes

29. When the LDO output voltage is set above 2.6 V the minimum allowed input voltage need to be at least the output voltage plus 0.25 V for proper regulation due to the dropout voltage generated through the internal LDO transistor.
30. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any VR5100 regulator, or external system supply.

**Table 19. Dynamic electrical characteristics – V33**

All parameters are specified at $T_A$ = -40 °C to 105 °C, $V_{IN}$ = 3.6 V, $V_{33}$ = 3.3 V, $I_{V33}$ = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN}$ = 3.6 V, $V_{33}$ = 3.3 V, $I_{V33}$ = 10 mA, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **V33 linear regulator** | | | | | | |
| $PSRR_{V33}$ | PSRR, $I_{V33}$ = 262.5 mA, 20 Hz to 20 kHz, $V_{33}$[1:0] = 00 - 11, $V_{IN}$ = $V_{33NOM}$ + 1.0 V | 52 | 60 | – | dB | (31) |
| $NOISE_{V33}$ | Output noise density, $V_{IN}$ = 2.8 V, $I_{V33}$ = 262.5 mA<br>• 100 Hz to <1.0 kHz<br>• 1.0 kHz to <10 kHz<br>• 10 kHz to 1.0 MHz | <br>–<br>–<br>– | <br>-114<br>-129<br>-135 | <br>-102<br>-123<br>-130 | dBV/√Hz | |
| $t_{ONV33}$ | Turn-On time, enable to 90% of end value, $V_{IN}$ = 2.8 V, to 4.5 V, $I_{V33}$ = 0.0 mA | 60 | – | 500 | µs | |

**Table 19. Dynamic electrical characteristics – V33 (continued)**

All parameters are specified at $T_A$ = -40 °C to 105 °C, $V_{IN}$ = 3.6 V, $V_{33}$ = 3.3 V, $I_{V33}$ = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN}$ = 3.6 V, $V_{33}$ = 3.3 V, $I_{V33}$ = 10 mA, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **V33 linear regulator (Continued)** | | | | | | |
| $t_{OFFV33}$ | Turn-Off time, disable to 10% of initial value, $V_{IN}$ = 2.8 V, $I_{V33}$ = 0.0 mA | – | – | 10 | ms | |
| $V_{33OSHT}$ | Start-up overshoot, $V_{IN}$ = 2.8 V to 4.5 V, $I_{V33}$ = 0.0 mA | – | 1.0 | 2.0 | % | |

Notes

31. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any VR5100 regulator, or external system supply.

**Table 20. Static electrical characteristics – LDO3**

All parameters are specified at $T_A$ = -40 °C to 105 °C, $V_{IN}$ = 3.6 V, $V_{LDOIN34}$ = 3.6 V, $V_{LDO3}$ = 3.3 V, $I_{LDO3}$ = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN}$ = 3.6 V, $V_{LDOIN34}$ = 3.6 V, $V_{LDO3}$ = 3.3 V, $I_{LDO3}$ = 10 mA, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **LDO3 linear regulator** | | | | | | |
| $V_{LDOIN34}$ | Operating input voltage<br>• 1.8 V ≤ $V_{LDO3NOM}$ ≤ 2.5 V<br>• 2.6 V ≤ $V_{LDO3NOM}$ ≤ 3.3 V | 2.8<br>$V_{LDO3NOM}$ +0.250 | –<br>– | 3.6<br>3.6 | V | (32) |
| $V_{LDO3NOM}$ | Nominal output voltage | – | Table 56 | – | V | |
| $I_{LDO3}$ | Rated output load current | 100 | – | – | mA | |
| $V_{LDO3TOL}$ | Output voltage tolerance, $V_{LDOIN34MIN}$ < $V_{LDOIN34}$ < 3.6 V, 0.0 mA < $I_{LDO3}$ < 100 mA, LDO3 = 1.8 V to 3.3 V | -3.0 | – | 3.0 | % | |
| $I_{LDO3Q}$ | Quiescent current, no load, change in $I_{VIN}$ and $I_{VLDOIN34}$, when $V_{LDO3}$ enabled | – | 13 | – | µA | |
| $I_{LDO3LIM}$ | Current limit, $I_{LDO3}$ when $V_{LDO3}$ is forced to $V_{LDO3NOM}$/2 | 122 | 167 | 280 | mA | |

Notes

32. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any VR5100 regulator, or external system supply.

**Table 21. Dynamic electrical characteristics – LDO3**

All parameters are specified at $T_A$ = -40 °C to 105 °C, $V_{IN}$ = 3.6 V, $V_{LDOIN34}$ = 3.6 V, $V_{LDO3}$ = 3.3 V, $I_{LDO3}$ = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN}$ = 3.6 V, $V_{LDOIN34}$ = 3.6 V, $V_{LDO3}$ = 3.3 V, $I_{LDO3}$ = 10 mA, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **LDO3 linear regulator** | | | | | | |
| $PSRR_{LDO3}$ | PSRR, $I_{LDO3}$ = 75 mA, 20 Hz to 20 kHz<br>• LDO3 = 1.8 V to 3.3 V, $V_{LDOIN34}$ = $V_{LDO34INMIN}$ + 100 mV<br>• LDO3 = 1.8 V to 3.3 V, $V_{LDOIN34}$ = $V_{LDO3NOM}$ + 1.0 V | <br>35<br>52 | <br>40<br>60 | <br>–<br>– | dB | |
| $NOISE_{LDO3}$ | Output noise density, $V_{LDO34IN}$ = $V_{LDOIN34MIN}$, $I_{LDO3}$ = 75 mA<br>• 100 Hz to <1.0 kHz<br>• 1.0 kHz to <10 kHz<br>• 10 kHz to 1.0 MHz | <br>–<br>–<br>– | <br>-114<br>-129<br>-135 | <br>-102<br>-123<br>-130 | dBV/√Hz | |

**Table 21. Dynamic electrical characteristics – LDO3 (continued)**

All parameters are specified at $T_A$ = -40 °C to 105 °C, $V_{IN}$ = 3.6 V, $V_{LDOIN34}$ = 3.6 V, $V_{LDO3}$ = 3.3 V, $I_{LDO3}$ = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN}$ = 3.6 V, $V_{LDOIN34}$ = 3.6 V, $V_{LDO3}$ = 3.3 V, $I_{LDO3}$ = 10 mA, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **LDO3 linear regulator (Continued)** | | | | | | |
| $t_{ONLDO3}$ | Turn-on time, enable to 90% of end value, $V_{LDOIN34}$ = $V_{LDOIN34MIN}$ to 3.6 V, $I_{LDO3}$ = 0.0 mA | 60 | – | 500 | µs | |
| $t_{OFFLDO3}$ | Turn-off time, disable to 10% of initial value, $V_{LDOIN34}$ = $V_{LDOIN34MIN}$, $I_{LDO3}$ = 0.0 mA | – | – | 10 | ms | |
| $LDO3_{OSHT}$ | Start-up overshoot, $V_{LDOIN34}$ = $V_{LDOIN34MIN}$ to 3.6 V, $I_{LDO3}$ = 0.0 mA | – | 1.0 | 2.0 | % | |

**Table 22. Static electrical characteristics - LDO4**

All parameters are specified at $T_A$ = -40 °C to 105 °C, $V_{IN}$ = 3.6 V, $V_{LDOIN34}$ = 3.6 V, VLDO4 = 3.3 V, $I_{LDO4}$ = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN}$ = 3.6 V, $V_{LDOIN34}$ = 3.6 V, VLDO4 = 3.3 V, $I_{LDO4}$ = 10 mA, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **LDO4 LINEAR REGULATOR** | | | | | | |
| $V_{LDOIN34}$ | Operating input voltage<br>• 1.8 V ≤ $V_{LDO4NOM}$ ≤ 2.5 V<br>• 2.6 V ≤ $V_{LDO4NOM}$ ≤ 3.3 V | 2.8<br>$V_{LDO4NOM}$ +0.250 | –<br>– | 3.6<br>3.6 | V | (33) |
| $V_{LDO4NOM}$ | Nominal output voltage | – | Table 56 | – | V | |
| $I_{LDO4}$ | Rated output load current | 350 | – | – | mA | |
| $V_{LDO4TOL}$ | Output voltage tolerance, $V_{LDOIN34MIN}$ < $V_{LDOIN34}$ < 3.6 V, 0.0 mA < $I_{LDO3}$ < 100 mA, VLDO4 = 1.9 V to 3.3 V | -3.0 | – | 3.0 | % | |
| $I_{LDO4Q}$ | Quiescent current, no load, change in $I_{VIN}$ and $I_{VLDOIN34}$, When $V_{LDO4}$ enabled | – | 13 | – | µA | |
| $I_{LDO4LIM}$ | Current limit, $I_{LDO4}$ when $V_{LDO4}$ is forced to $V_{LDO4NOM}$/2 | 435 | 584.5 | 950 | mA | |
| $PSRR_{VLDO4}$ | PSRR, $I_{LDO4}$ = 262.5 mA, 20 Hz to 20 kHz<br>• LDO4 = 1.9 V to 3.3 V, $V_{LDOIN34}$ = $V_{LDOIN34MIN}$ + 100 mV<br>• LDO4 = 1.9 V to 3.3 V, $V_{LDOIN34}$ = $V_{LDO4NOM}$ + 1.0 V | <br>35<br>52 | <br>40<br>60 | <br>–<br>– | dB | |

Notes

33. Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V). Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin. If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V. This voltage can be an output from any VR5100 regulator, or external system supply.

**Table 23. Dynamic electrical characteristics - LDO4**

All parameters are specified at $T_A$ = -40 °C to 105 °C, $V_{IN}$ = 3.6 V, $V_{LDOIN34}$ = 3.6 V, LDO4 = 3.3 V, $I_{LDO4}$ = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN}$ = 3.6 V, $V_{LDOIN34}$ = 3.6 V, LDO4 = 3.3 V, $I_{LDO4}$ = 10 mA, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **LDO4 linear regulator** | | | | | | |
| $NOISE_{LDO4}$ | Output noise density, $V_{LDOIN342}$ = $V_{LDOIN34MIN}$, $I_{LDO4}$ = 262.5 mA<br>• 100 Hz to <1.0 kHz<br>• 1.0 kHz to <10 kHz<br>• 10 kHz to 1.0 MHz | <br>–<br>–<br>– | <br>-114<br>-129<br>-135 | <br>-102<br>-123<br>-130 | dBV/√Hz | |
| $t_{ONLDO4}$ | Turn-on time, enable to 90% of end value, $V_{LDO34IN}$ = $V_{LDOIN34MIN}$, 3.6 V, $I_{LDO4}$ = 0.0 mA | 60 | – | 500 | µs | |
| $t_{OFFLDO4}$ | Turn-off time, disable to 10% of initial value, $V_{LDOIN34}$ = $V_{LDOIN34MIN}$, $I_{LDO4}$ = 0.0 mA | – | – | 10 | ms | |
| $LDO4_{OSHT}$ | Start-up overshoot, $V_{LDOIN34}$ = $V_{LDOIN34MIN}$, 3.6 V, $I_{LDO4}$ = 0.0 mA | – | 1.0 | 2.0 | % | |

**Table 24. Static electrical characteristics - REFOUT**

All parameters are specified at $T_A$ = -40 °C to 105 °C, $V_{IN}$ = 3.6 V, $I_{REFOUT}$ = 0.0 mA, $V_{REFIN}$ = 1.5 V, and typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN}$ = 3.6 V, $I_{REFOUT}$ = 0.0 mA, $V_{REFIN}$ = 1.5 V, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **REFOUT linear regulator** | | | | | | |
| $V_{REFIN}$ | Operating input voltage range | 1.2 | – | 1.65 | V | (34) |
| $V_{REFOUT}$ | Output voltage, 1.2 V < $V_{REFIN}$ < 1.65 V, 0.0 mA < $I_{REFOUT}$ < 10 mA | – | $V_{REFIN}$/2 | – | V | |
| $V_{REFOUTTOL}$ | Output voltage tolerance, as a percentage of $V_{REFIN}$, 1.2 V < $V_{REFIN}$ < 1.65 V, 0.6 mA < $I_{REFOUT}$ < 10 mA | 49.5 | 50 | 50.5 | % | |
| $I_{REFOUT}$ | Rated output load current | 10 | – | – | mA | |
| $I_{REFOUTQ}$ | Quiescent current | – | 12 | – | µA | (35) |
| $I_{REFOUTLM}$ | Current limit, $I_{REFOUT}$ when $V_{REFOUT}$ is forced to $V_{INREFOUT}$/4 | 10.5 | 15 | 25 | mA | |

Notes

34. When using SW3 as input, the REFOUT input voltage range specification refers to the voltage set point of SW3 and not the absolute value
35. When REFOUT is off there is a quiescent current of a typical 2.0 µA.

**Table 25. Dynamic electrical characteristics - REFOUT**

All parameters are specified at $T_A$ = -40 °C to 105 °C, $V_{IN}$ = 3.6 V, $I_{REFOUT}$ = 0.0 mA, $V_{REFIN}$ = 1.5 V, and typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN}$ = 3.6 V, $I_{REFOUT}$ = 0.0 mA, $V_{REFIN}$ = 1.5 V, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **REFOUT linear regulator** | | | | | | |
| $t_{ONREFOUT}$ | Turn-on time, enable to 90% of end value, $V_{REFIN}$ = 1.2 V to 1.65 V, $I_{REFOUT}$ = 0.0 mA | – | – | 100 | µs | |
| $t_{OFFREFOUT}$ | Turn-off time, disable to 10% of initial value, $V_{REFIN}$ = 1.2 V to 1.65 V, $I_{REFOUT}$ = 0.0 mA | – | – | 10 | ms | |
| $V_{REFOUTOSH}$ | Start-up overshoot, $V_{REFIN}$ = 1.2 V to 1.65 V, $I_{REFOUT}$ = 0.0 mA | – | 1.0 | 6.0 | % | |

**Table 26. Static electrical characteristics - Coin Cell**

All parameters are specified at $T_A$ = -40 °C to 105 °C, $V_{IN}$ = 3.6 V, typical external component values, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **Coin cell** | | | | | | |
| $V_{COINACC}$ | Charge voltage accuracy | -100 | – | -100 | mV | |
| $I_{COINACC}$ | Charge current accuracy | -30 | – | 30 | % | |
| $I_{COIN}$ | Coin cell charge current<br>• $I_{COINHI}$ (in On mode)<br>• $I_{COINLO}$ (in On mode) | <br>–<br>– | <br>60<br>10 | <br>–<br>– | µA | |

**Table 27. Static electrical characteristics - Digital I/O**

All parameters are specified at $T_A$ = -40 °C to 105 °C, $V_{CCI2C}$ = 1.7 V to 3.6 V, and typical external component values and full load current range, unless otherwise noted.

| Pin name | Parameter | Load condition | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| EN | • $V_L$<br>• $V_H$ | –<br>– | 0.0<br>0.8 * $V_{SNVS}$ | 0.2 * $V_{SNVS}$<br>3.6 | V | |
| PORB | • $V_{OL}$<br>• $V_{OH}$ | -2.0 mA<br>Open drain | 0.0<br>0.7 * $V_{CCI2C}$ | 0.4 * $V_{CCI2C}$<br>$V_{CCI2C}$ | V | |
| SCL | • $V_L$<br>• $V_H$ | –<br>– | 0.0<br>0.8 * $V_{CCI2C}$ | 0.2 * $V_{CCI2C}$<br>3.6 | V | |
| SDA | • $V_L$<br>• $V_H$<br>• $V_{OL}$<br>• $V_{OH}$ | –<br>–<br>-2.0 mA<br>Open drain | 0.0<br>0.8 * $V_{CCI2C}$<br>0.0<br>0.7 * $V_{CCI2C}$ | 0.2 * $V_{CCI2C}$<br>3.6<br>0.4 * $V_{CCI2C}$<br>$V_{CCI2C}$ | V | |
| INTB | • $V_{OL}$<br>• $V_{OH}$ | -2.0 mA<br>Open drain | 0.0<br>0.7 * $V_{CCI2C}$ | 0.4 * $V_{CCI2C}$<br>$V_{CCI2C}$ | V | |
| STBY | • $V_L$<br>• $V_H$ | –<br>– | 0.0<br>0.8 * $V_{SNVS}$ | 0.2 * $V_{SNVS}$<br>3.6 | V | |
| SD_VSEL | • $V_L$<br>• $V_H$ | – | 0.0<br>0.8 * $V_{CCI2C}$ | 0.2 * $V_{CCI2C}$<br>3.6 | V | |
| VDDOTP | • $V_L$<br>• $V_H$ | –<br>– | 0.0<br>1.1 | 0.3<br>1.7 | V | |

**Table 28. Static electrical characteristics - internal supplies**

All parameters are specified at $T_A$ = -40 °C to 105 °C, $V_{IN}$ = 2.8 V to 4.5 V, Licell = 1.8 V to 3.3 V and typical external component values. Typical values are characterized at $V_{IN}$ = 3.6 V, Licell = 3.0 V, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **VDIG (digital core supply)** | | | | | | |
| $V_{DIG}$ | Output voltage<br>• ON mode<br>• Coin cell mode and OFF mode | <br>–<br>– | <br>1.5<br>1.3 | <br>–<br>– | V | (36) |
| **VCC (analog core supply)** | | | | | | |
| $V_{CC}$ | Output voltage<br>• ON mode and charging<br>• Coin cell mode and OFF mode | <br>–<br>– | <br>2.775<br>0.0 | <br>–<br>– | V | (36) |

**Table 28. Static electrical characteristics - internal supplies (continued)**

All parameters are specified at $T_A$ = -40 °C to 105 °C, $V_{IN}$ = 2.8 V to 4.5 V, Licell = 1.8 V to 3.3 V and typical external component values. Typical values are characterized at $V_{IN}$ = 3.6 V, Licell = 3.0 V, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **VBG (BANDGAP regulator reference)** | | | | | | |
| $V_{BG}$ | Output voltage at 25 °C | – | 1.2 | – | V | (36) |
| $V_{BGACC}$ | Absolute trim accuracy | – | 0.5 | – | % | |
| $V_{BGTACC}$ | Temperature drift | – | 0.25 | – | % | |

Notes

36. 3.1 V < $V_{IN}$ < 4.5 V, no external loading on VDIG, VCC, or VBG.

**Table 29. Static electrical characteristics - UVDET threshold**

All parameters are specified at $T_A$ = -40 °C to 105 °C, $V_{IN}$ = 2.8 V to 4.5 V, Licell = 1.8 V to 3.3 V and typical external component values. Typical values are characterized at $V_{IN}$ = 3.6 V, Licell = 3.0 V, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **$V_{IN}$ UVDET threshold** | | | | | | |
| $V_{UVDET}$ | • Rising<br>• Falling | –<br>2.5 | –<br>– | 3.1<br>– | V | |

# 5 General description

The VR5100 is a high performance, highly integrate, multi-output, SMARTMOS, DC/DC regulator solution, with integrated power MOSFETs ideally suited for the LS1 family of communications processors.

## 5.1 Features

This section summarizes the VR5100 features.

- Input voltage range to PMIC: 2.8 V to 4.5 V
  - Buck regulators
    - Configurable three channels
    - SW1, 3.8 A (single); 0.7 V to 1.425 V, 1.8 V, 3.3 V
    - SW2, 1.25 A; 1.50 V to 1.85 V or 2.50 V to 3.30 V
    - SW3, 1.5 A; 0.90 V to 1.65 V
    - Dynamic voltage scaling
    - Modes: PWM, PFM, APS
    - Programmable output voltage
    - Programmable current limit
    - Programmable soft start sequence
    - Programmable PWM switching frequency
  - Boost regulator
    - SWBST, 5.0 V to 5.15  V, 0.6 A, OTG support
    - Modes: PFM and Auto
    - OCP fault interrupt
  - LDOs
    - VSD, 1.8 V or 3.3 V, 100 mA, based on SD_VSEL
    - V33, 2.85 V to 3.30 V, 350 mA
    - LDO1, 1.8 V to 3.3 V, 100 mA
    - LDO2, 0.80 V to 1.55 V, 250 mA
    - LDO3, 1.8 V to 3.3 V, 100 mA
    - LDO4, 1.8 V to 3.3 V, 350 mA
- Always ON RTC regulator/switch VSNVS 3.0 V, 1.0 mA
- Coin cell charger
- DDR memory reference voltage, REFOUT, 0.5 V to 0.9 V, 10 mA
- OTP (one time programmable) memory for device configuration, user-programmable start-up sequence and timing
- $I^2C$ interface
- User programmable Standby, Sleep/LPSR, and Off modes

## 5.2 Functional block diagram

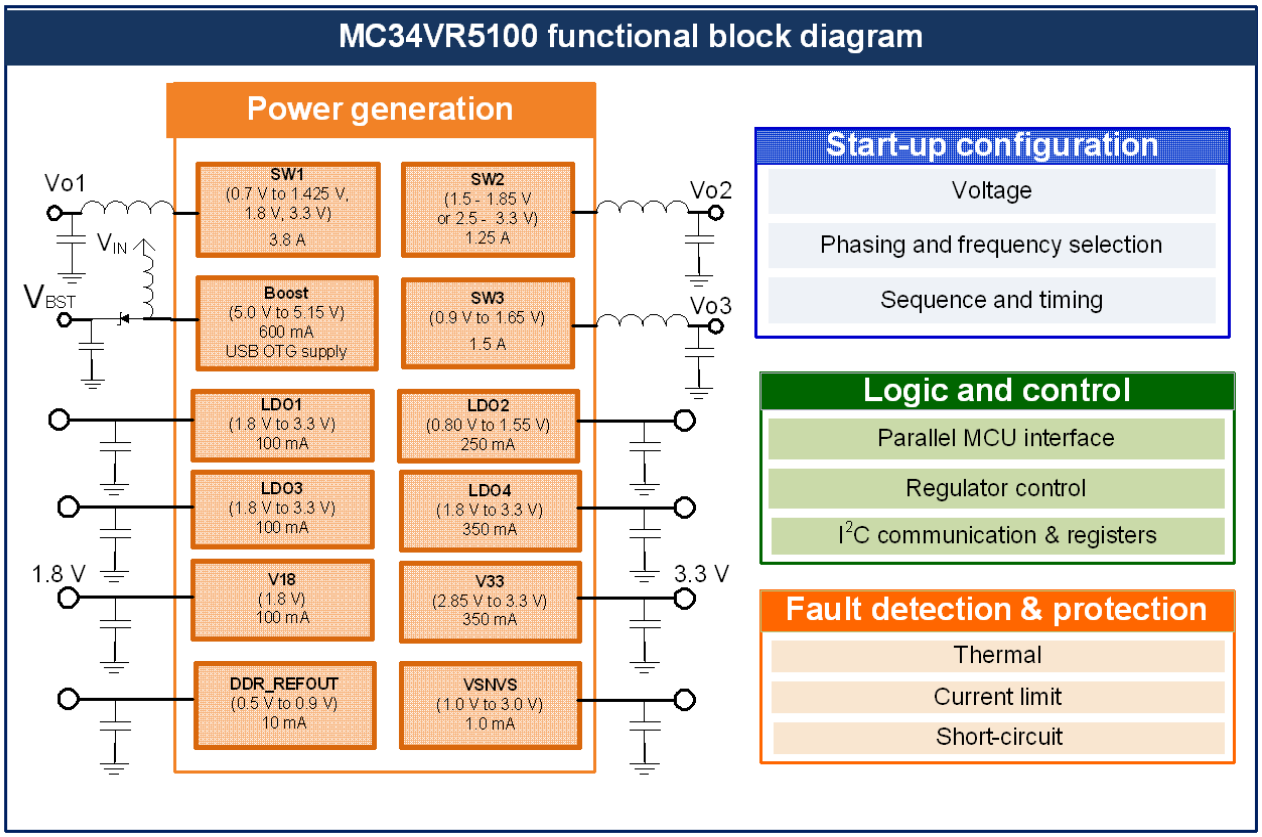



**Figure 4. Functional block diagram**

# 6 Functional description and application information

## 6.1 Introduction

The VR5100 is a highly integrated, low quiescent current power management IC featuring three buck regulators, one boost regulator, seven LDO regulators, and a DDR voltage reference. The VR5100 operates from an input voltage of up to 4.5 V. Output voltage, startup sequence, and other functions are set using integrated one time programmable (OTP) memory, thus providing flexibility and reducing external component count.

## 6.2 Power generation

The buck regulators in the VR5100 provide supply to the processor cores and to other voltage domains, such as I/O and memory. Dynamic voltage scaling is provided to allow controlled supply rail adjustments for the processor cores and other circuitry. The linear regulators in the VR5100 can be used as general purpose regulators to power peripherals and lower power processor rails.

The VSD LDO regulator supports the dual voltage requirement by high speed SD card readers. Depending on the system power path configuration, the LDO regulators can be directly supplied from the main input supply or from the switching regulators to power peripherals, such as audio, camera, Bluetooth, and Wireless LAN, etc.

Table 30 shows a summary of the voltage regulators in the VR5100.

**Table 30. VR5100 power tree**

| Supply | Output voltage (V) | Programming step size (mV) | Maximum load current (mA) |
|---|---|---|---|
| SW1 | 0.70 to 1.425<br>1.8 to 3.3 | 25<br>(N/A) | 3800 |
| SW2 | 1.50 to 1.85<br>2.50 to 3.30 | 50<br>variable | 1250 |
| SW3 | 0.90 to 1.65 | 50 | 1500 |
| SWBST | 5.00 to 5.15 | 50 | 600 |
| LDO1 | 1.8 to 3.3 | 50 | 100 |
| LDO2 | 0.80 to 1.55 | 50 | 250 |
| VSD | 1.85 | 50 | 100 |
| V33 | 2.85 to 3.30 | 150 | 350 |
| LDO3 | 1.8 to 3.3 | 100 | 100 |
| LDO4 | 1.8 to 3.3 | 100 | 350 |
| VSNVS | 3.0 | NA | 1.0 |
| REFOUT | 0.5*SW3_OUT | NA | 10 |

## 6.3 Functional description

### 6.3.1 Control logic and interface signals

The VR5100 is fully programmable via the $I^2C$ interface. Additional communication is provided by direct logic interfacing including INTB, PORB, STBY, EN, and SD_VSEL. Refer to Table 24 for logic levels for these pins.

### 6.3.1.1 EN

EN is an input signal to the IC which generates a turn-on event. A turn-on event brings the VR5100 out of OFF and Sleep modes and into the ON mode. Refer to Modes of operation for the various modes (states) of operation of the IC. The EN pin can be configured using OTP to detect a level, or an edge using the EN_CFG bit.

- If EN_CFG = 0, the EN signal is high and VIN > UVDET, the PMIC turns on; the interrupt and sense bits, ENI and ENS respectively, is set.
- If EN_CFG = 1, VIN > UVDET and EN transitions from high to low, the PMIC turns on; the interrupt and sense bits, ENI and ENS respectively, is set.

Any regulator enabled in the Sleep mode remains enabled when transitioning from Sleep to ON, i.e., the regulator is not turned off and then on again to match the start-up sequence.

When EN_CFG = 1, the EN input can be a mechanical switch debounced through a programmable debouncer ENDBNC[1:0], to avoid a response to a very short key press. The interrupt is generated for both the falling and the rising edge of the EN pin. By default, a 31.25 ms interrupt debounce is applied to both falling and rising edges. The falling edge debounce timing can be extended with ENDBNC[1:0] as defined in the table below. The interrupt is cleared by software, or when cycling through the OFF mode.

**Table 31. EN hardware debounce bit settings [37]**

| Bits | State | Turn on debounce (ms) | Falling edge INT debounce (ms) | Rising edge INT debounce (ms) |
|---|---|---|---|---|
| ENDBNC[1:0] | 00 | 0.0 | 31.25 | 31.25 |
| | 01 | 31.25 | 31.25 | 31.25 |
| | 10 | 125 | 125 | 31.25 |
| | 11 | 750 | 750 | 31.25 |

Notes

37. The sense bit, ENS, is not debounced and follows the state of the EN pin.

### 6.3.1.2 STBY

STBY is an input signal to the IC. When it is asserted the part enters standby mode and when de-asserted, the part exits standby mode. STBY can be configured as active high or active low using the STBYINV bit. See Standby mode for more details.

Note: When operating the PMIC at $V_{IN} \leq 2.85$ V a coin cell must be present to provide $V_{SNVS}$, or the PMIC does not reliably enter and exit the STANDBY mode.

### 6.3.1.3 PORB

PORB is an open-drain, active low output OTP configurable for two modes of operation. In its default mode, it is de-asserted 2.0 ms after the last regulator in the start-up sequence is enabled. In this mode, the signal can be used to bring the processor out of reset (POR), or as an indicator when all supplies have been enabled; it is only asserted during a turn-off event. In the default mode, the PORB signal is internal timer based and does not monitor the regulators. When configured for its fault mode, PORB is de-asserted after the start-up sequence is completed only if no faults occurred during start-up. At any time, if a fault occurs and persists for 1.8 ms, PORB is asserted LOW. The VR5100 is turned off if the fault persists for more than 100 ms. The EN signal can be used to restart the part, though if the fault persists, the sequence described above is repeated. To enter the fault mode, set bit OTP_PG_EN of register OTP PWRGD EN to “1” during OTP programming.

### 6.3.1.4 INTB

INTB is an open drain, active low output. It is asserted when any fault occurs, provided the fault interrupt is unmasked. INTB is de-asserted after the fault interrupt is cleared by software, which requires writing a “1” to the fault interrupt bit.

### 6.3.1.5 SD_VSEL

SD_VSEL is an input pin which sets the output voltage range of the VSD regulator. When SD_VSEL = HIGH, the VSD regulator operates in the lower output voltage range. When SD_VSEL = LOW, the VSD regulator operates in the higher output voltage range. The SD_VSEL input buffer is powered by the VCCI2C supply. When a valid VCCI2C voltage is not present, the output of the SD_VSEL buffer defaults to a logic high thus keeping the VSD regulator output in the lower voltage range.

## 6.3.2 One-time-programmable memory

One-time-programmable memory is used to store key startup parameters and regulators' configuration information. This eliminates the need to set regulator voltage and sequence using external components. The following parameters are programmable in the VR5100.

**General**: $I^2C$ slave address, EN pin configuration, PORB configuration

**Buck regulators:** Output voltage, switching frequency, regulator start-up sequence and timing

**Boost regulator and LDOs:** Output voltage, regulator start-up sequence and timing

The VR5100 starts up based on the contents of the TBBOTP registers. During power up, contents of the OTP memory are loaded on to the TBBOTP registers. There is an optional Try-before-buy mode of operation available which bypasses loading of the OTP memory onto the TBBOTP registers. Instead, regulators directly start up based on the current contents of the TBBOTP registers during this mode of operation. This mode is useful when trying to determine a suitable OTP configuration for the system. TBB mode can also be used in lieu of OTP programming provided a microcontroller can initiate the TBB sequence is available in the system.

### 6.3.2.1 Register naming convention

Register and bit names for the TBBOTP registers are prefixed with "OTP". This is to differentiate them from "Functional registers" which are responsible for real-time control of regulator settings. For example, "OTP_SW1_VOLT" refers to the TBBOTP register associated with the voltage setting for SW1 regulator. "SW1VOLT" refers to the functional register which is fed into the SW1 regulator block. During power up, contents of the OTP fuses are copied onto the "OTP_SW1_VOLT" register which is further copied on to the "SW1VOLT" register. During normal operation, writes to the "OTP_SW1_VOLT" register has no effect on the output voltage of the SW1 regulator. Writes to the "SW1VOLT" register do have an effect.

### 6.3.2.2 Regulator startup sequence programming

Each regulator has 3-bits or 4-bits allocated to program its start-up time slot from a turn-on event; therefore, each can be placed from position one to seven or one to fifteen in the start-up sequence as shown in Table 32. When the sequence is code is set to 0, the regulator remains off during the startup sequence. It can be enabled using $I^2C$ after the start up sequence is completed. The delay between each position can be programmed to be 0.5 ms or 2.0 ms as shown in Table 33. The start-up sequence terminates at the last programmed regulator. PORB pin is de-asserted HIGH 2.0 ms after the last utilized startup slot.

**Table 32. Start-up sequence**

| OTP_SWx_SEQ[2:0]/ OTP_V33_SEQ[2:0]/ OTP_VSD_SEQ[2:0] | OTP_LDOx_SEQ[3:0] | Sequence |
|---|---|---|
| 000 | 0000 | Off |
| 001 | 0001 | SEQ_CLK_SPEED * 1 |
| 010 | 0010 | SEQ_CLK_SPEED * 2 |
| 011 | 0011 | SEQ_CLK_SPEED * 3 |
| 100 | 0100 | SEQ_CLK_SPEED * 4 |
| 101 | 0101 | SEQ_CLK_SPEED * 5 |
| 110 | 0110 | SEQ_CLK_SPEED * 6 |
| 111 | 0111 | SEQ_CLK_SPEED * 7 |
| – | 1000 | SEQ_CLK_SPEED * 8 |
| – | 1001 | SEQ_CLK_SPEED * 9 |
| – | 1010 | SEQ_CLK_SPEED * 10 |
| – | 1011 | SEQ_CLK_SPEED * 11 |
| – | 1100 | SEQ_CLK_SPEED * 12 |
| – | 1101 | SEQ_CLK_SPEED * 13 |
| – | 1110 | SEQ_CLK_SPEED * 14 |
| – | 1111 | SEQ_CLK_SPEED * 15 |

**Table 33. Start-up sequence clock speed**

| SEQ_CLK_SPEED | Time (µs) |
|---|---|
| 0 | 500 |
| 1 | 2000 |

### 6.3.2.3 EN pin configuration

The EN pin can be configured as either a level sensitive input (EN_CFG = 0), or as an edge sensitive input (EN_CFG = 1). As a level sensitive input, an active high signal turns on the part and an active low signal turns off the part, or puts it into Sleep mode. As an edge sensitive input, such as when connected to a mechanical switch, a falling edge turns on the part and if the switch is held low for greater than or equal to 4.0 seconds, the part turns off or enters Sleep mode.

**Table 34. EN configuration**

| EN_CFG | Mode |
|---|---|
| 0 | EN pin HIGH = ON<br>EN pin LOW = OFF or Sleep mode |
| 1 | EN pin pulled LOW momentarily = ON<br>EN pin LOW for 4.0 seconds = OFF or Sleep mode |

### 6.3.2.4 $I^2C$ address configuration

The $I^2C$ device address can be programmed from 0x08 to 0x0F. This allows flexibility to change the $I^2C$ address to avoid bus conflicts. Address bit, I2C_SLV_ADDR[3] in OTP_I2C_ADDR register is hard coded to “1” while the lower three LSBs of the $I^2C$ address (I2C_SLV_ADDR[2:0]) are programmable as shown in Table 35. The $I^2C$ address of the VR5100 immediately changes after write instructions to the OTP_I2C_ADDR register are complete. To continue using the default address of 0x08, set bit 7 (USE_DEFAULT_ADD) of the OTP_I2C_ADDR register.

**Table 35. $I^2C$ address configuration**

| I2C_SLV_ADDR[3] hard coded | I2C_SLV_ADDR[2:0] | $I^2C$ device address (Hex) |
|---|---|---|
| 1 | 000 | 0x08 |
| 1 | 001 | 0x09 |
| 1 | 010 | 0x0A |
| 1 | 011 | 0x0B |
| 1 | 100 | 0x0C |
| 1 | 101 | 0x0D |
| 1 | 110 | 0x0E |
| 1 | 111 | 0x0F |

### 6.3.2.5 Buck regulator soft start ramp rate

The start-up ramp rate ramp rate or soft start ramp rate of buck regulators can be chosen by using the SWDVS_CLK bit during OTP. Table 36 shows the startup ramp rate options for the buck regulators in the VR5100.

**Table 36. DVS speed selection for SWx**

| SWDVS_CLK | Function |
|---|---|
| 0 | 25 mV step each 2.0 µs |
| 1 | 25 mV step each 4.0 µs |

## 6.3.3 Start-up

Regulators in the VR5100 start up based on the contents of the TBBOTP registers. During cold start, contents from the OTP memory are loaded into the TBBOTP registers when VIN > UVDET. Contents of the TBBOTP registers are reloaded from the fuses during a turn-on event.

The VR5100 is available in a number of pre-programmed flavors to suit a wide variety of system configurations. Refer to Table 37 for programming details of the different flavors. Refer to One-time-programmable memory, page 28 for a detailed explanation of the OTP block.

**Table 37. Start-up configuration (38)**

| OTP registers | Non-programmed | Pre-programmed OTP configuration | |
|---|---|---|---|
| | A0 | A1 | A2 |
| Default I2C Address | 0x08 | 0x08 | 0x08 |
| OTP_VSNVS_VOLT | 1.0 V | 3.0 V | 3.0 V |
| OTP_SW1_VOT | 0.7 V | 0.9 V | 1.8 V |
| OTP_SW1_SEQ | OFF | 2 | 1 |
| OTP_SW2_VOLT | 1.5 V | 1.8 V | 1.8 V |
| OTP_SW2_SEQ | OFF | 1 | OFF |
| OTP_SW3_VOLT | 0.9 V | 1.35 V | 0.9 V |
| OTP_SW3_SEQ | OFF | 1 | 2 |
| OTP_SWBST_VOLT | 5.0 V | 5.0 V | 5.0 V |
| OTP_SWBST_SEQ | OFF | OFF | OFF |
| OTP_LDO1_VOLT | 1.8 V | 1.8 V | 3.0 V |
| OTP_LDO1_SEQ | OFF | OFF | 2 |
| OTP_LDO2_VOLT | 0.8 V | 1.55 V | 0.8 V |
| OTP_LDO2_SEQ | OFF | 1 | 2 |
| OTP_LDO3_VOLT | 1.8 V | 3.3 V | 3.0 V |
| OTP_LDO3_SEQ | OFF | 1 | 3 |
| OTP_LDO4_VOLT | 1.8 V | 2.5 V | 2.5 V |
| OTP_LDO4_SEQ | OFF | 9 | 2 |
| OTP_V33_VOLT | 2.85 V | 3.3 V | 3.0 V |
| OTP_V33_SEQ | OFF | 1 | 6 |
| OTP_VSD_VOLT | 1.80 V | 3.3 V | 3.3 V |
| OTP_VSD_SEQ | OFF | 1 | OFF |
| OTP_SEQ_CLK_SPEED | 500 µs | 2000 µs | 2000 µs |
| OTP_SWDVS_CLK | 12.5 mV/µs | 12.5 mV/µs | 12.5 mV/µs |
| OTP_EN_CFG | Level sensitive | Level sensitive | Level sensitive |
| OTP_SW1_FREQ | 2.0 MHz | 2.0 MHz | 2.0 MHz |
| OTP_SW2_FREQ | 2.0 MHz | 2.0 MHz | 2.0 MHz |
| OTP_SW3_FREQ | 2.0 MHz | 2.0 MHz | 2.0 MHz |
| OTP_PG_EN | PORB in Default Mode | PORB in Default Mode | PORB in Default Mode |

Notes

38. This table specifies the default output voltage of the LDOs and SWx after start-up and/or when the LDOs and SWx are enabled. REFOUT_SEQ is internally fixed to be same as SW3_SEQ. VSD voltage depends on the state of the SD_VSEL pin.

### 6.3.3.1 Start-up timing diagram

The startup timing of the regulators is programmable through OTP and seq_clk_speed. Figure 5 shows the startup timing of the regulators as determined by their OTP sequence. The trimmed 32 kHz clock controls all the start-up timing.

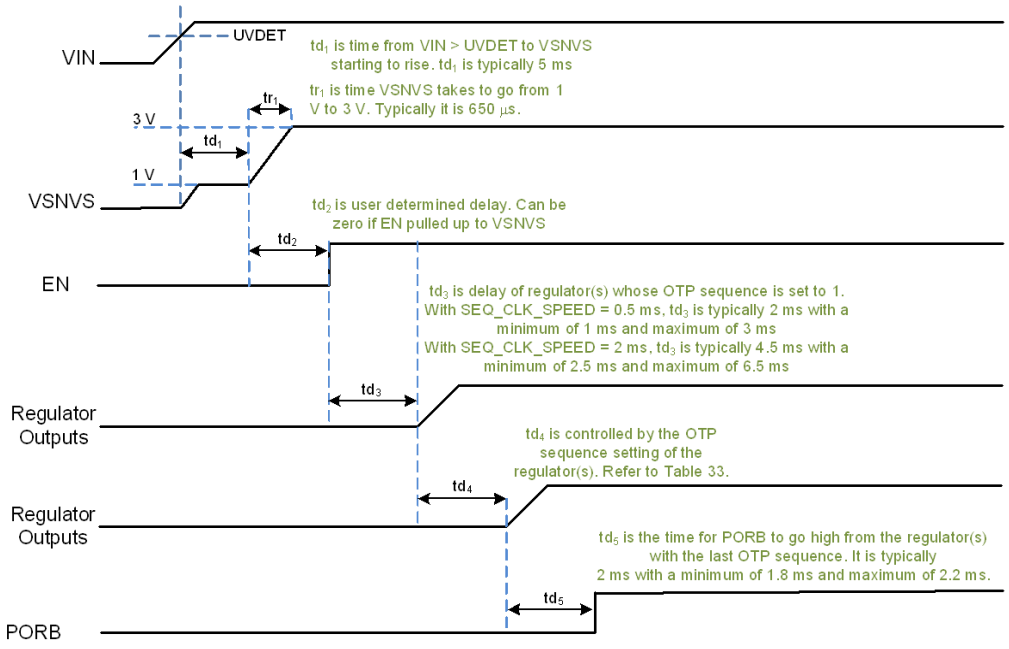



**Figure 5. Start-up timing diagram**

## 6.3.4 16 MHz and 32 kHz clocks

The VR5100 incorporates two clocks: a trimmed 16 MHz RC oscillator and an untrimmed 32 kHz RC oscillator. The 32 kHz untrimmed clock is only used in the following conditions:

- $V_{IN}$ < UVDET
- All regulators are in SLEEP mode
- All regulators are in PFM switching mode

A 32 kHz clock, derived from the 16 MHz trimmed clock, is used when accurate timing is needed under the following conditions:

- During start-up, $V_{IN}$ > UVDET
- EN_CFG = 1, for power button debounce timing

When the 16 MHz is active in the ON mode, the debounce times are referenced to the 32 kHz derived from the 16 MHz clock. The exceptions are the LOWVINI and ENI interrupts, which are referenced to the 32 kHz untrimmed clock. Switching frequency of the switching regulators is derived from the trimmed 16 MHz clock.

The 16 MHz clock and hence the switching frequency of the regulators, can be adjusted to improve the noise integrity of the system. By changing the factory trim values of the 16 MHz clock, the user may add an offset as small as ±3.0% of the nominal frequency. Contact your NXP representative for detailed information on this feature.

## 6.3.5 Internal core voltages

All regulators use the main bandgap as the reference. The main bandgap is bypassed with a capacitor at VBG. VDIG is a 1.5 V regulator which powers all the digital logic in the VR5100. VDIG is regulated at 1.28 V in Off and Coin Cell modes. The VCC supply is used to bias internal analog rails and the OTP fuses. No external DC loading is allowed on VCC, VDIG, or VBG. VDIG is kept powered as long as there is a valid supply

## 6.3.6 REFOUT voltage reference

REFOUT is an internal PMOS half supply voltage follower capable of supplying up to 10 mA. The output voltage is at one half the input voltage. It is typically used as the reference voltage for DDR memories. A filtered resistor divider is utilized to create a low frequency pole. This divider then uses a voltage follower to drive the load.

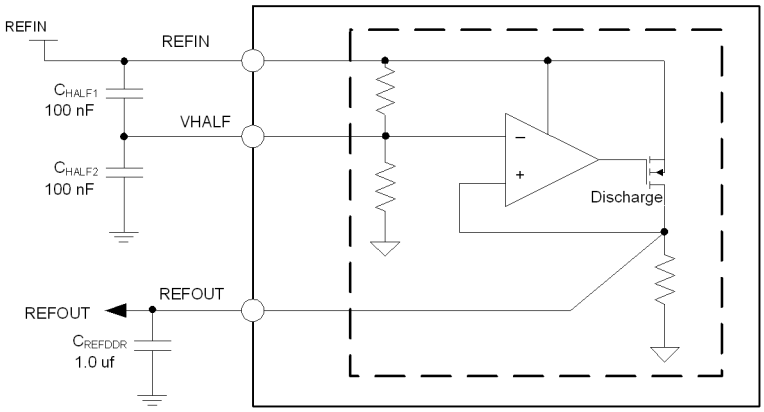



**Figure 6. REFOUT block diagram**

### 6.3.6.1 REFOUT external components

**Table 38. REFOUT external components** (39)

| Capacitor | Capacitance (μF) |
|---|---|
| REFIN (40) to VHALF | 0.1 |
| VHALF to GND | 0.1 |
| REFOUT | 1.0 |

Notes
39. Use X5R or X7R capacitors.
40. REFIN to GND, 1.0 μF minimum capacitance is provided by buck regulator output.

## 6.3.7 Buck regulators

The VR5100 integrates three independent buck regulators: SW1, SW2, and SW3. Output of the buck regulators during start up is programmable through OTP. Each regulator has associated registers controlling its output voltage during On, Standby, and Sleep modes. During start-up, contents of the OTP_SWx_VOLT register is copied onto the SWxVOLT[4:0], SWxSTBY[4:0] and SWxOFF[4:0]. After boot up, contents of the SWxVOLT, SWxSTBY and SWxOFF registers can be set through $I^2C$ to set the output voltage during On, Standby, and Sleep modes respectively.

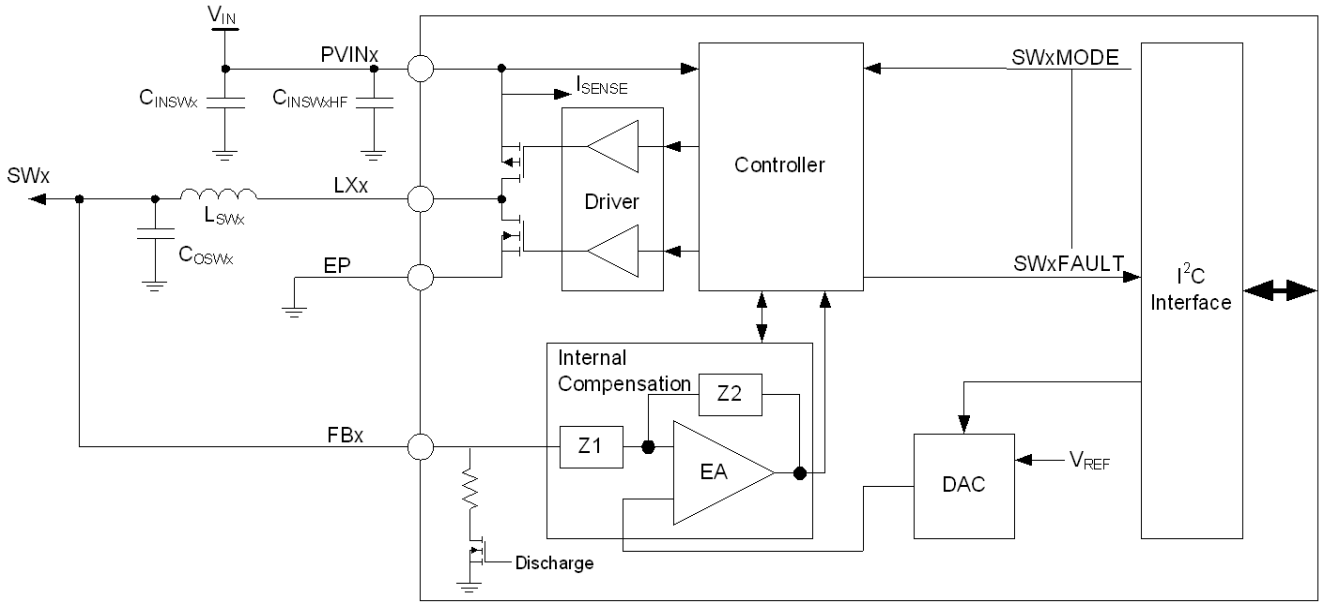



**Figure 7. Generic SWx block diagram**

**Table 39. SWx regulators external components**

| Components | Description | Values |
|---|---|---|
| CINSWx | SWx input capacitor | 4.7 µF |
| CINSWxHF | SWx decoupling input capacitor | 0.1 µF |
| COSWx | SWx output capacitor | 2 x 22 µF (10 V or higher voltage rated capacitors) or 3 x 22 µF (6.3 V rated capacitors) |
| LSWx | SWx inductor | 1.5 µH |

Use X5R or X7R capacitors with voltage rating at least two times the nominal voltage.

## 6.3.7.1 Switching modes

To improve system efficiency the buck regulators can operate in different switching modes. Changing between switching modes can occur by any of the following means: I²C programming, exiting/entering the Standby mode, exiting/entering Sleep mode, and load current variation. Available switching modes for buck regulators are presented in Table 40.

**Table 40. Switching mode description**

| Mode | Description |
|---|---|
| OFF | The regulator is switched off and the output voltage is discharged using an internal resistor |
| PFM | In this mode, the regulator operates in forced PFM mode. The main error amplifier is turned off and a hysteretic comparator is used to regulate output voltage. Use this mode for load currents less than 50 mA. |
| PWM | In this mode, the regulator operates in forced PWM mode. |
| APS | In this mode, the regulator operates in pulse skipping mode at light loads and switches over to PWM modes for heavier load conditions. This is the default mode in which the regulators power up during a turn-on event. |

During soft-start of the buck regulators, the controller transitions through the PFM, APS, and PWM switching modes. 3.0 ms after the output voltage reaches regulation, the controller transitions to the selected switching mode. Depending on the particular switching mode selected, additional ripple may be observed on the output voltage rail as the controller transitions between switching modes. The operating mode of the regulator in On and Standby Modes is controlled using the SWxMODE[3:0] bits associated with each regulator. Table 41 summarizes the Buck regulator programmability for Normal and Standby modes.

**Table 41. Regulator mode control**

| SWxMODE[3:0] | Normal mode | Standby mode |
|---|---|---|
| 0000 | Off | Off |
| 0001 | PWM | Off |
| 0010 | Reserved | Reserved |
| 0011 | PFM | Off |
| 0100 | APS | Off |
| 0101 | PWM | PWM |
| 0110 | PWM | APS |
| 0111 | Reserved | Reserved |
| 1000 (default) | APS | APS |
| 1001 | Reserved | Reserved |
| 1010 | Reserved | Reserved |
| 1011 | Reserved | Reserved |
| 1100 | APS | PFM |
| 1101 | PWM | PFM |
| 1110 | Reserved | Reserved |
| 1111 | Reserved | Reserved |

Transitioning between Normal and Standby modes can affect a change in switching modes as well as output voltage. When in Standby mode, the regulator outputs the voltage programmed in its standby voltage register and operates in the mode selected by the SWxMODE[3:0] bits. Upon exiting Standby mode, the regulator returns to its normal switching mode and its output voltage programmed in its voltage register.

Any regulators whose SWxOMODE bit is set to “1” enters Sleep mode if a EN turn-off event occurs, and any regulator whose SWxOMODE bit is set to “0” is turned off. In Sleep mode, the regulator outputs the voltage programmed in SWxOFF registers and operates in the PFM mode. The regulator exits the Sleep mode when a turn-on event occurs. Any regulator whose SWxOMODE bit is set to “1” remains on and changes to its normal configuration settings when exiting the Sleep state to the ON state. Any regulator whose SWxOMODE bit is set to “0” is powered up with the same delay in the start-up sequence as when powering ON from Off. At this point, the regulator returns to its default ON state output voltage and switch mode settings. When Sleep mode is activated by the SWxOMODE bit, the regulator uses the set point as programmed by SW1OFF[4:0] for SW1 and by SW2OFF[2:0] for SW2, and SW3OFF[3:0] for SW3.

### 6.3.7.2 Dynamic voltage scaling

To reduce overall power consumption, processor core voltages can be varied depending on the mode or activity level of the processor.

1. Normal operation: The output voltage is selected by $I^2C$ bits SW1[4:0] for SW1 and SW2[2:0] for SW2, and SW3[3:0] for SW3. A voltage transition initiated by $I^2C$ is governed by the DVS stepping rates shown in Table 42.

2. Standby mode: The output voltage can be selected by $I^2C$ bits SW1STBY[4:0] for SW1 and by bits SW2STBY[2:0] for SW2, and SW3STBY[3:0] for SW3. Voltage transitions initiated by a Standby event are governed by the DVS stepping rates shown in Table 42.

3. Sleep mode: The output voltage can be higher or lower than in normal operation, but is typically selected to be the lowest state retention voltage of a given processor; it is selected by $I^2C$ bits SW1OFF[4:0] for SW1 and by bits SW2OFF[2:0] for SW2, and SW3OFF[3:0] for SW3. Voltage transitions initiated by a turn-off event are governed by the DVS stepping rates shown in Table 42.

**Table 42. DVS speed selection for SWx**

| SWxDVSSPEED | Function |
|---|---|
| 0 | 25 mV step each 2.0 µs |
| 1 | 25 mV step each 4.0 µs |

The regulators have a strong sourcing capability and sinking capability in PWM mode, therefore the fastest rising and falling slopes are determined by the regulator in PWM mode. However, if the regulators are programmed in PFM or APS mode during a DVS transition, the falling slope can be influenced by the load. Additionally, as the current capability in PFM mode is reduced, controlled DVS transitions in PFM mode could be affected. Critically timed DVS transitions are best assured with PWM mode operation.

Figure 8 shows the general behavior for the regulators when initiated with $I^2C$ programming, or standby control. During the DVS period the overcurrent condition on the regulator should be masked.

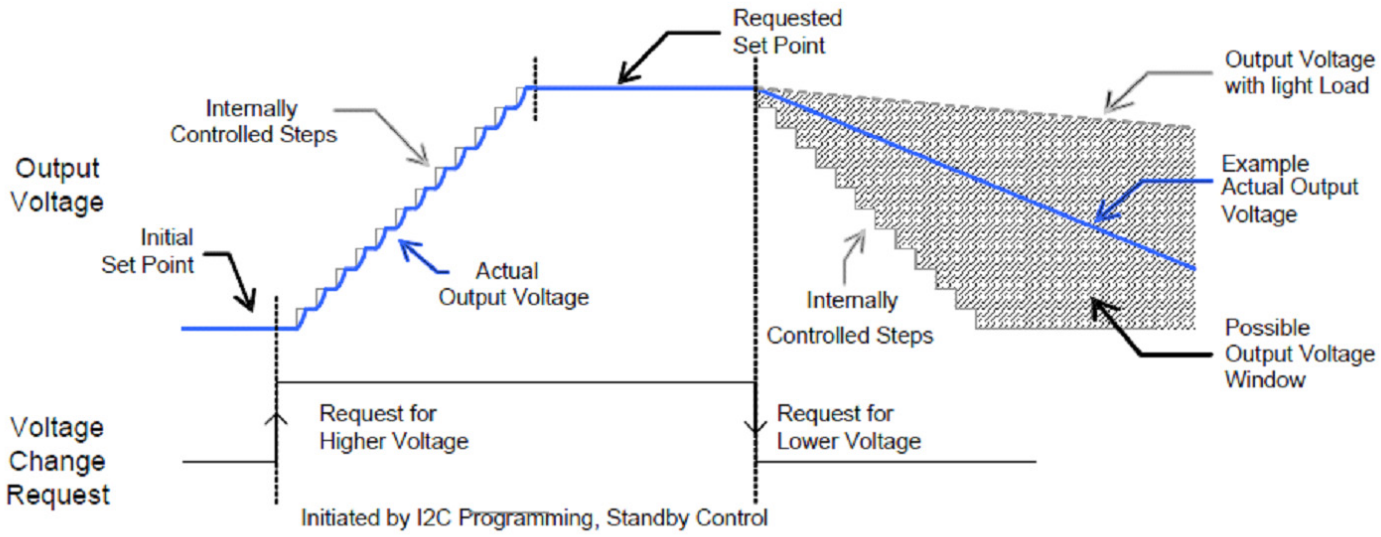



**Figure 8. Voltage stepping with DVS**

## 6.3.7.3 Regulator phase clock

The SWxPHASE[1:0] bits select the phase of the regulator clock as shown in Table 43. By default, each regulator is initialized at 90 ° out of phase with respect to each other. For example, SW1 is set to 0 °, SW2 is set to 90 °, and SW3 is set to 180 ° by default at power up.

**Table 43. Regulator phase clock selection**

| SWxPHASE[1:0] | Phase of clock sent to regulator (degrees) |
|---|---|
| 00 | 0 |
| 01 | 90 |
| 10 | 90 |
| 11 | 270 |

The SWxFREQ[1:0] register is used to set the desired switching frequency for each one of the buck regulators. Table 45 shows the selectable options for SWxFREQ[1:0]. For each frequency, all phases are available, this allows regulators operating at different frequencies to have different relative switching phases. However, not all combinations are practical. For example, 2.0 MHz, 90 ° and 4.0 MHz, 180 ° are the same in terms of phasing. Table 44 shows the optimum phasing when using more than one switching frequency.

**Table 44. Optimum phasing**

| Frequencies | Optimum phasing |
|---|---|
| 1.0 MHz<br>2.0 MHz | 0°<br>180° |
| 1.0 MHz<br>4.0 MHz | 0°<br>180° |
| 2.0 MHz<br>4.0 MHz | 0°<br>180° |
| 1.0 MHz<br>2.0 MHz<br>4.0 MHz | 0°<br>90°<br>90° |

**Table 45. Regulator Frequency Configuration**

| SWxFREQ[1:0] | Frequency |
|---|---|
| 00 | 1.0 MHz |
| 01 | 2.0 MHz (default) |
| 10 | 4.0 MHz |
| 11 | Reserved |

## 6.3.7.4 SW1

SW1 is a 3.8 A current capability for high current applications. The feedback and all other controls are accomplished by use of pin FB1 and SW1 control registers, respectively.

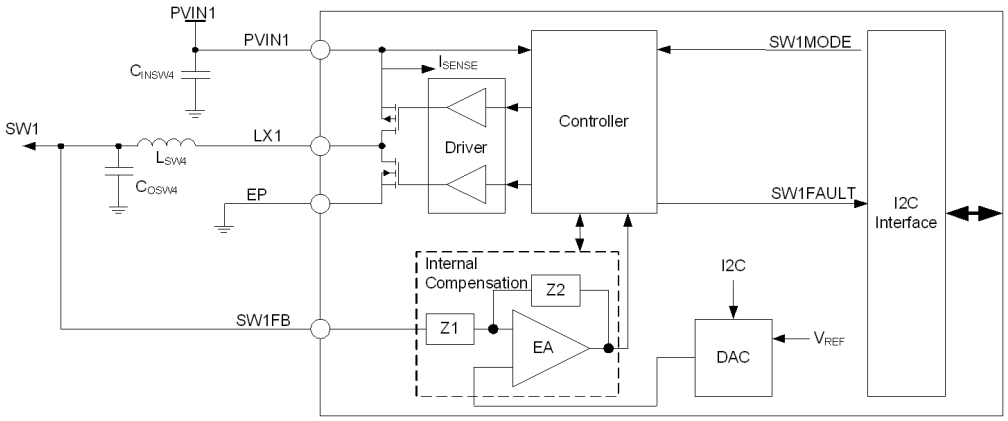



**Figure 9. SW1 diagram**

## 6.3.7.5 SW1 setup and control registers

SW1 output voltage is programmable from 0.700 V to 1.425 V in steps of 25 mV. They can additionally be programmed at 1.8 V or 3.3 V. The output voltage set point is independently programmed for Normal, Standby, and Sleep mode by setting the SW1[4:0], SW1STBY[4:0], and SW1OFF[4:0] bits respectively. Table 46 shows the output voltage coding for SW1. Values shown in Table 46 are also to be used during OTP programming by setting the OTP_SW1_VOLT register appropriately.

**Table 46. SW1 output voltage configuration**

| Set point | SW1[4:0] SW1STBY[4:0] SW1OFF[4:0] | SW1 output (V) | Set point | SW1[4:0] SW1STBY[4:0] SW1OFF[4:0] | SW1 output (V) |
|---|---|---|---|---|---|
| 0 | 00000 | 0.700 | 16 | 10000 | 1.100 |
| 1 | 00001 | 0.725 | 17 | 10001 | 1.125 |
| 2 | 00010 | 0.750 | 18 | 10010 | 1.150 |
| 3 | 00011 | 0.775 | 19 | 10011 | 1.175 |
| 4 | 00100 | 0.800 | 20 | 10100 | 1.200 |
| 5 | 00101 | 0.825 | 21 | 10101 | 1.225 |
| 6 | 00110 | 0.850 | 22 | 10110 | 1.250 |
| 7 | 00111 | 0.875 | 23 | 10111 | 1.275 |
| 8 | 01000 | 0.900 | 24 | 11000 | 1.300 |
| 9 | 01001 | 0.925 | 25 | 11001 | 1.325 |
| 10 | 01010 | 0.950 | 26 | 11010 | 1.350 |
| 11 | 01011 | 0.975 | 27 | 11011 | 1.375 |

**Table 46. SW1 output voltage configuration (continued)**

| Set point | SW1[4:0] SW1STBY[4:0] SW1OFF[4:0] | SW1 output (V) | Set point | SW1[4:0] SW1STBY[4:0] SW1OFF[4:0] | SW1 output (V) |
|---|---|---|---|---|---|
| 12 | 01100 | 1.000 | 28 | 11100 | 1.400 |
| 13 | 01101 | 1.025 | 29 | 11101 | 1.425 |
| 14 | 01110 | 1.050 | 30 | 11110 | 1.8 |
| 15 | 01111 | 1.075 | 31 | 11111 | 3.3 |

Table 47 provides a list of registers used to configure and operate SW1 regulator.

**Table 47. SW1 register summary**

| Register | Address | Output |
|---|---|---|
| SW1VOLT | 0x20 | SW1 Output voltage set point in normal operation |
| SW1STBY | 0x21 | SW1 Output voltage set point on Standby |
| SW1OFF | 0x22 | SW1 Output voltage set point on Sleep |
| SW1MODE | 0x23 | SW1 Switching mode selector register |
| SW1CONF | 0x24 | SW1 DVS, phase, and frequency configuration |
| SW1CONF | 0x32 | SW1 DVS, phase, and frequency configuration |

## 6.3.7.6 SW2 setup and control registers

SW2 is a single phase, 1.25 A rated buck regulator. SW2 output voltage is programmable from 1.500 V to 1.850 V in 50 mV steps if the OTP_SW2_HI bit is low or from 2.500 V to 3.300 V in 150 mV steps if the bit OTP_SW2_HI is set high. During normal operation, output voltage of the SW2 regulator can be changed through $I^2C$ only within the range set by the OTP_SW2_HI bit. The output voltage set point is independently programmed for Normal, Standby, and Sleep mode by setting the SW2[2:0], SW2STBY[2:0] and SW2OFF[2:0] bits, respectively. Table 48 shows the output voltage coding valid for SW2.

**Table 48. SW2 output voltage configuration**

| Low output voltage range (OTP_SW2_HI= 0) | | High output voltage range (OTP_SW2_HI=1) | |
|---|---|---|---|
| SW2[2:0] SW2STBY[2:0] SW2OFF[2:0] | SW2 output | SW2[2:0] SW2STBY[2:0] SW2OFF[2:0] | SW2 output |
| 000 | 1.500 | 000 | 2.500 |
| 001 | 1.550 | 001 | 2.800 |
| 010 | 1.600 | 010 | 2.850 |
| 011 | 1.650 | 011 | 3.000 |
| 100 | 1.700 | 100 | 3.100 |
| 101 | 1.750 | 101 | 3.150 |
| 110 | 1.800 | 110 | 3.200 |
| 111 | 1.850 | 111 | 3.300 |

Setup and control of SW2 is done through the $I^2C$ registers listed in Table 49.

**Table 49. SW2 register summary**

| Register | Address | Description |
|---|---|---|
| SW2VOLT | 0x35 | Output voltage set point on normal operation |
| SW2STBY | 0x36 | Output voltage set point on Standby |

**Table 49. SW2 register summary**

| Register | Address | Description |
|---|---|---|
| SW2OFF | 0x37 | Output voltage set point on Sleep |
| SW2MODE | 0x38 | Switching Mode selector register |
| SW2CONF | 0x39 | DVS, Phase, Frequency, and ILIM configuration |

### 6.3.7.7 SW3 setup and control registers

SW3 output voltage is programmable from 0.90 V to 1.65 V in 50 mV steps to support different types of DDR memory as listed in Table 50.

**Table 50. SW3 output voltage configuration**

| SW3[3:0] | SW3 output (V) | SW3[3:0] | SW3 output (V) |
|---|---|---|---|
| 0000 | 0.90 | 1000 | 1.30 |
| 0001 | 0.95 | 1001 | 1.35 |
| 0010 | 1.00 | 1010 | 1.40 |
| 0011 | 1.05 | 1011 | 1.45 |
| 0100 | 1.10 | 1100 | 1.50 |
| 0101 | 1.15 | 1101 | 1.55 |
| 0110 | 1.20 | 1110 | 1.60 |
| 0111 | 1.25 | 1111 | 1.65 |

Table 51 provides a list of registers used to configure and operate SW3.

**Table 51. SW3 register summary**

| Register | Address | Output |
|---|---|---|
| SW3VOLT | 0x3C | SW3 Output voltage set point on normal operation |
| SW3STBY | 0x3D | SW3 Output voltage set point on Standby |
| SW3OFF | 0x3E | SW3 Output voltage set point on Sleep |
| SW3MODE | 0x3F | SW3 Switching mode selector register |
| SW3CONF | 0x40 | SW3 DVS, phase, frequency and ILIM configuration |

## 6.3.8 Boost regulator

SWBST is a boost regulator with a programmable output from 5.0 V to 5.15 V. SWBST can supply the VUSB regulator for the USB PHY in OTG mode, as well as the VBUS voltage. Note that the parasitic leakage path for a boost regulator causes the SWBSTOUT and FBBST voltage to be a Schottky drop below the input voltage whenever SWBST is disabled. A load switch is recommended on the output path to isolate the output for applications where this is not desired. The switching NMOS transistor is integrated on-chip. Figure 10 shows the block diagram and component connection for the boost regulator.

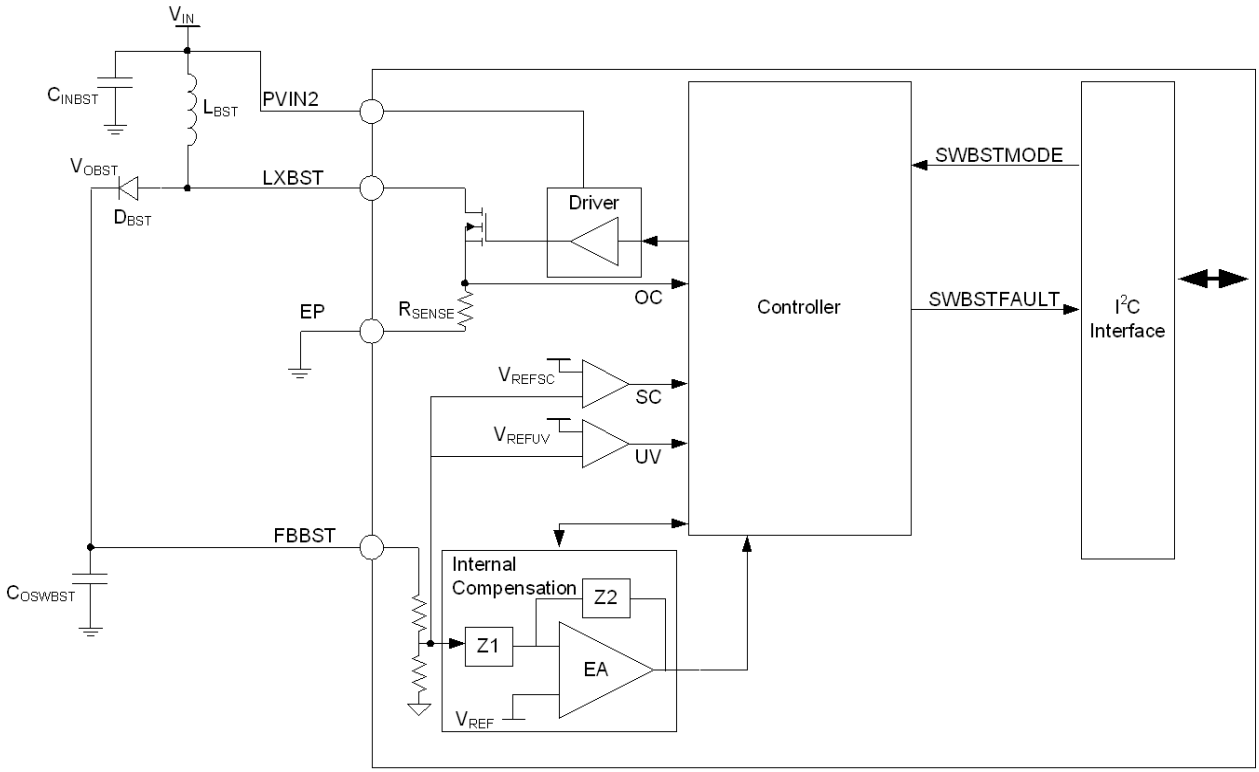



**Figure 10. Boost regulator architecture**

## 6.3.8.1 SWBST setup and control

Boost regulator control is done through a single register SWBSTCTL described in Table 52. SWBST is included in the power-up sequence if its OTP power-up timing bits, OTP_SWBST_SEQ[2:0], are not all zeros.

**Table 52. Register SWBSTCTL - ADDR 0x66**

| Name | Bit # | R/W | Default | Description |
|---|---|---|---|---|
| SWBST1VOLT | 1:0 | R/W | 0b00 | Set the output voltage for SWBST<br>00 = 5.000 V<br>01 = 5.050 V<br>10 = 5.100 V<br>11 = 5.150 V |
| SWBST1MODE | 3:2 | R | 0b10 | Set the Switching mode on Normal operation<br>00 = OFF<br>01 = PFM<br>10 = Auto (Default) (41)<br>11 = APS |
| UNUSED | 4 | – | 0b0 | UNUSED |
| SWBST1STBYMODE | 6:5 | R/W | 0b10 | Set the Switching mode on Standby<br>00 = OFF<br>01 = PFM<br>10 = Auto (Default) (41)<br>11 = APS |
| UNUSED | 7 | – | 0b0 | UNUSED |

Notes

41. In Auto mode, the controller automatically switches between PFM and APS modes depending on the load current. Regulator switches in Auto mode if enabled in the startup sequence.

### 6.3.8.2 SWBST external components

**Table 53. SWBST external component requirements**

| Components | Description | Values |
|---|---|---|
| $C_{INBST}$ (42) | SWBST input capacitor | 10 µF |
| $C_{INBSTHF}$ (42) | SWBST decoupling input capacitor | 0.1 µF |
| $C_{OSWBST}$ (42) | SWBST output capacitor | 2 x 22 µF |
| $L_{SBST}$ | SWBST inductor | 2.2 µH |
| $D_{BST}$ | SWBST boost diode | 1.0 A, 20 V Schottky |

Notes
42. Use X5R or X7R capacitors.

## 6.3.9 LDO regulators description

This section describes the LDO regulators provided by the VR5100. All regulators use the main bandgap as reference. When a regulator is disabled, the output is discharged by an internal pull-down resistor.

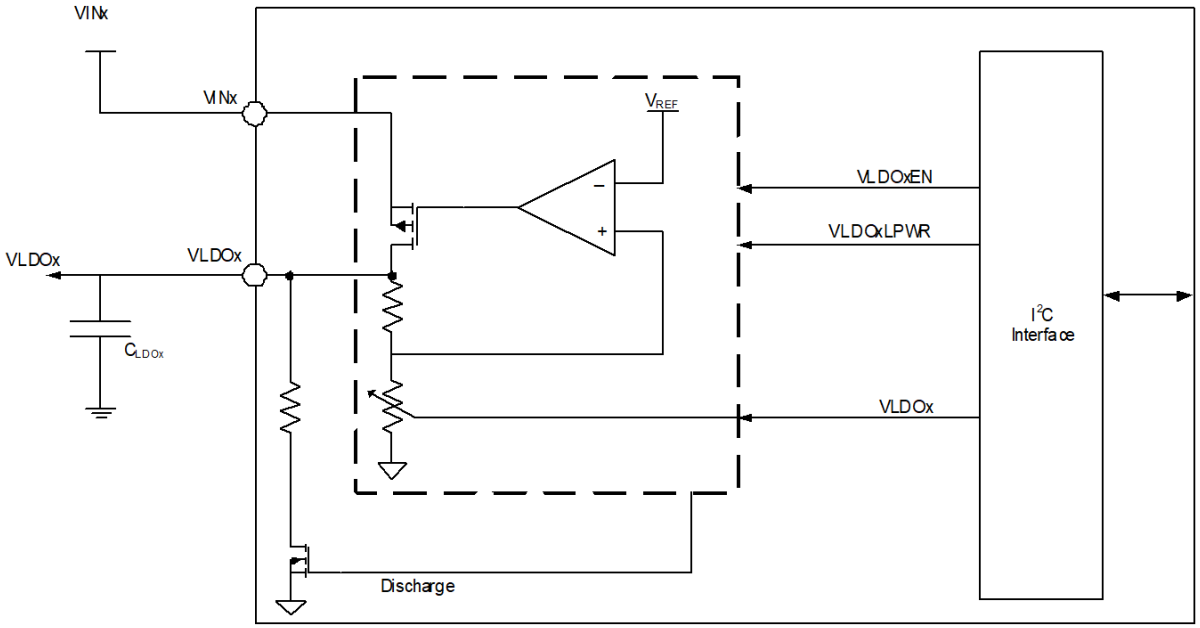



**Figure 11. General LDO block diagram**

### 6.3.9.1 External components

Table 54 lists the typical component values for the general purpose LDO regulators.

**Table 54. LDO external components**

| Regulator | Output capacitor (μF)[43] |
|---|---|
| LDO1 | 2.2 |
| LDO2 | 4.7 |
| LDO3 | 2.2 |
| LDO4 | 4.7 |
| V33 | 4.7 |
| VSD | 2.2 |

Notes
43. Use X5R/X7R ceramic capacitors.

### 6.3.9.2 Current limit protection

All the LDO regulators in the VR5100 have current limit protection. In the event of an overload condition, the regulators transitions from a voltage regulator to a current regulator regulating output current per the current limit threshold.

Additionally, if the REGSCPEN bit in Table 117 is set, the LDO is turned off if the current limit event lasts for more than 8.0 ms. The LDO is disabled by resetting its LDOxEN bit, while at the same time, an interrupt LDOxFAULTI is generated to flag the fault to the system processor. The LDOxFAULTI interrupt is maskable through the LDOxFAULTM mask bit. By default, the REGSCPEN is not set; therefore, at start-up none of the regulators is disabled if an overloaded condition occurs. A fault interrupt, LDOxFAULTI, is generated in an overload condition regardless of the state of the REGSCPEN bit.

### 6.3.9.3 LDO voltage control

Each LDO is fully controlled through its respective LDOxCTL register. This register enables the user to set the LDO output voltage according toTable 55 for LDO1 and LDO2; and uses the voltage set point on Table 56 for LDO3 and LDO4. Table 57 lists the voltage set points for the V33 LDO. During power-up, contents of the OTP_LDO_VOLT register is copied to the LDOxCTL registers.

**Table 55. LDO1, LDO2 output voltage configuration**

| LDO1[3:0] LDO2[3:0] | LDO1 output (V) | LDO2 output (V) |
|---|---|---|
| 0000 | 1.80 | 0.80 |
| 0001 | 1.90 | 0.85 |
| 0010 | 2.00 | 0.90 |
| 0011 | 2.10 | 0.95 |
| 0100 | 2.20 | 1.00 |
| 0101 | 2.30 | 1.05 |
| 0110 | 2.40 | 1.10 |
| 0111 | 2.50 | 1.15 |
| 1000 | 2.60 | 1.20 |
| 1001 | 2.70 | 1.25 |
| 1010 | 2.80 | 1.30 |
| 1011 | 2.90 | 1.35 |
| 1100 | 3.00 | 1.40 |
| 1101 | 3.10 | 1.45 |
| 1110 | 3.20 | 1.50 |
| 1111 | 3.30 | 1.55 |

**Table 56. LDO3, LDO4 output voltage configuration**

| LDO3[3:0] LDO4[3:0] | LDO3 or LDO4 output (V) |
|---|---|
| 0000 | 1.80 |
| 0001 | 1.90 |
| 0010 | 2.00 |
| 0011 | 2.10 |
| 0100 | 2.20 |
| 0101 | 2.30 |
| 0110 | 2.40 |
| 0111 | 2.50 |
| 1000 | 2.60 |
| 1001 | 2.70 |
| 1010 | 2.80 |
| 1011 | 2.90 |
| 1100 | 3.00 |
| 1101 | 3.10 |
| 1110 | 3.20 |
| 1111 | 3.30 |

**Table 57. V33 output voltage configuration**

| V33[1:0] | V33 output (V) |
|---|---|
| 00 | 2.85 |
| 01 | 3.00 |
| 10 | 3.15 |
| 11 | 3.30 |

**Table 58. VSD output voltage configuration**

| VSD[1:0] | VSD output (V) VSD_VSEL= 0 | VSD output (V) VSD_VSEL= 1 |
|---|---|---|
| 00 | 2.85 | 1.80 |
| 01 | 3.00 | 1.80 |
| 10 | 3.15 | 1.80 |
| 11 | 3.30 | 1.85 |

Along with the output voltage configuration, the LDOs can be enabled or disabled at anytime during normal mode operation, as well as programmed to stay “ON” or be disabled when the PMIC enters Standby mode. Each regulator has associated $I^2C$ bits for this. Table 59 presents a summary of all valid combinations of the control bits on LDOxCTL register and the expected behavior of the LDO output.

**Table 59. LDO control**

| LDOxEN/ V33EN/ VSD | LDOxSTBY/ V33STBY/ VSD | STANDBY (44) | LDOxOUT/ V33OUT/ VSD |
|---|---|---|---|
| 0 | X | X | Off |
| 1 | 0 | X | On |
| 1 | 1 | 0 | On |
| 1 | 1 | 1 | Off |

Notes
44. STANDBY refers to a Standby event as described earlier.

## 6.3.10 VSNVS LDO/Switch

VSNVS powers the low power, SNVS/RTC domain on the processor. It derives its power from either VIN, or coin cell, and cannot be disabled. When powered by both, $V_{IN}$ takes precedence when above the appropriate comparator threshold. When powered by $V_{IN}$, VSNVS is an LDO capable of supplying 3.0 V. When powered by coin cell, the VSNVS output tracks the coin cell voltage by means of a switch, whose maximum resistance is 100 Ω. In this case, the $V_{SNVS}$ voltage is simply the coin cell voltage minus the voltage drop across the switch, which is 100 mV at a rated maximum load current of 1000 μA.

When the coin cell is applied for the very first time, VSNVS outputs 1.0 V. Only when $V_{IN}$ is applied thereafter does $V_{SNVS}$ transition to its default value. Upon subsequent removal of $V_{IN}$, with the coin cell attached, $V_{SNVS}$ changes configuration from an LDO to a switch, provided certain conditions are met as described in Table 60.

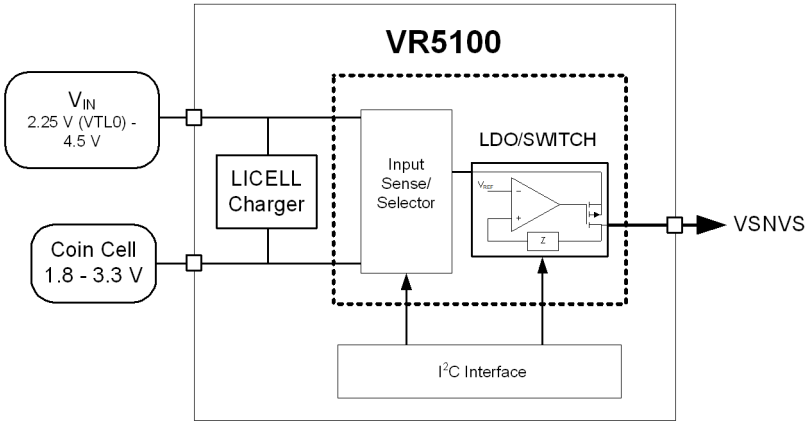



Table 60 provides a summary of the $V_{SNVS}$ operation at different input voltage $V_{IN}$ and with or without coin cell connected to the system.

**Table 60. SNVS modes of operation**

| VSNVSVOLT[2:0] | VIN | Mode |
|---|---|---|
| 110 | > VTH1 | VIN LDO 3.0 V |
| 110 | < VTL1 | Coin cell switch |

### 6.3.10.1 VSNVS control

The $V_{SNVS}$ output level is configured through the VSNVSVOLT[2:0] bits on VSNVSCTL register as shown in table Table 61.

**Table 61. Register VSNVSCTL - ADDR 0x6B**

| Name | Bit # | R/W | Default | Description |
|---|---|---|---|---|
| VSNVSVOLT | 2:0 | R/W | 0b000 | Configures VSNVS output voltage (45)<br>000 = RSVD<br>001 = RSVD<br>010 = RSVD<br>011 = RSVD<br>100 = RSVD<br>101 = RSVD<br>110 = 3.0 V (default)<br>111 = RSVD |
| UNUSED | 7:3 | – | 0b00000 | UNUSED |

Notes
45. Only valid when a valid input voltage is present.

### 6.3.10.2 VSNVS external components

**Table 62. VSNVS external components**

| Capacitor | Value (μF) |
|---|---|
| VSNVS | 0.47 |

### 6.3.10.3 Coin cell battery backup

The LICELL pin provides for a connection of a coin cell backup battery or a “super” capacitor. If the voltage at VIN goes below the $V_{IN}$ threshold (VTL1), contact-bounced, or removed, the coin cell maintained logic is powered by the voltage applied to LICELL. The supply for internal logic and the VSNVS rail switches over to the LICELL pin when $V_{IN}$ goes below VTL1, even in the absence of a voltage at the LICELL pin, resulting in clearing of memory and turning off VSNVS. Applications concerned about this behavior can tie the LICELL pin to any system voltage between 1.8 V and 3.0 V. A 0.47 μF capacitor should be placed from LICELL to ground under all circumstances.

### 6.3.10.4 Coin cell charger control

The coin cell charger circuit functions as a current-limited voltage source, resulting in the CC/CV taper characteristic typically used for rechargeable Lithium-Ion batteries. The coin cell charger is enabled via the COINCHEN bit while the coin cell voltage is programmable through the VCOIN[2:0] bits on register COINCTL on Table 63. The coin cell charger voltage is programmable. In the ON state, the charger current is fixed at ICOINHI. In Sleep and Standby modes, the charger current is reduced to a typical 10 μA. In the OFF state, coin cell charging is not available as the main battery could be depleted unnecessarily. The coin cell charging is stopped when $V_{IN}$ is below UVDET.

**Table 63. Coin cell charger voltage**

| VCOIN[2:0] | $V_{COIN}$ (V) (46) |
|---|---|
| 000 | 2.50 |
| 001 | 2.70 |
| 010 | 2.80 |
| 011 | 2.90 |
| 100 | 3.00 |
| 101 | 3.10 |
| 110 | 3.20 |
| 111 | 3.30 |

Notes
46. Coin cell voltages selected based on the type of LICELL used on the system.

**Table 64. Register COINCTL - ADDR 0x1A**

| Name | Bit # | R/W | Default | Description |
|---|---|---|---|---|
| VCOIN | 2:0 | R/W | 0x00 | Coin cell charger output voltage selection. See Table 63 for all options selectable through these bits. |
| COINCHEN | 3 | R/W | 0x00 | Enable or disable the Coin cell charger |
| UNUSED | 7:4 | – | 0x00 | UNUSED |

### 6.3.10.5 External components

**Table 65. Coin cell charger external components**

| Component | Value | Units |
|---|---|---|
| LICELL bypass capacitor | 100 | nF |

## 6.4 Power dissipation

During operation, the temperature of the die should not exceed the operating junction temperature noted in Table 4. To optimize the thermal management and to avoid overheating, the VR5100 provides thermal protection. An internal comparator monitors the die temperature. Interrupts THERM110, THERM120, THERM125, and THERM130 is generated when the respective thresholds specified in Table 66 are crossed in either direction. The temperature range can be determined by reading the THERMxxxS bits in register INTSENSE0.

In the event of excessive power dissipation, thermal protection circuitry shuts down the VR5100. This thermal protection acts above the thermal protection threshold listed in Table 66. To avoid any unwanted power downs resulting from internal noise, the protection is debounced for 8.0 ms. This protection should be considered as a fail-safe mechanism and therefore the system should be configured so this protection is not tripped under normal conditions.

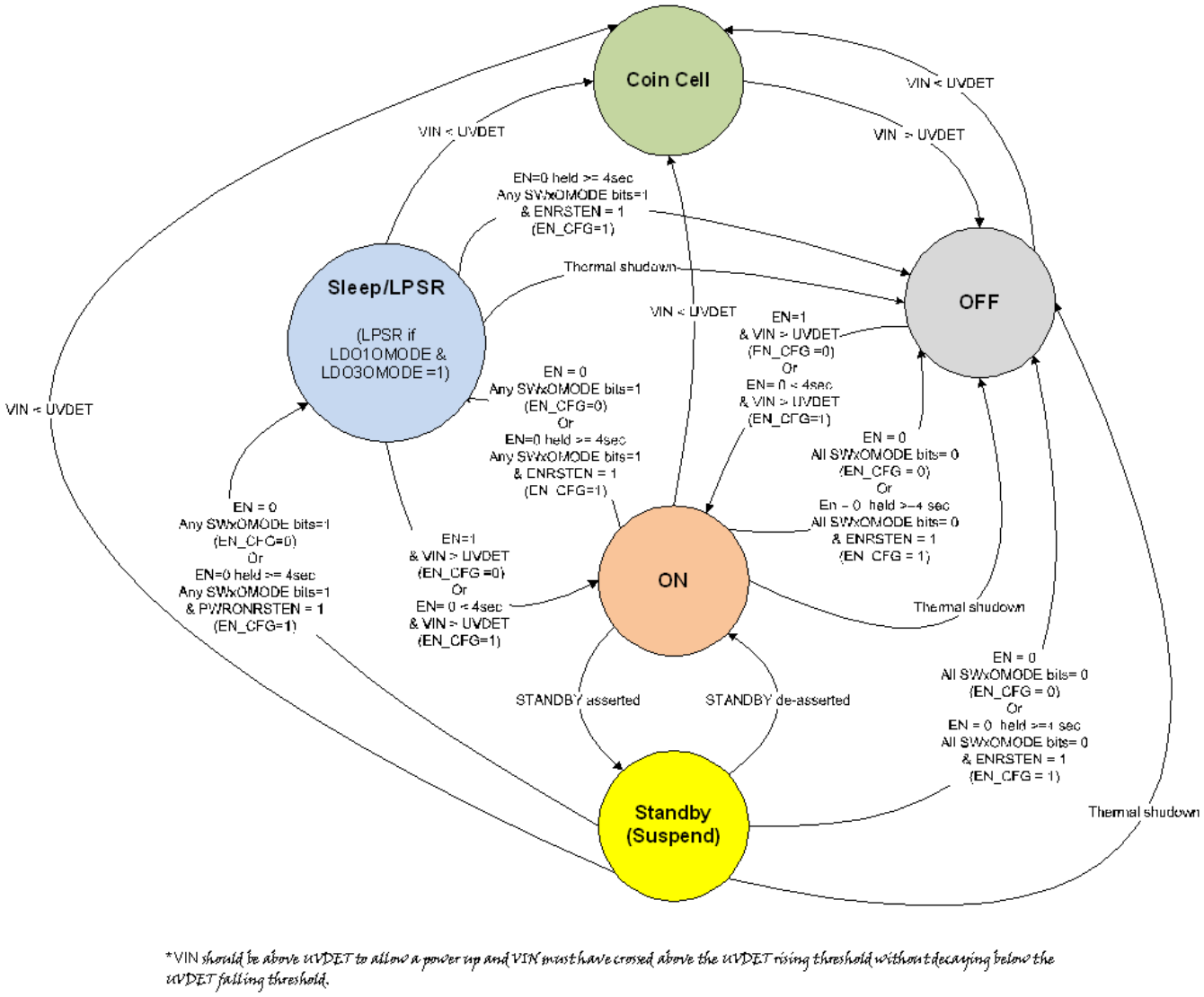
**Table 66. Thermal protection thresholds**

| Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| Thermal 110 °C Threshold (THERM110) | 100 | 110 | 120 | °C |
| Thermal 120 °C Threshold (THERM120) | 110 | 120 | 130 | °C |
| Thermal 125 °C Threshold (THERM125) | 115 | 125 | 135 | °C |
| Thermal 130 °C Threshold (THERM130) | 120 | 130 | 140 | °C |
| Thermal Warning Hysteresis | 2.0 | – | 4.0 | °C |
| Thermal Protection Threshold | 130 | 140 | 150 | °C |

# 6.5 Modes of operation

## 6.5.1 State diagram

The operation of the VR5100 can be reduced to five states, or modes: ON, OFF, Sleep, Standby and Coin Cell. Figure 12 shows the state diagram of the VR5100, along with the conditions to enter and exit from each state.




*VIN should be above UVDET to allow a power up and VIN must have crossed above the UVDET rising threshold without decaying below the UVDET falling threshold.

**Figure 12. State diagram**

To complement the state diagram in Figure 12, a description of the states is provided in following sections. Note that $V_{IN}$ must exceed the rising UVDET threshold to allow a power up. Refer to Table 27 for the UVDET thresholds. Additionally the interrupt signal, INTB, is only active in Sleep, Standby, and ON states.

### 6.5.1.1 ON mode

The VR5100 enters the On mode after a turn-on event. PORB is de-asserted, and pulled high via an external pull-up resistor, in this mode of operation. To enter the On mode, VIN voltage must surpass the rising UVDET threshold and EN must be asserted. From the On mode, when the voltage at VIN drops below the undervoltage falling threshold, UVDET, the state machine transitions to the Coin Cell mode.

### 6.5.1.2 OFF mode

The VR5100 enters the Off mode after a turn-off event. Only VDIG and VSNVS are powered in the mode of operation. To exit the Off mode, a valid turn-on event is required. PORB is asserted, LOW, in this mode. Turn off events can be achieved using the EN pin, thermal protection, as described below.

### 6.5.1.3 EN pin

The EN pin is used to power off the VR5100. The EN pin can be configured with OTP to power off the PMIC under the following two conditions:

1. EN_CFG bit = 0, SWxOMODE bit = 0 and EN pin is low.
2. EN_CFG bit = 1, SWxOMODE bit = 0, ENRSTEN = 1 and EN is held low for longer than 4.0 seconds. Alternatively, the system can be configured to restart automatically by setting the RESTARTEN bit.

### 6.5.1.4 Thermal protection

If the die temperature surpasses a given threshold, the thermal protection circuit powers off the PMIC to avoid damage. A turn-on event does not power on the PMIC while it is in thermal protection. The part remains in Off mode until the die temperature decreases below a given threshold. See Power dissipation section for more detailed information.

### 6.5.1.5 Standby mode

- Depending on STBY pin configuration, Standby is entered when the STBY pin is asserted. This is typically used for Low-power mode of operation.
- When STBY is de-asserted, Standby mode is exited.

A product may be designed to go into a Low-power mode after periods of inactivity. The STBY pin is provided for board level control of going in and out of such deep sleep modes (DSM). When a product is in DSM, it may be able to reduce the overall platform current by lowering the regulator output voltage, changing the operating mode of the regulators or disabling some regulators. The configuration of the regulators in Standby is pre-programmed through the $I^2C$ interface. Note that the STBY pin is programmable for Active High or Active Low polarity, and decoding of a Standby event takes into account the programmed input polarity as shown in Table 67. When the VR5100 is powered up first, regulator settings for the Standby mode are mirrored from the regulator settings for the ON mode. To change the STBY pin polarity to Active Low, set the STBYINV bit via software first, and then change the regulator settings for Standby mode as required. For simplicity, STBY is generally be referred to as active high throughout this document.

**Table 67. STBY pin and polarity control**

| STBY (pin) [48] | STBYINV ($I^2C$ bit) [49] | STBY control [50] |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Notes

47. STBY = 0: System is not in Standby, STBY = 1: System is in Standby
48. The state of the STBY pin only has influence in On mode.
49. Bit 6 in Power Control Register (ADDR - 0x1B)

Since STBY pin activity is driven asynchronously to the system, a finite time is required for the internal logic to qualify and respond to the pin level changes. A programmable delay is provided to hold off the system response to a Standby event. This allows the processor and peripherals some time after a standby instruction has been received to terminate processes to facilitate seamless entering into Standby mode.

When enabled (STBYDLY = 01, 10, or 11) per Table 68, STBYDLY delays the Standby initiated response for the entire IC, until the STBYDLY counter expires. An allowance should be made for three additional 32 kHz cycles required to synchronize the Standby event.

**Table 68. STBY delay - initiated response**

| STBYDLY[1:0] (50) | Function |
|---|---|
| 00 | No delay |
| 01 | One 32 kHz period (default) |
| 10 | Two 32 kHz periods |
| 11 | Three 32 kHz periods |

Notes
50. Bits [5:4] in power control register (ADDR - 0x1B)

### 6.5.1.6 Sleep/LPSR mode

- Depending on EN pin configuration, Sleep mode is entered when EN is de-asserted and SWxOMODE bit is set.
- To exit Sleep mode, assert the EN pin.

In the Sleep mode, the regulator uses the set point as programmed by SW1OFF[3:0] for SW1 and by SWxOFF[2:0] for SW2 and SW3. The activated regulators maintains settings for this mode and voltage until the next turn-on event. Table 69 shows the control bits in Sleep mode. During Sleep mode, interrupts are active and the INTB pin reports any unmasked fault event. If LPSR is activated by requesting VDD_LPSR and VCC_GPIO to stay ON, LDO1 and LDO3 enables in Low-power mode.

**Table 69. Regulator mode control**

| SWxOMODE | Off operational mode (Sleep) (51) |
|---|---|
| 0 | Off |
| 1 | PFM |

Notes
51. For sleep mode, activated switching regulators, should use the Off mode set point as programmed by SW1OFF[4:0] for SW1 and SW2OFF[2:0] for SW2, and SW3OFF[3:0] for SW3.

### 6.5.1.7 Coin cell mode

In the Coin Cell state, the coin cell is the only valid power source to the PMIC. No turn-on event is accepted in the Coin Cell state. Transition to the OFF state requires $V_{IN}$ surpasses UVDET threshold. PORB is held low in this mode. If the coin cell is depleted, a complete system reset occurs. At the next application of power and the detection of a turn-on event, the system re-initializes with all $I^2C$ bits including, those resetting on COINPORB are restored to their default states.

## 6.5.2 State machine flow summary

Table 70 provides a summary matrix of the VR5100 flow diagram to show the conditions needed to transition from one state to another.

**Table 70. State machine flow summary**

| STATE | | Next state | | | | |
|---|---|---|---|---|---|---|
| | | **OFF** | **Coin cell** | **Sleep** | **Standby** | **ON** |
| **Initial state** | **OFF** | X | $V_{IN}$ < UVDET | X | X | EN_CFG = 0<br>EN = 1 & $V_{IN}$ > UVDET<br>or<br>EN_CFG = 1<br>EN = 0 < 4.0 s<br>& $V_{IN}$ > UNDET |
| | **Coin cell** | $V_{IN}$ > UVDET | | | | |
| | **Sleep/ LPSR** | Thermal Shutdown<br>EN_CFG = 1<br>EN = 0 ≥ 4.0 s<br>Any SWxOMODE = 1 &<br>ENRSTEN = 1 | $V_{IN}$ < UVDET | X<br>LPSR (DO1 & DO3 or V33 Enabled) if LDO1OMODE =1<br>& LDO3OMODE=1 or V33OMODE=1 | X | EN_CFG = 0<br>EN = 1 & $V_{IN}$ > UVDET<br>or<br>EN_CFG = 1<br>EN = 0 < 4.0 s &<br>$V_{IN}$ > UNDET |
| | **Standby** | Thermal Shutdown<br>EN_CFG = 0<br>EN = 0<br>All SWxOMODE = 0<br>or<br>EN_CFG = 1<br>EN = 0 ≥ 4.0 s<br>All SWxOMODE = 0 &<br>ENRSTEN = 1 | $V_{IN}$ < UVDET | EN_CFG = 0<br>EN = 0<br>Any SWxOMODE = 1<br>or<br>EN_CFG = 1<br>EN = 0 ≥ 4.0 s<br>Any SWxOMODE = 1 &<br>ENRSTEN = 1 | X | Standby de-asserted |
| | **ON** | Thermal Shutdown<br>EN_CFG = 0<br>EN = 0<br>All SWxOMODE = 0<br>or<br>EN_CFG = 1<br>EN = 0 ≥ 4.0 s<br>All SWxOMODE = 0 &<br>ENRSTEN = 1 | $V_{IN}$ < UVDET | EN_CFG = 0<br>EN = 0<br>Any SWxOMODE = 1<br>or<br>EN_CFG = 1<br>EN = 0 ≥ 4.0 s<br>Any SWxOMODE = 1 &<br>ENRSTEN = 1 | Standby asserted | X |

## 6.5.3 Performance characteristics curves

($V_{IN}$ = 3.6 V, $SW1_{OUT}$ = 1.0 V; $SW2_{OUT}$ = 1.8 V, $SW3_{OUT}$ = 1.0 V, $SWBST_{OUT}$ = 5.0 V, Switching frequency = 2.0 MHz, Mode = APS; $LDO1_{OUT}$ = 1.8 V, $LDO2_{OUT}$ = 1.0 V, $LDO3_{OUT}$ = 1.8 V, $LDO4_{OUT}$ = 1.8 V, $V33_{OUT}$ = 3.3 V, $VSD_{OUT}$ = 3.3 V, unless otherwise noted)

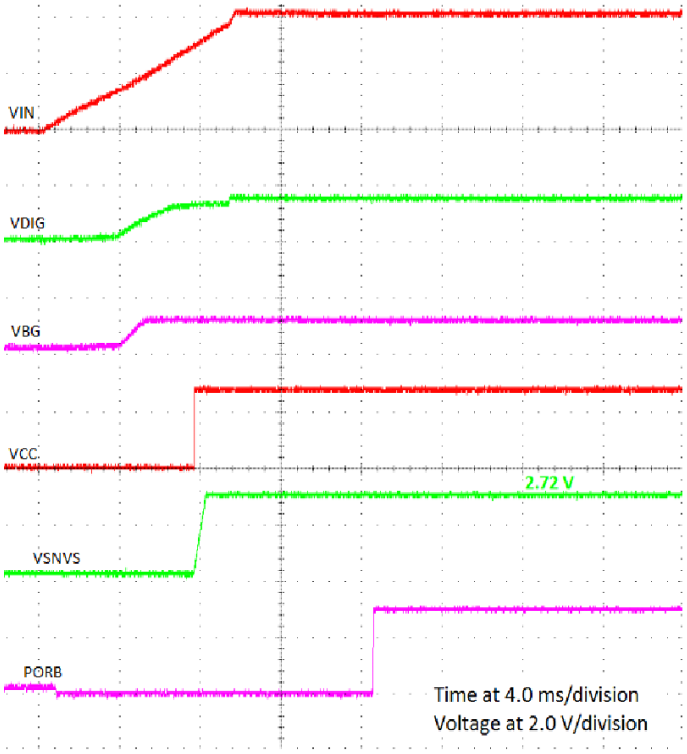



**Figure 13. Typical startup waveforms**

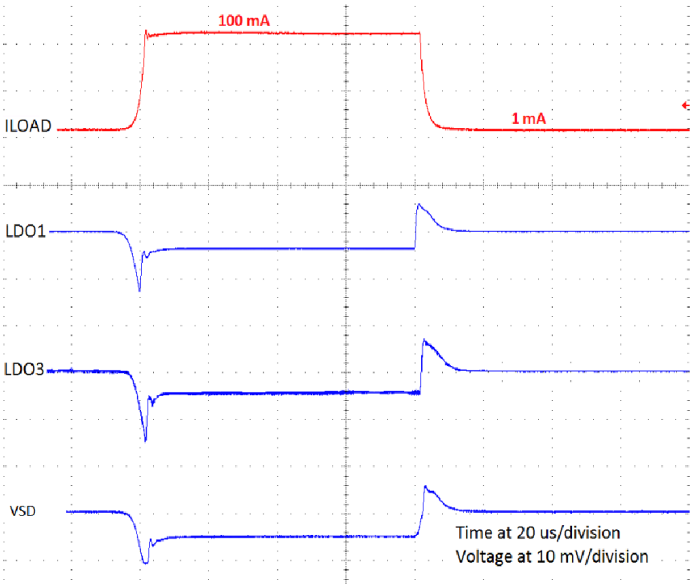



**Figure 14. Load transient response - LDO1, LDO3 and VSD**

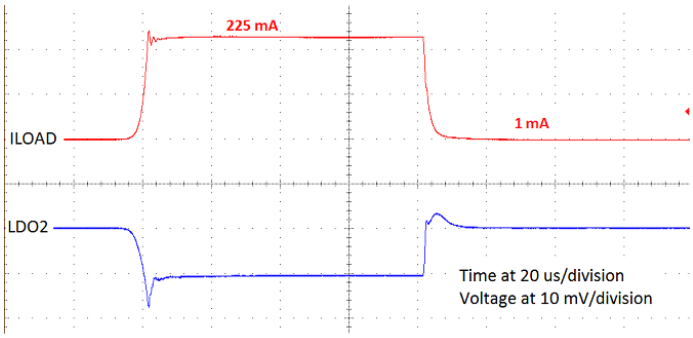



**Figure 15. Load transient response - LDO2**

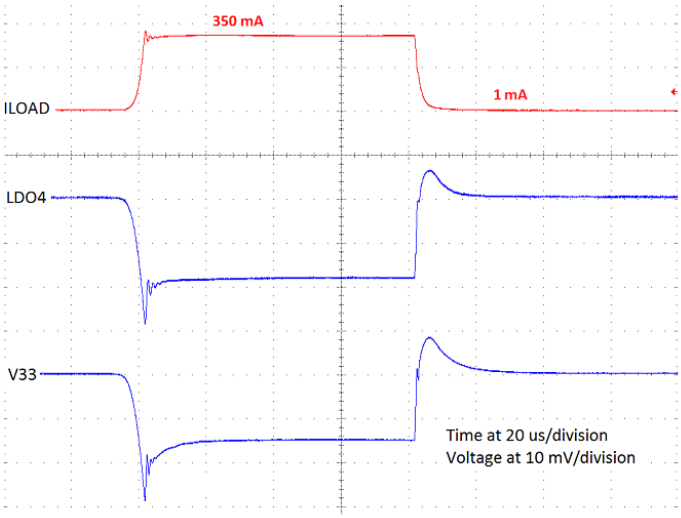



**Figure 16. Load transient response - LDO4 and V33**

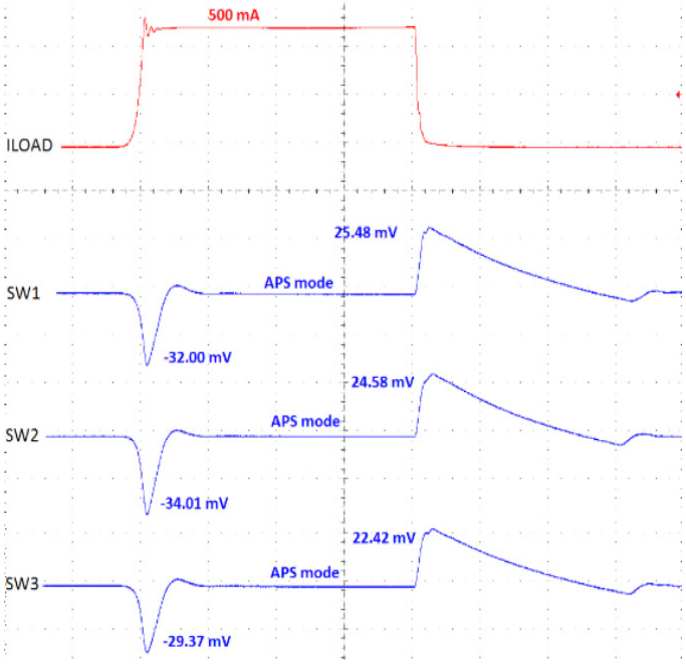



**Figure 17. Load transient response - Buck regulators**

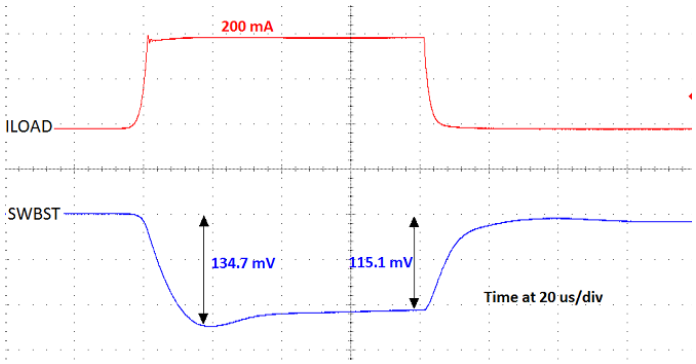



**Figure 18. Load transient response - SWBST**

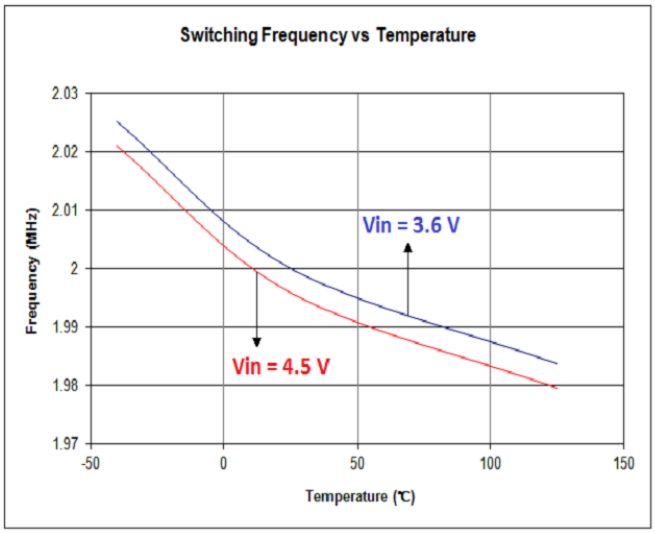



**Figure 19. Switching frequency vs temperature**

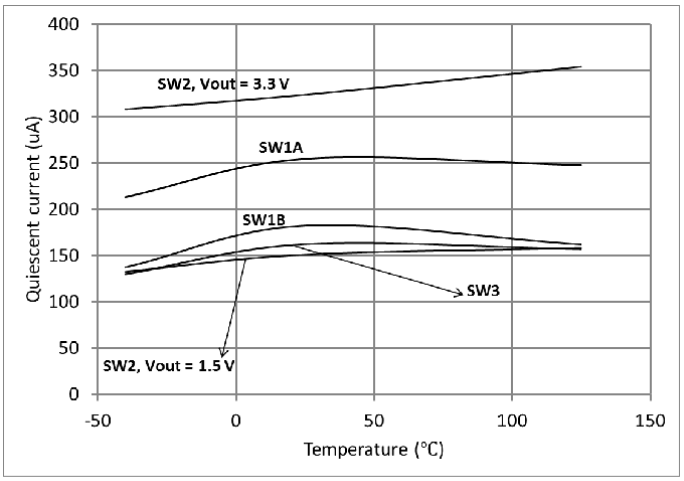



**Figure 20. Quiescent current - Buck regulators in APS mode**

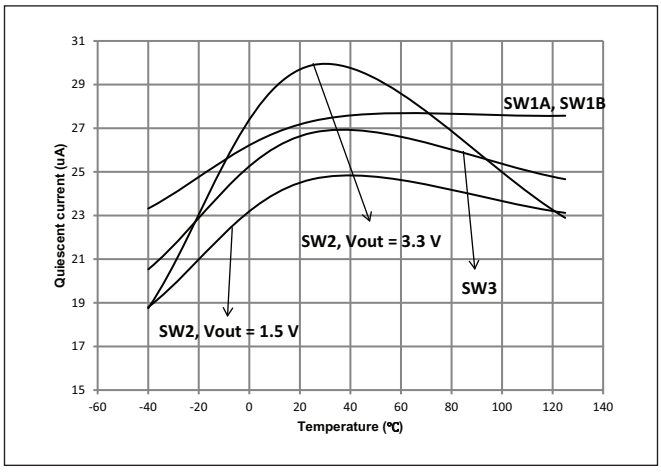



**Figure 21. Quiescent current - Buck regulators in PFM mode**

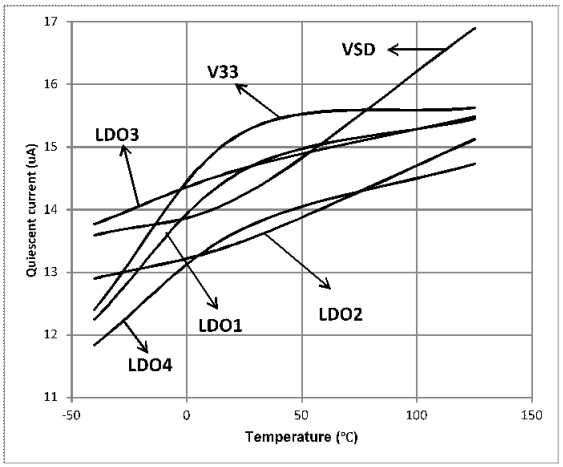



**Figure 22. Quiescent current - LDOs**

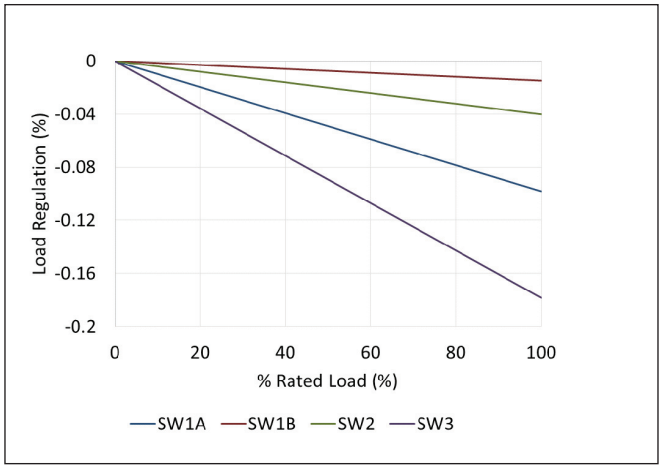



**Figure 23. Load regulation - Buck regulators**

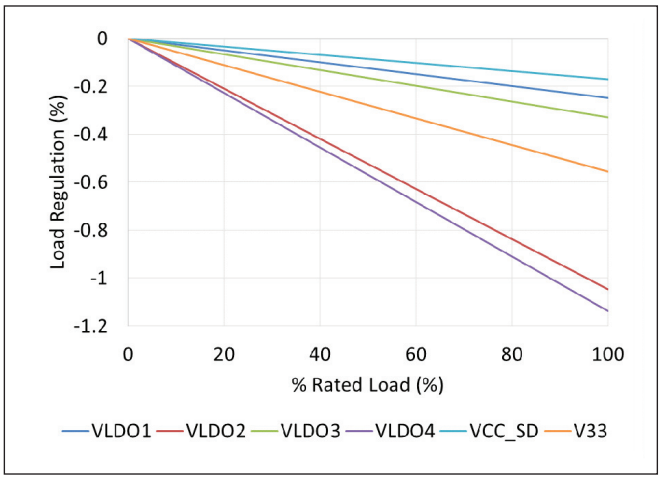



**Figure 24. Load regulation - LDOs**

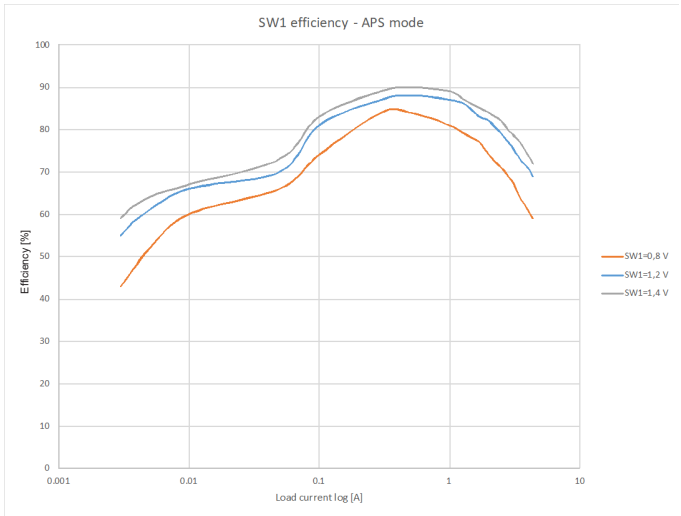



**Figure 25. SW1 efficiency - APS mode**

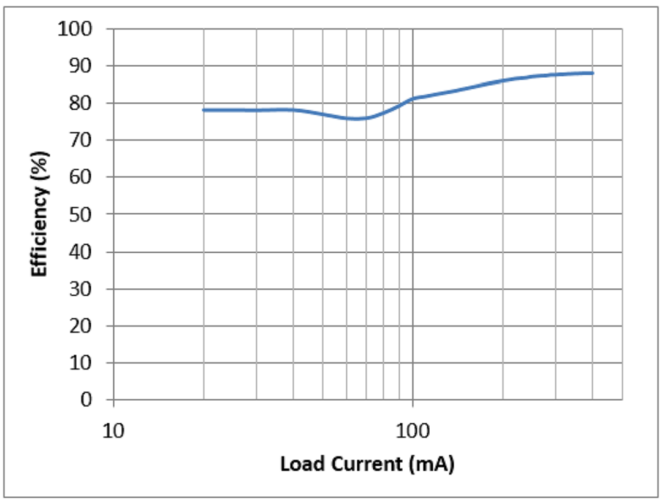



**Figure 26. SW1 efficiency - PFM mode, 0.8 V**

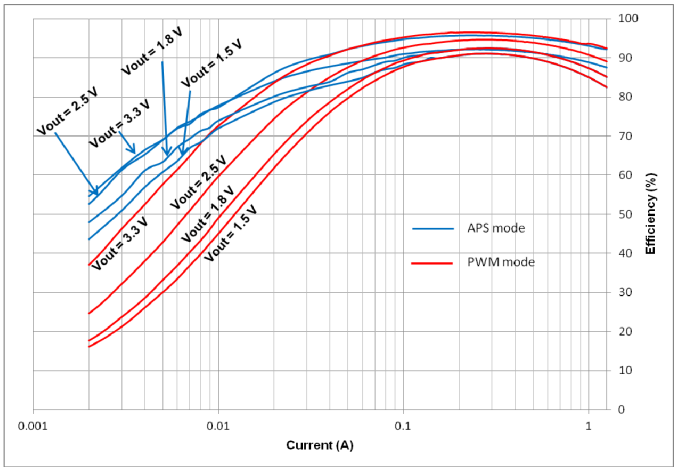



**Figure 27. SW2 efficiency - APS and PWM modes**

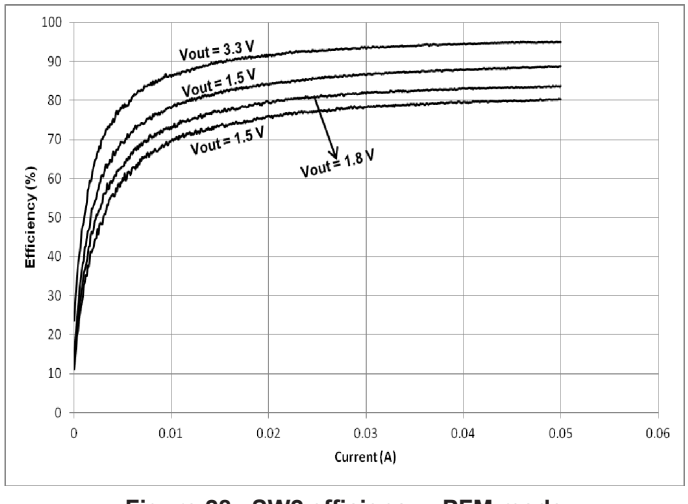



**Figure 28. SW2 efficiency - PFM mode**

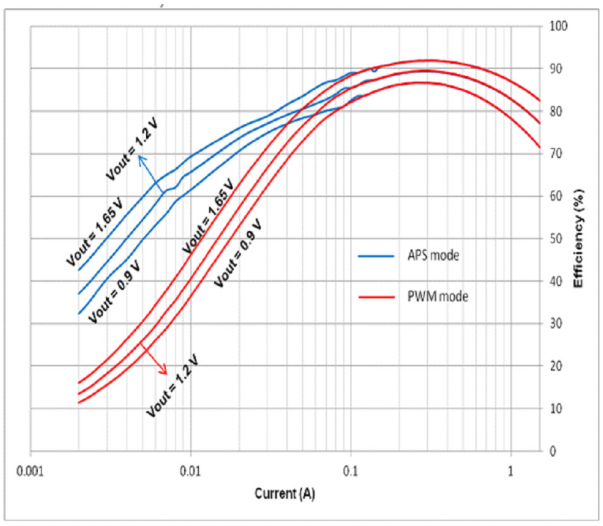



**Figure 29. SW3 efficiency - APS and PWM modes**

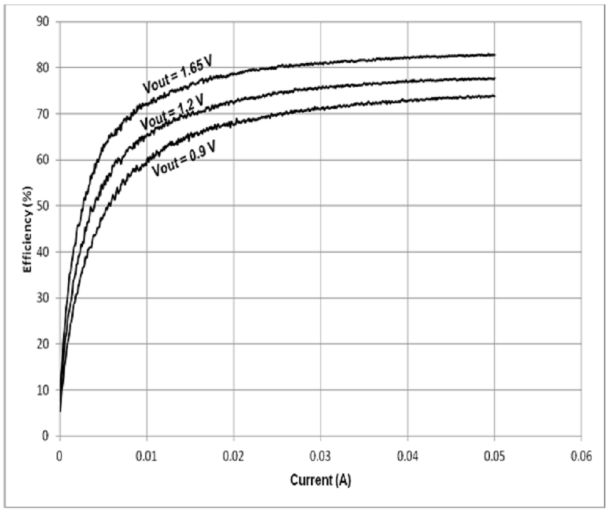



**Figure 30. SW3 efficiency - PFM mode**

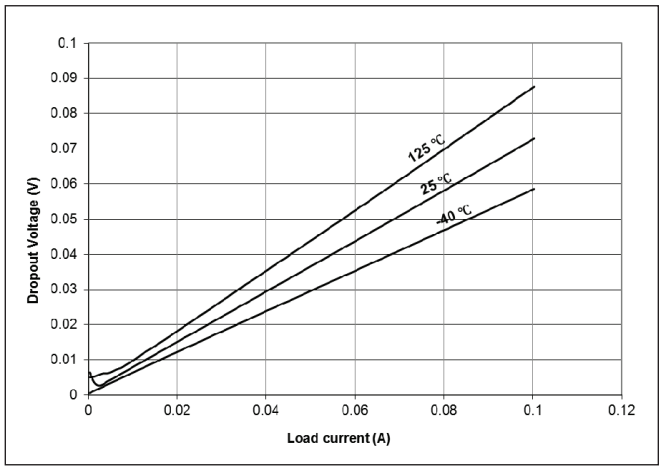



**Figure 31. Dropout voltage - LDO1, LDO3, VSD - $V_{OUT}$ = 3.3 V**

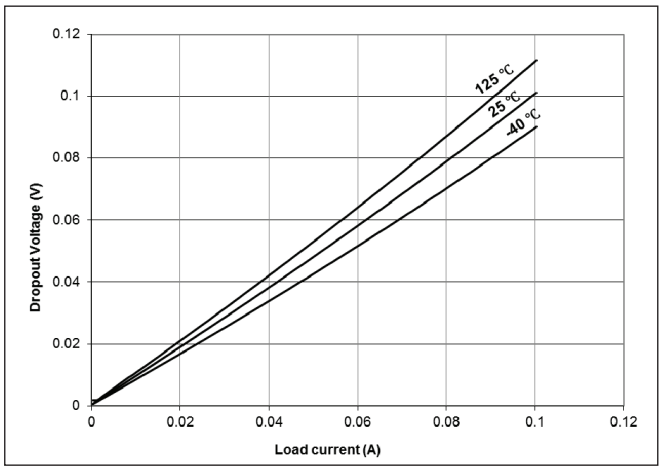



**Figure 32. Dropout voltage - LDO1, LDO3, VSD - $V_{OUT}$ = 1.8 V**

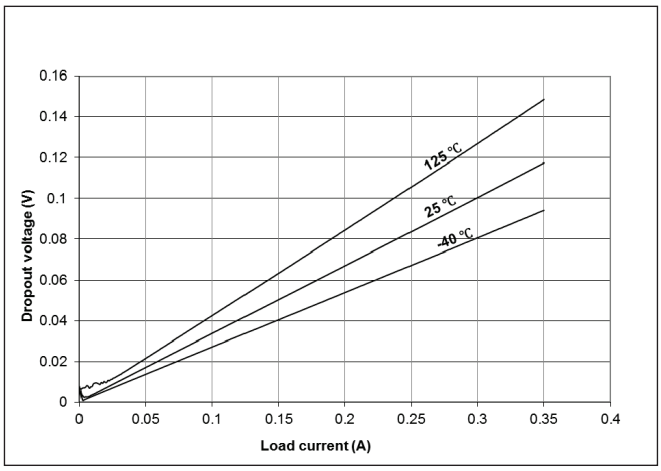



**Figure 33. Dropout voltage - LDO4, V33 - $V_{OUT}$ = 3.3 V**

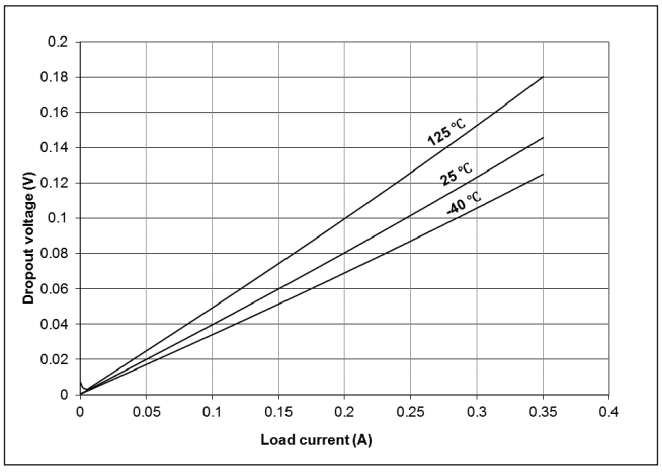



**Figure 34. Dropout voltage - LDO4 - $V_{OUT}$ = 1.8 V**

# 6.6 Control interface I²C block description

The VR5100 contains an I²C interface port which allows access by a processor, or any I²C master, to the register set. Via these registers the resources of the IC can be controlled. The registers also provide status information about how the IC is operating.

The SCL and SDA lines should be routed away from noisy signals and planes to minimize noise pick up. To prevent reflections in the SCL and SDA traces from creating false pulses, the rise and fall times of the SCL and SDA signals must be greater than 20 ns. This can be accomplished by reducing the drive strength of the I²C master via software. It is recommended to use a drive strength of 80 Ω or higher to increase the edge times. Alternatively, this can be accomplished by using small capacitors from SCL and SDA to ground. For example, use 5.1 pF capacitors from SCL and SDA to ground for bus pull-up resistors of 4.8 kΩ.

## 6.6.1 I²C device ID

I²C interface protocol requires a device ID for addressing the target IC on a multi-device bus. The I²C address is set to 0x08.

## 6.6.2 I²C operation

The I²C mode of the interface is implemented generally following the Fast mode definition which supports up to 400 kbits/s operation (exceptions to the standard are noted to be 7-bit only addressing and no support for General Call addressing.)

The I²C interface is configured as “Slave”. Timing diagrams, electrical specifications, and further details can be found in the I²C specification, which is available for download at: http://www.nxp.com/acrobat_download/literature/9398/39340011.pdf

I²C read operations are also performed in byte increments separated by an ACK. Read operations also begin with the MSB and each byte is sent out unless a STOP command or NACK is received prior to completion.

VR5100 only supports single-byte I²C transactions for read and write. The host initiates and terminates all communication. The host sends a master command packet after driving the start condition. The device responds to the host if the master command packet contains the corresponding slave address. In the following examples, the device is shown always responding with an ACK to transmissions from the host. If at any time a NACK is received, the host should terminate the current transaction and retry the transaction.

VR5100 uses the “repeated start” operation for reads as shown in Figure 36.

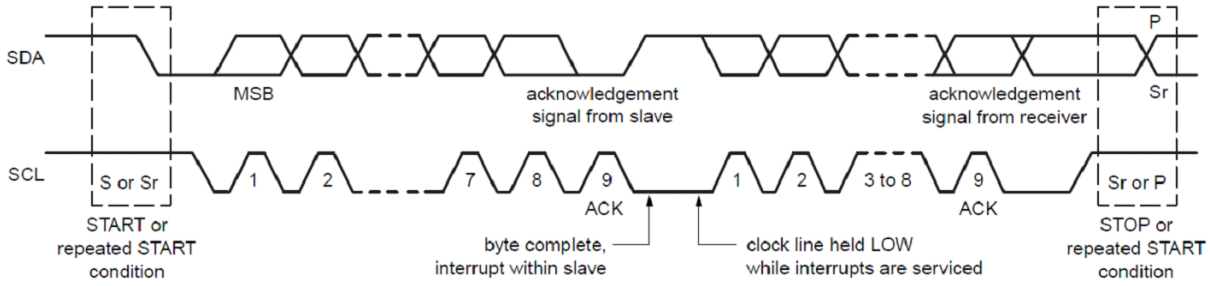



**Figure 35. Data transfer on the I²C bus**

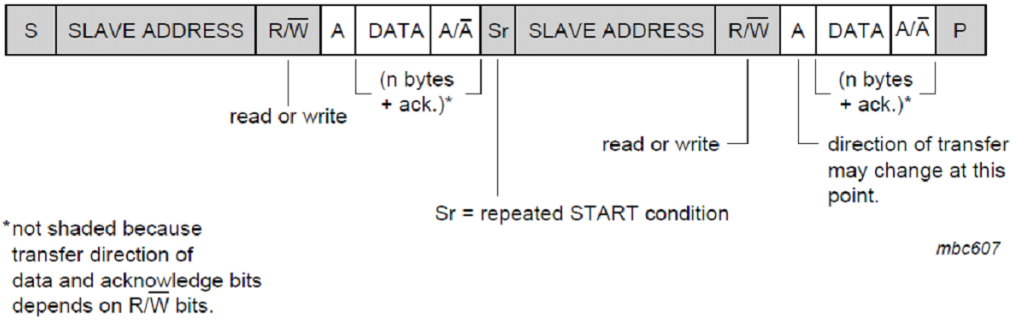



**Figure 36. Read operation**

## 6.6.3 Interrupt handling

The system is informed about important events based on interrupts. Unmasked interrupt events are signaled to the processor by driving the INTB pin low. Each interrupt is latched so even if the interrupt source becomes inactive, the interrupt remains set until cleared. Each interrupt can be cleared by writing a “1” to the appropriate bit in the Interrupt Status register; this causes the INTB pin to go high. If there are multiple interrupt bits set the INTB pin remains low until all are either masked or cleared. If a new interrupt occurs while the processor clears an existing interrupt bit, the INTB pin remains low.

Each interrupt can be masked by setting the corresponding mask bit to a 1. As a result, when a masked interrupt bit goes high, the INTB pin does not go low. A masked interrupt can still be read from the Interrupt Status register. This gives the processor the option of polling for status from the IC. The IC powers up with all interrupts masked, so the processor must initially poll the device to determine if any interrupts are active. Alternatively, the processor can unmask the interrupt bits of interest. If a masked interrupt bit was already high, the INTB pin goes low after unmasking.

The sense registers contain status and input sense bits so the system processor can poll the current state of interrupt sources. They are read only, and not latched or clearable. Interrupts generated by external events are debounced; therefore, the event needs to be stable throughout the debounce period before an interrupt is generated. Nominal debounce periods for each event are documented in the INT summary Table 71. Due to the asynchronous nature of the debounce timer, the effective debounce time can vary slightly.

## 6.6.4 Interrupt bit summary

Table 71 summarizes all interrupt, mask, and sense bits associated with INTB control. For more detailed behavioral descriptions, refer to the related chapters.

**Table 71. Interrupt, mask, and sense bits**

| Interrupt | Mask | Sense | Purpose | Trigger | Debounce time (ms) |
|---|---|---|---|---|---|
| LOWVINI | LOWVINM | LOWVINS | Low input voltage detect<br>Sense is 1 if below 2.70 V threshold | H to L | 3.9 (52) |
| ENI | ENM | ENS | Power on button event | H to L | 31.25 (52) |
| | | | Sense is 1 if EN is high. | L to H | 31.25 |
| THERM110 | THERM110M | THERM110S | Thermal 110 °C threshold<br>Sense is 1 if above threshold | Dual | 3.9 |
| THERM120 | THERM120M | THERM120S | Thermal 120 °C threshold<br>Sense is 1 if above threshold | Dual | 3.9 |
| THERM125 | THERM125M | THERM125S | Thermal 125 °C threshold<br>Sense is 1 if above threshold | Dual | 3.9 |
| THERM130 | THERM130M | THERM130S | Thermal 130 °C threshold<br>Sense is 1 if above threshold | Dual | 3.9 |
| SW1FAULTI | SW1FAULTM | SW1FAULTS | Regulator 1 overcurrent limit<br>Sense is 1 if above current limit | L to H | 8.0 |
| SW2FAULTI | SW2FAULTM | SW2FAULTS | Regulator 2 overcurrent limit<br>Sense is 1 if above current limit | L to H | 8.0 |
| SW3FAULTI | SW3FAULTM | SW3FAULTS | Regulator 3 overcurrent limit<br>Sense is 1 if above current limit | L to H | 8.0 |
| SWBSTFAULTI | SWBSTFAULTM | SWBSTFAULTS | SWBST overcurrent limit<br>Sense is 1 if above current limit | L to H | 8.0 |
| LDO1FAULTI | LDO1FAULTM | LDO1FAULTS | LDO1 overcurrent limit<br>Sense is 1 if above current limit | L to H | 8.0 |
| LDO2FAULTI | LDO2FAULTM | LDO2FAULTS | LDO2 overcurrent limit<br>Sense is 1 if above current limit | L to H | 8.0 |
| VSDFAULTI | VSDFAULTM | VSDFAULTS | VSD overcurrent limit<br>Sense is 1 if above current limit | L to H | 8.0 |
| V33FAULTI | V33FAULTM | V33FAULTS | V33 overcurrent limit<br>Sense is 1 if above current limit | L to H | 8.0 |
| LDO3FAULTI | LDO3FAULTM | LDO1FAULTS | LDO3 overcurrent limit<br>Sense is 1 if above current limit | L to H | 8.0 |

**Table 71. Interrupt, mask, and sense bits (continued)**

| Interrupt | Mask | Sense | Purpose | Trigger | Debounce time (ms) |
|---|---|---|---|---|---|
| LDO4FAULTI | LDO4FAULTM | LDO4FAULTS | LDO4 overcurrent limit<br>Sense is 1 if above current limit | L to H | 8.0 |
| OTP_ECCI | OTP_ECCM | OTP_ECCS | 1 or 2 bit error detected in OTP registers<br>Sense is 1 if error detected | L to H | - |
| OTP_AUTO_BLOW | OTP_AUTO_BLOWM | OTP_AUTO_BLOWS | Interrupt to indicate completion of fuse auto blow | L to H | - |

Notes
52. Debounce timing for the falling edge can be extended with ENDBNC[1:0].

A full description of all interrupt, mask, and sense registers is provided in Table 72 to Table 83.

**Table 72. Register INTSTAT0 - ADDR 0x05**

| Name | Bit # | R/W | Default | Description |
|---|---|---|---|---|
| ENI | 0 | R/W1C | 0 | Power on interrupt bit |
| LOWVINI | 1 | R/W1C | 0 | Low-voltage interrupt bit |
| THERM110I | 2 | R/W1C | 0 | 110 °C thermal interrupt bit |
| THERM120I | 3 | R/W1C | 0 | 120 °C thermal interrupt bit |
| THERM125I | 4 | R/W1C | 0 | 125 °C thermal interrupt bit |
| THERM130I | 5 | R/W1C | 0 | 130 °C thermal interrupt bit |
| Unused | 7:6 | – | 0b00 | Unused |

**Table 73. Register INTMASK0 - ADDR 0x06**

| Name | Bit # | R/W | Default | Description |
|---|---|---|---|---|
| ENM | 0 | R/W1C | 1 | Power on interrupt mask bit |
| LOWVINM | 1 | R/W1C | 1 | Low-voltage interrupt mask bit |
| THERM110M | 2 | R/W1C | 1 | 110 °C thermal interrupt mask bit |
| THERM120M | 3 | R/W1C | 1 | 120 °C thermal interrupt mask bit |
| THERM125M | 4 | R/W1C | 1 | 125 °C thermal interrupt mask bit |
| THERM130M | 5 | R/W1C | 1 | 130 °C thermal interrupt mask bit |
| Unused | 7:6 | – | 0b00 | Unused |

**Table 74. Register INTSENSE0 - ADDR 0x07**

| Name | Bit # | R/W | Default | Description |
|---|---|---|---|---|
| ENS | 0 | R | 0 | Power on sense bit<br>0 = EN low<br>1 = EN high |
| LOWVINS | 1 | R | 0 | Low voltage sense bit<br>0 = VIN > 2.7 V<br>1 = VIN ≤ 2.7 V |
| THERM110S | 2 | R | 0 | 110 °C Thermal sense bit<br>0 = Below threshold<br>1 = Above threshold |
| THERM120S | 3 | R | 0 | 120 °C Thermal sense bit<br>0 = Below threshold<br>1 = Above threshold |

**Table 74. Register INTSENSE0 - ADDR 0x07 (continued)**

| Name | Bit # | R/W | Default | Description |
|---|---|---|---|---|
| THERM125S | 4 | R | 0 | 125 °C thermal sense bit<br>0 = Below threshold<br>1 = Above threshold |
| THERM130S | 5 | R | 0 | 130 °C thermal sense bit<br>0 = Below threshold<br>1 = Above threshold |
| ICTESTS | 6 | R | 0 | 0 = ICTEST pin is grounded<br>1 = ICTEST to VDIG or greater |
| VDDOTPS | 7 | R | 0 | Additional VDDOTP voltage sense pin<br>0 = VDDOTP grounded<br>1 = VDDOTP to VDIG or greater |

**Table 75. Register INTSTAT1 - ADDR 0x08**

| Name | Bit # | R/W | Default | Description |
|---|---|---|---|---|
| SW1FAULTI | 0 | R/W1C | 0 | SW1 overcurrent interrupt bit |
| SW1FAULTI | 1 | R/W1C | 0 | SW1 overcurrent interrupt bit |
| Unused | 2 | R/W1C | 0 | Unused |
| SW2FAULTI | 3 | R/W1C | 0 | SW2 overcurrent interrupt bit |
| SW3FAULTI | 4 | R/W1C | 0 | SW3 overcurrent interrupt bit |
| Unused | 5 | R/W1C | 0 | Unused |
| Unused | 6 | R/W1C | 0 | Unused |
| Unused | 7 | – | 0 | Unused |

**Table 76. Register INTMASK1 - ADDR 0x09**

| Name | Bit # | R/W | Default | Description |
|---|---|---|---|---|
| SW1FAULTM | 0 | R/W | 1 | SW1 overcurrent interrupt mask bit |
| SW1FAULTM | 1 | R/W | 1 | SW1 overcurrent interrupt mask bit |
| Unused | 2 | R/W | 1 | Unused |
| SW2FAULTM | 3 | R/W | 1 | SW2 overcurrent interrupt mask bit |
| SW3FAULTM | 4 | R/W | 1 | SW3 overcurrent interrupt mask bit |
| Unused | 5 | R/W | 1 | Unused |
| Unused | 6 | R/W | 1 | Unused |
| Unused | 7 | – | 0 | Unused |

**Table 77. Register INTSENSE1 - ADDR 0x0A**

| Name | Bit # | R/W | Default | Description |
|---|---|---|---|---|
| SW1FAULTS | 0 | R | 0 | SW1 overcurrent sense bit<br>0 = Normal operation<br>1 = Above current limit |
| Unused | 1 | R | 0 | Unused |
| SW1FAULTS | 2 | R | 0 | SW1 overcurrent sense bit<br>0 = Normal operation<br>1 = Above current limit |

**Table 77. Register INTSENSE1 - ADDR 0x0A (continued)**

| Name | Bit # | R/W | Default | Description |
|---|---|---|---|---|
| SW2FAULTS | 3 | R | 0 | SW2 overcurrent sense bit<br>0 = Normal operation<br>1 = Above current limit |
| SW3FAULTS | 4 | R | 0 | SW3 overcurrent sense bit<br>0 = Normal operation<br>1 = Above current limit |
| Unused | 5 | R | 0 | Unused |
| Unused | 6 | R | 0 | Unused |
| Unused | 7 | – | 0 | Unused |

**Table 78. Register INTSTAT3 - ADDR 0x0E**

| Name | Bit # | R/W | Default | Description |
|---|---|---|---|---|
| SWBSTFAULTI | 0 | R/W1C | 0 | SWBST overcurrent limit interrupt bit |
| Unused | 1 | – | 0b0 | Unused |
| Unused | 2 | - | 0b0 | Unused |
| Unused | 5:3 | – | 0b0 | Unused |
| OTP AUTO BLOW | 6 | R/W1C | 0b0 | High after Auto Fuse Blow Sequence is completed |
| OTP_ECCI | 7 | R/W1C | 0 | OTP error interrupt bit |

**Table 79. Register INTMASK3 - ADDR 0x0F**

| Name | Bit # | R/W | Default | Description |
|---|---|---|---|---|
| SWBSTFAULTM | 0 | R/W | 1 | SWBST overcurrent limit interrupt mask bit |
| Unused | 1 | – | 0 | Unused |
| Unused | 2 | - | 1 | Unused |
| Unused | 5:3 | – | 0b000 | Unused |
| OTP_AUTO_BLOW_DONE_M | 6 | R/W | 1 | OTP auto blow mask bit |
| OTP_ECCM | 7 | R/W | 1 | OTP error interrupt mask bit |

**Table 80. Register INTSENSE3 - ADDR 0x10**

| Name | Bit # | R/W | Default | Description |
|---|---|---|---|---|
| SWBSTFAULTS | 0 | R | 0 | SWBST overcurrent limit sense bit<br>0 = Normal operation<br>1 = Above current limit |
| Unused | 1 | – | 0b0 | Unused |
| Unused | 2 | - | 0 | Unused |
| Unused | 5:3 | – | 0b000 | Unused |
| OTP_AUTO_BLOW_DONE_S | 6 | R | 0 | OTP auto blow sense bit. This bit is high while the auto blow sequence is running. Do not read/write the OTP TBB registers while this bit is 1. |
| OTP_ECCS | 7 | R | 0 | OTP error sense bit<br>0 = No error detected<br>1 = OTP error detected |

**Table 81. Register INTSTAT4 - ADDR 0x11**

| Name | Bit # | R/W | Default | Description |
|---|---|---|---|---|
| LDO1FAULTI | 0 | R/W1C | 0 | LDO1 overcurrent interrupt bit |
| LDO2FAULTI | 1 | R/W1C | 0 | LDO2 overcurrent interrupt bit |
| VSDFAULTI | 2 | R/W1C | 0 | VSD overcurrent interrupt bit |
| V33FAULTI | 3 | R/W1C | 0 | V33 overcurrent interrupt bit |
| LDO3FAULTI | 4 | R/W1C | 0 | LDO3 overcurrent interrupt bit |
| LDO4FAULTI | 5 | R/W1C | 0 | LDO4 overcurrent interrupt bit |
| Unused | 7:6 | – | 0b00 | Unused |

**Table 82. Register INTMASK4 - ADDR 0x12**

| Name | Bit # | R/W | Default | Description |
|---|---|---|---|---|
| LDO1FAULTM | 0 | R/W | 1 | LDO1 overcurrent interrupt mask bit |
| LDO2FAULTM | 1 | R/W | 1 | LDO2 overcurrent interrupt mask bit |
| VSDFAULTM | 2 | R/W | 1 | VSD overcurrent interrupt mask bit |
| V33FAULTM | 3 | R/W | 1 | V33 overcurrent interrupt mask bit |
| LDO3FAULTM | 4 | R/W | 1 | LDO3 overcurrent interrupt mask bit |
| LDO4FAULTM | 5 | R/W | 1 | LDO4 overcurrent interrupt mask bit |
| Unused | 7:6 | – | 0b00 | Unused |

**Table 83. Register INTSENSE4 - ADDR 0x13**

| Name | Bit # | R/W | Default | Description |
|---|---|---|---|---|
| LDO1FAULTS | 0 | R | 0 | LDO1 overcurrent sense bit<br>0 = Normal operation<br>1 = Above current limit |
| LDO2FAULTS | 1 | R | 0 | LDO2 overcurrent sense bit<br>0 = Normal operation<br>1 = Above current limit |
| VSDFAULTS | 2 | R | 0 | VSD overcurrent sense bit<br>0 = Normal operation<br>1 = Above current limit |
| V33FAULTS | 3 | R | 0 | V33 overcurrent sense bit<br>0 = Normal operation<br>1 = Above current limit |
| LDO3FAULTS | 4 | R | 0 | LDO3 overcurrent sense bit<br>0 = Normal operation<br>1 = Above current limit |
| LDO4FAULTS | 5 | R | 0 | LDO4 overcurrent sense bit<br>0 = Normal operation<br>1 = Above current limit |
| Unused | 7:6 | – | 0b00 | Unused |

## 6.6.5 Specific registers

### 6.6.5.1 IC and version identification

The IC and other version details can be read via identification bits. These are hard-wired on the chip and described in Table 84 to Table 86.

**Table 84. Register DEVICEID - ADDR 0x00**

| Name | Bit # | R/W | Default | Description |
|---|---|---|---|---|
| DEVICEID | 3:0 | R | 0x0 | 0000 = VR5100 |
| FAMILY | 7:4 | R | 0x3 | 0011 = VR5100 |

**Table 85. Register SILICON REV- ADDR 0x03**

| Name | Bit # | R/W | Default | Description |
|---|---|---|---|---|
| METAL_LAYER_REV | 3:0 | R | 0x0 | Represents the metal mask revision<br>Pass 0.0 = 0000<br>…<br>Pass 0.15 = 1111 |
| FULL_LAYER_REV | 7:4 | R | 0x1 | Represents the full mask revision<br>Pass 1.0 = 0001<br>…<br>Pass 15.0 = 1111 |

**Table 86. Register FABID - ADDR 0x04**

| Name | Bit # | R/W | Default | Description |
|---|---|---|---|---|
| FIN | 1:0 | R | 0b00 | Allows for characterizing different options within the same reticule |
| FAB | 3:2 | R | 0b00 | Represents the wafer manufacturing facility |
| Unused | 7:4 | R | 0b0000 | Unused |

### 6.6.5.2 Embedded Memory

There are four register banks of general purpose embedded memory to store critical data. The data written to MEMA[7:0], MEMB[7:0], MEMC[7:0], and MEMD[7:0] is maintained by the coin cell when the main battery is deeply discharged, removed, or contact-bounced. The contents of the embedded memory are reset by COINPORB. The banks can be used for any system need for bit retention with coin cell backup.

**Table 87. Register MEMA ADDR 0x1C**

| Name | Bit # | R/W | Default | Description |
|---|---|---|---|---|
| MEMA | 7:0 | R/W | 0x00 | Memory bank A |

**Table 88. Register MEMB ADDR 0x1D**

| Name | Bit # | R/W | Default | Description |
|---|---|---|---|---|
| MEMB | 7:0 | R/W | 0x00 | Memory bank B |

**Table 89. Register MEMC ADDR 0x1E**

| Name | Bit # | R/W | Default | Description |
|---|---|---|---|---|
| MEMC | 7:0 | R/W | 0x00 | Memory bank C |

**Table 90. Register MEMD ADDR 0x1F**

| Name | Bit # | R/W | Default | Description |
|---|---|---|---|---|
| MEMD | 7:0 | R/W | 0x00 | Memory bank D |

## 6.6.5.3 Register descriptions

This section describes all the VR5100 registers and their individual bits. Address order is as listed in Register map, page 92.

### 6.6.5.3.1 Interrupt status register 0 (INTSTAT0)

INSTAT0 is one of the four status interrupt registers. This register contains six status flags. Write a logic 1 to clear a flag.

**Table 91. Status interrupt register 0 (INTSTAT0)**

**Address: 0x05 functional page** **Access: user read/write (53)**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | | | THERM130I | THERM125I | THERM120I | THERM110I | LOWVINI | ENNI |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or reserved

Notes
53. Read: Anytime
Write: Anytime

**Table 92. INTSTAT0 Field descriptions**

| Field | Description |
|---|---|
| 5<br>THERM130I | **130 °C Thermal interrupt bit** — THERM130I is set to 1 when the THERM130 threshold specified in is crossed in either direction (bi-directional). This flag can only be cleared by writing a 1. Writing a 0 has no effect.<br>0 Die temperature has not crossed THERM130 threshold.<br>1 Die temperature has crossed THERM130 threshold. |
| 4<br>THERM125I | **125 °C Thermal interrupt bit** — THERM125I is set to 1 when the THERM125 threshold specified in is crossed in either direction (bi-directional). This flag can only be cleared by writing a 1. Writing a 0 has no effect.<br>0 Die temperature has not crossed THERM125 threshold.<br>1 Die temperature has crossed THERM125 threshold. |
| 3<br>THERM120I | **120 °C Thermal interrupt bit** — THERM120I is set to 1 when the THERM120 threshold specified in is crossed in either direction (bi-directional). This flag can only be cleared by writing a 1. Writing a 0 has no effect.<br>0 Die temperature has not crossed THERM120 threshold.<br>1 Die temperature has crossed THERM120 threshold. |
| 2<br>THERM110I | **110 °C Thermal interrupt bit** — THERM110I is set to 1 when the THERM110 threshold specified in<br>is crossed in either direction (bi-directional). This flag can only be cleared by writing a 1. Writing a 0 has no effect.<br>0 Die temperature has not crossed THERM110 threshold.<br>1 Die temperature has crossed THERM110 threshold. |
| 1<br>LOWVINI | **Low-voltage interrupt bit** — LOWVINI is set to 1 when a low-voltage event occurs on VIN. This flag can only be cleared by writing a 1. Writing a 0 has no effect.<br>0 $V_{IN}$ > 2.7 V (typical)<br>1 $V_{IN}$ < 2.7 V (typical) |
| 0<br>ENI | **Power on interrupt bit** —ENI is set to 1 when the turn on event occurs. This flag can only be cleared by writing a 1. Writing a 0 has no effect.<br>0 Power on has not occurred.<br>1 Power on has occurred. |

### 6.6.5.3.2 Interrupt status mask register 0 (INTMASK0)

INTMASK0 is the mask register for the status interrupt register INTSTAT0. Write a logic 0 to a bit to unmask the corresponding interrupt. When unmasked, the corresponding interrupt state is reflected on the INTB pin.

**Table 93. Interrupt status mask register 0 (INTMASK0)**

**Address: 0x06 functional page** **Access: user read/write (54)**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | | | THERM130M | THERM125M | THERM120M | THERM110M | LOWVINM | ENM |
| Default | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

= Unimplemented or reserved

Notes

54. Read: Anytime
Write: Anytime

**Table 94. INTMASK0 field descriptions**

| Field | Description |
|---|---|
| 5<br>THERM130M | 130 °C thermal interrupt mask bit<br>0 THERM130I unmasked<br>1 THERM130I masked |
| 4<br>THERM125M | 125 °C thermal interrupt mask bit<br>0 THERM125I unmasked<br>1 THERM125I masked |
| 3<br>THERM120M | 120 °C thermal interrupt mask bit<br>0 THERM120I unmasked<br>1 THERM120I masked |
| 2<br>THERM110M | 110 °C thermal interrupt mask bit<br>0 THERM110I unmasked<br>1 THERM110I masked |
| 1<br>LOWVINM | Low-voltage interrupt mask bit<br>0 LOWVINI unmasked<br>1 LOWVINI masked |
| 0<br>ENM | Power on interrupt mask bit<br>0 ENI unmasked<br>1 ENI masked |

### 6.6.5.3.3 Interrupt sense register 0 (INTSENSE0)

This register has seven read-only sense bits. These sense bits reflects the actual state of the corresponding function.

**Table 95. Interrupt sense register 0 (INTSENSE0)**

**Address: 0x07 functional page** **Access: user read-only [55]**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | VDDOTPS | | THERM130S | THERM125S | THERM120S | THERM110S | LOWVINS | ENS |
| W | | | | | | | | |
| Default | X [59] | 0 | X [58] | X [58] | X [58] | X [58] | X [57] | X [56] |

= Unimplemented or reserved

Notes
55. Read: Anytime
56. Default value depends on the initial EN pin state.
57. Default value depends on the initial VIN voltage.
58. Default value depends on the initial temperature of the die.
59. Default value depends on the initial VDDOTP pin state.

**Table 96. INTSENSE0 field descriptions**

| Field | Description |
|---|---|
| 7<br>VDDOTPS | **VDDOTP voltage sense bit**<br>0 VDDOTP grounded.<br>1 VDDOTP to VDIG or greater. |
| 5<br>THERM130S | **130 °C thermal interrupt sense bit**<br>0 Die temperature below THERM130 threshold.<br>1 Die temperature above THERM130 threshold. |
| 4<br>THERM125S | 125 °C thermal interrupt sense bit<br>0 Die temperature below THERM125 threshold.<br>1 Die temperature has crossed THERM125 threshold. |
| 3<br>THERM120S | 120 °C thermal interrupt sense bit<br>0 Die temperature below THERM120 threshold.<br>1 Die temperature has crossed THERM120 threshold. |
| 2<br>THERM110S | 110 °C thermal interrupt sense bit<br>0 Die temperature below THERM110 threshold.<br>1 Die temperature has crossed THERM110 threshold. |
| 1<br>LOWVINS | Low-voltage interrupt sense bit<br>0 $V_{IN}$ > 2.7 V (typical)<br>1 $V_{IN}$ < 2.7 V (typical) |
| 0<br>ENS | Power on interrupt sense bit<br>0 EN low.<br>1 EN high. |

### 6.6.5.3.4 Interrupt status register 1 (INTSTAT1)

INSTAT1 is one of the four status interrupt registers. This register contains four status flags. Write a logic 1 to clear a flag.

**Table 97. Status interrupt register 1 (INTSTAT1)**

| | Address: 0x08 functional page | | | | | | Access: user read/write (60) | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R<br>W | | | | SW3FAULTI | SW2FAULTI | | SW1FAULTI | SW1FAULTI |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or reserved

Notes
60. Read: Anytime
Write: Anytime

**Table 98. INTSTAT1 field descriptions**

| Field | Description |
|---|---|
| 4<br>SW3FAULTI | **SW3 overcurrent interrupt bit** — SW3FAULTI is set to 1 when the SW3 regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect.<br>0 SW3 in normal operation<br>1 SW3 above current limit |
| 3<br>SW2FAULTI | **SW2 overcurrent interrupt bit** — SW2FAULTI is set to 1 when the SW2 regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect.<br>0 SW2 in normal operation<br>1 SW2 above current limit |
| 1<br>SW1FAULTI | **SW1 overcurrent interrupt bit** — SW1FAULTI is set to 1 when the SW1 regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect.<br>0 SW1 in normal operation<br>1 SW1 above current limit |
| 0<br>SW1FAULTI | **SW1 overcurrent interrupt bit** — SW1FAULTI is set to 1 when the SW1 regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect.<br>0 SW1 in normal operation<br>1 SW1 above current limit |

### 6.6.5.3.5 Interrupt status mask register 1 (INTMASK1)

INTMASK1 is the mask register for the status interrupt register INTSTAT1. Write a logic 0 to a bit to unmask the corresponding interrupt. When unmasked, the corresponding interrupt state is reflected on the INTB pin.

**Table 99. Interrupt status mask register 1 (INTMASK1)**

| | Address: 0x09 functional page | | | | | | Access: user read/write (61) | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R<br>W | | | | SW3FAULTM | SW2FAULTM | | SW1FAULTM | SW1FAULTM |
| Default | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |

= Unimplemented or reserved

Notes
61. Read: Anytime
Write: Anytime

**Table 100. INTMASK1 field descriptions**

| Field | Description |
|---|---|
| 4<br>SW3FAULTM | SW3 overcurrent interrupt mask bit<br>0 SW3FAULTI Unmasked<br>1 SW3FAULTI Masked |
| 3<br>SW2FAULTM | SW2 overcurrent interrupt mask bit<br>0 SW2FAULTI Unmasked<br>1 SW2FAULTI Masked |
| 1<br>SW1FAULTM | SW1 overcurrent interrupt mask bit<br>0 SW1FAULTI Unmasked<br>1 SW1FAULTI Masked |
| 0<br>SW1FAULTM | SW1 overcurrent interrupt mask bit<br>0 SW1FAULTI Unmasked<br>1 SW1FAULTI Masked |

### 6.6.5.3.6 Interrupt sense register 1 (INTSENSE1)

This register has four read-only sense bits. These sense bits reflect the actual state of the corresponding function.

**Table 101. Interrupt sense register 1 (INTSENSE1)**

**Address: 0x0A functional page** — **Access: user read-only (62)**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | | | | SW3FAULTS | SW2FAULTS | | SW1FAULTS | SW1FAULTS |
| W | | | | | | | | |
| Default | 0 | 0 | 0 | X (63) | X (63) | 0 | X (63) | X (63) |

= Unimplemented or reserved

Notes
62. Read: Anytime
63. Default value depends on the regulator initial state

**Table 102. INTSENSE1 field descriptions**

| Field | Description |
|---|---|
| 4<br>SW3FAULTS | SW3 overcurrent sense bit<br>0 SW3 in normal operation<br>1 SW3 above current limit |
| 3<br>SW2FAULTS | SW2 overcurrent sense bit<br>0 SW2 in normal operation<br>1 SW2 above current limit |
| 1<br>SW1FAULTS | SW1 overcurrent sense bit<br>0 SW1 in normal operation<br>1 SW1 above current limit |
| 0<br>SW1FAULTS | SW1 overcurrent sense bit<br>0 SW1 in normal operation<br>1 SW1 above current limit |

### 6.6.5.3.7 Interrupt status register 3 (INTSTAT3)

INSTAT3 is one of the four status interrupt registers. This register contains four status flags. Write a logic 1 to clear a flag.

**Table 103. Status interrupt register 3 (INTSTAT3)**

| Address: 0x0E functional page | | | | | | | Access: user read/write (64) |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R<br>W | OTP_ECCI | OTP_AUTO_BLOW_DONEI | | | | | SWBSTFAULTI |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or reserved

Notes
64. Read: Anytime
Write: Anytime

**Table 104. INTSTAT3 field descriptions**

| Field | Description |
|---|---|
| 7<br>OTP_ECCI | **OTP error interrupt bit** — OTP_ECCI is set to 1 when an error is detected in OTP registers. This flag can only be cleared by writing a 1. Writing a 0 has no effect.<br>0 No error detected<br>1 OTP error detected |
| 6<br>OTP_AUTO_BLOW_DONEI | **OTP auto fuse blow interrupt bit** — OTP_AUTO_BLOW_DONEI is set to 1 after the Auto Fuse Blow Sequence is completed. This flag can only be cleared by writing a 1. Writing a 0 has no effect.<br>0 OTP Auto Fuse Blow Sequence not completed<br>1 OTP Auto Fuse Blow Sequence completed |
| 0<br>SWBSTFAULTI | **SWBST overcurrent limit interrupt bit** — SWBSTFAULTI is set to 1 when the SWBST regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect.<br>0 SWBST in normal operation<br>1 SWBST above current limit |

### 6.6.5.3.8 Interrupt status mask register 3 (INTMASK3)

INTMASK3 is the mask register for the status interrupt register INTSTAT3. Write a logic 0 to a bit to unmask the corresponding interrupt. When unmasked, the corresponding interrupt state is reflected on the INTB pin.

**Table 105. Interrupt status mask register 3 (INTMASK3)**

| Address: 0x0F functional page | | | | | | | Access: user read/write (65) |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R<br>W | OTP_ECCM | OTP_AUTO_BLOW_DONEM | | | | | SWBSTFAULTM |
| Default | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |

= Unimplemented or reserved

Notes
65. Read: Anytime
Write: Anytime

**Table 106. INTMASK3 field descriptions**

| Field | Description |
|---|---|
| 7<br>OTP_ECCM | OTP error interrupt mask bit<br>0 OTP_ECCI unmasked<br>1 OTP_ECCI masked |
| 6<br>OTP_AUTO_BLOW_DONEM | OTP auto blow mask bit<br>0 OTP_AUTO_BLOW_DONEI unmasked<br>1 OTP_AUTO_BLOW_DONEI masked |
| 0<br>SWBSTFAULTM | SWBST overcurrent limit interrupt mask bit<br>0 SWBSTFAULTI unmasked<br>1 SWBSTFAULTI masked |

### 6.6.5.3.9 Interrupt sense register 3 (INTSENSE3)

This register has four read-only sense bits. These sense bits reflect the actual state of the corresponding function.

**Table 107. Interrupt sense register 3 (INTSENSE3)**

**Address: 0x10 functional page** — **Access: user read-only (66)**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | OTP_ECCS | OTP_AUTO_BLOW_DONES | | | | | | SWBSTFAULTS |
| W | | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | X (67) |

= Unimplemented or reserved

Notes
66. Read: Anytime
67. Default value depends on the regulator initial state

**Table 108. INTSENSE3 field descriptions**

| Field | Description |
|---|---|
| 7<br>OTP_ECCS | OTP error sense bit<br>0 No error detected<br>1 OTP error detected |
| 6<br>OTP_AUTO_BLOW_DONES | **OTP auto blow sense bit** — This bit is high while the auto blow sequence is running. Do not read/write the OTP TBB registers while this bit is 1.<br>0 SW2 in normal operation<br>1 SW2 at current limit |
| 0<br>SWBSTFAULTS | SWBST overcurrent limit sense bit<br>0 SWBST in normal operation<br>1 SWBST above current limit |

### 6.6.5.3.10 Interrupt status register 4 (INTSTAT4)

INSTAT4 is one of the four status interrupt registers. This register contains six status flags. Write a logic 1 to clear a flag.

**Table 109. Status interrupt register 4 (INTSTAT4)**

**Address: 0x11 functional page** **Access: user read/write (68)**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | | | LDO4FAULTI | LDO3FAULTI | V33FAULTI | VSDFAULTI | LDO2FAULTI | LDO1FAULTI |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or reserved

Notes
68. Read: Anytime
Write: Anytime

**Table 110. INTSTAT4 field descriptions**

| Field | Description |
|---|---|
| 5<br>LDO4FAULTI | **LDO4 overcurrent interrupt bit** — LDO4FAULTI is set to 1 when the LDO4 regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect.<br>0 LDO4 in normal operation<br>1 LDO4 above current limit |
| 4<br>LDO3FAULTI | **LDO3 overcurrent interrupt bit** — LDO3FAULTI is set to 1 when the LDO3 regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect.<br>0 LDO3 in normal operation<br>1 LDO3 above current limit |
| 3<br>V33FAULTI | **V33 overcurrent interrupt bit** — V33FAULTI is set to 1 when the V33 regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect.<br>0 V33 in normal operation<br>1 V33 above current limit |
| 2<br>VSDFAULTI | **VSD overcurrent interrupt bit** — VSDFAULTI is set to 1 when the VSD regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect.<br>0 VSD in normal operation<br>1 VSD above current limit |
| 1<br>LDO2FAULTI | **LDO2 overcurrent interrupt bit** — LDO2FAULTI is set to 1 when the LDO2 regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect.<br>0 LDO2 in normal operation range.<br>1 LDO2 above current limit |
| 0<br>LDO1FAULTI | **LDO1 overcurrent interrupt bit** — LDO1FAULTI is set to 1 when the LDO1 regulator is in current limit protection. This flag can only be cleared by writing a 1. Writing a 0 has no effect.<br>0 LDO1 in normal operation range.<br>1 LDO1 above current limit |

### 6.6.5.3.11 Interrupt status mask register 4 (INTMASK4)

INTMASK4 is the mask register for the status interrupt register INTSTAT4. Write a logic 0 to a bit to unmask the corresponding interrupt. When unmasked, the corresponding interrupt state is reflected on the INTB pin.

**Table 111. Interrupt status mask register 4 (INTMASK4)**

**Address: 0x12 functional page** **Access: user read/write (69)**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | | | LDO4FAULTM | LDO3FAULTM | V33FAULTM | VSDFAULTM | LDO2FAULTM | LDO1FAULTM |
| Default | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

= Unimplemented or reserved

Notes
69. Read: Anytime
Write: Anytime

**Table 112. INTMASK4 field descriptions**

| Field | Description |
|---|---|
| 5<br>LDO4FAULTM | LDO4 overcurrent interrupt mask bit<br>0 LDO4FAULTI unmasked<br>1 LDO4FAULTI masked |
| 4<br>LDO3FAULTM | LDO3 overcurrent interrupt mask bit<br>0 LDO3FAULTI unmasked<br>1 LDO3FAULTI masked |
| 3<br>V33FAULTM | V33 overcurrent interrupt mask bit<br>0 V33FAULTI unmasked<br>1 V33FAULTI masked |
| 2<br>VSDFAULTM | VSD overcurrent interrupt mask bit<br>0 VSDFAULTI unmasked<br>1 VSDFAULTI masked |
| 1<br>LDO2FAULTM | LDO2 overcurrent interrupt mask bit<br>0 LDO2FAULTI unmasked<br>1 LDO2FAULTI masked |
| 0<br>LDO1FAULTM | LDO1 overcurrent interrupt mask bit<br>0 LDO1FAULTI unmasked<br>1 LDO1FAULTI masked |

### 6.6.5.3.12 Interrupt sense register 4 (INTSENSE4)

This register has four read-only sense bits. These sense bits reflect the actual state of the corresponding function.

**Address: 0x13 functional page** **Access: user read-only (70)**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R | | | LDO4FAULTS | LDO3FAULTS | V33FAULTS | VSDFAULTS | LDO2FAULTS | LDO1FAULTS |
| W | | | | | | | | |
| Default | 0 | 0 | X (71) | X (71) | X (71) | X (71) | X (71) | X (71) |

= Unimplemented or reserved

Notes
70. Read: Anytime
71. Default value depends on the regulator initial state

**Table 113. INTSENSE4 field descriptions**

| Field | Description |
|---|---|
| 5<br>LDO4FAULTS | LDO4 overcurrent sense bit<br>0 LDO4 in normal operation<br>1 LDO4 above current limit |
| 4<br>LDO3FAULTS | LDO3 overcurrent sense bit<br>0 LDO3 in normal operation<br>1 LDO3 above current limit |
| 3<br>V33FAULTS | V33 overcurrent sense bit<br>0 V33 in normal operation<br>1 V33 above current limit |
| 2<br>VSDFAULTS | VSD overcurrent sense bit<br>0 VSD in normal operation<br>1 VSD above current limit |
| 1<br>LDO2FAULTS | LDO2 overcurrent sense bit<br>0 LDO2 in normal operation<br>1 LDO2 above current limit |
| 0<br>LDO1FAULTS | LDO1 overcurrent sense bit<br>0 LDO1 in normal operation<br>1 LDO1 above current limit |

### 6.6.5.3.13 Coin cell control register (COINCTL)

This register is used to control the coin cell charger.

**Table 114. Coin cell control register (COINCTL)**

| | Address: 0x1A functional page | | | | | | | Access: user read/write (72) |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R<br>W | | | | | COINCHEN | VCOIN | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or reserved

Notes
72. Read: Anytime
Write: Anytime

**Table 115. COINCTL field descriptions**

| Field | Description |
|---|---|
| 3<br>COINCHEN | Coin cell charger enable bit<br>0 Coin cell charger disabled.<br>1 Coin cell charger enabled. |
| 2:0<br>VCOIN | **Coin cell charger output voltage selection** — This field is used to set the coin cell charging voltage from 2.50 V to 3.30 V. See Table 63 for all options selectable through these bits. |

### 6.6.5.3.14 Power control register (PWRCTL)

**Table 116. Power control register (PWRCTL)**

| | Address: 0x1B functional page | | | | | | | Access: user read/write (73) |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R<br>W | REGSCPEN | STBYINV | STBYDLY | | ENBDBNC | | ENRSTEN | RESTARTEN |
| Default | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

= Unimplemented or reserved

Notes
73. Read: Anytime
Write: Anytime

**Table 117. PWRCTL field descriptions**

| Field | Description |
|---|---|
| 7<br>REGSCPEN | **Short-circuit protection enable bit** — When REGSCPEN is set to 1, whenever a current limit event occurs on a LDO regulator, this regulator is shutdown.<br>0 Short-circuit protection disabled<br>1 Short-circuit protection enabled |
| 6<br>STBYINV | **STBY inversion bit** —STBYINV is used to control the polarity of the STBY pin.<br>0 Standby pin is active high<br>1 Standby pin is active low |
| 4:3<br>STBYDLY | **STBY delay bits** — STBYDLY is used to set the delay between a standby request from the STBY pin and the entering in standby mode.<br>00 No delay<br>01 One 32 kHz period (default)<br>10 Two 32 kHz periods<br>11 Three 32 kHz periods |
| 3:2<br>ENDBNC | **EN programmable debouncer bits** — ENDBNC is used to set the debounce time for the EN input pin. For configuration, see Table 31. |
| 1<br>ENRSTEN | **EN reset enable bit** — When set to 1, the VR5100 can enter OFF mode when the EN pin is held low for 4 seconds or longer. See EN Pin section for details.<br>0 Disallow OFF mode after EN held low<br>1 Allow OFF mode after ENheld low |
| 0<br>RESTARTEN | **Restart enable bit** — When set to 1, the VR5100 restarts automatically after a power off event generated by the EN (held low for 4 seconds or longer) when PWR_CFG bit = 1.<br>0 Automatic restart disabled.<br>1 Automatic restart enabled. |

## 6.6.5.3.15 Embedded memory register A (MEMA)

**Table 118. Embedded memory register A (MEMA)**

**Address: 0x1C functional page** — **Access: user read/write** (74)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | MEMA | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or reserved

Notes
74. Read: Anytime
Write: Anytime

**Table 119. MEMA field descriptions**

| Field | Description |
|---|---|
| 7:0<br>MEMA | **Memory bank A** — This register is maintained in case of a main battery loss as long as the coin cell is present. The contents of the embedded memory are reset by COINPORB. |

## 6.6.5.3.16 Embedded memory register B (MEMB)

**Table 120. Embedded memory register B (MEMB)**

| Address: 0x1D functional page | | | | | | | Access: user read/write |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R<br>W | MEMB | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or reserved

Notes

75. Read: Anytime
Write: Anytime

**Table 121. MEMB field descriptions**

| Field | Description |
|---|---|
| 7:0<br>MEMB | **Memory bank B** — This register is maintained in case of a main battery loss as long as the coin cell is present. The contents of the embedded memory are reset by COINPORB. |

## 6.6.5.3.17 Embedded memory register C (MEMC)

**Table 122. Embedded memory register C (MEMC)**

| Address: 0x1E functional page | | | | | | | Access: user read/write (76) |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R<br>W | MEMC | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or reserved

Notes

76. Read: Anytime
Write: Anytime

**Table 123. MEMC field descriptions**

| Field | Description |
|---|---|
| 7:0<br>MEMC | **Memory bank C** — This register is maintained in case of a main battery loss as long as the coin cell is present. The contents of the embedded memory are reset by COINPORB. |

### 6.6.5.3.18 Embedded memory register D (MEMD)

**Table 124. Embedded memory register D (MEMD)**

| Address: 0x1F functional page | | | | | | | Access: user read/write (77) |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R<br>W | MEMD | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or reserved

Notes
77. Read: Anytime
Write: Anytime

**Table 125. MEMD field descriptions**

| Field | Description |
|---|---|
| 7:0<br>MEMD | **Memory bank D** — This register is maintained in case of a main battery loss as long as the coin cell is present. The contents of the embedded memory are reset by COINPORB. |

### 6.6.5.3.19 SW1 voltage control register (SW1VOLT)

This register is used to set the output voltage of the SW1 regulator in normal operation.

**Table 126. SW1 voltage control register (SW1VOLT)**

| Address: 0x20 functional page | | | | | | | Access: user read/write (78) |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R<br>W | | | | SW1 | | | |
| Default | 0 | 0 | 0 | X (79) | X (79) | X (79) | X (79) | X (79) |

= Unimplemented or reserved

Notes
78. Read: Anytime
Write: Anytime
79. Default value depends on OTP content.

**Table 127. SW1VOLT field descriptions**

| Field | Description |
|---|---|
| 4:0<br>SW1 | **SW1 output voltage** — Refer to Table 46 |

### 6.6.5.3.20 SW1 standby voltage control register (SW1STBY)

This register is used to set the output voltage of the SW1 regulator in standby operation.

**Table 128. SW1 standby voltage control register (SW1STBY)**

**Address: 0x21 functional page** **Access: user read/write (80)**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | | | | SW1STBY | | | | |
| Default | 0 | 0 | 0 | X (81) | X (81) | X (81) | X (81) | X (81) |

= Unimplemented or reserved

Notes
80. Read: Anytime
Write: Anytime
81. Default value depends on OTP content.

**Table 129. SW1STBY field descriptions**

| Field | Description |
|---|---|
| 4:0<br>SW1STBY | **SW1 standby output voltage** — Refer to Table 46 |

### 6.6.5.3.21 SW1 Sleep mode voltage control register (SW1OFF)

This register is used to set the output voltage of the SW1 regulator in Sleep mode operation.

**Table 130. SW1 Sleep mode voltage control register (SW1OFF)**

**Address: 0x22 functional page** **Access: user read/write (82)**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | | | | SW1OFF | | | | |
| Default | 0 | 0 | 0 | X (83) | X (83) | X (83) | X (83) | X (83) |

= Unimplemented or Reserved

Notes
82. Read: Anytime
Write: Anytime
83. Default value depends on OTP content.

**Table 131. SW1OFF field descriptions**

| Field | Description |
|---|---|
| 4:0<br>SW1STBY | **SW1 Sleep mode output voltage** — Refer to Table 46 |

### 6.6.5.3.22 SW1 Switching mode selector register (SW1MODE)

This register is used to set the switching mode of the SW1 regulator.

**Table 132. SW1 Switching mode selector register (SW1MODE)**

| Address: 0x23 functional page | | | | | | | Access: user read/write (84) |
|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R<br>W | | | SW1OMODE | | SW1MODE | | | |
| Default | 0 | 0 | 0 | 0 | X (85) | X (85) | X (85) | X (85) |

= Unimplemented or reserved

Notes
84. Read: Anytime
Write: Anytime
85. Default value depends on OTP content.

**Table 133. SW1MODE field descriptions**

| Field | Description |
|---|---|
| 5<br>SW1OMODE | **SW1 Off mode bit**— This bit configures the mode entered by SW1 after a turn-off event<br>0 OFF mode entered after a turn-off event.<br>1 Sleep mode entered after a turn-off event. |
| 3:0<br>SW1MODE | **SW1 Switching mode selector** — Refer to Table 41 |

### 6.6.5.3.23 SW1 configuration register (SW1CONF)

This register is used to configure DVS, switching frequency, phase and current limit settings of the SW1 regulator.

**Table 134. SW1 configuration register (SW1CONF)**

| Address: 0x24 functional page | | | | | | | Access: user read/write (86) |
|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R<br>W | | SW1DVSSPEED | SW1PHASE | | SW1FREQ | | | SW1ILIM |
| Default | 0 | X (87) | 0 | 0 | X (87) | X (87) | 0 | X (87) |

= Unimplemented or reserved

Notes
86. Read: Anytime
Write: Anytime
87. Default value depends on OTP content.

**Table 135. SW1CONF field descriptions**

| Field | Description |
|---|---|
| 6<br>SW1DVSSPEED | **SW1 DVS speed bit**— This bit configures the DVS stepping rates speed for SW1. Refer to the Table 42.<br>0 25 mV step each 2.0 µs.<br>1 25 mV step each 4.0 µs. |
| 5:4<br>SW1PHASE | **SW1 phase clock bit**— SW1PHASE is used to set the phase clock for SW1. Refer to Table 43. |
| 3:2<br>SW1FREQ | **SW1 switching frequency**— SW1PHASE is used to set the desired switching frequency for SWA. Refer to Table 45. |
| 0<br>SW1ILIM | **SW1 current limiter bit**— This bit configures the current limit for SW1.<br>0 4 A (typ).<br>1 2.0 A (typ). |

## 6.6.5.3.24 SW1 configuration register (SW1CONF)

This register is used to configure DVS, switching frequency, phase and current limit settings of the SW1 regulator.

**Table 136. SW1 configuration register (SW1CONF)**

**Address: 0x32 functional page** **Access: user read/write** X (88)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | SW1DVSSPEED | | SW1PHASE | | SW1FREQ | | | SW1ILIM |
| Default | 0 | X (89) | 0 | 0 | X (89) | X (89) | 0 | X (89) |

= Unimplemented or reserved

Notes
88. Read: Anytime
Write: Anytime
89. Default value depends on OTP content.

**Table 137. SW1CONF field descriptions**

| Field | Description |
|---|---|
| 6<br>SW1DVSSPEED | **SW1 DVS speed bit**— This bit configures the DVS stepping rates speed for SW1. Refer to the Table 42.<br>0 25 mV step each 2.0 µs.<br>1 25 mV step each 4.0 µs. |
| 5:4<br>SW1PHASE | **SW1 phase clock bit**— SW1PHASE is used to set the phase clock for SW1. Refer to Table 43. |
| 3:2<br>SW1FREQ | **SW1 switching frequency**— SW1PHASE is used to set the desired switching frequency for SW1. Refer to Table 45. |
| 0<br>SW1ILIM | **SW1 current limiter bit**— This bit configures the current limit for SW1.<br>0 4.0 A (typ).<br>1 2.0 A (typ). |

## 6.6.5.3.25 SW2 voltage control register (SW2VOLT)

This register is used to set the output voltage of the SW2 regulator in normal operation.

**Table 138. SW2 voltage control register (SW2VOLT)**

**Address: 0x35 functional page** — **Access: user read/write (90)**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | | | SW2_HI | SW2 | | | | |
| Default | 0 | 0 | X (91) | X (91) | X (91) | X (91) | X (91) | X (91) |

= Unimplemented or reserved

Notes
90. Read: Anytime
Write: Anytime
91. Default value depends on OTP content.

**Table 139. SW2VOLT field descriptions**

| Field | Description |
|---|---|
| 4:0<br>SW2 | **SW2 output voltage** — Refer to Table 48. |
| 5<br>SW2_HI | **SW2 output voltage range** —This bit configures the range of SW2 Output voltage. Refer to Table 48.<br>0 Low output voltage settings<br>1 High output voltage settings |

## 6.6.5.3.26 SW2 standby voltage control register (SW2STBY)

This register is used to set the output voltage of the SW2 regulator in standby operation.

**Table 140. SW2 standby voltage control register (SW2STBY)**

**Address: 0x36 functional page** — **Access: user read/write (92)**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | | | SW2_HI | SW2STBY | | | | |
| Default | 0 | 0 | X (93) | X (93) | X (93) | X (93) | X (93) | X (93) |

= Unimplemented or reserved

Notes
92. Read: Anytime
Write: Anytime
93. Default value depends on OTP content.

**Table 141. SW2STBY field descriptions**

| Field | Description |
|---|---|
| 4:0<br>SW2STBY | **SW2 standby output voltage** — Refer to Table 48. |
| 5<br>SW2_HI | **SW2 output voltage range** —This bit configures the range of SW2 output voltage. Refer to Table 48.<br>0 Low output voltage settings<br>1 High output voltage settings |

### 6.6.5.3.27 SW2 Sleep mode voltage control register (SW2OFF)

This register is used to set the output voltage of the SW2 regulator in Sleep mode operation.

**Table 142. SW2 Sleep mode voltage control register (SW2OFF)**

| | Address: 0x37 functional page | | | | | | | Access: user read/write (94) |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R<br>W | | | SW2_HI | SW2OFF | | | | |
| Default | 0 | 0 | X (95) | X (95) | X (95) | X (95) | X (95) | X (95) |

= Unimplemented or reserved

Notes
94. Read: Anytime
Write: Anytime
95. Default value depends on OTP content.

**Table 143. SW2OFF field descriptions**

| Field | Description |
|---|---|
| 4:0<br>SW2STBY | **SW2 Sleep mode output voltage** — Refer to Table 48. |
| 5<br>SW2_HI | **SW2 output voltage range** —This bit configures the range of SW2 output voltage. Refer to Table 48.<br>0 Low output voltage settings<br>1 High output voltage settings |

### 6.6.5.3.28 SW2 Switching mode selector register (SW2MODE)

This register is used to set the switching mode of the SW2 regulator.

**Table 144. SW2 Switching mode selector register (SW2MODE)**

| | Address: 0x38 functional page | | | | | | | Access: user read/write (96) |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R<br>W | | | SW2OMODE | | SW2MODE | | | |
| Default | 0 | 0 | 0 | 0 | X (97) | X (97) | X (97) | X (97) |

= Unimplemented or reserved

Notes
96. Read: Anytime
Write: Anytime
97. Default value depends on OTP content.

**Table 145. SW2MODE field descriptions**

| Field | Description |
|---|---|
| 5<br>SW2OMODE | **SW2 Off mode bit**— This bit configures the mode entered by SW2 after a turn-off event<br>0 OFF mode entered after a turn-off event.<br>1 Sleep mode entered after a turn-off event. |
| 3:0<br>SW2MODE | **SW2 Switching mode selector** — Refer to Table 41. |

### 6.6.5.3.29 SW2 configuration register (SW2CONF)

This register is used to configure DVS, switching frequency, phase and current limit settings of the SW2 regulator.

**Table 146. SW2 configuration register (SW2CONF)**

**Address: 0x39 functional page** — **Access: user read/write (98)**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | | SW2DVSSPEED | SW2PHASE | | SW2FREQ | | | SW2ILIM |
| Default | 0 | X (99) | 0 | 0 | X (99) | X (99) | 0 | X (99) |

= Unimplemented or reserved

Notes
98. Read: Anytime
Write: Anytime
99. Default value depends on OTP content.

**Table 147. SW2CONF field descriptions**

| Field | Description |
|---|---|
| 6<br>SW2DVSSPEED | SW2 DVS Speed bit- This bit configures the DVS stepping rates speed for SW2. Refer to the Table 42.<br>0 25 mV step each 2.0 µs.<br>1 25 mV step each 4.0 µs. |
| 5:4<br>SW2PHASE | **SW2 phase clock bit**— SW2PHASE is used to set the phase clock for SW2. Refer to Table 43. |
| 3:2<br>SW2FREQ | **SW2 switching frequency**— SW2PHASE is used to set the desired switching frequency for SW2. Refer to Table 45. |
| 0<br>SW2ILIM | **SW2 current limiter bit**— This bit configures the current limit for SW2.<br>0 2.75 A (typ).<br>1 2.0 A (typ). |

### 6.6.5.3.30 SW3 voltage control register (SW3VOLT)

This register is used to set the output voltage of the SW3 regulator in normal operation.

**Table 148. SW3 voltage control register (SW3VOLT)**

**Address: 0x3C functional page** — **Access: user read/write (100)**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | | | | SW3 | | | | |
| Default | 0 | 0 | 0 | X (101) | X (101) | X (101) | X (101) | X (101) |

= Unimplemented or reserved

Notes
100. Read: Anytime
Write: Anytime
101. Default value depends on OTP content.

**Table 149. SW3VOLT field descriptions**

| Field | Description |
|---|---|
| 4:0<br>SW3 | **SW3 output voltage** — Refer to Table 50. |

## 6.6.5.3.31 SW3 standby voltage control register (SW3STBY)

This register is used to set the output voltage of the SW3 regulator in standby operation.

**Table 150. SW3 standby voltage control register (SW3STBY)**

| Address: 0x3D functional page | | | | | | | Access: user read/write (102) |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R<br>W | | | | SW3STBY | | | |
| Default | 0 | 0 | 0 | X (103) | X (103) | X (103) | X (103) | X (103) |

= Unimplemented or reserved

Notes
102. Read: Anytime
Write: Anytime
103. Default value depends on OTP content.

**Table 151. SW3STBY field descriptions**

| Field | Description |
|---|---|
| 4:0<br>SW3STBY | **SW3 standby output voltage** — Refer to Table 50. |

## 6.6.5.3.32 SW3 Sleep mode voltage control register (SW3OFF)

This register is used to set the output voltage of the SW3 regulator in sleep mode operation.

**Table 152. SW3 Sleep mode voltage control register (SW3OFF)**

| Address: 0x3E functional page | | | | | | | Access: user read/write (104) |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R<br>W | | | | SW3OFF | | | |
| Default | 0 | 0 | 0 | X (105) | X (105) | X (105) | X (105) | X (105) |

= Unimplemented or reserved

Notes
104. Read: Anytime
Write: Anytime
105. Default value depends on OTP content.

**Table 153. SW3OFF field descriptions**

| Field | Description |
|---|---|
| 4:0<br>SW3STBY | **SW3 Sleep mode output voltage** — Refer to Refer to Table 50. |

### 6.6.5.3.33 SW3 Switching mode selector register (SW3MODE)

This register is used to set the switching mode of the SW3 regulator.

**Table 154. SW3 Switching mode selector register (SW3MODE)**

| Address: 0x3F functional page | | | | | | | Access: user read/write (106) | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R<br>W | | | SW3OMODE | | SW3MODE | | | |
| Default | 0 | 0 | 0 | 0 | X (107) | X (107) | X (107) | X (107) |

= Unimplemented or reserved

Notes
106. Read: Anytime
Write: Anytime
107. Default value depends on OTP content.

**Table 155. SW3MODE field descriptions**

| Field | Description |
|---|---|
| 5<br>SW3OMODE | **SW3 Off mode bit**— This bit configures the mode entered by SW3 after a turn-off event<br>0 OFF mode entered after a turn-off event.<br>1 Sleep mode entered after a turn-off event. |
| 3:0<br>SW3MODE | **SW3 Switching mode selector** — Refer to Table 41. |

### 6.6.5.3.34 SW3 configuration register (SW3CONF)

This register is used to configure DVS, switching frequency, phase and current limit settings of the SW3 regulator.

**Table 156. SW3 configuration register (SW3CONF)**

| Address: 0x40 functional page | | | | | | | Access: user read/write (108) | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R<br>W | | SW3DVSSPEED | SW3PHASE | | SW3FREQ | | | SW3ILIM |
| Default | 0 | X (109) | 0 | 0 | X (109) | X (109) | 0 | X (109) |

= Unimplemented or reserved

Notes
108. Read: Anytime
Write: Anytime
109. Default value depends on OTP content.

**Table 157. SW3CONF field descriptions**

| Field | Description |
|---|---|
| 6<br>SW3DVSSPEED | **SW3 DVS speed bit**— This bit configures the DVS stepping rates speed for SW3. Refer to the Table 42.<br>0 25 mV step each 2.0 µs.<br>1 25 mV step each 4.0 µs. |
| 5:4<br>SW3PHASE | **SW3 phase clock bit**— SW3PHASE is used to set the phase clock for SW3. Refer to Table 43. |
| 3:2<br>SW3FREQ | **SW3 switching frequency**— SW3PHASE is used to set the desired switching frequency for SW3. Refer to Table 45. |
| 0<br>SW3ILIM | **SW3 current limiter bit**— This bit configures the current limit for SW3.<br>0 2.75 A (typ).<br>1 2.0 A (typ). |

## 6.6.5.3.35 SWBST setup and control register (SWBSTCTL)

This register is used to configure both the output voltage and switching modes of the SWBST regulator.

**Table 158. SWBST configuration register (SWBSTCTL)**

**Address: 0x66 functional page** — **Access: user read/write (110)**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | | SWBST1STBYMODE | | | SWBST1MODE | | SWBST1VOLT | |
| Default | 0 | X (111) | X (111) | 0 | X (111) | X (111) | X (111) | X (111) |

= Unimplemented or reserved

Notes
110. Read: Anytime
Write: Anytime
111. Default value depends on OTP content.

**Table 159. SWBSTCTL Field Descriptions**

| Field | Description |
|---|---|
| 6:5<br>SWBST1STBYMODE | **SWBST Switching mode in standby**— SWBST1MODE is used to set the switching mode in Standby mode.<br>00 OFF<br>01 PFM<br>10 Auto (112)<br>11 APS |
| 3:2<br>SWBST1MODE | **SWBST Switching mode in normal operation**— SWBST1MODE is used to set the switching mode on Normal operation.<br>00 OFF<br>01 PFM<br>10 Auto (112)<br>11 APS |
| 1:0<br>SWBST1VOLT | **SWBST output voltage**— SWBST1VOLT is used to set the output voltage for SWBST.<br>00 5.000 V (typ).<br>01 5.050 V (typ).<br>10 5.100 V (typ).<br>11 5.150 V (typ). |

Notes
112. In Auto mode, the controller automatically switches between PFM and APS modes depending on the load current. Regulator switches in Auto mode if enabled in the startup sequence.

### 6.6.5.3.36 REFOUT control register (REFOUTCTL)

This register is used to control the REFOUT supply operation.

**Table 160. REFOUT control register (REFOUTCTL)**

**Address: 0x6A functional page** **Access: user read/write (113)**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | | | | | | | | REFOUTEN |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or reserved

Notes
113. Read: Anytime
Write: Anytime

**Table 161. REFOUT field descriptions**

| Field | Description |
|---|---|
| 0<br>REFOUTEN | **REFOUT supply enable bit**— REFOUTEN is used to enable or disable the REFOUT supply.<br>0 REFOUT supply disabled<br>1 REFOUT supply enabled |

### 6.6.5.3.37 VSNVS control register (VSNVSCTL)

This register is used to control the VSNVS supply operation.

**Table 162. VSNVS control register (VSNVSCTL)**

| Address: 0x6B functional page | | | | | | | Access: user read/write (114) |
|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R<br>W | | | | | | VSNVSVOLT | | |
| Default | 0 | 0 | 0 | 0 | 0 | X (115) | X (115) | X (115) |

= Unimplemented or Reserved

Notes
114. Read: Anytime
Write: Anytime
115. Default value depends on OTP content.

**Table 163. VSNVSCTL field descriptions**

| Field | Description |
|---|---|
| 2:0<br>VSNVSVOLT | **VSNVS output voltage configuration**— VSNVSVOLT is used to configure the VSNVS output voltage. Values below are typical voltages.<br>000 = RSVD<br>001 = RSVD<br>010 = RSVD<br>011 = RSVD<br>100 = RSVD<br>101 = RSVD<br>110 = 3.0 V (default)<br>111 = RSVD |

### 6.6.5.3.38 LDO1 control register (LDO1CTL)

This register is used to configure output voltage, normal and standby mode operation of the LDO1 regulator.

**Table 164. LDO1 control register (LDO1CTL)**

| Address: 0x6C functional page | | | | | | | Access: user read/write (116) |
|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R<br>W | LDO1OMODE | LDO1LPWR | LDO1STBY | LDO1EN | LDO1 | | | |
| Default | 0 | 0 | 0 | X (117) | X (117) | X (117) | X (117) | X (117) |

= Unimplemented or reserved

Notes
116. Read: Anytime
Write: Anytime
117. Default value depends on OTP content.

**Table 165. LDO1CTL field descriptions**

| Field | Description |
|---|---|
| 7<br>LDO1OMODE | **LDO1 OFF mode bit**—LDO1OMODE is used to configure LDO1 operating mode when a EN turn-off event occurs.<br>0 LDO1 in OFF mode if a EN turn off event occurs<br>1 LDO1 in Sleep mode if a EN turn off event occurs |
| 6<br>LDO1LPWR | **LDO1 Low-power mode enable bit**— When LDO1LPWR is set to 1, LDO1 can enter Low-power mode per the conditions in the Table 59.<br>0 Low-power mode disabled<br>1 Low-power mode enabled |
| 5<br>LDO1STBY | **LDO1 standby enable bit**— When LDO1STBY is set to 1, LDO1 is turned off during Standby mode. Refer to Table 59.<br>0 LDO1 is ON during Standby mode.<br>1 LDO1 is OFF during Standby mode. |
| 4<br>LDO1EN | **LDO1 enable bit** — LDO1EN is used to enable or disable the LDO1 regulator.<br>0 LDO1 disabled<br>1 LDO1 enabled |
| 3:0<br>LDO1 | **LDO1 output voltage configuration**— Refer to Table 55. |

## 6.6.5.3.39 LDO2 control register (LDO2CTL)

This register is used to configure output voltage, Normal and Standby mode operation of the LDO2 regulator.

**Table 166. LDO2 control register (LDO2CTL)**

**Address: 0x6D functional page** **Access: user read/write (118)**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | LDO2OMODE | LDO2LPWR | LDO2STBY | LDO2EN | LDO2 | | | |
| Default | 0 | 0 | 0 | X (119) | X (119) | X (119) | X (119) | X (119) |

= Unimplemented or reserved

Notes
118. Read: Anytime
Write: Anytime
119. Default value depends on OTP content.

**Table 167. LDO2CTL field descriptions**

| Field | Description |
|---|---|
| 7<br>LDO2OMODE | **LDO2 OFF mode bit**—LDO2OMODE is used to configure LDO2 operating mode when a EN turn-off event occurs.<br>0 LDO2 in OFF mode if a EN turn off event occurs<br>1 LDO2 in Sleep mode if a EN turn off event occurs |
| 6<br>LDO2LPWR | **LDO2 low power mode enable bit**— When LDO2LPWR is set to 1, LDO2 can enter Low-power mode per the conditions in the LDO Control table.<br>0 Low-power mode disabled<br>1 Low-power mode enabled |
| 5<br>LDO2STBY | **LDO2 standby enable bit**— When LDO2STBY is set to 1, LDO2 is turned off during Standby mode. Refer to Table 59.<br>0 LDO2 is ON during Standby mode.<br>1 LDO2 is OFF during Standby mode. |
| 4<br>LDO2EN | **LDO2 enable bit** — LDO2EN is used to enable or disable the LDO2 regulator.<br>0 LDO2 disabled<br>1 LDO2 enabled |
| 3:0<br>LDO2 | **LDO2 output voltage configuration**— Refer to Table 55. |

## 6.6.5.3.40 VSD control register (VSDCTL)

This register is used to configure output voltage, Normal and Standby mode operation of the VSD regulator.

**Table 168. VSD control register (VSDCTL)**

**Address: 0x6E functional page** — **Access: user read/write (120)**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | VSDOMODE | VSDLPWR | VSDSTBY | VSDEN | | | VSD | |
| Default | 0 | 0 | 0 | X (121) | 0 | 0 | X (121) | X (121) |

= Unimplemented or reserved

Notes

120. Read: Anytime
Write: Anytime

121. Default value depends on OTP content.

**Table 169. VSDCTL field descriptions**

| Field | Description |
|---|---|
| 7<br>VSDOMODE | **VSD OFF mode bit**— VSDOMODE is used to configure VSD operating mode when a EN turn-off event occurs.<br>0 VSD in OFF mode if a EN turn off event occurs<br>1 VSD in Sleep mode if a EN turn off event occurs |
| 6<br>VSDLPWR | **VSD low-power mode enable bit**— When VSDLPWR is set to 1, VSD can enter Low-power mode per the conditions in Table 58.<br>0 Low-power mode disabled<br>1 Low-power mode enabled |
| 5<br>VSDSTBY | **VSD standby enable bit**— When VSDSTBY is set to 1, VSD is turned off during Standby mode. Refer to Table 58.<br>0 VSD is ON during Standby mode.<br>1 VSD is OFF during Standby mode. |
| 4<br>VSDEN | **VSD enable bit** — VSDEN is used to enable or disable the VSD regulator.<br>0 VSD disabled<br>1 VSD enabled |
| 1:0<br>VSD | **VSD output voltage configuration**— Refer to Table 58. |

## 6.6.5.3.41 V33 control register (V33CTL)

This register is used to configure output voltage, Normal and Standby mode operation of the V33 regulator.

**Table 170. V33 control register (V33CTL)**

**Address: 0x6F functional page** **Access: user read/write (122)**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | V33OMODE | V33LPWR | V33STBY | V33EN | | | V33 | |
| Default | 0 | 0 | 0 | X (123) | 0 | 0 | X (123) | X (123) |

= Unimplemented or reserved

Notes
122. Read: Anytime
Write: Anytime
123. Default value depends on OTP content.

**Table 171. V33CTL field descriptions**

| Field | Description |
|---|---|
| 7<br>V33OMODE | **V33 OFF mode bit**— V33OMODE is used to configure V33 operating mode when a turn-off event (using pin EN) occurs.<br>0 V33 in OFF mode if a PWRON turn-off event (using pin EN) occurs<br>1 V33 in Sleep mode if a PWRON turn-off event (using pin EN) occurs |
| 6<br>V33LPWR | **V33 Low-power mode enable bit**— When V33LPWR is set to 1, V33 can enter Low-power mode per the conditions in the Table 57.<br>0 Low-power mode disabled<br>1 Low-power mode enabled |
| 5<br>V33STBY | **V33 standby enable bit**— When V33STBY is set to 1, V33 is turned off during Standby mode. Refer to Table 57.<br>0 V33 is ON during Standby mode.<br>1 V33 is OFF during Standby mode. |
| 4<br>V33EN | **V33 enable bit** — V33EN is used to enable or disable the V33 regulator.<br>0 V33 disabled<br>1 V33 enabled |
| 1:0<br>V33 | **V33 output voltage configuration**— Refer to Table 57. |

### 6.6.5.3.42 LDO3 control register (LDO3CTL)

This register is used to configure output voltage, Normal and Standby mode operation of the LDO3 regulator.

**Table 172. LDO3 control register (LDO3CTL)**

**Address: 0x70 functional page** **Access: user read/write (124)**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | LDO3OMODE | LDO3LPWR | LDO3STBY | LDO3EN | LDO3 | | | |
| Default | 0 | 0 | 0 | X (125) | X (125) | X (125) | X (125) | X (125) |

= Unimplemented or reserved

Notes
124. Read: Anytime
Write: Anytime
125. Default value depends on OTP content.

**Table 173. LDO3CTL field descriptions**

| Field | Description |
|---|---|
| 7<br>LDO3OMODE | **LDO3 OFF mode bit**—LDO3OMODE is used to configure LDO3 operating mode when a EN turn-off event occurs.<br>0 LDO3 in OFF mode if a EN turn off event occurs<br>1 LDO3 in Sleep mode if a EN turn off event occurs |
| 6<br>LDO3LPWR | **LDO3 Low-power mode enable bit**— When LDO3LPWR is set to 1, LDO3 can enter Low-power mode per the conditions in Table 59.<br>0 Low-power mode disabled<br>1 Low-power mode enabled |
| 5<br>LDO3STBY | **LDO3 standby enable bit**— When LDO3STBY is set to 1, LDO3 is turned off during Standby mode. Refer to Table 59.<br>0 LDO3 is ON during Standby mode.<br>1 LDO3 is OFF during Standby mode. |
| 4<br>LDO3EN | **LDO3 enable bit** — LDO3EN is used to enable or disable the LDO3 regulator.<br>0 LDO3 disabled<br>1 LDO3 enabled |
| 3:0<br>LDO3 | **LDO3 output voltage configuration**— Refer to Table 56. |

### 6.6.5.3.43 LDO4 control register (LDO4CTL)

This register is used to configure output voltage, Normal and Standby mode operation of the LDO4 regulator.

**Table 174. LDO4 control register (LDO4CTL)**

**Address: 0x71 functional page** **Access: user read/write (126)**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | LDO4OMODE | LDO4LPWR | LDO4STBY | LDO4EN | LDO4 | | | |
| Default | 0 | 0 | 0 | X (127) | X (127) | X (127) | X (127) | X (127) |

= Unimplemented or reserved

Notes
126. Read: Anytime
Write: Anytime
127. Default value depends on OTP content.

**Table 175. LDO4CTL field descriptions**

| Field | Description |
|---|---|
| 7<br>LDO4OMODE | **LDO4 OFF mode bit**—LDO4OMODE is used to configure LDO4 operating mode when a EN turn-off event occurs.<br>0 LDO4 in OFF mode if a EN turn off event occurs<br>1 LDO4 in Sleep mode if a EN turn off event occurs |
| 6<br>LDO4LPWR | **LDO4 Low-power mode enable bit**— When LDO4LPWR is set to 1, LDO4 can enter Low-power mode per the conditions in Table 59.<br>0 Low-power mode disabled<br>1 Low-power mode enabled |
| 5<br>LDO4STBY | **LDO4 standby enable bit**— When LDO4STBY is set to 1, LDO4 is turned off during Standby mode. Refer to Table 59.<br>0 LDO4 is ON during Standby mode.<br>1 LDO4 is OFF during Standby mode. |
| 4<br>LDO4EN | **LDO4 Enable bit** — LDO4EN is used to enable or disable the LDO4 regulator.<br>0 LDO4 disabled<br>1 LDO4 enabled |
| 3:0<br>LDO4 | **LDO4 output voltage configuration**— Refer to Table 56. |

### 6.6.5.3.44 Page selection register

This register is used to access the extended register pages.

**Table 176. Page Selection Register**

**Address: 0x7F functional page** **Access: user read/write (128)**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| R<br>W | | | | | PAGE | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or reserved

Notes
128. Read: Anytime
Write: Anytime

**Table 177. Page register field descriptions**

| Field | Description |
|---|---|
| 3:0<br>PAGE | **Register page selection** — The PAGE field is used to select one of the three available register pages.<br>0000 Functional page selected<br>0001 Extended page 1 selected<br>0010 Extended page 2 selected |

## 6.6.6 Register map

The register map is comprised of thirty-two pages, and its address and data fields are each eight bits wide. Only the first two pages can be accessed. On each page, registers 0 to 0x7F are referred to as 'functional', and registers 0x80 to 0xFF as 'extended'. On each page, the functional registers are the same, but the extended registers are different. To access registers in Extended page 1, one must first write 0x01 to the page register at address 0x7F, and to access registers Extended page 2, one must first write 0x02 to the page register at address 0x7F. To access the Functional page from one of the extended pages, no write to the page register is necessary.

Registers missing in the sequence are reserved; reading from them returns a value 0x00, and writing to them has no effect. The contents of all registers are given in the tables defined in this chapter; each table is structure as follows:

**Name:** Name of the bit

**Bit #:** The bit location in the register (7-0)

**R/W:** Read / Write access and control

- R is read-only access
- R/W is read and write access
- RW1C is read and write access with write 1 to clear

**Reset:** Reset signals are color coded based on the following legend.

| |
|---|
| Bits reset by SC and VDIG_PORB |
| Bits reset by EN or loaded default or OTP configuration |
| Bits reset by DIGRESETB |
| Bits reset by PORB |
| Bits reset by VDIG_PORB |
| Bits reset by POR or OFFB |

**Default:** The value after reset, as noted in the Default column of the memory map.

- Fixed defaults are explicitly declared as 0 or 1.
- “X” corresponds to Read/Write bits initialized at start-up, based on the OTP fuse settings or default if $V_{DDOTP}$ = 1.5 V. Bits are subsequently $I^2C$ modifiable, when their reset has been released. “X” may also refer to bits which may have other dependencies. For example, some bits may depend on the version of the IC, or a value from an analog block, for instance the sense bits for the interrupts.

### 6.6.6.1 Register map

**Table 178. Functional page**

| | | | | BITS[7:0] | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Add** | **Register name** | **R/W** | **Default** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| **00** | **DeviceID** | R | 8'b0011_0000 | – | – | – | – | DEVICE ID [3:0] | | | |
| | | | | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| **03** | **SILICON-REVID** | R | 8'b0001_0000 | FULL_LAYER_REV[3:0] | | | | METAL_LAYER_REV[3:0] | | | |
| | | | | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| **04** | **FABID** | R | 8'b0000_0000 | – | – | – | – | FAB[1:0] | | FIN[1:0] | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **05** | **INTSTAT0** | RW1C | 8'b0000_0000 | – | – | THERM130I | THERM125I | THERM120I | THERM110I | LOWVINI | ENI |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **06** | **INTMASK0** | R/W | 8'b0011_1111 | – | – | THERM130M | THERM125M | THERM120M | THERM110M | LOWVINM | ENM |
| | | | | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| **07** | **INT-SENSE0** | R | 8'b00xx_xxxx | VDDOTPS | ICTESTS | THERM130S | THERM125S | THERM120S | THERM110S | LOWVINS | ENS |
| | | | | 0 | 0 | x | x | x | x | x | x |
| **08** | **INTSTAT1** | RW1C | 8'b0000_0000 | – | – | – | SW3FAULTI | SW2FAULTI | – | SW1FAULTI | SW1FAULTI |
| | | | | 0 | 0 | 0 | 0 | 0 | x | 0 | 0 |
| **09** | **INTMASK1** | R/W | 8'b0111_1111 | – | – | – | SW3FAULTM | SW2FAULTM | – | SW1FAULTM | SW1FAULTM |
| | | | | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| **0A** | **INT-SENSE1** | R | 8'b0xxx_xxxx | – | – | – | SW3FAULTS | SW2FAULTS | – | SW1FAULTS | SW1FAULTS |
| | | | | 0 | x | x | x | x | x | x | x |
| **0E** | **INTSTAT3** | RW1C | 8'b0000_0000 | OTP_ECCI | OTP AUTO BLOW DONE | – | – | – | – | – | SWBSTFAULTI |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **0F** | **INTMASK3** | R/W | 8'b1100_0101 | OTP_ECCM | OTP_AUTO_BLOW_DONEM | – | – | – | – | – | SWBSTFAULTM |
| | | | | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| **10** | **INT-SENSE3** | R | 8'b0000_000x | OTP_ECCS | OTP_AUTO_BLOW_DONES | – | – | – | – | – | SWBSTFAULTS |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **11** | **INTSTAT4** | RW1C | 8'b0000_0000 | – | – | LDO4FAULTI | LDO3FAULTI | V33FAULTI | VSDFAULTI | LDO2FAULTI | LDO1FAULTI |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **12** | **INTMASK4** | R/W | 8'b0011_1111 | – | – | LDO4 FAULTM | LDO3 FAULTM | V33 FAULTM | VSDFAULTM | LDO2FAULTM | LDO1FAULTM |
| | | | | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| **13** | **INT-SENSE4** | R | 8'b00xx_xxxx | – | – | LDO4 FAULTS | LDO3 FAULTS | V33 FAULTS | VSD FAULTS | LDO2 FAULTS | LDO1 FAULTS |
| | | | | 0 | 0 | x | x | x | x | x | x |
| **1A** | **COINCTL** | R/W | 8'b0000_0000 | – | – | – | – | COINCHEN | VCOIN[2:0] | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **1B** | **PWRCTL** | R/W | 8'b0001_0000 | REGSCPEN | STBYINV | STBYDLY[1:0] | | ENBDBNC[1:0] | | ENRSTEN | RESTARTEN |
| | | | | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

**Table 178. Functional page (continued)**

| | | | | BITS[7:0] | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Add** | **Register name** | **R/W** | **Default** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| **1C** | **MEMA** | R/W | 8'b0000_0000 | MEMA[7:0] | | | | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **1D** | **MEMB** | R/W | 8'b0000_0000 | MEMB[7:0] | | | | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **1E** | **MEMC** | R/W | 8'b0000_0000 | MEMC[7:0] | | | | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **1F** | **MEMD** | R/W | 8'b0000_0000 | MEMD[7:0] | | | | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **20** | **SW1VOLT** | R/W | 8'b000x_xxxx | – | – | – | SW1[4:0] | | | | |
| | | | | 0 | 0 | 0 | – | – | – | – | – |
| **21** | **SW1STBY** | R/W | 8'b000x_xxxx | – | – | – | SW1STBY[4:0] | | | | |
| | | | | 0 | 0 | 0 | – | – | – | – | – |
| **22** | **SW1OFF** | R/W | 8'b000x_xxxx | – | – | – | SW1OFF[4:0] | | | | |
| | | | | 0 | 0 | 0 | – | – | – | – | – |
| **23** | **SW1-MODE** | R/W | 8'b0000_xxxx | – | – | SW1OMODE | – | SW1MODE[3:0] | | | |
| | | | | 0 | 0 | 0 | x | – | – | – | – |
| **24** | **SW1CONF** | R/W | 8'bxx00_0100 | – | SW1DVSSPEED | SW1PHASE[1:0] | | SW1FREQ[1:0] | | – | SW1ILIM |
| | | | | x | -1 | 0 | 0 | – | – | 0 | 0 |
| **32** | **SW1CONF** | R/W | 8'bx100_0100 | – | SW1DVSSPEED | SW1PHASE[1:0] | | SW1FREQ[1:0]- | | – | SW1ILIM |
| | | | | x | – | 0 | 0 | – | – | 0 | 0 |
| **35** | **SW2VOLT** | R/W | 8'b0xxx_0110 | – | – | – | – | SW2_HI | SW2[2:0] | | |
| | | | | 0 | x | x | x | – | – | – | — |
| **36** | **SW2STBY** | R/W | 8'b0xxx_xxxx | – | – | – | – | SW2_HI | SW2STBY[2:0] | | |
| | | | | 0 | x | x | x | – | – | – | — |
| **37** | **SW2OFF** | R/W | 8'b0xxx_xxxx | – | – | – | – | SW2_HI | SW2STBY[2:0] | | |
| | | | | 0 | x | x | x | – | – | – | — |
| **38** | **SW2-MODE** | R/W | 8'b0010_1000 | – | – | SW2OMODE | – | SW2MODE[3:0] | | | |
| | | | | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| **39** | **SW2CONF** | R/W | 8'bxx01_0100 | – | SW2DVS SPEED | SW2PHASE[1:0] | | SW2FREQ[1:0] | | – | SW2ILIM |
| | | | | x | – | 0 | 1 | – | – | 0 | 0 |
| **3C** | **SW3VOLT** | R/W | 8'b0xxx_1100 | – | – | – | – | SW3[3:0] | | | |
| | | | | 0 | x | x | x | – | – | – | – |
| **3D** | **SW3STBY** | R/W | 8'b0xxx_1100 | – | – | – | – | SW3STBY[3:0] | | | |
| | | | | 0 | x | x | x | – | – | – | – |
| **3E** | **SW3OFF** | R/W | 8'b0xxx_1100 | – | – | – | – | SW3OFF[3:0] | | | |
| | | | | 0 | x | x | x | – | – | – | – |

**Table 178. Functional page (continued)**

| | | | | BITS[7:0] | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Add** | **Register name** | **R/W** | **Default** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| 3F | SW3MODE | R/W | 8'b0011_1000 | – | – | SW3OMODE | – | SW3MODE[3:0] | | | |
| | | | | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 40 | SW3CONF | R/W | 8'bxx10_0100 | – | SW3DVS SPEED | SW3PHASE[1:0] | | SW3FREQ[1:0] | | – | SW3ILIM |
| | | | | x | – | 1 | 0 | – | – | 0 | 0 |
| 66 | SWBSTCTL | R/W | 8'b0xx0_10xx | – | SWBST1STBYMODE[1:0] | | – | SWBST1MODE[1:0] – | | SWBST1VOLT[1:0] | |
| | | | | 0 | – | – | 0 | – | – | – | – |
| 69 | LDOGCTL | R/W | 8'b0xxx_xxx0 | – | – | – | – | – | – | – | STBY_LP_B |
| | | | | 0 | x | x | x | x | x | x | x |
| 6A | REFOUTCTL | R/W | 8'b000x_0000 | – | – | – | REFOUTEN | – | – | – | – |
| | | | | 0 | 0 | 0 | – | 0 | 0 | 0 | 0 |
| 6B | VSNVSCTL | R/W | 8'b0000_0110 | – | – | – | – | – | VSNVSVOLT[2:0] | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 6C | LDO1CTL | R/W | 8'b010x_1110 | LDO1OMODE | LDO1LPWR | LDO1STBY | LDO1EN | LDO1[3:0] | | | |
| | | | | 0 | 0 | 0 | – | – | – | – | –– |
| 6D | LDO2CTL | R/W | 8'b000x_1000 | LDO2OMODE | LDO2LPWR | LDO2STBY | LDO2EN | LDO2[3:0] | | | |
| | | | | 0 | 0 | 0 | – | – | – | – | –– |
| 6E | VSDCTL | R/W | 8'b000x_xx10 | VSDOMODE | VSDLPWR | VSDSTBY | VSDEN | – | – | VSD[1:0] | |
| | | | | 0 | 0 | 0 | – | x | x | – | – |
| 6F | V33CTL | R/W | 8'b000x_xx10 | V33OMODE | V33LPWR | V33STBY | V33EN | – | – | V33[1:0] | |
| | | | | 0 | 0 | 0 | – | x | x | – | – |
| 70 | LDO3CTL | R/W | 8'b010x_0000 | LDO3OMODE | LDO3LPWR | LDO3STBY | LDO3EN | LDO3[3:0] | | | |
| | | | | 0 | 0 | 0 | – | – | – | – | – |
| 71 | LDO4CTL | R/W | 8'b000x_xxxx | LDO4OMODE | LDO4LPWR | LDO4STBY | LDO4EN | LDO4[3:0] | | | |
| | | | | 0 | 0 | 0 | – | – | – | – | – |
| 7F | Page Register | R/W | 8'b0000_0000 | – | – | – | PAGE[4:0] | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 179. Extended page 1**

| **Address** | **Register Name** | **TYPE** | **Default** | BITS[7:0] | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| 80 | OTP FUSE READ EN | R/W | 8'b000x_xxx0 | – | – | – | – | – | – | – | OTP FUSE READ EN |
| | | | | 0 | 0 | 0 | x | x | x | x | x |
| 84 | OTP LOAD MASK | R/W | 8'b0000_0000 | START | RL PWBRTN | FORCE PWRCTL | RL PWRCTL | RL OTP | RL OTP ECC | RL OTP FUSE | RL TRIM FUSE |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 8A | OTP ECC SE1 | R | 8'bxxx0_0000 | – | – | – | ECC5_SE | ECC4_SE | ECC3_SE | ECC2_SE | ECC1_SE |
| | | | | x | x | x | 0 | 0 | 0 | 0 | 0 |

**Table 179. Extended page 1 (continued)**

| Address | Register Name | TYPE | Default | BITS[7:0] | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 8B | RSVD | R | 8'bxxx0_0000 | | | | | | | | |
| | | | | | | | | | | | |
| 8C | OTP ECC DE1 | R | 8'bxxx0_0000 | – | – | – | ECC5_DE | ECC4_DE | ECC3_DE | ECC2_DE | ECC1_DE |
| | | | | x | x | x | 0 | 0 | 0 | 0 | 0 |
| 8D | RSVD | R | 8'bxxx0_0000 | | | | | | | | |
| | | | | | | | | | | | |
| A0 | OTP SW1 VOLT | R/W | 8'b00xx_xxxx | | | | OTP_SW1_VOLT[4:0] | | | | |
| | | | | x | x | x | x | x | x | x | x |
| A1 | OTP SW1 SEQ | | | | | | | | OTP_SW1_SEQ[2:0] | | |
| | | | | | | | | | | | |
| A2 | OTP SW1 CONFIG | R/W | 8'b000x_xxXx | – | – | – | – | OTP_SW1_CONFIG[1:0] | | OTP_SW1_FREQ[1:0] | |
| | | | | x | x | x | x | x | x | x | x |
| AA | RSVD | R/W | 8'b00xx_xxxx | | | | | | | | |
| | | | | x | x | x | x | x | x | x | x |
| AC | OTP SW2 VOLT | R/W | 8'b0xxx_xxxx | | | | | OTP_SW2_HI | OTP_SW2_VOLT[2:0] | | |
| | | | | x | x | x | x | x | x | x | x |
| AD | OTP SW2 SEQ | R/W | 8'b0xxx_xxxx | | | | | – | OTP_SW2_SEQ[2:0] | | |
| | | | | x | x | x | x | x | x | x | x |
| AE | OTP SW2 CONFIG | R/W | 8'b0000_00xx | – | – | – | – | – | – | OTP_SW2_FREQ[1:0] | |
| | | | | 0 | 0 | 0 | x | x | 0 | x | x |
| B0 | OTP SW3 VOLT | R/W | 8'b0xxx_xxxx | | | | – | OTP_SW3_VOLT[3:0] | | | |
| | | | | x | x | x | x | x | x | x | x |
| B1 | OTP SW3 SEQ | R/W | 8'b0xxx_xxxx | | | | | – | OTP_SW3_SEQ[2:0] | | |
| | | | | x | x | x | x | x | x | x | x |
| B2 | OTP SW3 CONFIG | R/W | 8'b0xxx_xxxx | | | | – | | | OTP_SW3_FREQ[1:0] | |
| | | | | x | x | x | x | x | x | x | x |
| BC | OTP SWBST VOLT | R/W | 8'b0000_00xx | – | – | – | – | – | – | OTP_SWBST_VOLT[1:0] | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BD | OTP SWBST SEQ | R/W | 8'b0000_xxxx | – | – | – | – | – | OTP_SWBST_SEQ[2:0] | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| C0 | OTP VSNVS VOLT | R/W | 8'b0000_0xxx | – | – | – | – | – | OTP_VSNVS_VOLT[2:0] | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| C4 | RSVD | R/W | 8'b000x_x0xx | – | – | – | – | – | – | – | – |
| | | | | 0 | 0 | 0 | x | x | x | x | x |
| C8 | OTP LDO1 VOLT | R/W | 8'b0000_xxxx | | | | | OTP_LDO1_VOLT[3:0] | | | |
| | | | | 0 | 0 | 0 | 0 | x | x | x | x |
| C9 | OTP LDO1 SEQ | R/W | 8'b0000_xxxx | | | | | OTP_LDO1_SEQ[3:0] | | | |
| | | | | 0 | 0 | 0 | 0 | x | x | x | x |

**Table 179. Extended page 1 (continued)**

| Address | Register Name | TYPE | Default | BITS[7:0] | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CC | OTP LDO2 VOLT | R/W | 8'b0000_xxxx | | | | | OTP_LDO2_VOLT[3:0] | | | |
| | | | | 0 | 0 | 0 | 0 | x | x | x | x |
| CD | OTP LDO2 SEQ | R/W | 8'b0000_xxxx | | | | | OTP_LDO2_SEQ[3:0] | | | |
| | | | | 0 | 0 | 0 | 0 | x | x | x | x |
| D0 | OTP VSD VOLT | R/W | 8'b0000_xxxx | | | | | – | | OTP_VSD_VOLT[2:0] | |
| | | | | 0 | 0 | 0 | 0 | x | x | x | x |
| D1 | OTP VSD SEQ | R/W | 8'b0000_xxxx | | | | | | OTP_VSD_SEQ[2:0] | | |
| | | | | 0 | 0 | 0 | 0 | 0 | x | x | x |
| D4 | OTP V33 VOLT | R/W | 8'b0000_xxxx | | | | | | | OTP_V33_VOLT[2:0] | |
| | | | | 0 | 0 | 0 | 0 | x | x | x | x |
| D5 | OTP V33 SEQ | R/W | 8'b0000_xxxx | | | | | | OTP_V33_SEQ[3:0] | | |
| | | | | 0 | 0 | 0 | 0 | x | x | x | x |
| D8 | OTP LDO3 VOLT | R/W | 8'b0000_xxxx | | | | | OTP_LDO3_VOLT[3:0] | | | |
| | | | | 0 | 0 | 0 | 0 | x | x | x | x |
| D9 | OTP LDO3 SEQ | R/W | 8'b0000_xxxx | | | | | OTP_LDO3_SEQ[3:0] | | | |
| | | | | 0 | 0 | 0 | 0 | x | x | x | x |
| DC | OTP LDO4 VOLT | R/W | 8'b0000_xxxx | | | | | OTP_LDO4_VOLT[3:0] | | | |
| | | | | 0 | 0 | 0 | 0 | x | x | x | x |
| DD | OTP LDO4 SEQ | R/W | 8'b0000_xxxx | | | | | OTP_LDO4_SEQ[3:0] | | | |
| | | | | 0 | 0 | 0 | 0 | x | x | x | x |
| E0 | OTP PU CONFIG1 | R/W | 8'b000x_xxxx | | | | OTP_EN_CFG | | OTP_SWDVS_CLK | | OTP_SEQ_CLK_SPEED |
| | | | | x | x | x | x | x | x | x | x |
| E4 | OTP FUSE POR1 | R/W | 8'b0000_00x0 | TBB_POR | – | – | – | – | – | – | – |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | x | 0 |
| E5 | RSVD | R/W | 8'b0000_00x0 | – | – | – | – | – | – | | – |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | | 0 |
| E6 | RSVD | R/W | 8'b0000_00x0 | – | – | – | – | – | – | | – |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | | 0 |
| E7 | RSVD | R | 8'b0000_00x0 | – | – | – | – | – | – | | – |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | | 0 |
| E8 | OTP PWRGD EN | R/W/M | 8'b0000_000x | – | – | – | – | – | – | – | OTP_PG_EN |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | x | 0 |
| F0 | RSVD | R/W | 8'b000x_xxxx | – | – | – | | | | | |
| | | | | 0 | 0 | 0 | x | x | x | x | x |
| F1 | RSVD | R/W | 8'b000x_xxxx | – | – | – | | | | | |
| | | | | 0 | 0 | 0 | x | x | x | x | x |

**Table 179. Extended page 1 (continued)**

| Address | Register Name | TYPE | Default | BITS[7:0] | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| F7 | OTP BLOWN | R/W | 8'b0000_000x | – | – | – | – | – | – | – | OTP_BLOWN |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | x |
| FF | OTP I2C ADDR | R/W | 8'b0000_1xxx | USE_DEFAULT_ADD | | – | | I2C_SLV ADDR[3] | OTP_I2C_SLV ADDR[2:0] | | |
| | | | | 0 | 0 | 0 | 0 | 1 | x | x | x |

**Table 180. Extended page 2**

| Address | Register Name | TYPE | Default | BITS[7:0] | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 81 | SW1 PWRSTG | R/W | 8'b1111_1111 | RSVD | RSVD | RSVD | RSVD | RSVD | SW1_PWRSTG[2:0] | | |
| | | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 83 | SW1 PWRSTG | R | 8'b1111_1111 | RSVD | RSVD | RSVD | RSVD | RSVD | SW1_PWRSTG[2:0] RSVD | | |
| | | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 84 | SW2 PWRSTG | R | 8'b1111_1111 | RSVD | RSVD | RSVD | RSVD | RSVD | SW2_PWRSTG[2:0] RSVD | | |
| | | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 85 | SW3 PWRSTG | R | 8'b1111_1111 | RSVD | RSVD | RSVD | RSVD | RSVD | SW3_PWRSTG[2:0] RSVD | | |
| | | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 88 | PWRCTRL OTP CTRL | R | 8'b0000_0001 | – | – | – | – | – | – | OTP_PWRGD_EN | PG_SHDWN_EN |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 8D | I2C WRITE ADDRESS TRAP | R/W | 8'b0000_0000 | I2C_WRITE_ADDRESS_TRAP[7:0] | | | | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 8E | I2C TRAP PAGE | R/W | 8'b0000_0000 | LET_IT_ROLL | RSVD | RSVD | I2C_TRAP_PAGE[4:0] | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 8F | I2C TRAP CNTR | R/W | 8'b0000_0000 | I2C_WRITE_ADDRESS_COUNTER[7:0] | | | | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 90 | IO DRV | R/W | 8'b00xx_xxxx | SDA_DRV[1:0] | | RSVD | | INTB_DRV[1:0] | | PORBMCU_DRV[1:0] | |
| | | | | 0 | 0 | x | x | x | x | x | x |
| D0 | OTP AUTO ECC0 | R/W | 8'b0000_0000 | – | – | – | AUTO_ECC_BANK5 | AUTO_ECC_BANK4 | AUTO_ECC_BANK3 | AUTO_ECC_BANK2 | AUTO_ECC_BANK1 |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D8 | Reserved | – | 8'b0000_0000 | AUTO_BLOW_TIME[7:0] | | | | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D9 | Reserved | – | 8'b0000_0000 | START | RELOAD | EN_RW | AUTO_FUSE_BLOW5 | AUTO_FUSE_BLOW4 | AUTO_FUSE_BLOW3 | AUTO_FUSE_BLOW2 | AUTO_FUSE_BLOW1 |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| E1 | OTP ECC CTRL1 | R/W | 8'b0000_0000 | RSVD | ECC1_CALC_CIN | ECC1_CIN_TBB[5:0] | | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| E2 | OTP ECC CTRL2 | R/W | 8'b0000_0000 | RSVD | ECC2_CALC_CIN | ECC2_CIN_TBB[5:0] | | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| E3 | OTP ECC CTRL3 | R/W | 8'b0000_0000 | RSVD | ECC3_CALC_CIN | ECC3_CIN_TBB[5:0] | | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| E4 | OTP ECC CTRL4 | R/W | 8'b0000_0000 | RSVD | ECC4_CALC_CIN | ECC4_CIN_TBB[5:0] | | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 180. Extended page 2 (continued)**

| Address | Register Name | TYPE | Default | BITS[7:0] | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| E5 | OTP ECC CTRL5 | R/W | 8'b0000_0000 | RSVD | ECC5_CALC_CIN | ECC5_CIN_TBB[5:0] | | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| F1 | OTP FUSE CTRL1 | R/W | 8'b0000_0000 | – | – | – | – | ANTIFUSE1_EN | ANTIFUSE1_LOAD | ANTIFUSE1_RW | BYPASS1 |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| F2 | OTP FUSE CTRL2 | R/W | 8'b0000_0000 | – | – | – | – | ANTIFUSE2_EN | ANTIFUSE2_LOAD | ANTIFUSE2_RW | BYPASS2 |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| F3 | OTP FUSE CTRL3 | R/W | 8'b0000_0000 | – | – | – | – | ANTIFUSE3_EN | ANTIFUSE3_LOAD | ANTIFUSE3_RW | BYPASS3 |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| F4 | OTP FUSE CTRL4 | R/W | 8'b0000_0000 | – | – | – | – | ANTIFUSE4_EN | ANTIFUSE4_LOAD | ANTIFUSE4_RW | BYPASS4 |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| F5 | OTP FUSE CTRL5 | R/W | 8'b0000_0000 | – | – | – | – | ANTIFUSE5_EN | ANTIFUSE5_LOAD | ANTIFUSE5_RW | BYPASS5 |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

# 7 Typical applications

## 7.1 Application diagram

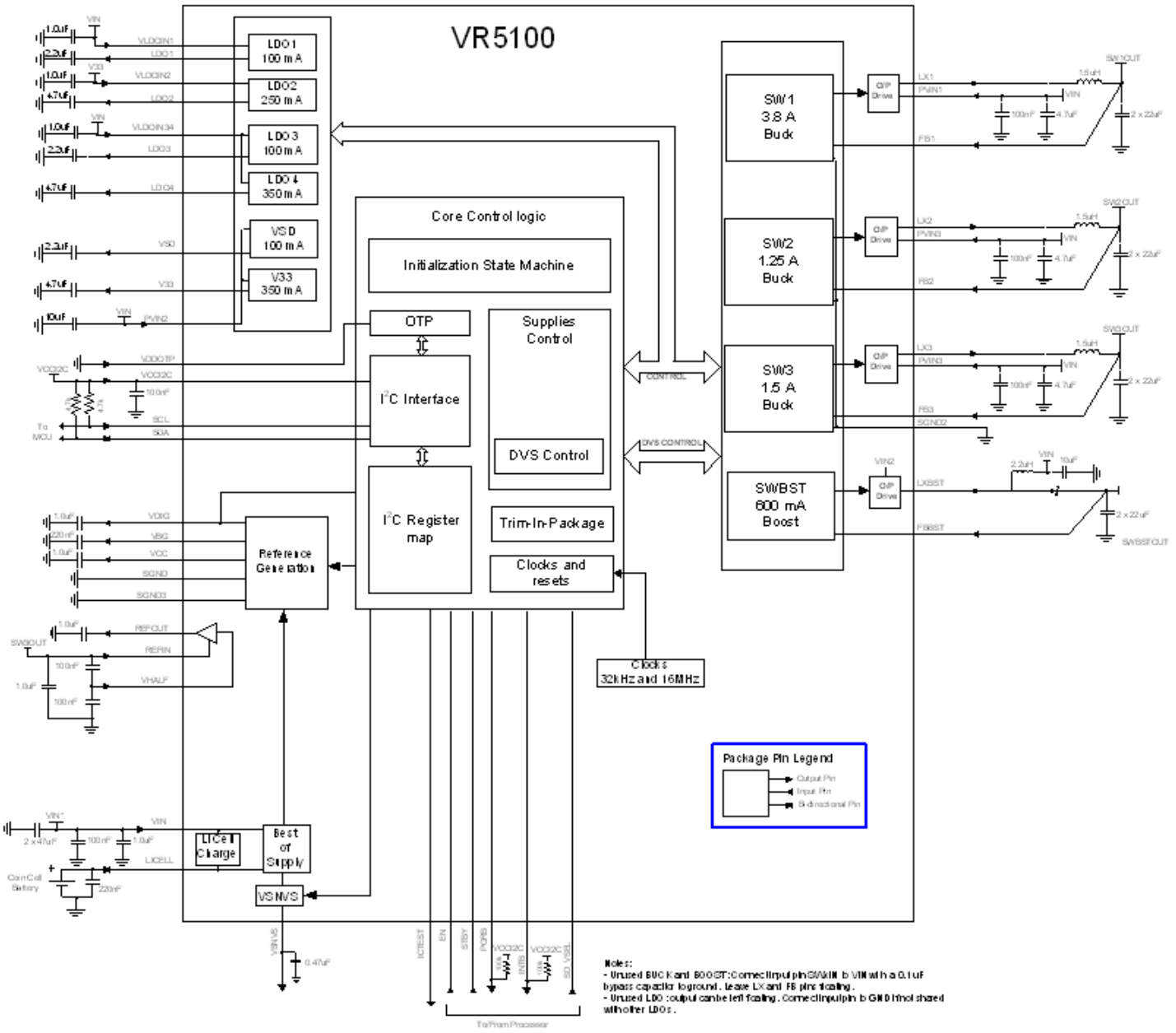



**Figure 37. Typical application schematic**

# 8 Bill of materials

The following table provides a complete list of the recommended components on a full featured system using the VR5100 device for -40 °C to 85 °C applications. Components are provided with an example part number; equivalent components may be used.

**Table 181. Bill of material for -40 °C to 85 °C applications**

| Value | Qty | Description | Part# | Manufacturer | Component/Pin |
|---|---|---|---|---|---|
| **PMIC** | | | | | |
| N/A | 1 | Power management IC | VR5100 | NXP | IC |
| **Buck regulators** | | | | | |
| 1.5 µH | 4 | IND PWR 1.5 uH at 1.0 MHz 7.1 A 20% 2016 | XAL4020-152ME | Coilcraft | SW1 inductor |
| | | IND PWR 1.5 uH at 1.0 MHz 2.6 A 20% 2016 | LPS4012-152MR | Coilcraft | SW2 and SW3 inductors |
| 4.7 µF | 4 | CAP CER 4.7 µF 10 V 20% X5R 0402 | GRM155R61A475MEAA | Murata | SW1, SW2, SW3 input capacitors |
| 0.1 µF | 4 | CAP CER 0.1 µF 10 V 20% X5R 0201 | GRM033R61A104ME84 | Murata | SW1, SW2, SW3 input capacitors (optional) |
| 22 µF | 8 | CAP CER 22 µF 10 V 20% X5R 0603 | GRM188R61A226ME15 | Murata | SW1, SW2, SW3 output capacitors |
| **Boost regulator** | | | | | |
| 2.2 µH | 1 | IND PWR 2.2 µH at 1.0 MHz 2.4 A 20% 2016 | DFE201610E-2R2M | TOKO INC. | SWBST inductor |
| | | IND PWR 2.2 µH at 1.0 MHz 1.85 A 20% 1210 | BRL3225T2R2M | Taiyo Yuden | Alternate for low power applications |
| 10 µF | 1 | CAP CER 10 µF 10 V 20% X5R 0402 | GRM155R61A106ME11 | Murata | SWBST input capacitor |
| N/A | 1 | DIODE SCH PWR RECT 1.0 A 20 V SMT | MBR120LSFT3G | ON Semi | SWBST diode |
| 22 µF | 2 | CAP CER 22 µF 10 V 20% X5R 0603 | GRM188R61A226ME15D | Murata | SWBST output capacitors |
| **Linear regulators** | | | | | |
| 1.0 µF | 3 | CAP CER 1.0 µF 10 V 20% X5R 0201 | GRM033R61A105ME44 | Murata | LDO1, LDO2, LDO3 and LDO4 input capacitors |
| 2.2 µF | 3 | CAP CER 2.2 µF 10 V 20% X5R 0201 | GRM033R61A225ME47 | Murata | LDO1, LDO3, VSD output capacitors |
| 10 µF | 1 | CAP CER 10 µF 10 V 20% X5R 0402 | GRM155R61A106ME11 | Murata | V33 and VSD input capacitor |
| 4.7 µF | 3 | CAP CER 4.7 µF 10 V 20% X5R 0402 | GRM155R61A475MEAA | Murata | LDO2, LDO4, V33 output capacitors |
| **Miscellaneous** | | | | | |
| 1.0 µF | 4 | CAP CER 1.0 µF 10 V 20% X5R 0201 | GRM033R61A105ME44 | Murata | VCC, VBG, REFOUT, VINREFOUT capacitors |
| 0.22 µF | 2 | CAP CER 0.22 µF 10 V 20% X5R 0201 | GRM033R61A224ME90 | Murata | VDIG and coin cell output capacitors |
| 0.47 µF | 1 | CAP CER 0.47 µF 10 V 20% X5R 0201 | GRM033R61A474ME90 | Murata | VSNVS output capacitor |
| 2.2 µF | 1 | CAP CER 2.2 µF 10 V 20% X5R 0201 | GRM033R61A225ME47 | Murata | VIN input capacitor when not using Front-end LDO |

**Table 181. Bill of material for -40 °C to 85 °C applications (continued)**

| Value | Qty | Description | Part# | Manufacturer | Component/Pin |
|---|---|---|---|---|---|
| 0.1 µF | 5 | CAP CER 0.1 µF 10 V 10% X5R 0201 | GRM033R61A104KE84 | Murata | VCCI2C, VIN input capacitors |
| 100 k | 2 | RES MF 100 k 1/16 W 1% 0402 | RC0402FR-07100KL | YAGEO AMERICA | Pull-up resistors |
| 4.7 k | 2 | RES MF 4.70 k 1/20 W 1% 0201 | RC0201FR-074K7L | YAGEO AMERICA | I²C Pull-up resistors |

The following table provides a complete list of the recommended components on a full featured system using the VR5100 Device for -40 °C to 105 °C applications. Components are provided with an example part number, equivalent components may be used.

**Table 182. Bill of material for -40 °C to 105 °C applications**

| Value | Qty | Description | Part# | Manufacturer | Component/Pin |
|---|---|---|---|---|---|
| **PMIC** | | | | | |
| N/A | 1 | Power management IC | VR5100 | NXP | IC |
| **Buck regulators** | | | | | |
| 1.5 µH | 4 | IND PWR 1.5 µH at 1.0 MHz 2.9 A 20% 2016 | DFE201610E-1R5M | TOKO INC. | SW1, SW2, SW3 inductors |
| | | IND PWR 1.5 µH at 1.0 MHz 2.2 A 20% 1210 | BRL3225T1R5M | Taiyo Yuden | Alternate for low-power applications |
| 4.7 µF | 4 | CAP CER 4.7 µF 10 V 10% X7S 0603 | GRM188C71A475KE11 | Murata | SW1, SW2, SW3 input capacitors |
| 0.1 µF | 4 | CAP CER 0.1 µF 10 V 10% X7S 0201 | GRM033C71A104KE14 | Murata | SW1, SW2, SW3 input capacitors (optional) |
| 22 µF | 8 | CAP CER 22 µF 10 V 20% X7T 0805 | GRM21BD71A226ME44 | Murata | SW1, SW2, SW3 output capacitors |
| **Boost regulator** | | | | | |
| 2.2 µH | 1 | IND PWR 2.2 µH at 1.0 MHz 2.4 A 20% 2016 | DFE201610E-2R2M | TOKO INC. | SWBST inductor |
| | | IND PWR 2.2 µH at 1.0 MHz 1.85 A 20% 1210 | BRL3225T2R2M | Taiyo Yuden | Alternate for low-power applications |
| 10 µF | 1 | CAP CER 10 µF 10 V 20% X7T 0603 | GRM188D71A106MA73 | Murata | SWBST input capacitor |
| N/A | 1 | DIODE SCH PWR RECT 1.0 A 20 V SMT | MBR120LSFT3G | ON Semi | SWBST diode |
| 22 µF | 2 | CAP CER 22 µF 10 V 20% X5R 0603 | GRM188R61A226ME15D | Murata | SWBST output capacitors |
| **Linear regulators** | | | | | |
| 1.0 µF | 3 | CAP CER 1.0 µF 10 V 10% X7S 0402 | GRM155C71A105KE11 | Murata | LDO1, LDO2, LDO3 and LDO4 input capacitors |
| 2.2 µF | 3 | CAP CER 2.2 µF 10 V 10% X7S 0402 | GRM155C71A225KE11 | Murata | LDO1, LDO3, VSD output capacitors |
| 10 µF | 1 | CAP CER 10 µF 10 V 20% X7T 0603 | GRM188D71A106MA73 | Murata | V33 and VSD input capacitor |
| 4.7 µF | 3 | CAP CER 4.7 µF 10 V 10% X7S 0603 | GRM188C71A475KE11 | Murata | LDO2, LDO4, V33 output capacitors |
| **Miscellaneous** | | | | | |
| 1.0 µF | 4 | CAP CER 1.0 µF 10 V 10% X7R 0402 | GRM155C71A105KE11 | Murata | VCC, VDIG, REFOUT, VINREFOUT capacitors |
| 0.22 µF | 2 | CAP CER 0.22 µF 10 V 10% X7R 0402 | GRM155R71A224KE01 | Murata | VBG and coin cell output capacitors |

**Table 182. Bill of material for -40 °C to 105 °C applications (continued)**

| Value | Qty | Description | Part# | Manufacturer | Component/Pin |
|---|---|---|---|---|---|
| 0.47 µF | 1 | CAP CER 0.47 µF 10 V 20% X5R 0201 | GRM155R71A474KE01 | Murata | VSNVS output capacitor |
| 2.2 µF | 1 | CAP CER 2.2 µF 10 V 10% X7S 0402 | GRM155C71A225KE11 | Murata | VIN input capacitor |
| 0.1 µF | 5 | CAP CER 0.1 µF 10 V 10% X7S 0201 | GRM033C71A104KE14 | Murata | VCCI2C, VHALF, VIN input capacitors |
| 100 k | 2 | RES MF 100 k 1/16 W 1% 0402 | RC0402FR-07100KL | YAGEO AMERICA | Pull-up resistors |
| 4.7 k | 2 | RES MF 4.70 K 1/20 W 1% 0201 | RC0201FR-074K7L | YAGEO AMERICA | I²C pull-up resistors |

# 9 Thermal information

## 9.1 Rating data

The thermal rating data of the packages has been simulated with the results listed in Thermal ratings. Junction to Ambient Thermal Resistance Nomenclature: the JEDEC specification reserves the symbol $R_{\theta JA}$ or θJA (Theta-JA) strictly for junction-to-ambient thermal resistance on a 1s test board in natural convection environment. $R_{\theta JMA}$ or θJMA (Theta-JMA) is used for both junction-to-ambient on a 2s2p test board in natural convection and for junction-to-ambient with forced convection on both 1s and 2s2p test boards. It is anticipated the generic name, Theta-JA, continues to be commonly used. The JEDEC standards can be consulted at http://www.jedec.org.

## 9.2 Estimation of junction temperature

An estimation of the chip junction temperature $T_J$ can be obtained from the equation:

$T_J = T_A + (R_{\theta JA} \times P_D)$

with:

$T_A$ = Ambient temperature for the package in °C

$R_{\theta JA}$ = Junction to ambient thermal resistance in °C/W

$P_D$ = Power dissipation in the package in W

The junction to ambient thermal resistance is an industry standard value providing a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board $R_{\theta JA}$ and the value obtained on a four layer board $R_{\theta JMA}$. Actual application PCBs show a performance close to the simulated four layer board value, although this may be somewhat degraded in case of significant power dissipated by other components placed close to the device.

At a known board temperature, the junction temperature $T_J$ is estimated using the following equation

$T_J = T_B + (R_{\theta JB} \times P_D)$ with

$T_B$ = Board temperature at the package perimeter in °C

$R_{\theta JB}$ = Junction to board thermal resistance in °C/W

$P_D$ = Power dissipation in the package in W

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made.

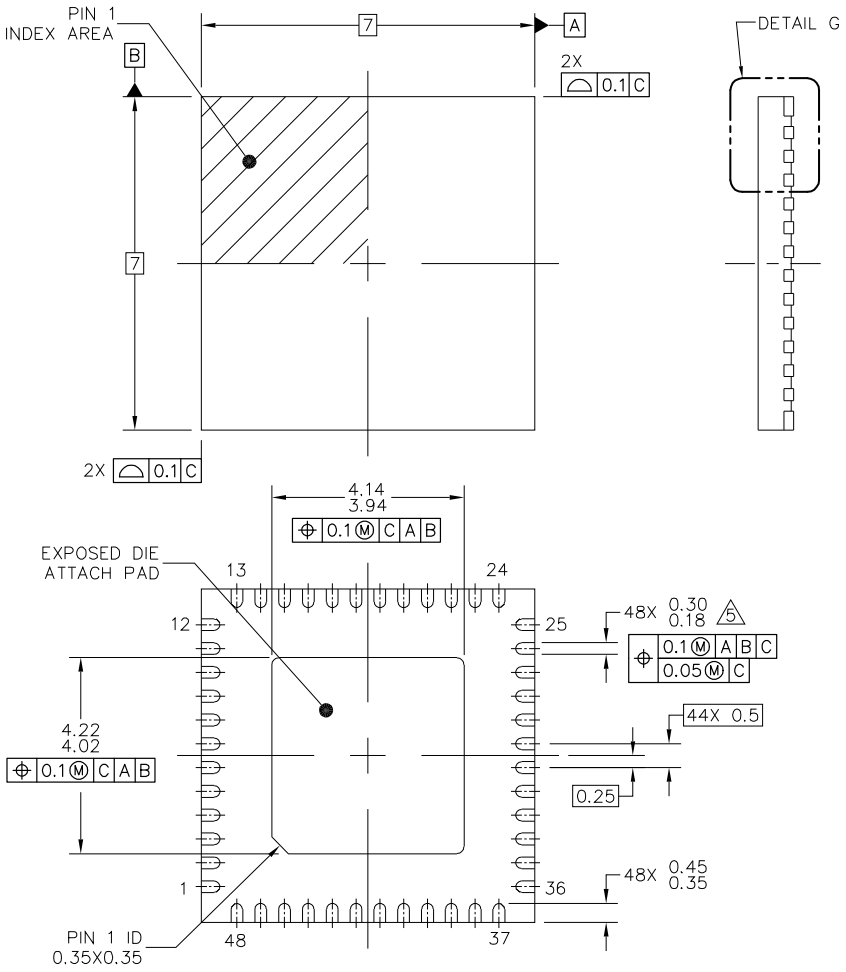
# 10 Packaging

## 10.1 Packaging dimensions

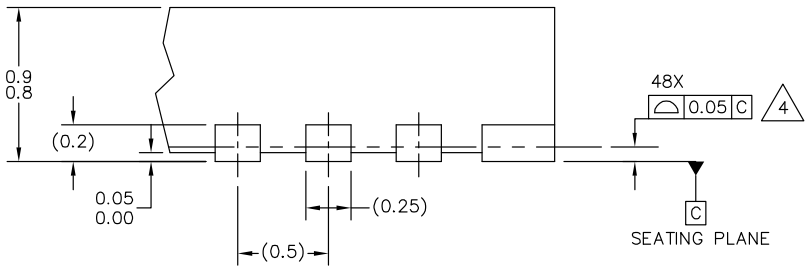
Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number. See the Thermal characteristics section for specific thermal characteristics for each package.

**Table 183. Package drawing information**

| Package | Suffix | Package outline drawing number |
|---|---|---|
| 48-pin QFN 7X7 mm - 0.5 mm pitch | EP | 98ASA00719D |




| © FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. | MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE |
|---|---|---|
| TITLE: QFN, THERMALLY ENHANCED, 7 X 7 X 0.85, 0.5 PITCH, 48 TERMINAL | DOCUMENT NO: 98ASA00719D | REV: B |
| | STANDARD: NON-JEDEC | |
| | 27 JUN 2014 | |




DETAIL G
VIEW ROTATED 90°CW

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|---|---|---|
| TITLE: QFN, THERMALLY ENHANCED, 7 X 7 X 0.85, 0.5 PITCH, 48 TERMINAL | DOCUMENT NO: 98ASA00719D | REV: B |
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NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THIS IS A NON–JEDEC REGISTERED PACKAGE.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.
5. DIMENSION APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.3 MM FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

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| | 27 JUN 2014 |

# 11 Revision history

| Revision | Date | Description of changes |
|---|---|---|
| 1.0 | 12/2015 | • Initial release |
| 2.0 | 2/2016 | • Relabeled REFDDR as REFOUT<br>• Updated form and style |
| 3.0 | 2/2016 | • VLDOIN34 max. voltage updated to 3.6 V |
| 4.0 | 2/2017 | • Replaced Figure 1<br>• Removed PC34VR5100A2EP from Table 1<br>• Corrected Figure 4<br>• Removed A2 column from Table 37<br>• Updated Figure 25<br>• Corrected title for Figure 26<br>• Changed PC parts to MC in Table 1<br>• Updated Table 73 (changed default values to 1 for bits [5:0]) |
| 5.0 | 12/2018 | • Added MC34VR5100A2EP to Table 1<br>• Added A2 and its values in Table 37 |

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