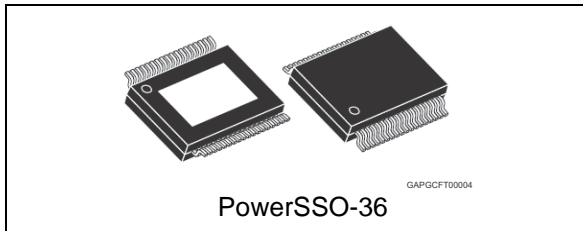


## Advanced power management system IC with embedded LIN and high speed CAN transceiver supporting CAN Partial Networking

Datasheet – production data



- 5 fully protected high-side drivers with internal 4-channel PWM generator
- 2 low-side drivers with active Zener clamping
- 4 Internal PWM timers
- 2 operational amplifiers with rail-to-rail outputs ( $V_S$ ) and low voltage inputs
- Temperature warning and thermal shutdown

### Features

- Two 5 V voltage regulators for microcontroller and peripheral supply
- No electrolytic capacitor required on regulator outputs
- Ultra low quiescent current in standby modes
- Programmable reset generator for power-on and undervoltage
- Configurable window watchdog and fail safe output
- LIN 2.1 compliant (SAEJ2602 compatible) transceiver
- Advanced high speed CAN transceiver (ISO 11898-2/-5 and SAE J2284 compliant) with local failure and bus failure diagnosis and selective wake-up functionality according to ISO 11898-6
- Complete 3 channel contact monitoring interface with programmable cyclic sense functionality
- Programmable periodic system wake-up feature
- ST SPI interface for mode control and diagnosis

### Applications

- Automotive ECU's such as door zone and body control modules description

### Description

The L99PM72GXP is a power management system IC providing electronic control units with enhanced system power supply functionality including various standby modes as well as LIN and HS CAN physical communication layers. It contains two low drop voltage regulators to supply the system microcontroller and external peripheral loads such as sensors and provides enhanced system standby functionality with programmable local and remote wake up capability.

In addition, five high-side drivers, two low-side drivers and two operational amplifiers increase the system integration level.

The ST standard SPI Interface (3.0) allows control and diagnosis of the device and enables generic software development.

**Table 1. Device summary**

| Package     | Order code |               |
|-------------|------------|---------------|
|             | Tube       | Tape and reel |
| PowerSSO-36 | L99PM72GXP | L99PM72GXPTR  |

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# 1 Block diagram and pin description

Figure 1. Block diagram

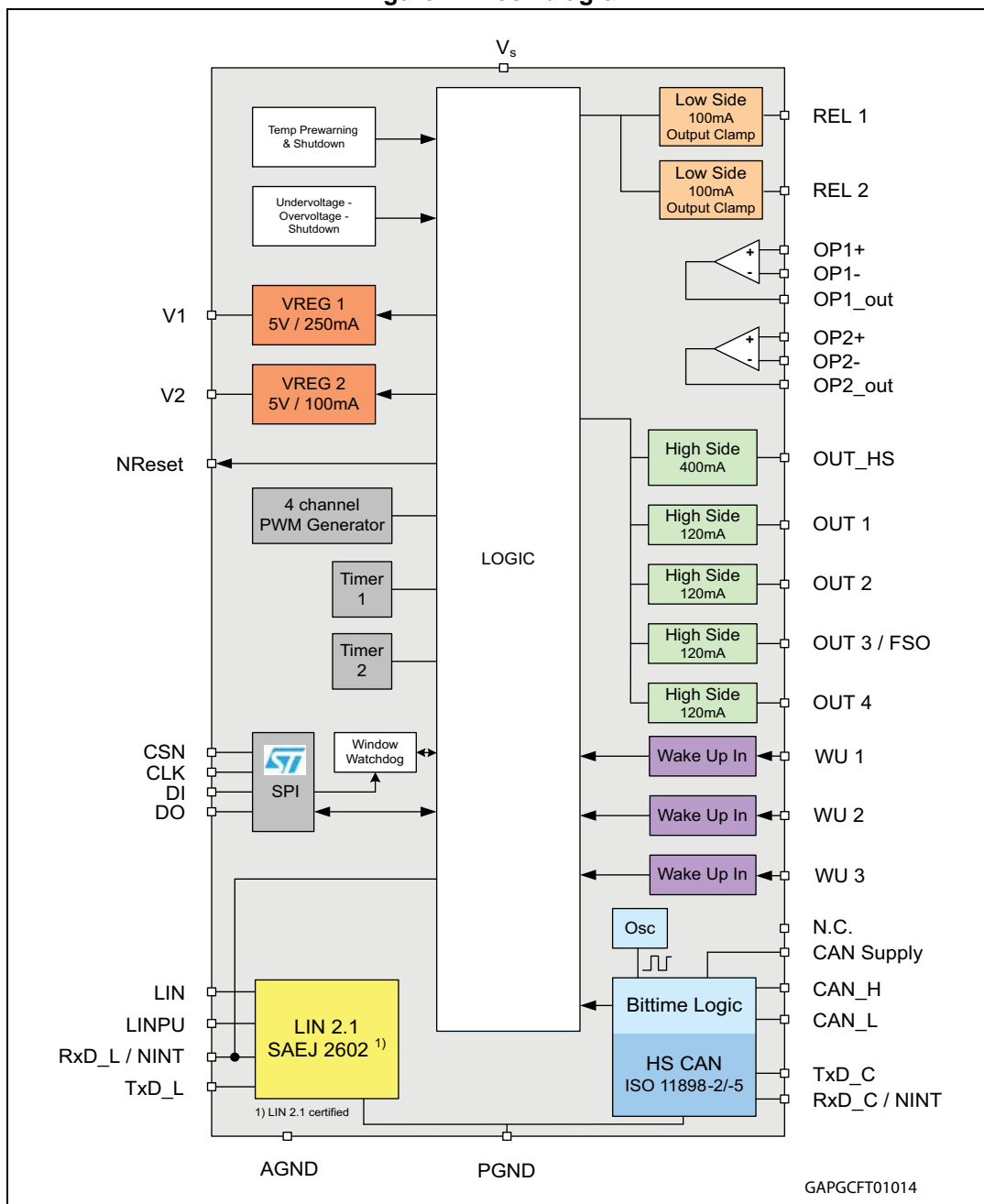


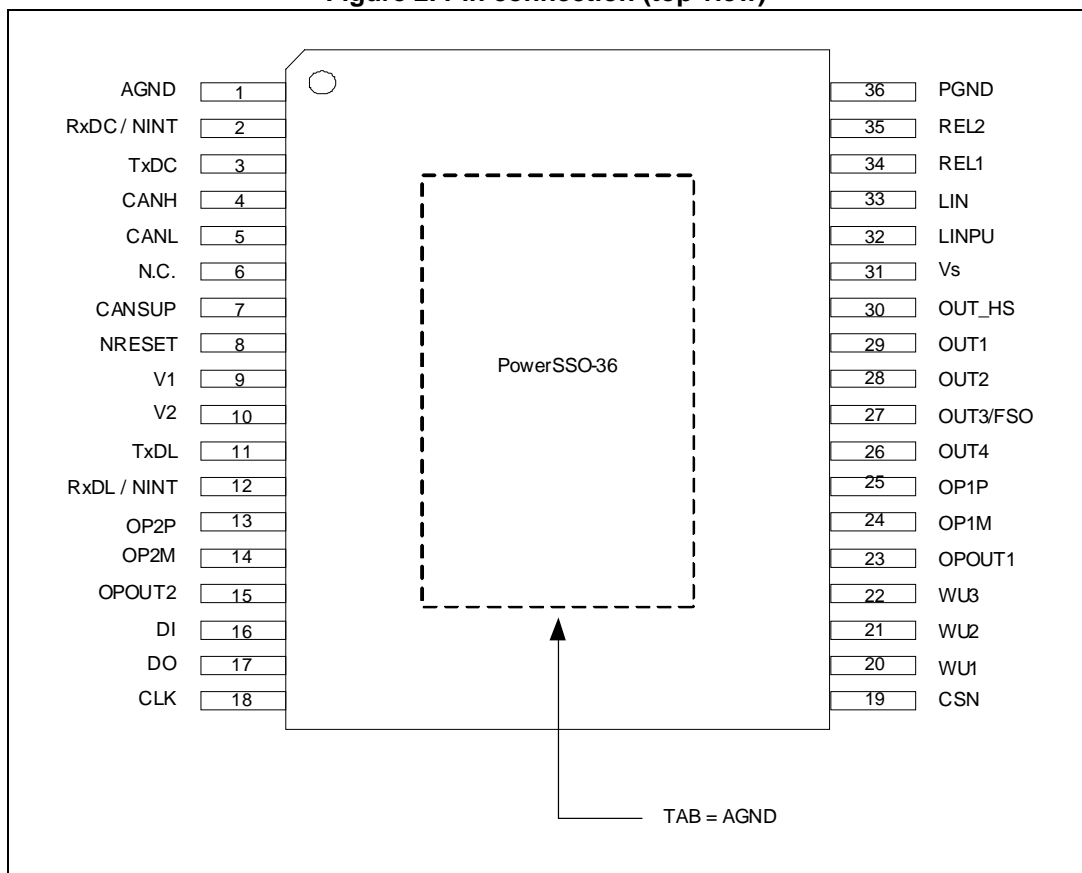
Table 2. Pin definitions and functions

| Pin     | Symbol    | Function  |
|---------|-----------|---|
| 1       | AGND      | Analog ground   |
| 2       | RxDC/NINT | RxDC -> CAN receive data output<br>NINT -> indicates remote CAN wake-up events in Active Mode (transceiver in TRX_STBY; CAN_ACT = 0)                                    |
| 3       | TxDC      | CAN transmit data Input   |
| 4       | CANH      | CAN high level voltage I/O  |
| 5       | CANL      | CAN low level voltage I/O   |
| 6       | N.C.      | TBC   |
| 7       | CANSUP    | CAN supply input; to allow external CAN supply from V <sub>1</sub> or V <sub>2</sub> regulator.   |
| 8       | NRESET    | NRESET output to microcontroller; Internal pull-up of typ. 100 K $\Omega$ (reset state = LOW)   |
| 9       | V1        | Voltage regulator 1 output: 5 V supply e.g. micro controller, CAN transceiver   |
| 10      | V2        | Voltage regulator 2 output: 5 V supply for external loads (IR receiver, potentiometer, sensors) or CAN transceiver. V <sub>2</sub> is protected against reverse supply. |
| 11      | TxDL      | LIN transmit data input   |
| 12      | RxDL/NINT | RxDL -> LIN receive data output<br>NINT -> indicates local/remote wake-up events except CAN wake-up in Active Mode provides a programmable timer interrupt signal       |
| 13      | OP2+      | Non inverting input of operational amplifier 2  |
| 14      | OP2-      | Inverting input of operational amplifier 2  |
| 15      | OP2_OUT   | Output of operational amplifier 2   |
| 16      | DI        | SPI: serial data input  |
| 17      | DO        | SPI: serial data output   |
| 18      | CLK       | SPI: serial clock input   |
| 19      | CSN       | SPI: chip select not input  |
| 20...22 | WU1...3   | Wake-up Inputs 1...3: Input pins for static or cyclic monitoring of external contacts   |
| 23      | OP1_OUT   | Output of operational amplifier 1   |
| 24      | OP1-      | Inverting input of operational amplifier 1  |
| 25      | OP1+      | Non inverting input of operational amplifier 1  |
| 26      | OUT4      | High side driver output (7 $\Omega$ , typ)  |
| 27      | OUT3/FSO  | Configurable as:<br>– High-side driver output (7 $\Omega$ , typ)<br>– Fail safe output pin (default)  |
| 28      | OUT2      | High side driver output (7 $\Omega$ , typ)  |
| 29      | OUT1      | High side driver output (7 $\Omega$ , typ)  |
| 30      | OUT_HS    | High side driver (1 $\Omega$ , typ)   |

Table 2. Pin definitions and functions (continued)

| Pin | Symbol         | Function   |
|-----|----------------|--|
| 31  | V <sub>S</sub> | Power supply voltage   |
| 32  | LINPU          | High side driver output to switch off LIN master pull up resistor          |
| 33  | LIN            | LIN bus line   |
| 34  | REL1           | Low side driver output (2 Ω typ)   |
| 35  | REL2           | Low side driver output (2 Ω typ)   |
| 36  | PGND           | Power ground (REL1/2, LIN and CAN GND), to be connected to AGND externally |

Figure 2. Pin connection (top view)



## 2 Detailed description

### 2.1 Voltage regulators

The L99PM72GXP contains two independent and fully protected low drop voltage regulators, which are designed for very fast transient response and do not require electrolytic output capacitors for stability.

The output voltage is stable with ceramic load capacitors  $\geq 220$  nF.

#### 2.1.1 Voltage regulator: $V_1$

The  $V_1$  voltage regulator provides 5 V supply voltage and up to 250 mA continuous load current and is mainly intended for supply of the system microcontroller. The  $V_1$  regulator is embedded in the power management and Fail\_safe functionality of the device and operates according to the selected operating mode.

It can be used to supply the internal HS CAN Transceiver via the CANSUP pin externally. In case of a short circuit condition on the CAN bus, the output current of the transmitter is limited to 100 mA and the transceiver is turned off in order to ensure continued supply of the microcontroller.

In addition the regulator  $V_1$  drives the L99PM72GXP internal 5 V loads. The voltage regulator is protected against overload and overtemperature. An external reverse current protection has to be provided by the application circuitry to prevent the input capacitor from being discharged by negative transients or low input voltage. Current limitation of the regulator ensures fast charge of external bypass capacitors. The output voltage is stable for ceramic load capacitors  $\geq 220$  nF.

If the device temperature exceeds the TSD1 threshold, all outputs (OUTx, RELx, V2, LIN) are deactivated except  $V_1$ . Hence the micro controller has the possibility for interaction or error logging. In case of exceeding TSD2 threshold ( $TSD2 > TSD1$ ), also  $V_1$  is deactivated (see [Figure 23: Thermal shutdown protection and diagnosis](#)). A timer is started and the voltage regulator is deactivated for  $t_{TSD} = 1$  sec. During this time, all other wakeup sources (CAN, LIN, WU1...3 and wake up of  $\mu C$  by timer) are disabled. After 1 sec, the voltage regulator tries to restart automatically. If the restart fails 7 times, within one minute, without clearing and thermal shutdown condition still exists, the L99PM72GXP enters the Forced  $V_{Bat\_standby}$  Mode.

In case of short to GND at " $V_1$ " after initial turn on ( $V_1 < 2$  V for  $t > t_{V1\_short}$ ) the L99PM72GXP enters the Forced  $V_{Bat\_standby}$  Mode. Reactivation (wake-up) of the device can be achieved with signals from CAN, LIN, WU1..3 or periodic wake by timer.

#### 2.1.2 Voltage regulator: $V_2$

The voltage regulator  $V_2$  can supply additional 5 V loads (e.g. logic components or the integrated HS CAN transceiver or external loads such as sensors or potentiometers). The maximum continuous load current is 100 mA. The regulator is protected against:

- Overload
- Overtemperature
- Short circuit (short to ground and battery supply voltage)
- Reverse biasing

### 2.1.3 Increased output current capability for voltage regulator V<sub>2</sub>

For applications, which require high output currents, the output current capability of the regulator can be increased by means of the integrated operational amplifiers and an external pass transistor.

Figure 3. Voltage source with external PNP

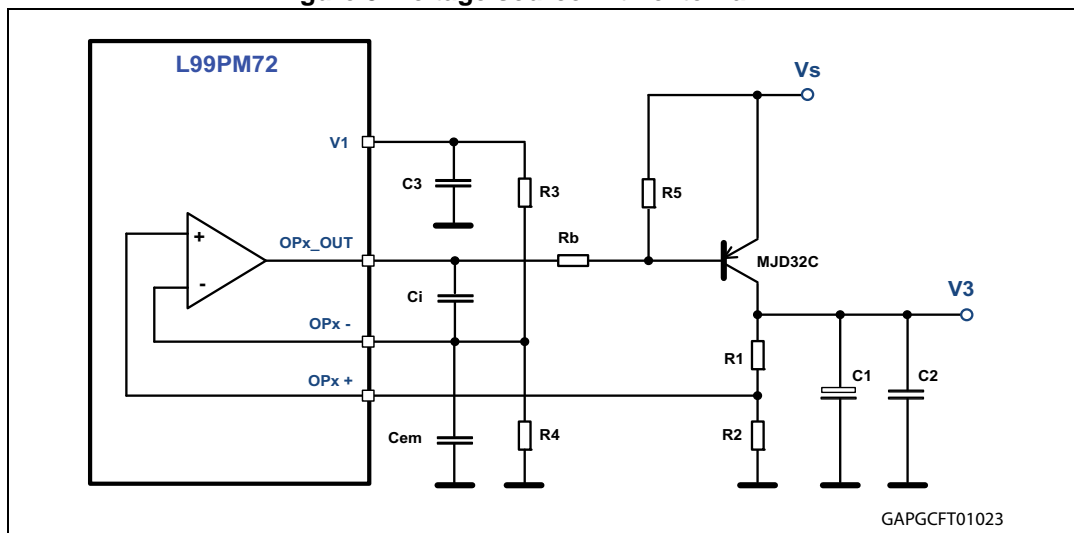


Figure 4. Voltage source with external PNP and current limitation

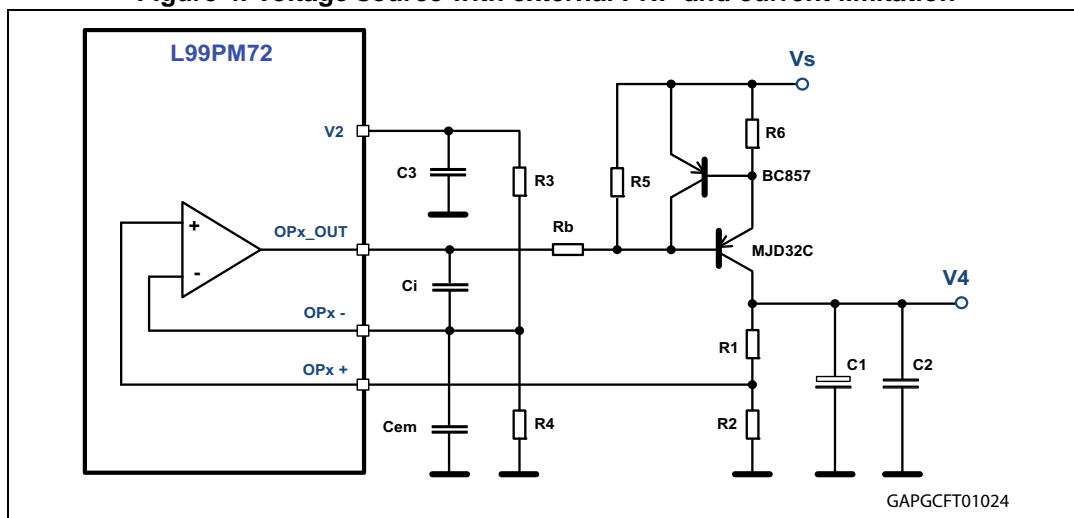


Figure 3 shows a possible configuration with a PNP pass element using Voltage Regulator 2 to provide the voltage reference for the regulated output voltage V<sub>3</sub>.

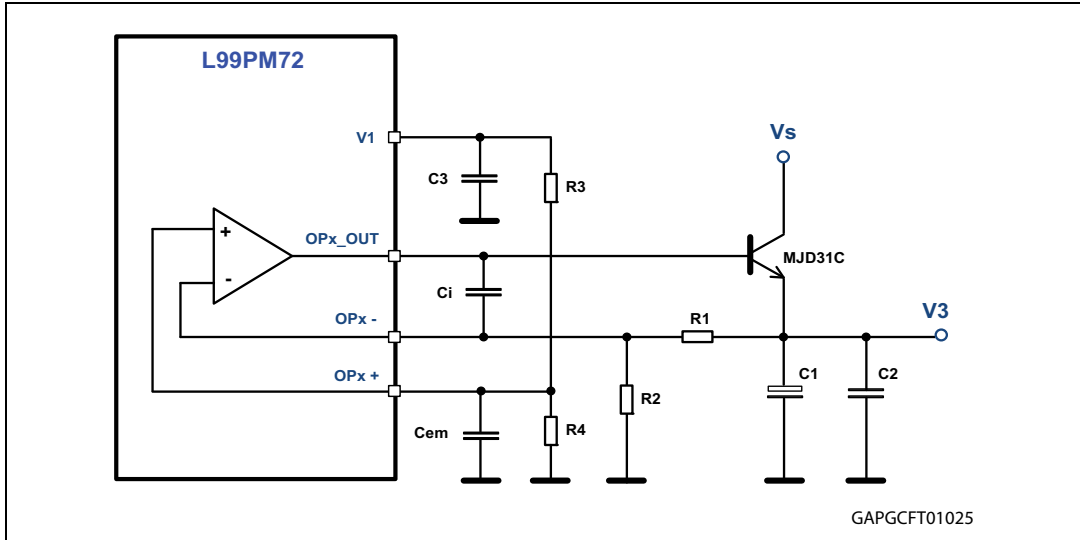
The V<sub>S</sub> operating range for this circuit is 5.5 V to 18 V. It is important respect the input common mode range specified for the operational amplifiers.

The output voltage V<sub>3</sub> can be calculated using the following formula (for R<sub>3</sub> = R<sub>4</sub>):

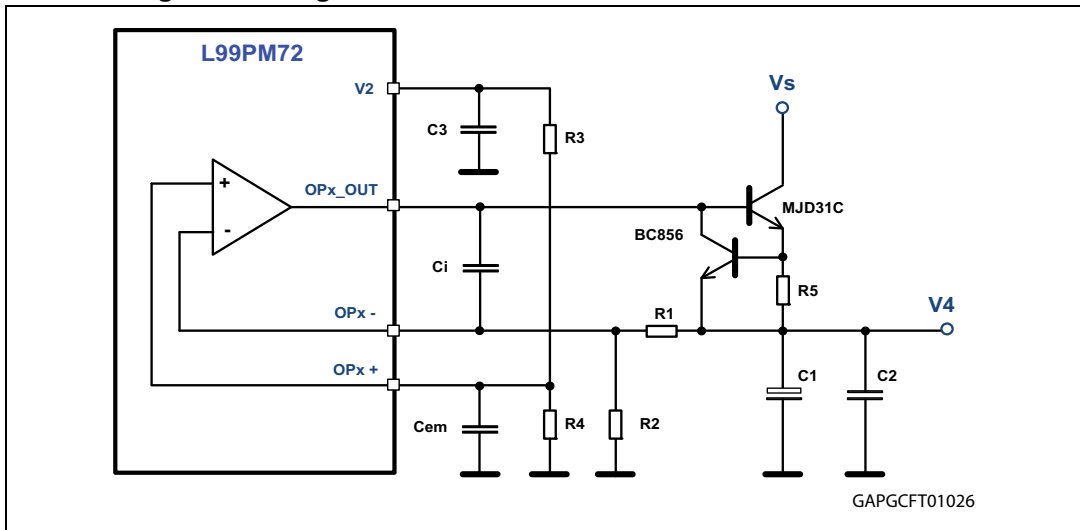
$$V_3 = \frac{V_2}{2} \cdot \frac{R_1 + R_2}{R_2} [V]$$

The circuit in *Figure 4* provides additional current limitation using an additional PNP transistor and R6, which allows setting the current limit.

**Figure 5. Voltage source with external NPN**



**Figure 6. Voltage source with external NPN and current limitation**



*Figure 5* shows a possible configuration with an NPN pass element using Voltage Regulator 2 to provide the voltage reference for the regulated output voltage V3. This circuit requires fewer components compared to the configuration in *Figure 3* but has a limited  $V_S$  operating range (6 V to 18 V).

The output voltage V3 can be calculated using the following formula (for  $R3 = R4$ ):

$$V_3 = \frac{V_2}{2} \cdot \frac{R_1 + R_2}{R_2} [V]$$

The circuit in *Figure 6* provides additional current limitation using an additional NPN transistor and R5 which allows setting the current limit.

Alternatively, Voltage Regulator 1 can be used to provide the 5 V reference for this topology. However, the additional current consumption through R3 and R4 has to be considered in  $V_{1\_standby}$  Mode.

#### 2.1.4 Voltage regulator failure

The  $V_1$  and  $V_2$  regulator output voltages are monitored.

In case of a drop below the  $V_1, V_2$  - fail thresholds ( $V_{1,2} < 2$  V, typ for  $t > 2$   $\mu$ s), the  $V_{1,2}$  -fail bits are latched. The fail bits can be cleared by a dedicated SPI command.

##### Short to ground detection

If 4 ms after turn on of the regulator the  $V_{1,2}$  voltage is below the  $V_{1,2}$  fail thresholds, (independent for  $V_{1,2}$ ), the L99PM72GXP identifies a short circuit condition at the related regulator output and the regulator are switched off.

In case of  $V_1$  short to GND failure the device enters  $V_{Bat\_standby}$  mode automatically. Bits Forced VBAT TSD2/SHTV1 and  $V_{1\_fail}$  were set.

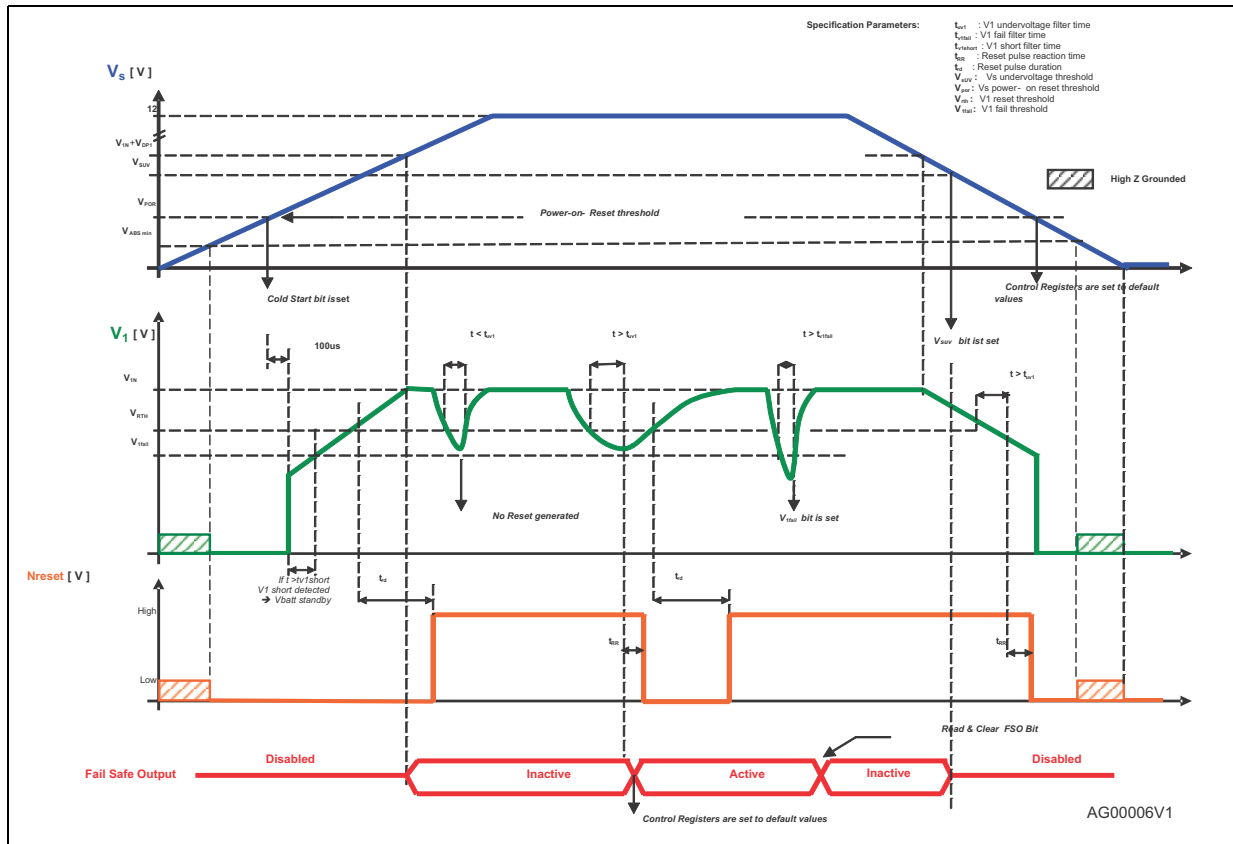
In case of a  $V_2$  short to GND failure the  $V_2$  short and  $V_2$  fail bit is set.

If the output voltage of the corresponding regulator once exceeded the  $V_{1,2\_fail}$  thresholds the short to ground detection is disabled. If a short to ground condition occurs the regulator outputs switch off due to Thermal shutdown ( $V_1$  at TSD2;  $V_2$  at TSD1).



### 2.1.5 Voltage regulator behavior

Figure 7. Voltage regulator behaviour and diagnosis during supply voltage ramp-up / ramp-down conditions



## 2.2 Operating modes

The L99PM72GXP can be operated in 4 different operating modes:

- Active
- FLASH
- $V_1$ \_standby
- $V_{Bat}$ \_standby

A cyclic monitoring of wake-up inputs and a periodic interrupt / wake-up by timer is available in standby modes.

### 2.2.1 Active Mode

All functions are available and the device is controlled by the ST SPI Interface.

### 2.2.2 Flash Mode

To program the system microcontroller via LIN or HS CAN bus signals, the device can be operated in LIN Flash Mode or CAN Flash Mode where the internal watchdog is disabled.

All other device features in Flash Mode are available as in Active Mode.

CAN Transmitter and CAN Receiver are enabled in CAN Flash Mode by default.

A transition from Flash Modes to  $V_{1\_standby}$  or  $V_{bat\_standby}$  is not possible.

The modes can be entered by applying an external voltage at the respective pin:

- $V_{TxDL} \geq V_{flash}$  (CAN Flash Mode)
- $V_{TxDC} \geq V_{flash}$  (LIN Flash Mode)

At exit from Flash Modes ( $V_{TxD} < V_{flash}$ ) no NRESET pulse is generated and the watchdog starts with a long open window.

*Note: Setting both TxDL and TxDC to high voltage levels ( $> V_{flash}$ ) is not allowed Communication at the respective TxD pin is not possible*

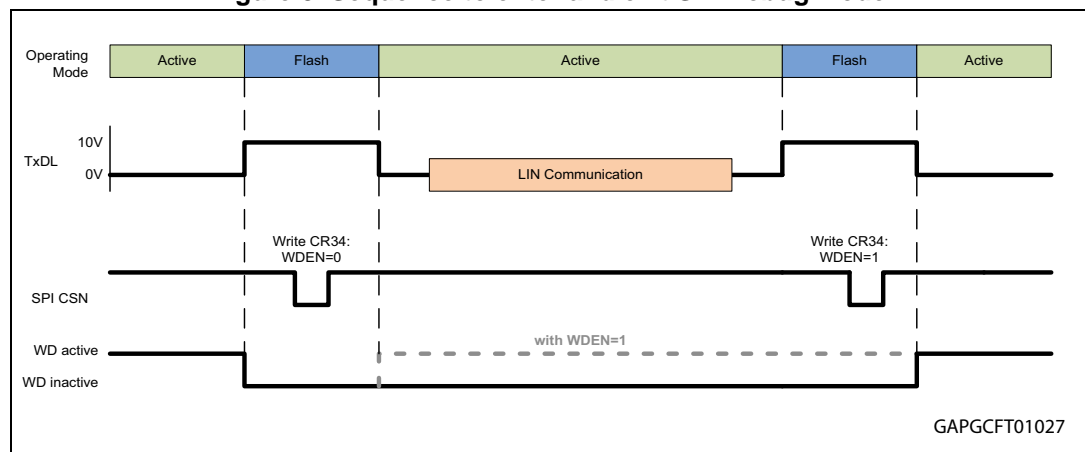
### 2.2.3 SW-Debug Mode

To allow software debugging, the watchdog can be deactivated by setting CR34: WDEN = 0.

Write access to this bit is only possible during CAN Flash Mode in order to prevent accidental deactivation of the watchdog. After setting the WDEN bit the CAN Flash Mode can be left ( $V_{TxDL} < V_{Flash}$ ) and the Watchdog remains deactivated (see [Figure 8](#))

In SW-Debug Mode, the full device functionality is available.

**Figure 8. Sequence to enter and exit SW Debug Mode**



### 2.2.4 $V_{1\_standby}$ mode

The transition from Active Mode to  $V_{1\_standby}$  mode is controlled by SPI.

To supply the micro controller in a low power mode, the voltage regulator 1 ( $V_1$ ) remains active. In order to reduce the current consumption, the regulator goes in low current mode as soon as the supply current of the microcontroller goes below the  $I_{CMP}$  current threshold. At this transition, the L99PM72GXP also deactivates the internal watchdog.

Relay outputs, LIN and CAN Transmitters are switched off in  $V_{1\_standby}$  Mode. High side outputs and the  $V_2$  regulator remain in the configuration programmed prior to the standby command.

A cyclic supply of external contacts and a synchronized monitoring of the contact state can be activated and configured by SPI.

In  $V_{1\_standby}$  mode various wake-up sources can be individually programmed. Each wake-up event puts the device into Active Mode and forces the RxDL/NINT pin to a low level indicating the wake-up condition to the microcontroller.

After Power ON Reset (POR) all wake up sources are activated by default except the periodic interrupt / wake timer.

With the interrupt timer the micro controller can be forced from 'stop' to 'run' after a programmable period. The RxDL/NINT pin is forced low after the timer is elapsed. The L99PM72GXP enters active mode and is awaiting a valid watchdog trigger.

Both internal timers can be used for this feature.

The interrupt timer (TINT) at pin RxDL/NINT is only available in  $V_{1\_standby}$  mode.

*Note: Inputs TxDL, TxDC must be at recessive (high) level and CSN must be at high level or at high impedance in order to achieve minimum standby current in  $V_{1\_standby}$  Mode. Inputs DI and CLK must be at GND or at high impedance to achieve minimum standby current in  $V_{1\_standby}$  Mode.*

## 2.2.5 Interrupt

The interrupt signal (linked to RxDL/NINT) indicates a wake-up event from  $V_{1\_standby}$  mode. In case of a wake-up by Wake-up Inputs, activity on LIN or CAN, SPI access or Timer-Interrupt the RxDL/NINT pin is pulled low for  $t = t_{interrupt}$ .

If the CAN transceiver is deactivated during Active Mode (CAN\_ACT = 0), a WUP (SWEN = 0) or a WUF (SWEN = 1) generates an interrupt at RxDC/NINT to signalize CAN communication on the bus to the microcontroller.

In case of a CAN communication timeout an interrupt at RxDC /NINT is generated and the CAN\_TO flag is set.

In case of  $V_{1\_standby}$  mode and ( $I_{V1} > I_{CMP}$ ), the device remains in standby mode, the  $V_1$  regulator switches to high current mode and the watchdog starts. No Interrupt signal is generated.

**Table 3. CAN wake-up signalization**

| Operating mode   | Event                     | Wake-up transition to active | Status flag             | Interrupt | Transceiver state |
|------------------|---------------------------|------------------------------|-------------------------|-----------|-------------------|
| Active           | WUP or WUF <sup>(1)</sup> | Not applicable               | Wake_CAN WUP or WUP/WUF | RxDC      | TRX_STBY          |
|                  | CAN timeout               |                              | CAN_TO                  | RxDC      | TRX_STBY          |
| $V_{1\_standby}$ | WUP or WUF <sup>(1)</sup> | Yes                          | Wake_CAN WUP or WUP/WUF | RxDL      | TRX_STBY          |
|                  | CAN timeout               | No                           | CAN_TO                  | RxDC      | TRX_STBY          |

**Table 3. CAN wake-up signalization (continued)**

| Operating mode           | Event                         | Wake-up transition to active | Status flag      | Interrupt      | Transceiver state |
|--------------------------|-------------------------------|------------------------------|------------------|----------------|-------------------|
| V <sub>bat_standby</sub> | WUP or WUP/WUF <sup>(2)</sup> | Yes                          | Wake_CAN WUP/WUF | Not applicable | TRX_STBY          |
|                          | CAN timeout                   | Transition to TRX_SLEEP      | CAN_TO           |                | TRX_SLEEP         |

1. SW\_EN = 0:
  - wake-up according ISO 11898-5 (WUP)
  - Flags: Wake\_CAN, WUP
- SW\_EN = 1:
  - wake-up according ISO 11898-6 (on WUP/WUF combination)
  - Flags: Wake\_CAN, WUP, WUF (the WUP flag is set only if the received WUF also contained a WUP)
2. SW\_EN = 0:
  - wake-up according ISO 11898-5 (on WUP)
  - Flags: Wake\_CAN, WUP
- SW\_EN = 1:
  - wake-up according ISO 11898-6 (on WUP/WUF combination)
  - After the reception of a wake-up pattern (WUP) the CAN Enhanced Voltage Biasing is turned on until a CAN timeout is detected
  - Flags: Wake\_CAN, WUP, WUF

### 2.2.6 V<sub>Bat\_standby</sub> mode

The transition from Active Mode to V<sub>Bat\_standby</sub> mode is initiated by an SPI command.

In V<sub>Bat\_standby</sub> Mode, the V<sub>1</sub> voltage regulator, relay outputs, LIN and CAN Transmitters are switched off. High side Outputs and the V<sub>2</sub> Regulator remain in the configuration programmed prior to the standby command.

In V<sub>Bat\_standby</sub> mode the current consumption of the L99PM72GXP is reduced to a minimum level.

An NRESET pulse is generated upon wake-up from V<sub>bat\_standby</sub> Mode.

*Note: Inputs TXDL, TXDC and CSN must be terminated to GND in V<sub>bat\_standby</sub> to achieve minimum standby current. This can be achieved with the internal ESD protection diodes of the microcontroller (microcontroller is not supplied in this mode; V<sub>1</sub> is pulled to GND).*

### 2.2.7 Wake up from Standby Modes

A wake-up from standby mode switches the device to active mode. This can be initiated by one or more of the following events:

**Table 4. Wake up from Standby Modes**

| Wake up source          | Description  |
|-------------------------|--|
| LIN bus activity        | Can be disabled by SPI   |
| CAN bus activity        | Can be disabled by SPI<br>Selective Wake-up can be configured by SPI |
| Level change of WU1 - 3 | Can be individually configured or disabled by SPI                    |



Table 4. Wake up from Standby Modes (continued)

| Wake up source                                   | Description  |
|--|--|
| $I_{V1} > I_{CMP}$                               | Device remains in $V_{1\_standby}$ mode but watchdog is enabled (If $I_{CMP} = 0$ ) and the $V_1$ regulator goes into High Current Mode (Increased Current Consumption). No interrupt is generated.  |
| Timer Interrupt /<br>Wake up of $\mu C$ by TIMER | programmable by SPI<br><ul style="list-style-type: none"> <li>- <math>V_{1\_standby}</math> Mode: device wakes up and Interrupt signal is generated at RxDL/NINT when programmable timeout has elapsed</li> <li>- <math>V_{Bat\_standby}</math> Mode: device wakes up, <math>V_1</math> regulator is turned on and NRESET signal is generated when programmable timeout has elapsed</li> </ul> |
| SPI Access                                       | Always active (except in $V_{Bat\_standby}$ mode)<br>Wake up event: CSN is low and first rising edge on CLK  |

To prevent the system from a deadlock condition (no wake up possible) a configuration where the periodic timer interrupt and wake up by LIN and HS CAN are disabled, is not allowed. The default configuration is entered for all wake-up sources in case of such an invalid setting.

All wake-up events from  $V_{1\_standby}$  mode (except  $I_{V1} > I_{CMP}$ ) are indicated to the microcontroller by a low-pulse (duration: 56  $\mu s$ ) at RxDL/NINT or RxDC/NINT (see [Table 3: CAN wake-up signalization](#))

Wake-up from  $V_{1\_standby}$  by SPI Access might be used to check the interrupt service handler.

## 2.2.8 Wake up inputs

The de-bounced digital inputs WU1...WU3 can be used to wake up the L99PM72GXP from standby modes. These inputs are sensitive to any level transition (positive and negative edge)

For static contact monitoring, a filter time of 64 $\mu s$  is implemented at WU1-3. The filter is started when the input voltage passes the specified threshold.

In addition to the continuous sensing (static contact monitoring) at the wake up inputs, a cyclic sense functionality is implemented. This feature allows periodical activation of the wake-up inputs to read the status of the external contacts. The periodical activation can be linked to Timer 1 or Timer 2 (see [Section 2.2.9](#)). The input signal is filtered with a filter time of 16  $\mu s$  after a programmable delay (80  $\mu s$  or 800  $\mu s$ ) according to the configured Timer On-time. A wake-up is processed if the status has changed versus the previous cycle.

The Outputs OUT\_HS and OUT1-4 can be used to supply the external contacts with the timer setting according to the cyclic monitoring of the wake-up inputs.

If the wake-up inputs are configured for cyclic sense mode the input filter timing and input filter delay ( $WUx\_filt$  in control register 2) must correspond to the setting of the High Side Output which supplies the external contact switches (OUTx in control register 0).

In Standby Mode, the inputs WU1-3 are SPI configurable for pull-up or pull-down current source configuration according to the setup of the external. In active mode the inputs have a pull down resistor.

In Active Mode, the input status can be read by SPI (Status Register 2). Static sense should be configured (Control Register 2) before the read operation is started (In cyclic sense

configuration, the input status is updated according to the cyclic sense timing; therefore, reading the input status in this mode may not reflect the actual status).

### 2.2.9 Cyclic contact supply

In  $V_{1\_standby}$  and  $V_{Bat\_standby}$  modes, any high side driver output (OUT1..4, OUTHS) can be used to periodically supply external contacts.

The timing is selectable by SPI

Timer 1: period is X s. The on-time is 10 ms resp. 20 ms: with  $X \in \{1, 2, 3, 4s\}$

Timer 2: period is X ms. The on-time is 100  $\mu$ s resp. 1 ms: with  $X \in \{10, 20, 50, 200\}$  ms}

Timer 1 and Timer 2 are re-started with every valid write command to CR3 (CSN low to high transition). The timers start with the off-phase.

### 2.2.10 Timer interrupt / wake-up of microcontroller by timer

During standby modes the cyclic wake up feature, configured via SPI, allows waking up the  $\mu$ C after a programmable timeout according to timer1 or timer 2.

From  $V_{1\_standby}$  mode, the L99PM72GXP wakes up (after the selected timer has elapsed) and sends an interrupt signal (via RxDL/NINT pin) to the  $\mu$ C. The device enters active mode and the watchdog is started with a long open window. The microcontroller can send the device back into  $V_{1\_standby}$  after finishing its tasks.

From  $V_{bat\_standby}$  mode, the L99PM72GXP wakes up (after the selected timer has elapsed), turns on the  $V_1$  regulator and provides an NRESET signal to the  $\mu$ C. The device enters active mode and the watchdog is started with a long open window. The microcontroller can send the device back into  $V_{bat\_standby}$  after finishing its tasks.

## 2.3 Functional overview (truth table)

Table 5. Functional overview (truth table)

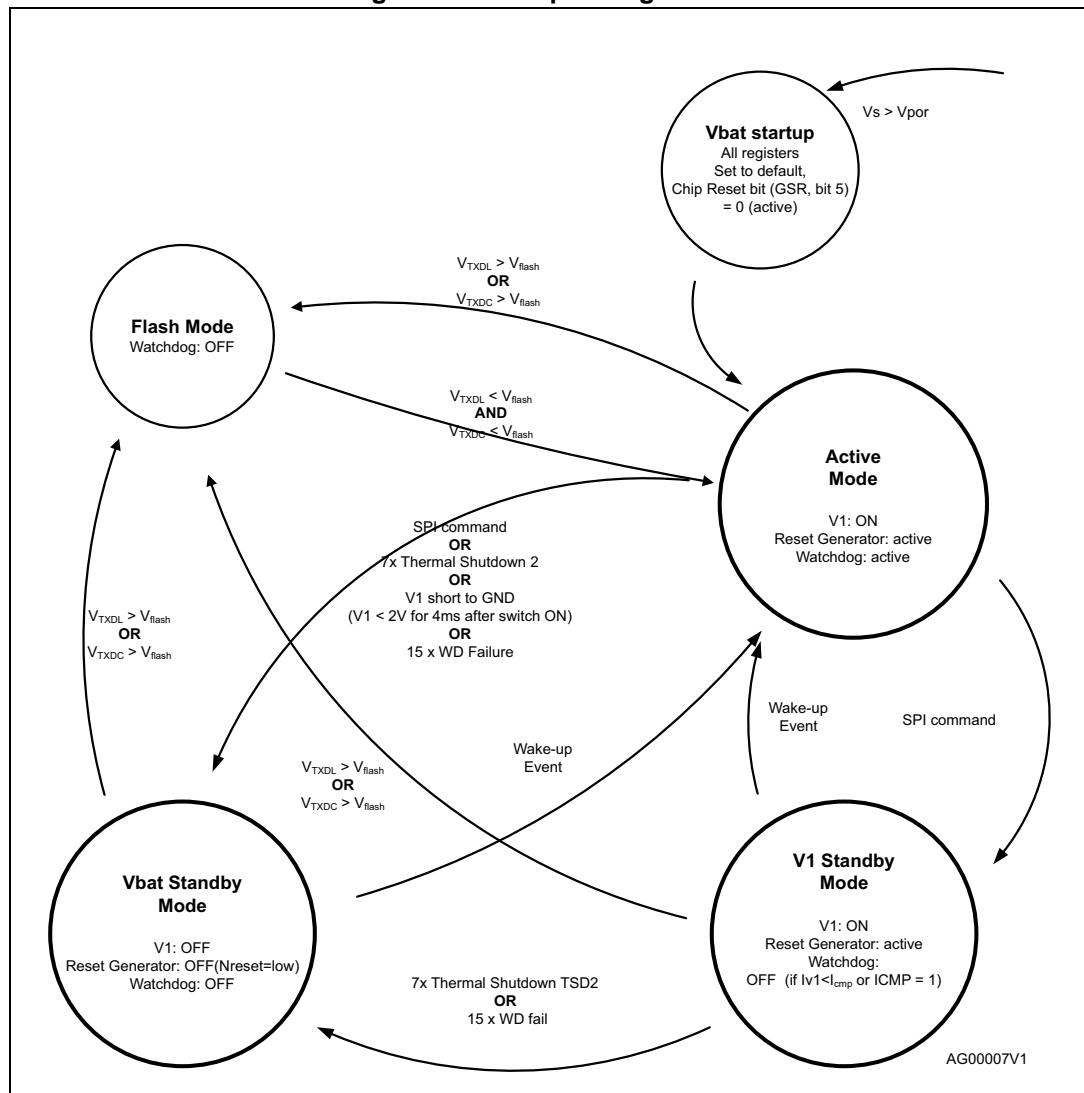
| Function                 | Comments             | Operating modes        |  |   |
|--------------------------|----------------------|------------------------|--|---|
|                          |                      | Active Mode            | $V_{1\_standby}$ static mode (cyclic sense)                | $V_{Bat\_standby}$ static mode (cyclic sense) |
| Voltage regulator, $V_1$ | VOUT=5V              | On                     | On <sup>(1)</sup>  | Off   |
| Voltage regulator, $V_2$ | VOUT=5V              | On/ Off <sup>(2)</sup> | On <sup>(2)</sup> / Off                                    | On <sup>(2)</sup> / Off                       |
| Reset generator          |                      | On                     | On   | Off   |
| Window watchdog          | $V_1$ monitor        | On                     | Off (ON: $I_{V1} > I_{CMP}$ -threshold and $I_{CMP} = 0$ ) | Off   |
| Wake up                  |                      | Off                    | Active <sup>(3)</sup>                                      | Active <sup>(3)</sup>                         |
| HS-cyclic supply         | Oscillator time base | On / Off               | On <sup>(2)</sup> / Off                                    | On <sup>(2)</sup> / Off                       |
| Relay driver             |                      | On                     | Off  | Off   |

Table 5. Functional overview (truth table) (continued)

| Function                                      | Comments         | Operating modes             |   |   |
|---|------------------|-----------------------------|---|---|
|   |                  | Active Mode                 | V <sub>1_standby</sub> static mode (cyclic sense) | V <sub>Bat_standby</sub> static mode (cyclic sense) |
| Operational amplifiers                        |                  | On                          | Off   | Off   |
| LIN   | LIN 2.1          | On                          | Off <sup>(4)</sup>                                | Off <sup>(4)</sup>                                  |
| HS_CAN  |                  | On / Off <sup>(5)</sup>     | Off <sup>(4)</sup>                                | Off <sup>(4)</sup>                                  |
| FSO (if configured by SPI), active by default | Fail safe output | OUT3/FSO OFF <sup>(6)</sup> | OUT3/FSO OFF <sup>(6)</sup>                       | OUT3/FSO OFF <sup>(6)</sup>                         |
| Oscillator                                    |                  | On                          | Off <sup>(7)</sup>                                | Off <sup>(7)</sup>                                  |
| V <sub>S</sub> -Monitor                       |                  | On                          | <sup>(8)</sup>                                    | <sup>(8)</sup>                                      |

1. Supply the processor in low current mode.
2. Only active when selected via SPI.
3. Unless disabled by SPI
4. The bus state is internally stored when going to standby mode. A change of bus state leads to a wake-up after exceeding of internal filter time (if wake-up by LIN or CAN is not disabled by SPI). Selective Wake functionality if enabled by SPI
5. After power-on, the HS CAN transceiver is in 'CAN Trx Standby' Mode. It is activated by SPI command (CAN\_ACT = 1)
6. ON in Failsafe Condition: If Standby mode is entered with active Fail Safe mode, the output remains ON in Standby mode.
7. ON, if cyclic sense is enabled.
8. Cyclic activation = pulsed ON during cyclic sense

Figure 9. Main operating modes



## 2.4 Configurable window watchdog

During normal operation, the watchdog monitors the micro controller within a programmable trigger cycle: (10 ms, 50 ms, 100 ms, 200 ms)

In  $V_{Bat\_standby}$  and Flash program modes, the watchdog circuit is automatically disabled. In  $V_{1\_standby}$  mode a wake up by timer is programmable in order to wake up the  $\mu C$  (see [Section 2.2.10](#)). After wake-up, the Watchdog starts with a long open window. After serving the watchdog, the microcontroller may send the device back to  $V_{1\_standby}$  mode.

After power-on or Standby mode, the watchdog is started with a long open window (65 ms nominal). The long open window allows the micro controller to run its own setup and then to trigger the watchdog via the SPI. The trigger is processed when the CSN input becomes HIGH after the transmission of the SPI word.

Writing '1' to the watchdog trigger bit terminates the long open window and start the window watchdog (the timing is programmable by SPI). Subsequently, the micro controller has to



serve the watchdog by alternating the watchdog trigger bit within the safe trigger area (refer to [Figure 32](#)).

A correct watchdog trigger signal immediately starts the next cycle.

After 8 watchdog failures in sequence, the  $V_1$  regulator is switched off for 200 ms. If subsequently, 7 additional watchdog failures occur, the  $V_1$  regulator is completely turned off and the device goes into  $V_{Bat\_standby}$  mode until a wakeup occurs.

In case of a Watchdog failure, the outputs (RELx, OUTx, V2) are switched off and the device enters Fail\_safe mode (i. e. all control registers are set to default values except the 'OUT3 control bit').

The following diagrams illustrate the Watchdog behavior of the L99PM72GXP. The diagrams are split into 3 parts. First diagram shows the functional behavior of the watchdog without any error. The second diagram covers the behavior covering all the error conditions, which can affect the watchdog behavior. Third diagram shows the transition in and out of FLASH mode. All 3 diagrams can be overlapped to get all the possible state transitions under all circumstances. For a better readability, they were split in normal operating, operating with errors and flash mode.

**Figure 10. Watchdog in normal operating mode (no errors)**

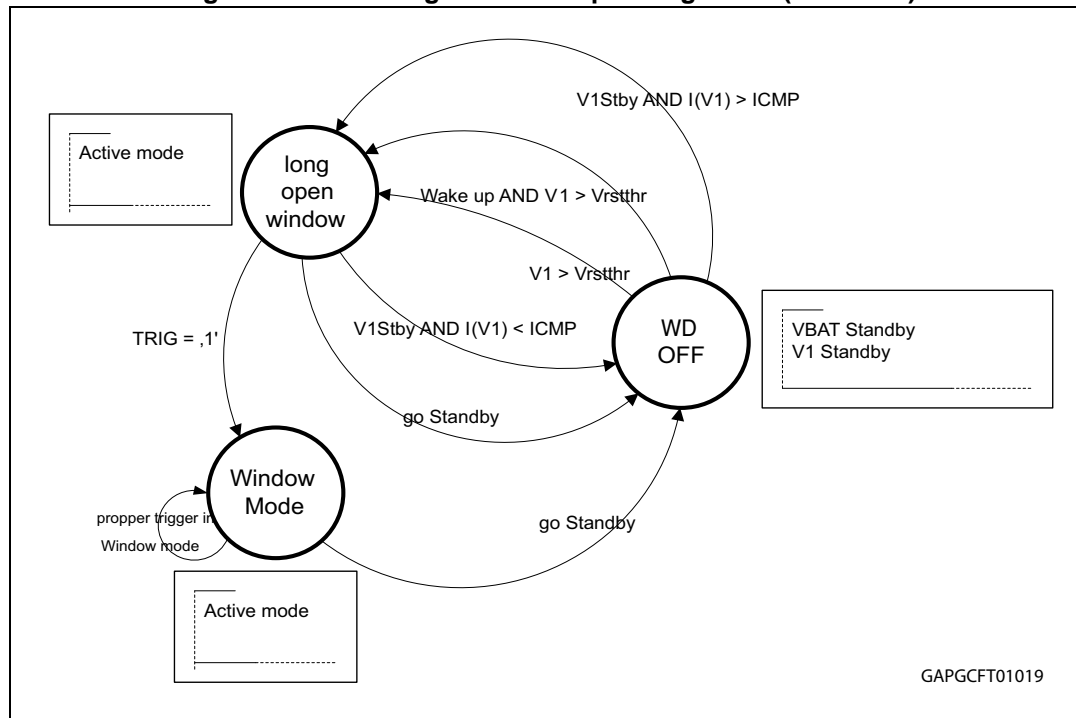


Figure 11. Watchdog with error conditions

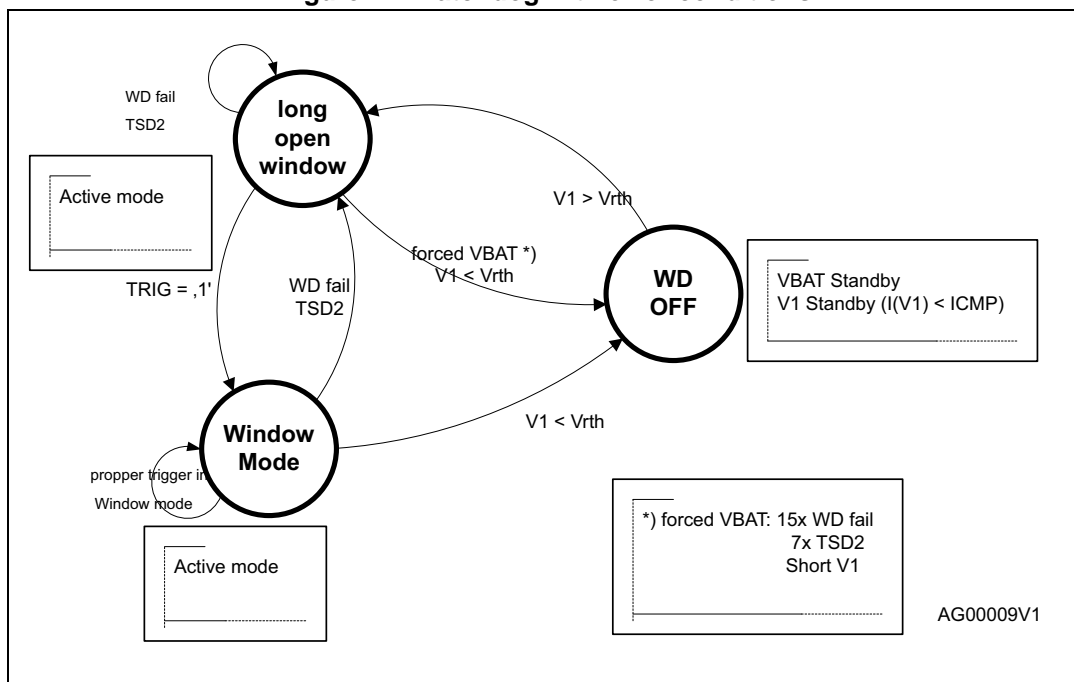
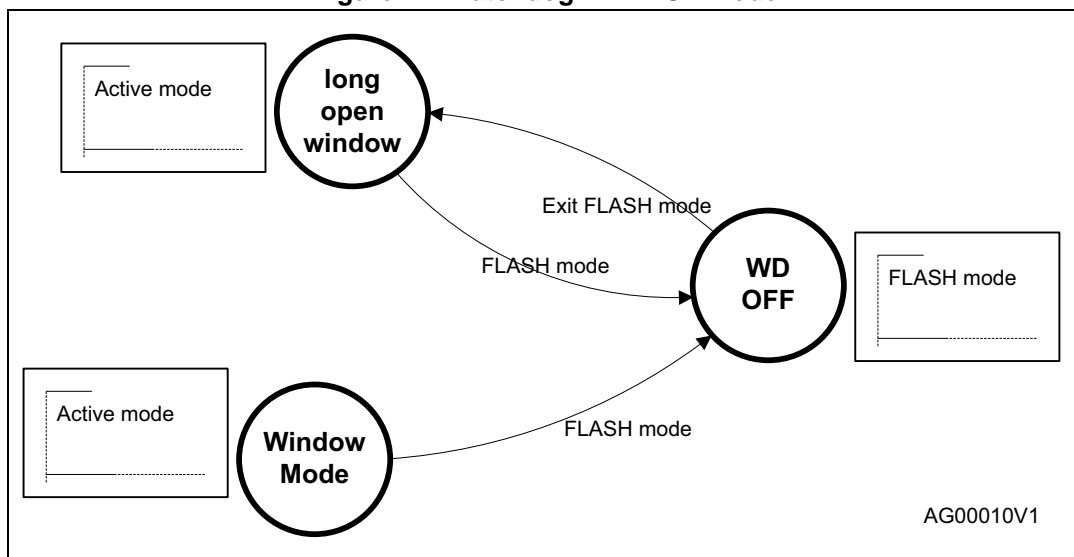


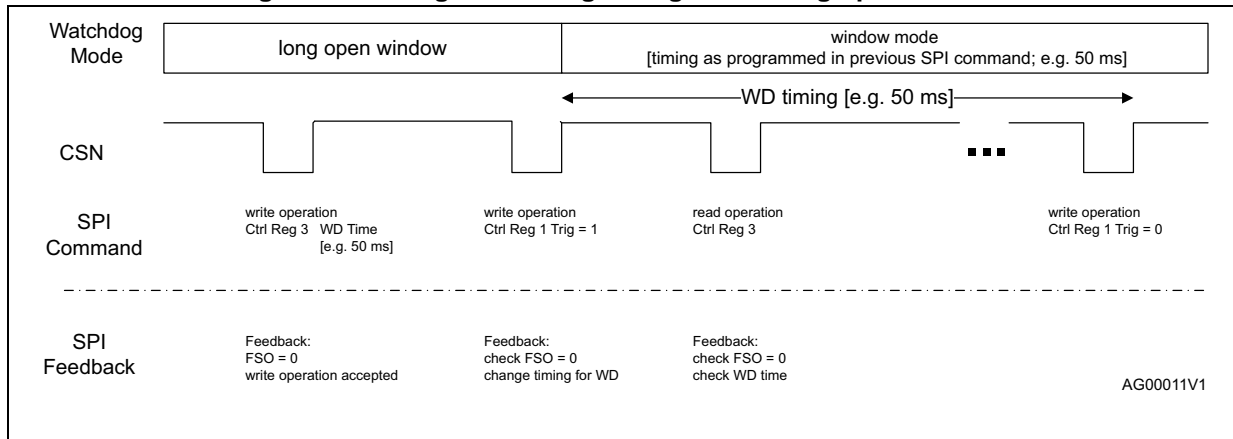
Figure 12. Watchdog in FLASH Mode



### 2.4.1 Change watchdog timing

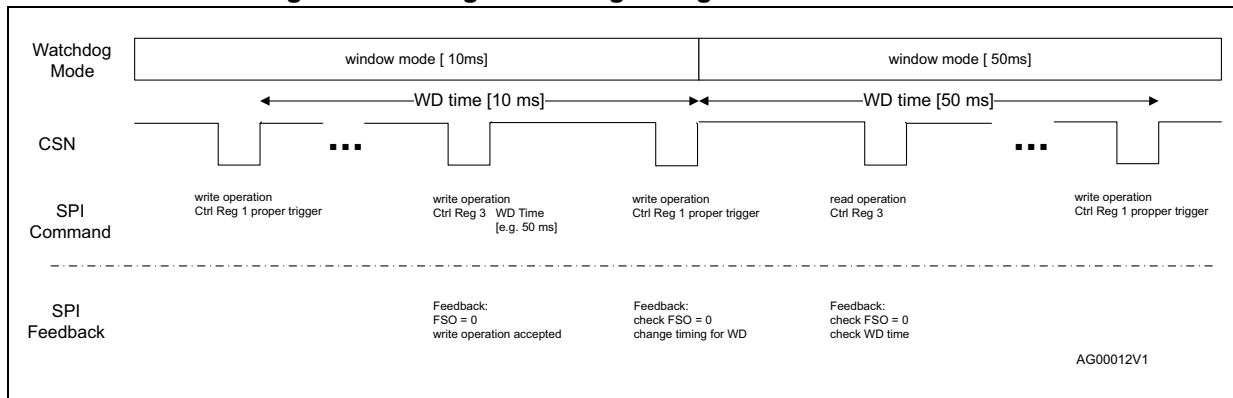
There are 4 programmable Watchdog timings available, which represent the nominal trigger time in window mode. To change the watchdog timing, a new timing has to be written by SPI. The new timing gets active with the next valid watchdog trigger. The following figures illustrate the sequence, which is recommended to use, changing the timing within long open window and within window mode.

Figure 13. Change watchdog timing within long open window



AG00011V1

Figure 14. Change watchdog timing within window mode



AG00012V1

If the device is in Fail\_safe mode, the Control Registers are locked for writing. To change the watchdog timing out of Fail\_safe mode, first the Fail\_safe condition must be solved, respective confirmed from the microcontroller. Afterwards the new watchdog timing can be programmed using the sequence from [Figure 15](#). Since the actions to remove, a Fail\_safe condition can differ from the root cause of the fail safe the following diagram shows the general procedure how to change the watchdog timing out of Fail\_safe mode. [Figure 16](#) shows the procedure to change watchdog timing with a previous watchdog failure, since this is a special Fail\_safe scenario.

Figure 15. General procedure to change watchdog timing out of Fail safe mode

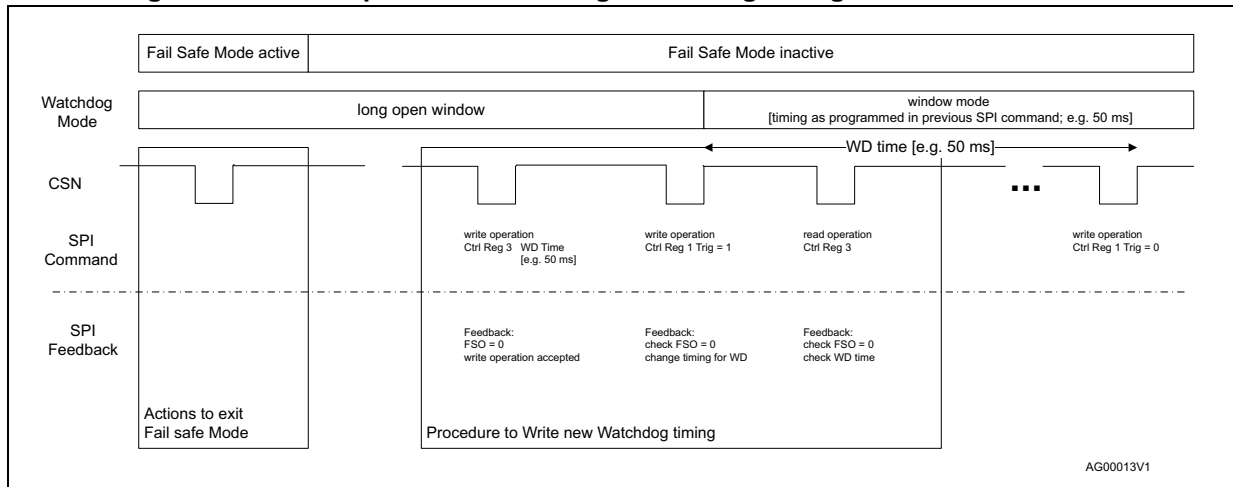
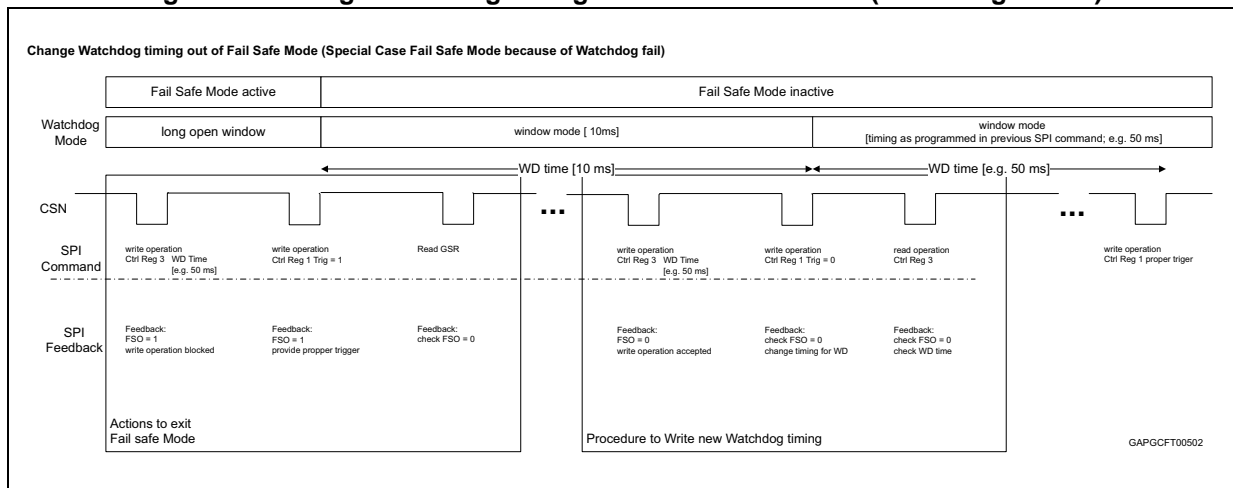


Figure 16. Change watchdog timing out of Fail safe mode (Watchdog failure)



## 2.5 Fail Safe Mode

### 2.5.1 Single failures

L99PM72GXP enters Fail Safe Mode in case of:

- Watchdog failure
- $V_1$  turn on failure
  - $V_1$  short ( $V_1 < V_{1fail}$  for  $t > t_{V1short}$ )
- $V_1$  undervoltage ( $V_1 < V_{RTH}$  for  $t > t_{UV1}$ )
- Thermal Shutdown TSD2
- SPI failure
  - DI stuck to GND or  $V_{CC}$  (SPI frame = '00 00 00' or 'FF FF FF')

The Fail Safe functionality is also available in  $V_{1\_standby}$  Mode. During  $V_{1\_standby}$  Mode the Fail Safe Mode is entered in the following cases:

- $V_1$  undervoltage ( $V_1 < V_{RTH}$  for  $t > t_{UV1}$ )
- Watchdog failure (if watchdog still running due to  $I_{V1} > I_{CMP}$ )
- Thermal shutdown TSD2

In Fail Safe Mode the L99PM72GXP returns to a default. The Fail Safe condition is indicated to the remaining system in the Global Status Register. The conditions during Fail Safe Mode are:

- All outputs are turned off
- All Control Registers are set to default values (except OUT3/FSO configuration)
  - This includes the programmed wake-up-frame. Therefore it is mandatory to reprogram the wake-up-frame before entering the selective wake-up mode after a Fail\_safe event<sup>(a)</sup>
- Write operations to Control Registers are blocked until the Fail Safe condition is cleared (see [Table 6](#))
- LIN and HS CAN transmitter, operational amplifiers and SPI remain on
- Corresponding Failure Bits in Status Registers are set.
- FSO Bit (Bit 0 Global Status Register) is set
- OUT3/FSO is activated if configured as Fail Safe Output

If OUT3 is configured as FSO, the internal Fail-Safe Mode can be monitored at OUT3 (High side driver is turned on in Fail-safe Mode). Self-protection features for OUT3 when configured as FSO are active (See [Section 3.3: High side driver outputs](#))

OUT3 is configured as Fail Safe Output by default. It can be configured to normal high side driver operation by SPI. In this case, the configuration remains until  $V_S$  Power On.

If the Fail Safe Mode was entered it keeps active until the Fail safe condition is removed and the Fail Safe was read by SPI. Depending on the root cause of the Fail Safe operation, the actions to exit Fail safe Mode are as shown in the following table.

**Table 6. Fail-Safe conditions and exit modes**

| Failure source       | Failure condition                              | Diagnosis                                       | Exit from Fail_safe Mode                    |
|----------------------|--|---|---|
| $\mu C$ (oscillator) | Watchdog early write failure or expired window | Fail_safe = 1; $WD_{fail} = n + 1$              | TRIG = 1 during LOWi and read Fail_safe bit |
| $V_1$                | Short at turn-on                               | Fail_safe = 1;<br>Forced_Sleep_TSD2_SHTV1 = 1   | Read & Clear SR3 after wake                 |
|                      | Undervoltage                                   | Fail_safe = 1; $V_{1\_fail} = 1$ <sup>(1)</sup> | $V_1 > V_{RTH}$<br>Read Fail_safe bit       |

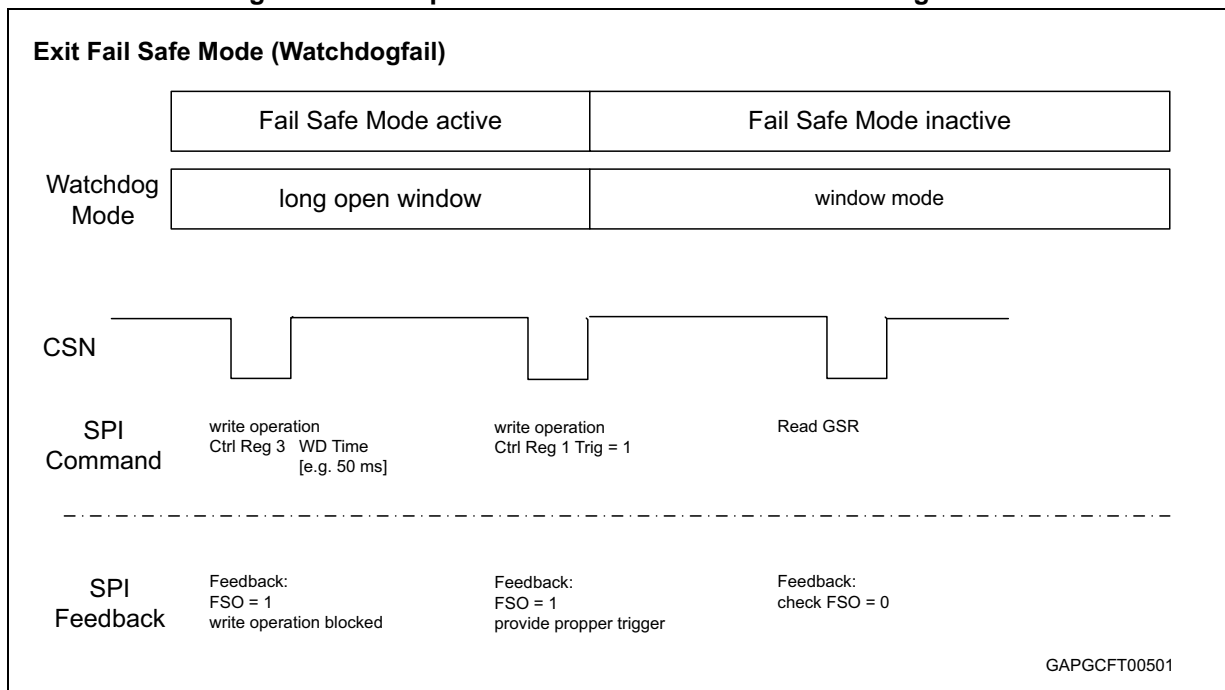
a. Even though it is still possible after a Fail\_safe event to enter the selective-wake-up mode, the device wakes only up with the default values of the configuration register (see [Section 6.2.2: Overview control register](#)).

**Table 6. Fail-Safe conditions and exit modes (continued)**

| Failure source | Failure condition           | Diagnosis                                 | Exit from Fail_safe Mode         |
|----------------|-----------------------------|---|----------------------------------|
| Temperature    | $T_j > TSD2$                | Fail_safe = 1; TW = 1; TSD1 = 1; TSD2 = 1 | $T_j < TSD2$<br>Read & Clear SR3 |
| SPI            | DI short to GND or $V_{CC}$ | Fail_safe = 1                             | Valid SPI command                |

1. If  $V_1 < V_{1\_Fail}$  (for  $t > t_{v1fail}$ )  
The Fail\_safe Bit is located in the Global Status Register (Bit 0)

**Figure 17. Example: exit Fail-Safe mode from Watchdog failure**



### 2.5.2 Multiple failures – entering forced $V_{Bat\_standby}$ Mode

If the Fail-Safe condition persists and all attempts to return to normal system operation fail, the L99PM72GXP enters the Forced  $V_{bat\_standby}$  Mode in order to prevent damage to the system. The Forced  $V_{bat\_standby}$  Mode can be terminated by any regular wake-up event. The root cause of the Forced  $V_{bat\_standby}$  is indicated in the SPI Status Registers

The forced  $V_{bat\_standby}$  Mode is entered in case of:

- Multiple watchdog failures: forced sleep WD = 1 (15 x watchdog failure)
- Multiple thermal shutdown 2: forced sleep TSD2/SHTV1 = 1 (7 x TSD2)
- $V_1$  short at turn-on: forced sleep TSD2/SHTV1 = 1 ( $V_1 < V_{1\_Fail}$  for  $t > t_{v1fail}$ )

Table 7. Persisting fail safe conditions and exit modes

| Failure source             | Failure condition                | Diagnosis  | Exit from Fail_safe Mode                            |
|----------------------------|----------------------------------|--|---|
| $\mu\text{C}$ (oscillator) | 15 consecutive watchdog failures | Fail_safe = 1;<br>Forced_Sleep_WD = 1                                      | Wake-up<br>TRIG = 1 during LOWi<br>Read & Clear SR3 |
| $V_1$                      | short at turn-on                 | Fail_safe = 1;<br>Forced_Sleep_TSD2_SHTV1 = 1                              | Read & Clear SR3 after<br>wake-up                   |
| Temperature                | 7 times TSD2                     | Fail_safe = 1; TW = 1; TSD1 = 1;<br>TSD2 = 1;<br>Forced_Sleep_TSD2_SHTV1=1 | Read & Clear SR3 after<br>wake-up                   |

## 2.6 Reset output (NRESET)

If  $V_1$  is turned on and the voltage exceeds the  $V_1$  reset threshold, the reset output "NRESET" is pulled up by internal pull up resistor to  $V_1$  voltage after a reset delay time ( $t_{rd}$ ). This is necessary for a defined start of the micro controller when the application is switched on. Since the NRESET output is realized as an open drain output it is also possible to connect an external NRESET open drain NRESET source to the output. As soon as the NRESET is released by the L99PM72 the Watchdog timing starts with a long open window.

A reset pulse is generated in case of:

- $V_1$  drops below  $V_{RTH}$  (configurable by SPI) for  $t > t_{UV1}$
- watchdog failure
- turn-on of the  $V_1$  regulator ( $V_S$  power-on or wake-up from  $V_{bat\_standby}$  mode)

## 2.7 Operational amplifiers

The operational amplifiers are especially designed to be used for sensing and amplifying the voltage drop across ground connected shunt resistors. Therefore the input common mode range includes -0.2 V to 3V.

The operational amplifiers are designed for -0.2 V to 3 V input voltage swing and rail-to-rail output voltage range.

All pins (positive, negative and outputs) are available to be able to operate in non-inverting and inverting mode. Both operational amplifiers are on-chip compensated for stability over the whole operating range within the defined load impedance.

The Operational Amplifiers may also be used to setup an additional high current voltage source with an external pass element. Refer to [Section 2.1.3](#) for a detailed description.

## 2.8 LIN Bus Interface

Features:

- Speed communication up to 20kbit/s.
- LIN 2.1 compliant (SAEJ2602 compatible) transceiver.
- GND disconnection fail safe at module level.
- Off mode: does not disturb network.
- GND shift operation at system level.
- Micro controller Interface with CMOS compatible I/O pins.
- Internal Pull-up resistor
- Internal High Side Switch to disconnect Master Pull-up resistor in case of short circuit of bus signal <sup>(b)</sup>
- ESD and transient immunity according to ISO7637 and EN / IEC61000-4-2
- Matched output slopes and propagation delay

In order to further reduce the current consumption in standby mode, the integrated LIN bus interface offers an ultra low current consumption.

### 2.8.1 Error handling

The L99PM72GXP provides the following three error handling features which are not described in the LIN Spec. V2.1, but are realized in different stand alone LIN transceivers / micro controllers to switch the application back to normal operation mode.

At  $V_S > V_{POR}$  (i.e.  $V_S$  power-on reset threshold), the LIN transceiver is enabled.

The LIN transmitter is disabled in case of the following errors:

- Dominant TxDL time out
- LIN permanent recessive
- Thermal Shutdown 1
- $V_S$  Over- / Undervoltage

The LIN receiver is not disabled in case of any failure condition.

#### Dominant TxDL time out

If TXDL is in dominant state (low) for more than 12 ms (typ) the transmitter is disabled, the status bit is latched and can be read and optionally cleared by SPI. The transmitter remains disabled until the status register is cleared. This feature can be disabled via SPI.

#### Permanent recessive

If TXDL changes to dominant (low) state but RXDL signal does not follow within 40  $\mu$ s the transmitter is disabled, the status bit is latched and can be read and optionally cleared by SPI. The transmitter remains disabled until the status register is cleared.

---

b. Use of the Master Pull-up switch is optional.



**Permanent dominant**

If the bus state is dominant (low) for more than 12 ms a permanent dominant status is detected. The status bit is latched and can be read and optionally cleared by SPI. The transmitter is not disabled.

**2.8.2 Wake up (from LIN)**

In standby mode the L99PM72GXP can receive a wake up from LIN bus. For the wake up feature the L99PM72GXP logic differentiates two different conditions.

**Normal wake up**

Normal wake up can occur when the LIN transceiver was set in standby mode while LIN was in recessive (high) state. A dominant level at LIN for  $t_{linbus}$ , switches the L99PM72GXP to active mode.

**Wake up from short to GND condition**

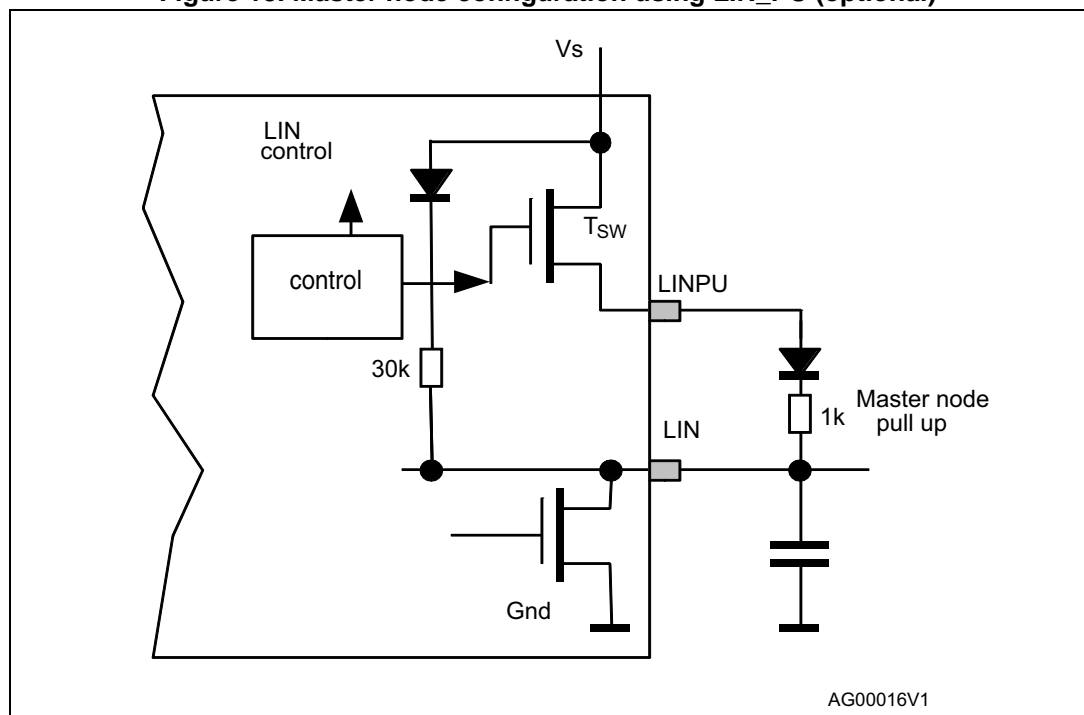
If the LIN transceiver was set in standby mode while LIN was in dominant (low) state, recessive level at LIN for  $t_{linbus}$ , switches the L99PM72GXP to active mode.

*Note: A wake up caused by a message on the bus starts the voltage regulator and the microcontroller to switch the application back to normal operation mode.*

**2.8.3 LIN Pull-Up**

The master node pull-up resistor (1 kΩ) can be connected to  $V_S$  using the internal LIN\_PU high side switch. This high side switch can be controlled by SPI in order to allow disconnection of the pull-up resistor in case of LIN bus short to GND conditions.

**Figure 18. Master node configuration using LIN\_PU (optional)**



LIN\_PU high side driver characteristics:

- Activated by default and can be turned off by SPI Command (CR4)
- remains active in standby modes
- Switch off only in case of over-temperature (TSD2 = thermal shut down #2)
- no over current protection.
- Typical  $R_{DS(on)}$ , 10  $\Omega$

## 2.9 High speed CAN bus transceiver

General requirements:

- Communication Speed up to 1Mbit/s.
- ISO 11898-2 and ISO 11898-5 compliant
- Selective wake-up functionality according to ISO 11898-6
- Non-selective wake-up functionality according to ISO 11898-5
- SAE J2284 compliant
- Function range from -27 V to 40 V DC at CAN pins.
- GND disconnection fail safe at module level.
- GND shift operation at system level.
- Microcontroller Interface with CMOS compatible I/O pins.
- ESD and transient immunity according to ISO7637 and EN / IEC61000-4-2
- Matched output slopes and propagation delay
- Receive-only mode available

For further reducing the current consumption in standby mode, the integrated CAN bus interface offers an ultra-low current consumption.

### 2.9.1 CAN transceiver operating modes

Figure 19. Transceiver state diagram if selective wake-up is disabled (CR16 SW\_EN = 0)

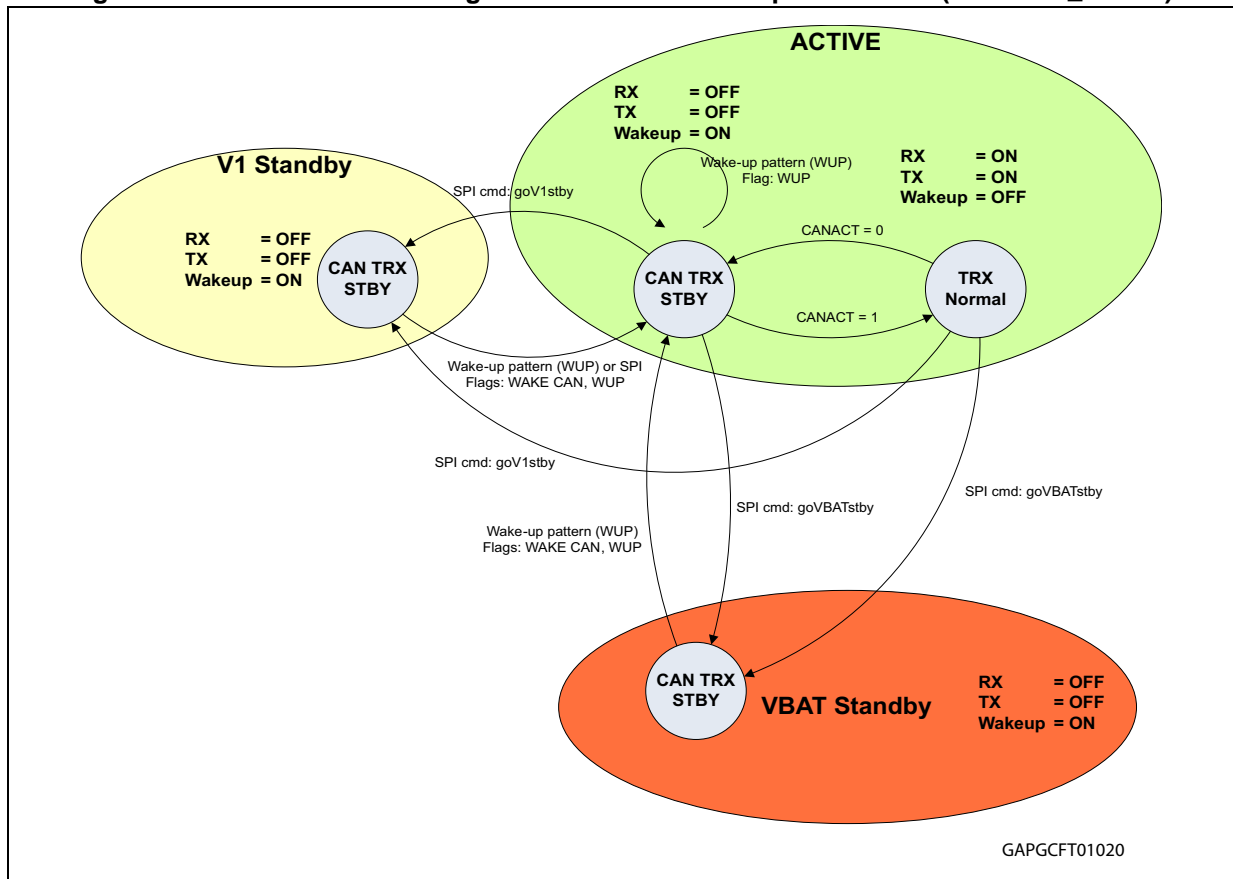
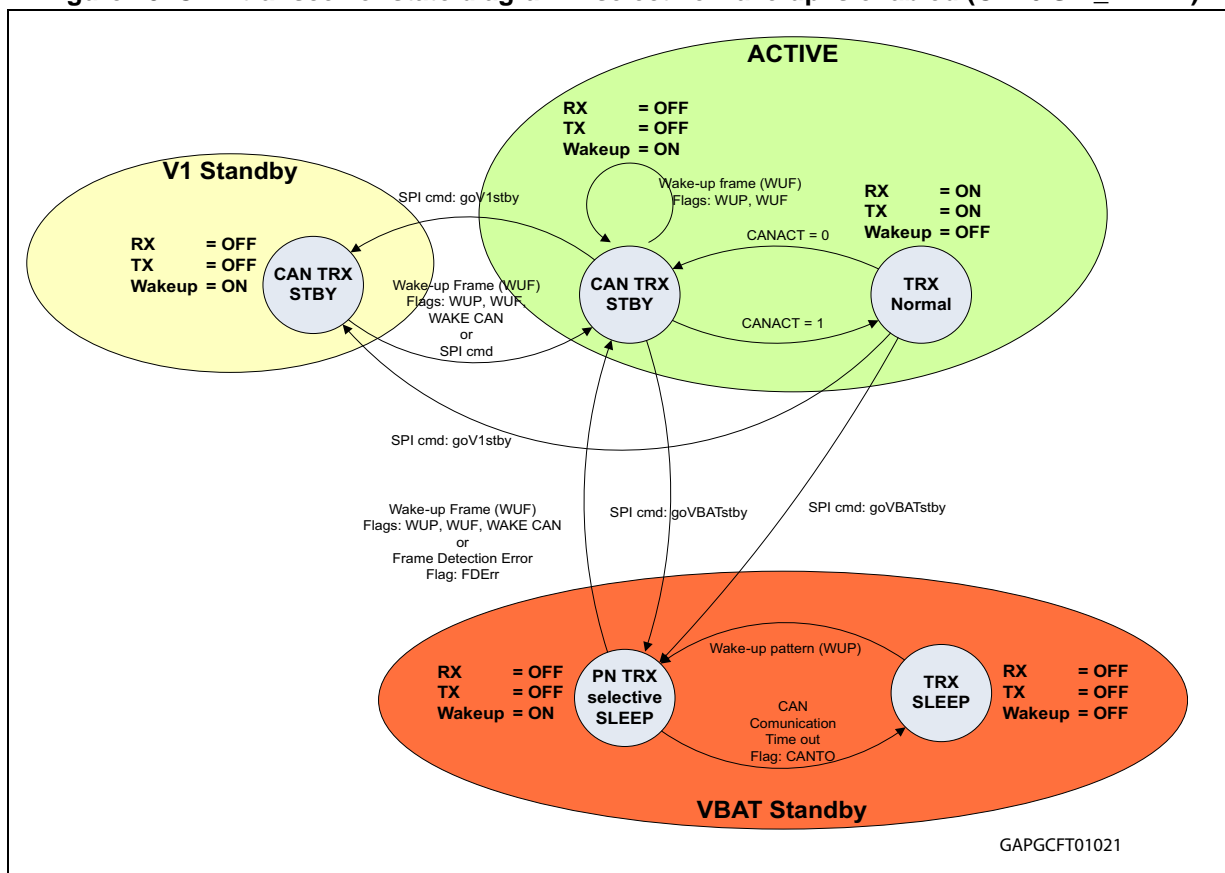


Figure 20. CAN transceiver state diagram if selective wake-up is enabled (CR16 SW\_EN = 1)



GAPGCFT01021

### TRX Normal Mode

Full functionality of the CAN-Transceiver is available (transmitter and receiver) and the bus biasing is enabled.

State transitions from 'TRX Normal' mode to 'V<sub>Bat\_standby</sub>' and 'V<sub>1\_standby</sub>' are possible. No interrupt is generated in this mode.

### CAN TRX\_STBY Mode

The CAN-Transmitter is disabled in this mode and the RxDc-pin is kept at high ('recessive') level.

If selective wake-up is enabled (SW\_EN=1), the receiver, CAN biasing and the reference oscillator are active. Once a wake up frame (WUF) is detected by the internal CAN frame detection logic, this wake-up event is indicated to the micro-controller by an interrupt signal (see [Section 2.2.5: Interrupt](#) for more details). A wake-up pattern (WUP) is not required and does not count as a frame error.

Since a further CAN-timeout cannot be indicated, if the CAN\_TO bit has already been set, it is recommended to clear this bit before entering V<sub>1\_standby</sub> Mode.

If selective wake-up is disabled (SW\_EN = 0), the CAN-Receiver is capable to detect a wake-up pattern (WUP). In V<sub>1\_standby</sub> Mode and Active Mode, a WUP is indicated to the micro-controller by an interrupt signal (see [Section 2.2.5: Interrupt](#) for more details). In this

mode (SW\_EN = 0) the automatic voltage biasing is disabled and the transceiver biasing works according to ISO 11898-5.

There is no automatic state transition into TRX Normal Mode in case of a detected CAN wake-up (WUF or WUP). After serving the interrupt the micro controller can initiate a state transition into TRX Normal Mode by setting the SPI bit CAN\_ACT to '1'.

### **TRX\_SLEEP (SW\_EN=1)**

The CAN and LIN Transceivers are disabled. The CAN selective wakeup reference oscillator is off, while the receiver is in low power mode.

After the detection of CAN communication (WUP), the transceiver enters 'PN\_TRX\_selective\_sleep' mode, starts the oscillator and decodes the CAN frame.

'TRX\_SLEEP' mode is entered automatically after a CAN communication timeout.

### **PN TRX Selective Sleep (SW\_EN=1)**

In this mode the CAN frame detection logic is enabled (receiver and reference oscillator enabled). In case of receiving a wake up frame (WUF) a state transition to 'CAN TRX\_STBY' is done. After the biasing has been switched on, not more than four CAN frames are ignored before a wake-up frame is recognized and the device wakes up.

If there is no CAN communication and the CAN bus is recessive for longer than  $t_{\text{silence}}$ , an automatic state transition to 'TRX\_SLEEP' is done.

In case of a Frame-Detect-Error (SR4, FDERR=1), an automatic wake up is performed and the selective wakeup feature is disabled (SW\_EN=0).

### **Oscillator monitoring**

While selective wake-up is enabled, a timer is started with each recessive to dominant edge.

If after the expiration of 300  $\mu\text{s}$  on this timer less than 6 recessive bits are counted, an oscillator fail is detected and the osc\_mon bit is set to '1'. Subsequently the device enters wake-up mode according to ISO11898-5 (wake-up pattern wake-up).

## **2.9.2 Sequence for enabling selective wakeup**

After power-on reset the selective wakeup feature is disabled.

The Configuration Registers 7 to 15 have to be read and verified by the microcontroller in order to ensure a valid configuration. A read operation to Registers 7 to 15 is required to allow enabling the selective wake-up feature (set SW\_EN=1).

A valid read operation is indicated by the SW\_RDxx bits in SR 4. The SW\_RDxx bits are reset to 0 with every WRITE operation.

When all SW\_RD bits are set, the SW\_EN bit in CR 16 can be set to enable the Selective Wakeup function. In case the SYSERROR bit in SR 4 is set while Selective Wakeup is enabled, the Selective Wakeup is automatically disabled. In case SYSERROR is set, enabling the Selective Wakeup function is prohibited.

## **2.9.3 CAN error handling**

The L99PM72GXP provides the following four error handling features.

After power-on reset ( $V_S > V_{POR}$ ) the CAN transceiver is disabled. The transceiver is enabled by setting the CAN\_ACT bit in Control Register 4.

The CAN transmitter is disabled automatically in case of the following errors:

- Dominant TxDC time out
- CAN permanent recessive
- RxDC permanent recessive
- Thermal shutdown 1

The CAN receiver is not disabled in case of any failure condition.

#### **Dominant TxDC time out**

If TXDC is in dominant state (low) for  $t > t_{dom(TxD)}$  the transmitter is disabled, status bit is latched and can be read and optionally cleared by SPI. The transmitter remains disabled until the status register is cleared.

#### **CAN permanent recessive**

If TXDC changes to dominant (low) state but CAN bus does not follow for 4 times, the transmitter is disabled, status bit is latched and can be read and optionally cleared by SPI. The transmitter remains disabled until the status register is cleared.

#### **CAN permanent dominant**

If the bus state is dominant (low) for  $t > t_{CAN}$  a permanent dominant status is detected. The status bit is latched and can be read and optionally cleared by SPI. The transmitter is not disabled.

#### **RXDC permanent recessive**

If RXDC pin is clamped to recessive (high) state, the controller is not able to recognize a bus dominant state and could start messages at any time, which results in disturbing the overall bus communication. Therefore, if RXDC does not follow TXDC for 4 times the transmitter is disabled. The status bit is latched and can be read and optionally cleared by SPI. The transmitter remains disabled until the status register is cleared.

### **2.9.4 Wake up by CAN**

The L99PM72GXP supports 2 wakeup modes. The selective wakeup according to ISO 11898-6 or the wakeup by any bus activity according to ISO 11898-2/-5. The wake up behavior can be configured by SPI (see [Chapter 6: ST SPI](#)).

#### **Wake up by CAN pattern (WUP)**

The default setting for the wake up behavior after power-on reset is the wake up by regular communication on the CAN bus. When the CAN transceiver is in a Standby Mode (CAN TRX\_STBY or TRX\_SLEEP) the device can be woken up by sending two consecutive dominant bits separated by a recessive bit.

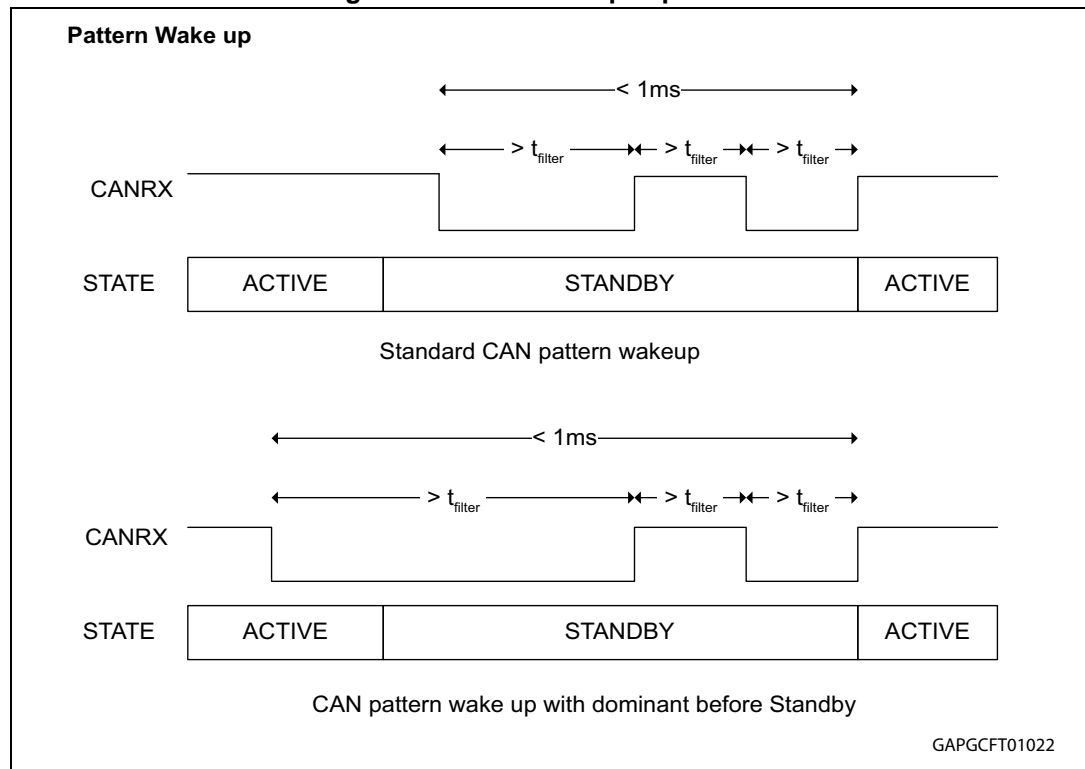
Normal pattern wake up can occur when CAN pattern wake up option is enabled and the CAN transceiver was set in Standby Mode (CAN TRX\_STBY or TRX\_SLEEP) while CAN

bus was in recessive (high) state or dominant (low) state. In order to wake up the L99PM72GXP, the following criteria must be fulfilled:

- The CAN interface wake-up receiver must receive a series of two consecutive valid dominant pulses, each of which must be longer than  $t_{filter}$
- The distance between 2 pulses must be longer than  $t_{filter}$
- The two pulses must occur within a time frame of 1.0 ms

*Note:* A wake up caused by a message on the bus starts the voltage regulator and the microcontroller to switch the application back to normal operation mode.

**Figure 21. CAN wake up capabilities**



*Note:* Pictures above illustrate the wake up behaviour from  $V_{1\_standby}$  Mode. For wake up from  $V_{Bat\_standby}$  Mode the NRESET signal (with 2 ms timing) is generated instead of the RXDL(Interrupt) signal.

**Wakeup by CAN Frame (WUF)**

**Wake from CAN TRX\_STBY**

If the CAN transceiver is in STBY the CAN frame detection logic is active.

In case of a valid wake up frame the Interrupt on pin RxDc is generated and the WUF flag for wake up identification is set. There is no automatic state transition from CAN Transceiver point of view. After serving the interrupt the micro can bring the CAN Transceiver into TRX\_NORMAL by setting CAN\_ACT = 1 (CR 4).

**Wake up from TRX\_SLEEP**

If the CAN Transceiver is in TRX\_SLEEP mode the CAN frame detection logic is disabled. The wake up can be done in two steps. To enable the CAN frame detection logic a wake up

pattern must be sent on the bus. With the detection of the wake up pattern an automatic state transition to 'PN\_TRX\_Selective\_Sleep' state is done. WUP flag is set.

In 'PN\_TRX\_Selective\_Sleep' the CAN frame detection logic is enabled. If a valid wake up frame is detected a state transition to TRX\_STBY is done, the WUF flag is set and the micro is powered up. The remote transition request bit is ignored in wake-up frames. Also masking of the data length code (DLC) bits is not supported.

After expiration of the frame error counter (FEC), a wake up is performed and the selective wakeup feature is disabled.

The frame-error-counter (FEC) is cleared after each expiration of the time  $t_{\text{silence}}$  whenever the frame detection logic is enabled.

### 2.9.5 CAN receive only mode

With the CAN\_rec\_only bit in Control register 4 it is possible to disable the CAN Transmitter in active mode. In this mode it is possible to listen to the bus but not sending to it. The Receiver termination network is still activated in this mode.

### 2.9.6 CAN looping mode

If the CAN\_Loop\_en bit in Control register 4 is set the TxDC input is mapped directly to the RxDC pin. This mode can be used in combination with the CAN Receive only mode, to run diagnosis for the CAN protocol handler of the micro controller.

## 2.10 Serial Peripheral Interface (ST SPI Standard 3.0)

A 24 bit SPI is used for bi-directional communication with the micro controller.

During active mode, the SPI

- triggers the watchdog
- controls the modes and status of all L99PM72GXP modules (incl. input and output drivers)
- provides driver output diagnostic
- provide L99PM72GXP diagnostic (incl. over temperature warning, L99PM72GXP operation status)

**The SPI can be driven by a micro controller with its SPI peripheral running in following mode: CPOL = 0 and CPHA = 0.**

For this mode input data is sampled by the low to high transition of the clock CLK, and output data is changed from the high to low transition of CLK.

This device is not limited to micro controller with a built-in SPI. Only three CMOS-compatible output pins and one input pin are needed to communicate with the device. A fault condition can be detected by setting CSN to low. If CSN = 0, the DO pin reflects the global error flag (fault condition) of the device.

### Chip Select Not (CSN)

The input pin is used to select the serial interface of this device. When CSN is high, the output pin (DO) is in high impedance state. A low signal activates the output driver and a



serial communication can be started. The state during CSN = 0 is called a communication frame.

If CSN = low for  $t > t_{\text{CSNfail}}$  the DO output is switched to high impedance in order to not block the signal line for other SPI nodes.

### Serial Data In (DI)

The input pin is used to transfer data serial into the device. The data applied to the DI are sampled at the rising edge of the CLK signal and shifted into an internal 24 bit shift register. At the rising edge of the CSN signal the contents of the shift register is transferred to Data Input Register. The writing to the selected Data Input Register is only enabled if exactly 24 bits are transmitted within one communication frame (i.e. CSN low). If more or less clock pulses are counted within one frame the complete frame is ignored. This safety function is implemented to avoid an activation of the output stages by a wrong communication frame.

*Note: Due to this safety functionality a daisy chaining of SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected IC's is recommended.*

### Serial Data Out (DO)

The data output driver is activated by a logical low level at the CSN input and goes from high impedance to a low or high level depending on the global error flag (fault condition). The first rising edge of the CLK input after a high to low transition of the CSN pin transfers the content of the selected status register into the data out shift register. Each subsequent falling edge of the CLK shifts the next bit out.

### Serial Clock (CLK)

The CLK input is used to synchronize the input and output serial bit streams. The data input (DI) is sampled at the rising edge of the CLK and the data output (DO) changes with the falling edge of the CLK signal. The SPI can be driven with a CLK Frequency up to 1 MHz.

## 3 Protection and diagnosis

### 3.1 Power supply fail

Overvoltage and undervoltage detection on  $V_S$

#### 3.1.1 $V_S$ overvoltage

If the supply voltage  $V_S$  reaches the over voltage threshold ( $V_{SOV}$ ):

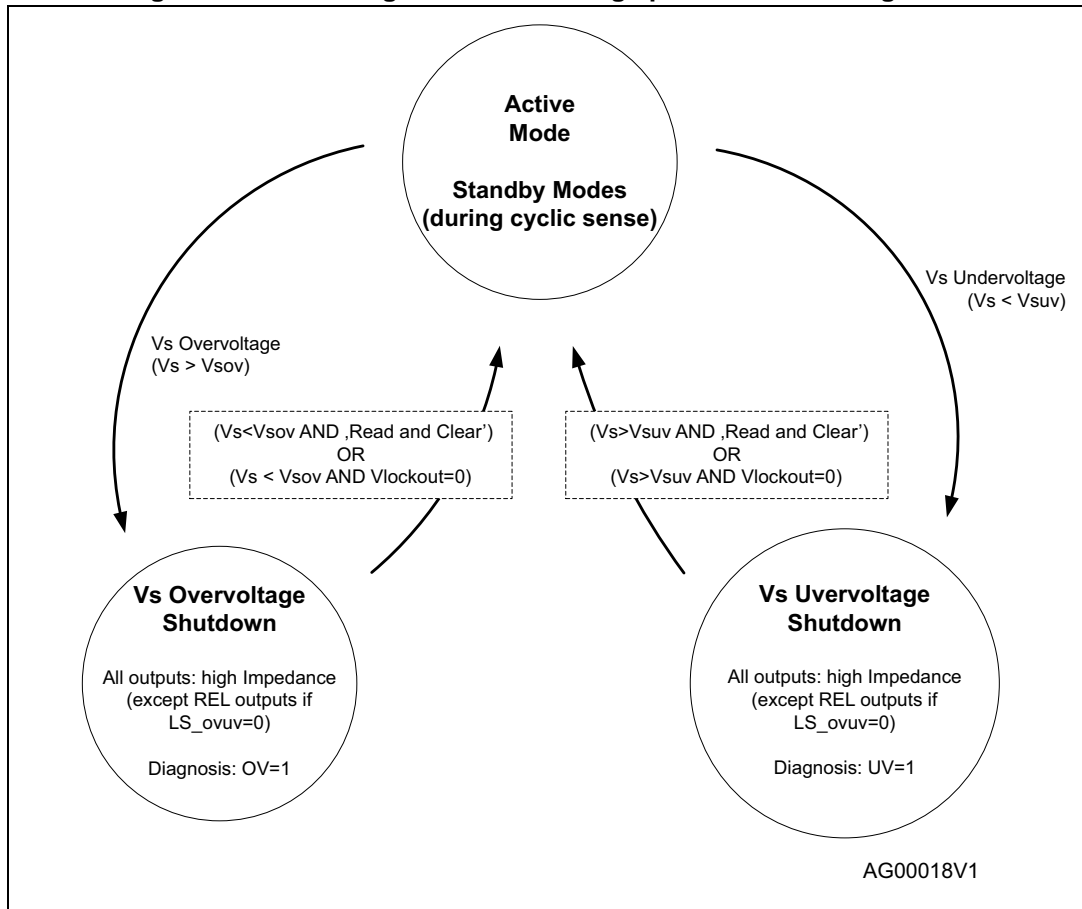
- Outputs  $OUT_x$ ,  $REL_x$  and LIN are switched to high impedance state (load protection). CAN is not disabled. Recovery of outputs when the overvoltage condition disappears is depending on the setting of VLOCK\_OUT\_EN bit in Control Register 4.
  - VLOCK\_OUT\_EN = 1: Outputs are off until read and clear SR3.
  - VLOCK\_OUT\_EN = 0: Outputs switch automatically on when overvoltage condition disappears.
- The over voltage bit is set and can be cleared with a 'Read and Clear' command. The overvoltage bit is removed automatically if VLOCK\_OUT\_EN = 0 and the overvoltage condition disappears.
- Outputs REL1,2 can be excluded from a shutdown in case of overvoltage by SPI (LS\_OV/UV\_shutdown\_en in CR4)

#### 3.1.2 $V_S$ undervoltage

If the supply voltage  $V_S$  drops below the under voltage threshold voltage ( $V_{SUV}$ )

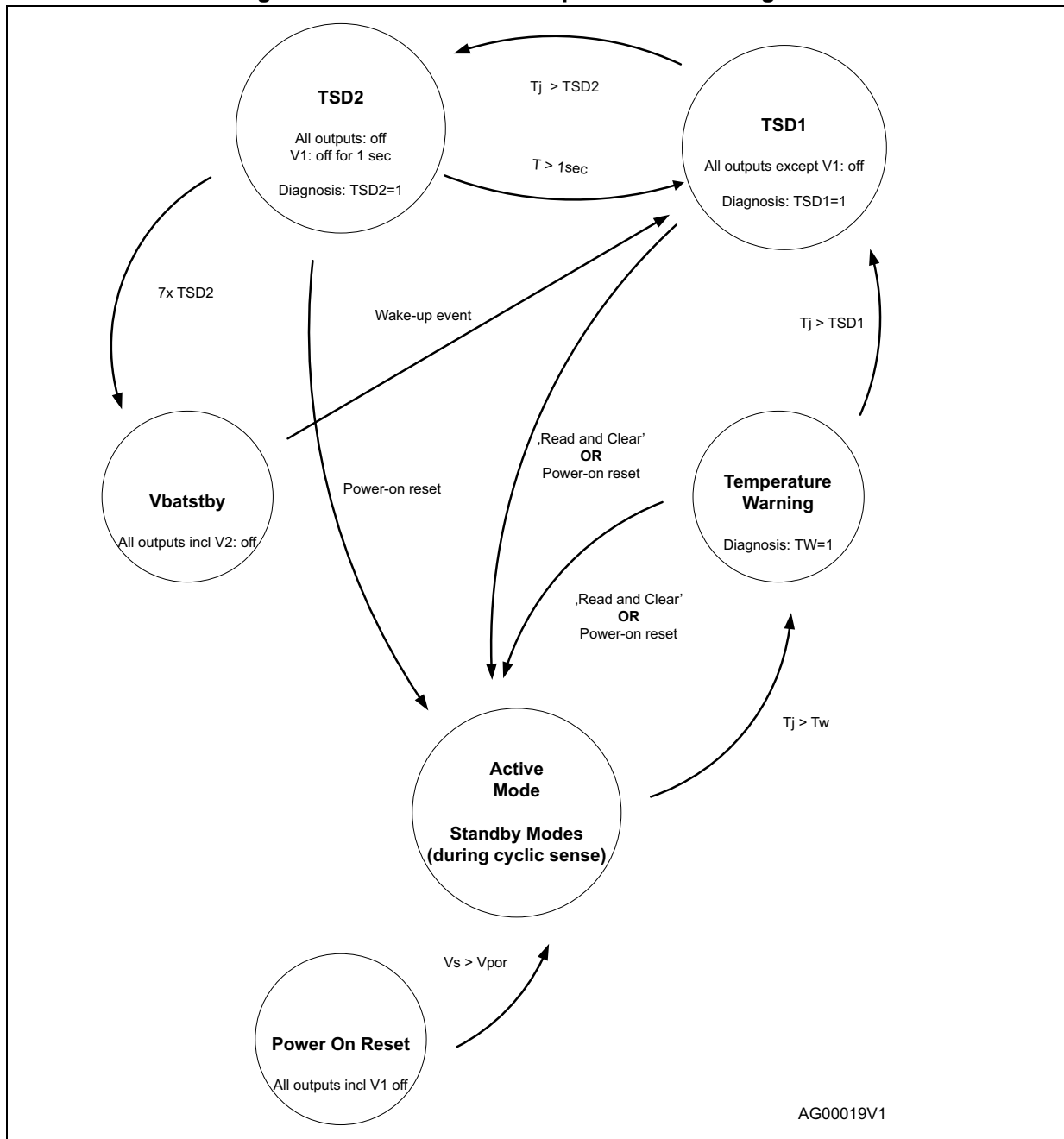
- Outputs  $OUT_x$ ,  $REL_x$  and LIN are switched to high impedance state (load protection). CAN is not disabled. Recovery of outputs when the undervoltage condition disappears is depending on the setting of VLOCK\_OUT\_EN bit.
  - VLOCK\_OUT\_EN = 1: Outputs are off until read and clear SR3.
  - VLOCK\_OUT\_EN = 0: Outputs switch on automatically when undervoltage condition disappears.
- The undervoltage bit is set and can be cleared with a 'Read and Clear' command. The undervoltage bit is removed automatically if VLOCK\_OUT\_EN = 0 and the undervoltage condition disappears
- Outputs REL1,2 can be excluded from a shutdown in case of undervoltage by SPI (LS\_OV/UV\_shutdown\_en in CR4)

Figure 22. Overvoltage and undervoltage protection and diagnosis



### 3.2 Temperature warning and thermal shut-down

Figure 23. Thermal shutdown protection and diagnosis



Note: The Thermal State machine recovers the same state were it was before entering Standby Mode. In case of a TSD2 it enters TSD1 state.

### 3.3 High side driver outputs

The component provides a total of 4 high side outputs Out1...4, (7  $\Omega$  typ. at 25°C) to drive e.g. LED's or hall sensors and 1 high side output OUT\_HS with 1  $\Omega$  typ. at 25°C).

- The high side outputs switch off in case of:
- $V_S$  overvoltage and undervoltage
- Overcurrent
- Overtemperature (TSD1) with pre warning<sup>(c)</sup>

In case of overcurrent or overtemperature (TSD1) condition, the drivers switch off. The according status bit is latched and can be read and optionally cleared by SPI. The drivers remain off until the status is cleared.

In case overvoltage or undervoltage condition, the drivers are switched off. The according status bit is latched and can be read and optionally cleared by SPI. If the VLOCK\_OUT\_EN bit (Control Register 4) is set to '1' the drivers remain off until the status is cleared. If the VLOCK\_OUT\_EN bit is set to '0' the drivers switch on automatically if the error condition disappears.

In case of open load condition, the according status register is latched. The status can be read and optionally cleared by SPI. The High sides are not switched off.

For OUT\_HS the auto recovery feature (OUTHHS\_rec\_en bit Control Register 4) can be enabled. If this bit is set to '1' the driver automatically restarts from a overload condition. This overload recovery feature is intended for loads which have an initial current higher than the over current limit of the output (e.g. Inrush current of cold light bulbs). During auto recovery mode the over current status bit can not be read from SPI.

The device itself cannot distinguish between a real overload and a non linear load like a light bulb. A real overload condition can only be qualified by time. As an example, the micro controller can switch on light bulbs by setting the over current recovery bit for the first 50 ms. After clearing the recovery bit, the output is automatically disabled if the overload condition still exists.

In case of a fail safe condition, the high side drivers are switched off. The control bits are set to default values. (except OUT3/FSO if it is used as a High Side Driver Output)

*Note:* The maximum voltage and current applied to the High Side Outputs is specified in 2.1 'Absolute Maximum Ratings'. Appropriate external protection may be required in order to respect these limits under application conditions.

Each high side driver can be driven whether with a PWM signal or with a internal Timer (see [Table 8](#)).

For more details please refer to [Section 6.2.3: Control Register 1](#)

**Table 8. PWM configuration for high-side outputs**

| High side output | PWM channel | Internal timer |
|------------------|-------------|----------------|
| OUT1             | PWM 1       | Timer 1        |
| OUT2             | PWM 2       | Timer 2        |

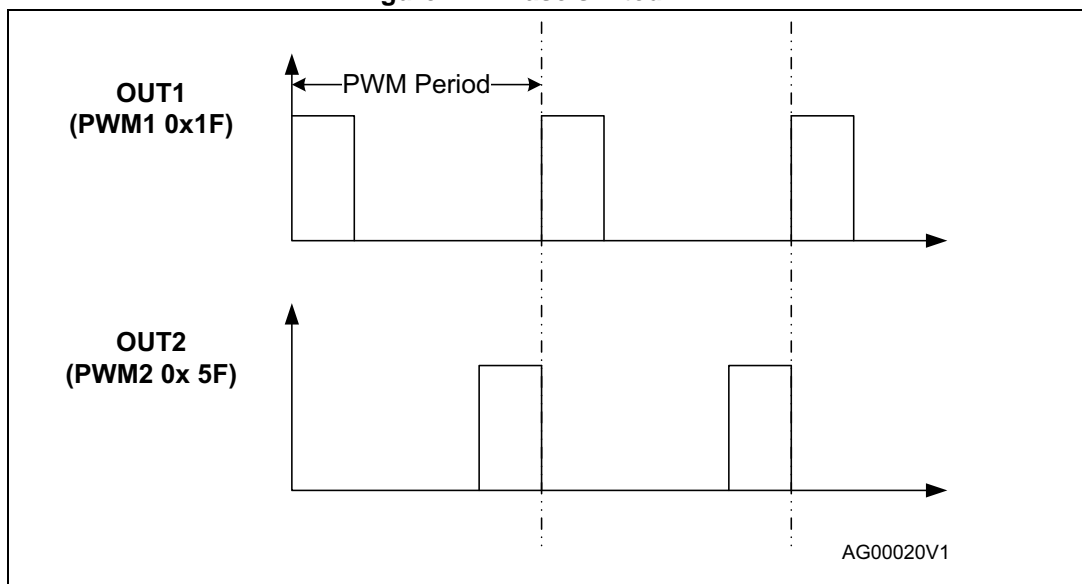
c. Except OUT3 when configured as FSO

**Table 8. PWM configuration for high-side outputs (continued)**

| High side output | PWM channel   | Internal timer    |
|------------------|---------------|-------------------|
| OUT3             | PWM 3         | -                 |
| OUT4             | PWM 4         | Timer 2           |
| OUTH5            | PWM 3 / PWM 4 | Timer 1 / Timer 2 |

The PWM 1/3 channels start a PWM period with the ON phase, while the PWM 2/4 channels start with the OFF phase. In this way it is possible to use the 4 PWM channels in a phase shifted way. The picture below shows this feature with a duty cycle of 25% for both PWM channels.

**Figure 24. Phase shifted PWM**



### 3.4 Low side driver outputs REL1, REL2

The outputs REL1, REL2 ( $R_{DSon} = 2 \Omega$  typ. @25 °C) are specially designed to drive relay loads.

The outputs provide an active output zener clamping (45 V typ.) feature for the demagnetization of the relay coil, even though a load dump condition exists.

For Fail\_safe reasons the relay drivers are linked with the fail safe operation: In case of entering the Fail Safe Mode, the relay drivers switch off and the SPI control bits are set to default (i.e. driver is off).

The low side drivers switch off in case of:

- $V_S$  overvoltage and undervoltage
- Overcurrent
- Overtemperature with pre warning

In case of overload or overtemperature (TSD1) condition, the drivers switch off. The according status bit is latched and can be read and optionally cleared by SPI. The drivers remain off until the status is cleared.

In case  $V_S$  overvoltage or undervoltage condition, the drivers are switched off. The according status bit is latched and can be read and optionally cleared by SPI. If the VLOCK\_OUT\_EN bit (Control Register 4) is set to '1' the drivers remain off until the status is cleared. If the VLOCK\_OUT\_EN bit is set to '0' the drivers are switched on automatically if the error condition disappears.

With the LS\_OV/UV\_shutdown\_en bit (Control Register 4) the drivers can be excluded from a switch off in case of  $V_S$  overvoltage or undervoltage. If the bit is set to '1' the driver switches off, otherwise the drivers remain on.

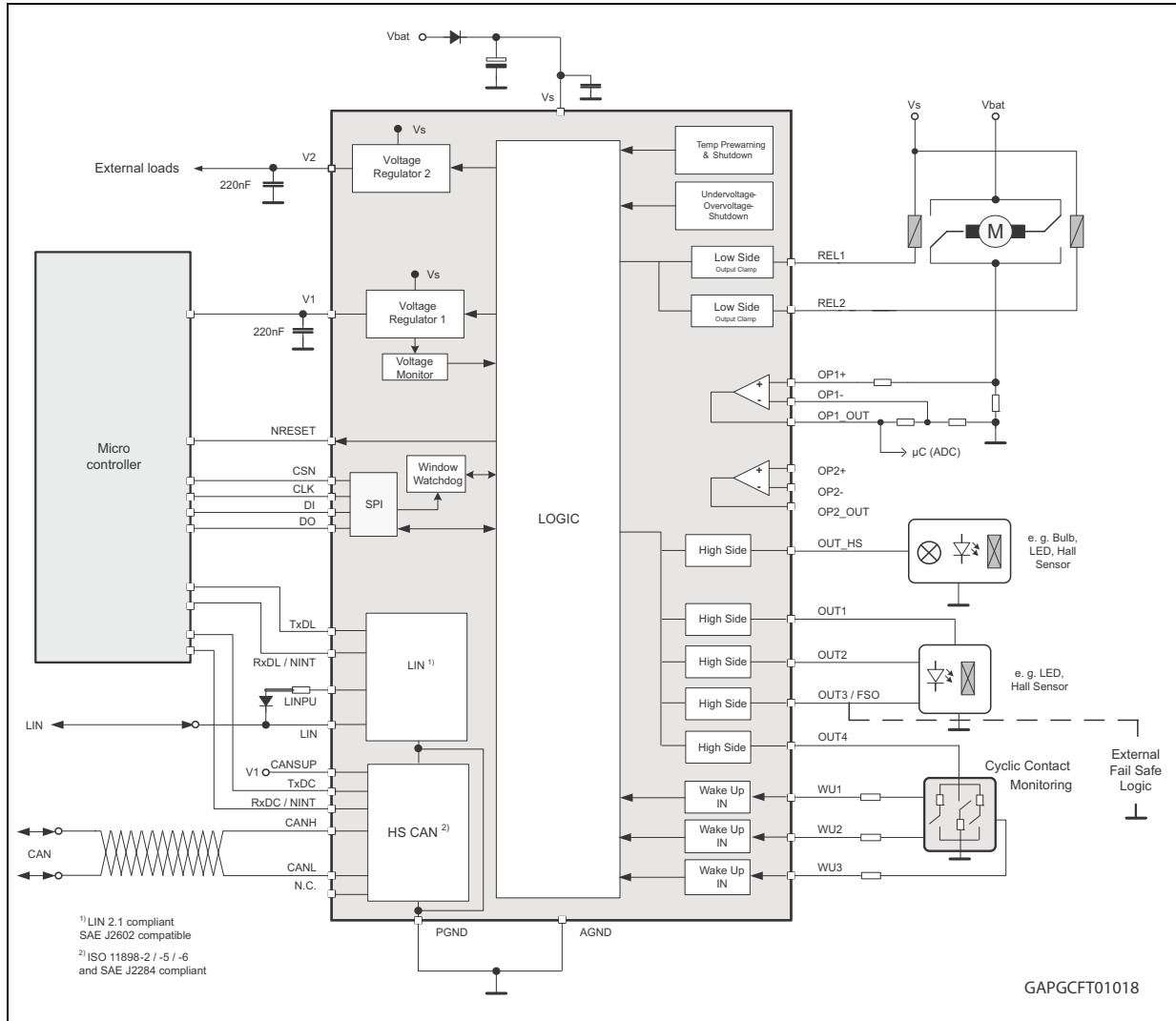
### 3.5 SPI diagnosis

Digital diagnosis features are provided by SPI (for details please refer to [Section 6.2: SPI registers](#))

- $V_1$  reset threshold programmable
- Overtemperature including. pre warning
- Open load separately for each output stage except REL1/REL2
- Overload status separately for each output stage
- $V_S$ -supply overvoltage/undervoltage
- $V_1$  and  $V_2$  fail bit
- $V_2$  output short to GND
- Status of the WU1...3
- Wake-up sources (CAN, LIN, SPI, Timer, WU1...3)
- Chip reset bit (start from power-on reset)
- Number of unsuccessful  $V_1$  restarts after thermal shutdown
- Number of sequential watchdog failures
- LIN diagnosis (permanent recessive/dominant, dominant TxD)
- CAN diagnosis (permanent recessive/dominant, dominant TxD, recessive RXD)
- Device State (wake-up from  $V_{1\_standby}$  or  $V_{bat\_standby}$ )
- Forced  $V_{bat\_standby}$  after WD-fail, forced  $V_{bat\_standby}$  after overtemperature
- Watchdog timer state (diagnosis of watchdog)
- Failsafe status
- SPI communication error
- Diagnosis of selective wake functionality according to ISO 11898-6

# 4 Typical application

Figure 25. Typical application diagram



1. In case a LIN/CAN conformance test has to be executed on the device, some capacitances have to be placed on the Fixed-Function-Unit pins:
  - 22 nF (low ESR and close to the pin) for all power outputs (OUT\_HS, OUT1 ... 4, REL1 and REL2) and also for the wake-up inputs, if they go out of the PCB.
  - 47 µF and a 100 nF low ESR capacitance (close to the pin) at the power supply Vs.



## 5 Electrical specifications

### 5.1 Absolute maximum ratings

All maximum ratings are absolute ratings. Leaving the limitation of any of these values may cause an irreversible damage of the integrated circuit.

Loss of ground or ground shift with externally grounded loads: ESD structures are configured for nominal currents only. If external loads are connected to different grounds, the current load must be limited to this nominal current.

**Table 9. Absolute maximum ratings**

| Symbol   | Parameter / Test condition                               | Value [DC Voltage]                | Unit |
|--|--|-----------------------------------|------|
| $V_S$  | DC supply voltage / "jump start"                         | -0.3 to +28                       | V    |
|  | Load dump  | -0.3 to +40                       | V    |
| $V_1$  | stabilized supply voltage, logic supply                  | -0.3 to $(V_1 + 0.3) - V_1 < V_S$ | V    |
| $V_2$  | stabilized supply voltage                                | -0.3 to +28                       | V    |
| $V_{DI}, V_{CLK}, V_{DO}, V_{RXDL}, V_{NRESET}, V_{RXDC}, V_{CSN}$ | Logic input / output voltage range                       | -0.3 to $V_1 + 0.3$               | V    |
| $V_{TXDC}, V_{TXDL}$   | Multi Level Inputs                                       | -0.3 to $V_S + 0.3$               | V    |
| $V_{REL1}, V_{REL2}$   | Low side output voltage range                            | -0.3 to +40                       | V    |
| $V_{OUT1..4}, V_{OUT\_HS}$   | High side output voltage range                           | -0.3 to $V_S + 0.3$               | V    |
| $V_{WU1..3}$   | Wake up input voltage range                              | -0.3 to $V_S + 0.3$               | V    |
| $V_{OP1P}, V_{OP1M}, V_{OP2P}, V_{OP2M}$                           | Opamp1 input voltage range<br>Opamp2 input voltage range | -0.3 to $V_1 + 0.3$               | V    |
| $V_{OPOUT1}, V_{OPOUT2}$   | Analog output voltage range                              | -0.3 to $V_S + 0.3$               | V    |
| $V_{LIN}, V_{LINPU}$   | LIN bus I/O voltage range                                | -20 to +40                        | V    |
| $I_{Input}$  | Current injection into $V_S$ related input pins          | 20                                | mA   |
| $I_{out\_inj}$   | Current injection into $V_S$ related outputs             | 20                                | mA   |
| $V_{CANSUP}$   | CAN supply   | -0.3 to +5.25                     | V    |
| $V_{CANH}, V_{CANL}$   | CAN bus I/O voltage range                                | -27 to +40                        | V    |
| $V_{Pin6}$   | Not connected  | -0.3 to $V_S + 0.3$               | V    |

## 5.2 ESD protection

Table 10. ESD protection

| Parameter                      | Value  | Unit |
|--------------------------------|--|------|
| All pins <sup>(1)</sup>        | +/-2   | kV   |
| All output pins <sup>(2)</sup> | +/-4   | kV   |
| LIN                            | +/-8 <sup>(2)</sup><br>+/-10 <sup>(3)</sup><br>+/-6 <sup>(4)</sup> | kV   |
| CAN_H, CAN_L                   | +/-8 <sup>(2)</sup><br>+/-6 <sup>(4)</sup>                         | kV   |
| All pins <sup>(5)</sup>        | +/-500   | V    |
| Corner pins <sup>(5)</sup>     | +/-750   | V    |
| All pins <sup>(6)</sup>        | +/-200   | V    |

1. HBM (Human Body Model, C = 100 pF, R = 1.5 kΩ) according to MIL 883C, Method 3015.7 or EIA/JESD22A114-A.
2. HBM with all none zapped pins grounded.
3. Indirect ESD test according to IEC 61000-4-2 (C = 150 pF, R = 330 Ω) and 'Hardware Requirements for LIN, CAN and Flexray Interfaces in Automotive Applications' (version 1.1, 2009-12-02).
4. Direct ESD test according to IEC 61000-4-2 (C = 150pF, R = 330 Ω) and 'Hardware Requirements for LIN, CAN and Flexray Interfaces in Automotive Applications' (version 1.1, 2009-12-02).
5. Charged device model.
6. Machine model: C = 200 pF; R = 0 Ω

## 5.3 Thermal data

Table 11. Operating junction temperature

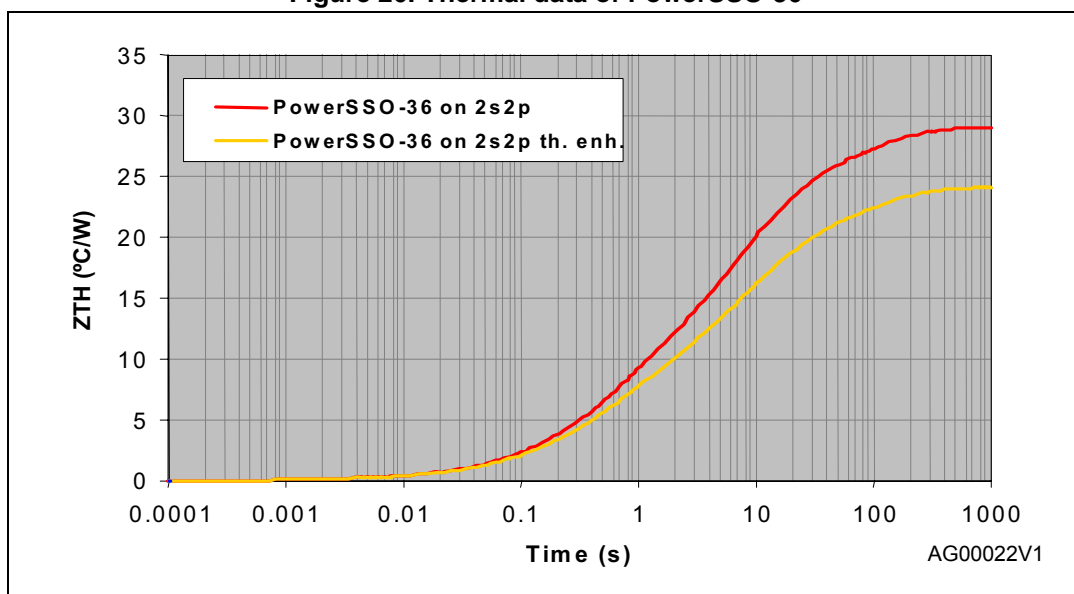
| Symbol               | Parameter                           | Value                         | Unit |
|----------------------|-------------------------------------|-------------------------------|------|
| T <sub>j</sub>       | Operating junction temperature      | -40 to 150                    | °C   |
| R <sub>thj_amb</sub> | Thermal resistance junction ambient | See <a href="#">Figure 29</a> | K/W  |

Table 12. Temperature warning and thermal shutdown

| Symbol                | Parameter                                  |                               | Min. | Typ. | Max. | Unit |
|-----------------------|--|-------------------------------|------|------|------|------|
| T <sub>W_ON</sub>     | Thermal over temperature warning threshold | T <sub>j</sub> <sup>(1)</sup> | 120  | 130  | 140  | °C   |
| T <sub>SD1_OFF</sub>  | Thermal shut-down junction temperature 1   | T <sub>j</sub> <sup>(1)</sup> | 130  | 140  | 150  | °C   |
| T <sub>SD2_OFF</sub>  | Thermal shut-down junction temperature 2   | T <sub>j</sub> <sup>(1)</sup> | 150  | 160  | 170  | °C   |
| T <sub>SD12_hys</sub> |  | Hysteresis                    |      | 5    |      | °C   |

1. Non-overlapping.

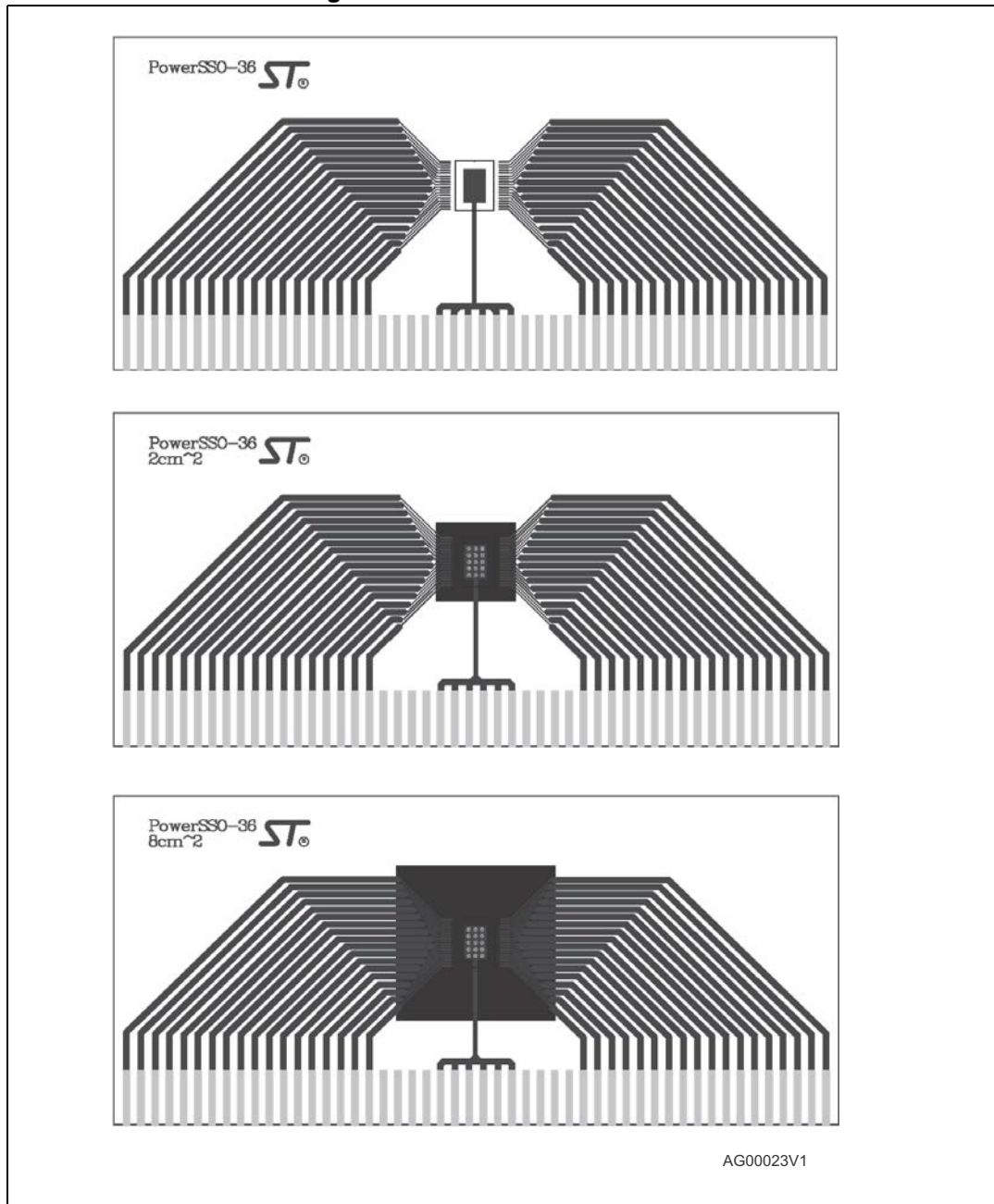
Figure 26. Thermal data of PowerSSO-36



## 5.4 Package and PCB thermal data

### 5.4.1 PowerSSO-36 thermal data

Figure 27. PowerSSO-36 PC board



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (board finish thickness 1.6 mm +/- 10% board double layer, board dimension 129x60, board Material FR4, Cu thickness 0.070 mm (front and back side), thermal via separation 1.2 mm, thermal via diameter 0.3 mm +/- 0.08 mm, Cu thickness on vias 0.025 mm).

Figure 28. PowerSSO-36 thermal resistance junction to ambient vs PCB copper area (V<sub>1</sub> ON)

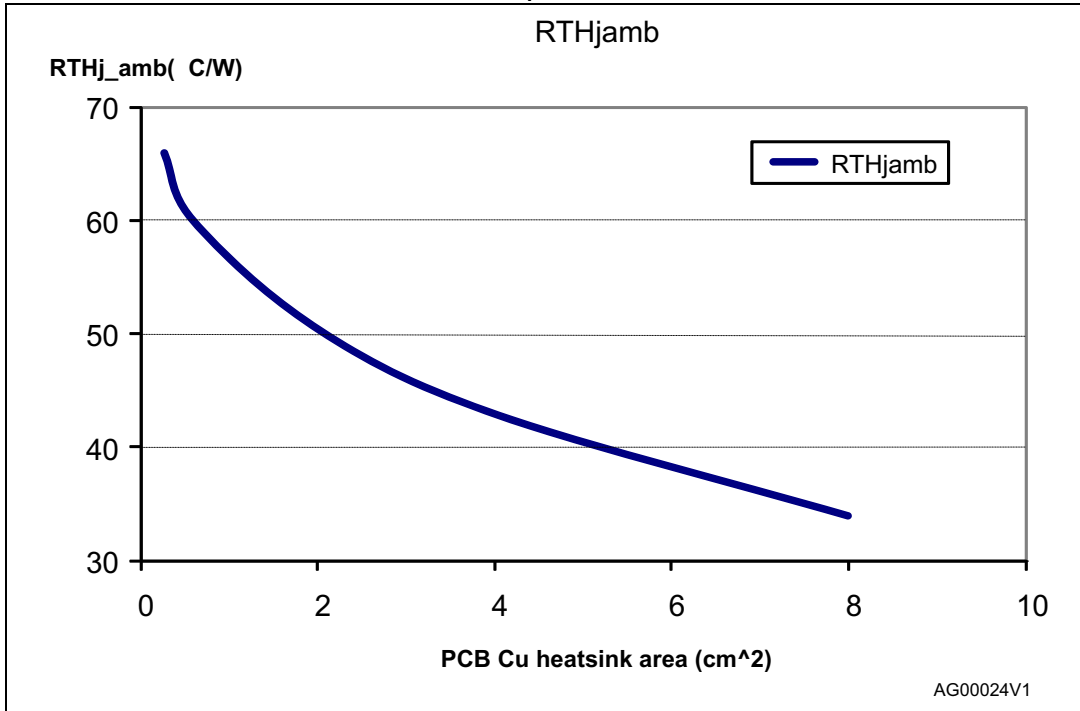


Figure 29. PowerSSO-36 thermal impedance junction to ambient vs PCB copper area (single pulse with V<sub>1</sub> ON)

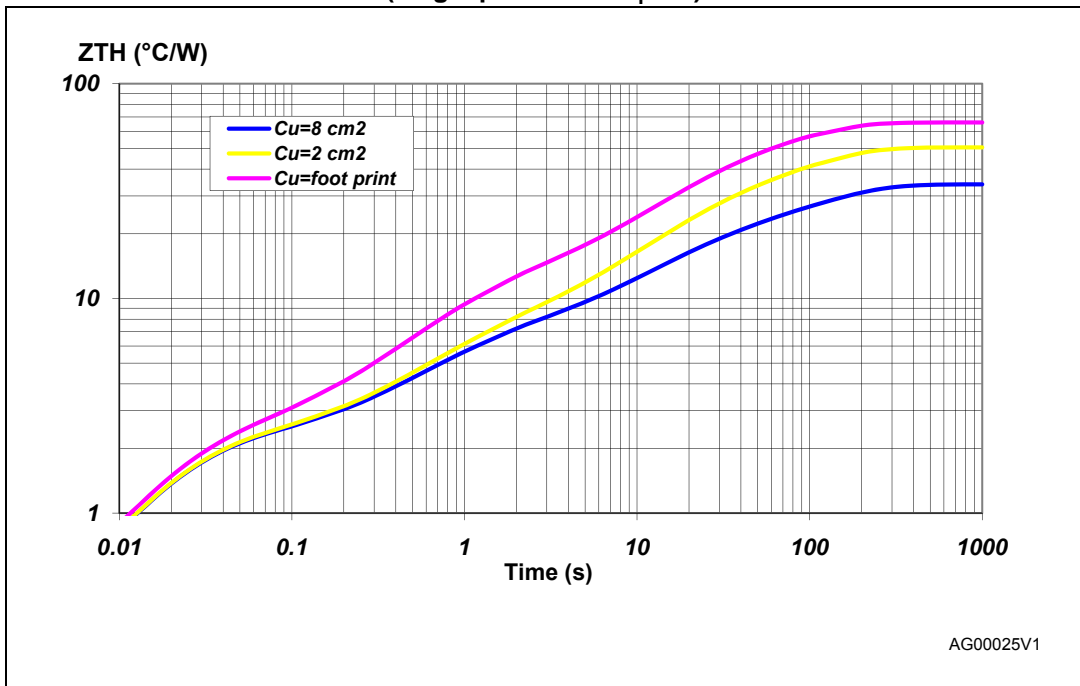
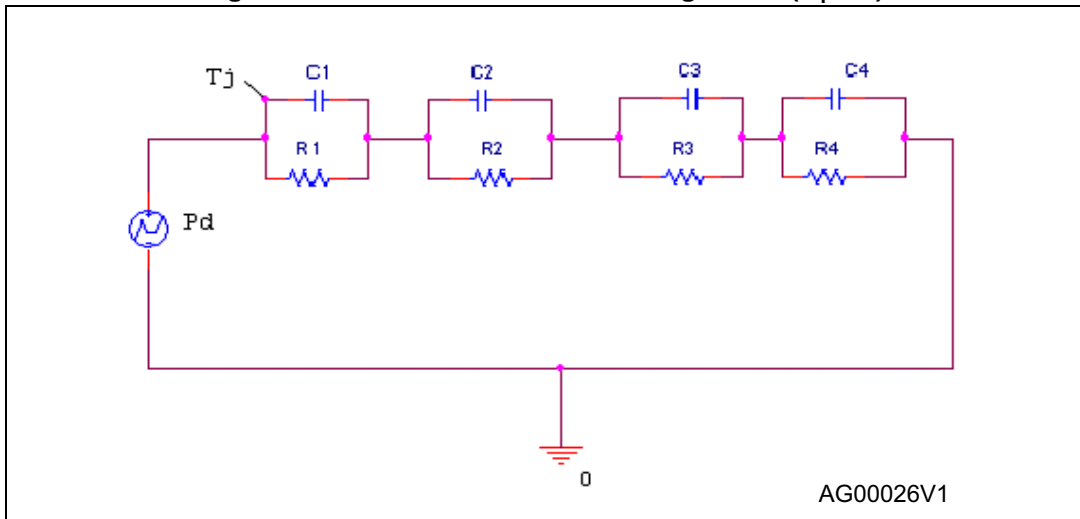


Figure 30. PowerSSO-36 thermal fitting model (V<sub>1</sub> ON)



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Table 13. Thermal parameter

| Area/island (cm <sup>2</sup> ) | Footprint | 2    | 8   |
|--------------------------------|-----------|------|-----|
| R1 (°C/W)                      | 2         |      |     |
| R2 (°C/W)                      | 8         | 4    | 4   |
| R3 (°C/W)                      | 20        | 15.5 | 10  |
| R4 (°C/W)                      | 36        | 29   | 18  |
| C1 (W.s/°C)                    | 0.01      |      |     |
| C2 (W.s/°C)                    | 0.1       | 0.2  | 0.2 |
| C3 (W.s/°C)                    | 0.8       | 1    | 1.5 |
| C4 (W.s/°C)                    | 2         | 3    | 6   |

## 5.5 Electrical characteristics

### 5.5.1 Supply and supply monitoring

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.  $T_j = -40^{\circ}\text{C}$  to  $130^{\circ}\text{C}$ , unless otherwise specified.

**Table 14. Supply and supply monitoring**

| Symbol                       | Parameter   | Test condition   | Min. | Typ.                  | Max. | Unit          |
|------------------------------|---|--|------|-----------------------|------|---------------|
| $V_{\text{SUV}}$             | $V_S$ undervoltage threshold  | $V_S$ increasing / decreasing  | 5.11 |                       | 5.81 | V             |
| $V_{\text{hyst\_UV}}$        | $V_S$ undervoltage hysteresis   |  | 0.05 | 0.11                  | 0.16 | V             |
| $V_{\text{SOV}}$             | $V_S$ overvoltage threshold   | $V_S$ increasing / decreasing  | 18.5 |                       | 22   | V             |
| $V_{\text{hyst\_OV}}$        | $V_S$ overvoltage hysteresis  | hysteresis   | 0.5  | 1                     | 1.5  | V             |
| $t_{\text{ovuv\_filt}}$      | $V_S$ overvoltage /undervoltage filter time   |  |      | $64 * T_{\text{osc}}$ |      |               |
| $I_{V(\text{act})}$          | Current consumption in active mode  | $V_S = 12\text{ V}$ ; TxDC = high; TxDL = high; $V_1 = \text{ON}$ ; $V_2 = \text{ON}$ ; HS/LS Driver OFF           |      | 6                     | 12   | mA            |
| $I_{V(\text{BAT})}$          | Current consumption in $V_{\text{Bat\_standby}}$ mode <sup>(1)</sup>  | $V_S = 12\text{V}$ ; both voltage regulators deactivated; HS/LS driver OFF; no CAN communication                   | 8    | 12                    | 28   | $\mu\text{A}$ |
| $I_{V(\text{BAT})\text{CS}}$ | Current consumption in $V_{\text{Bat\_standby}}$ mode with cyclic sense enabled <sup>(1)</sup>  | $V_S = 12\text{ V}$ ; both voltage regulators deactivated; $T = 50\text{ ms}$ ; $t_{\text{ON}} = 100\ \mu\text{s}$ | 40   | 75                    | 125  | $\mu\text{A}$ |
| $I_{V(\text{BAT})\text{CW}}$ | Current consumption in $V_{\text{Bat\_standby}}$ mode with cyclic wake enabled <sup>(1)</sup>   | $V_S = 12\text{ V}$ ; both voltage regulators deactivated during standby phase                                     | 40   | 75                    | 125  | $\mu\text{A}$ |
| $I_{V(V1\text{stby})}$       | Current consumption in $V_1$ standby mode <sup>(1)</sup>  | $V_S = 12\text{ V}$ ; voltage regulator $V_1$ active ( $I_{V1} < I_{\text{CMP}}$ ); HS/LS driver OFF               | 16   | 51                    | 76   | $\mu\text{A}$ |
| $I_{V(\text{SW})}$           | Current consumption in standby mode but selective wakeup enabled and CAN communication on the bus (PN_TRX_selective_Sleep) <sup>(1)</sup> | $V_S = 12\text{ V}$ ; both voltage regulators deactivated; HS/LS driver OFF  |      |                       | 1200 | $\mu\text{A}$ |

1. Conditions for specified current consumption:

$$V_{\text{LIN}} > (V_S - 1.5\text{ V})$$

$$(\text{CAN\_H} - \text{CAN\_L}) < 0.4\text{ V} \text{ or } (\text{CAN\_H} - \text{CAN\_L}) > 1.2\text{ V}$$

$$V_{\text{WU}} < 1\text{ V} \text{ or } V_{\text{WU}} > (V_S - 1.5\text{V})$$

The current consumption in standby modes with cyclic sense can be calculated using the following formulas:

$$I_{V(\text{BAT})\text{CS}} = I_{V(\text{BAT})} + 55\ \mu\text{A} + (2\ \text{mA} * (t_{\text{ON}} + 100\ \mu\text{s}) / T)$$

$$I_{(V1)\text{CS}} = I_{V1} + 55\ \mu\text{A} + (2\ \text{mA} * (t_{\text{ON}} + 100\ \mu\text{s}) / T)$$

### 5.5.2 Oscillator

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.  $4.5\text{ V} \leq V_S \leq 28\text{ V}$ ;  $T_j = -40^\circ\text{C}$  to  $130^\circ\text{C}$ , unless otherwise specified.

**Table 15. Oscillator**

| Symbol           | Parameter             | Test condition | Min. | Typ. | Max. | Unit |
|------------------|-----------------------|----------------|------|------|------|------|
| $F_{\text{CLK}}$ | Oscillation frequency |                | 0.80 | 1.0  | 1.35 | MHz  |

All outputs open;  $T_j = -40^\circ\text{C}$  to  $130^\circ\text{C}$ , unless otherwise specified.

### 5.5.3 Power-on reset ( $V_S$ )

**Table 16. Power-on reset ( $V_S$ )**

| Symbol           | Parameter                  | Test condition                  | Min. | Typ. | Max. | Unit |
|------------------|----------------------------|---------------------------------|------|------|------|------|
| $V_{\text{POR}}$ | $V_{\text{POR}}$ threshold | $V_S$ increasing                |      | 3.45 | 4.5  | V    |
|                  |                            | $V_S$ decreasing <sup>(1)</sup> | 2.35 |      | 3.5  | V    |

1. This threshold is valid if  $V_S$  had already reached 7 V previously.

### 5.5.4 Voltage regulator $V_1$

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.  $4.5\text{ V} \leq V_S \leq 28\text{ V}$ ;  $T_j = -40^\circ\text{C}$  to  $130^\circ\text{C}$ , unless otherwise specified.

**Table 17. Voltage regulator  $V_1$**

| Symbol              | Parameter   | Test condition   | Min. | Typ. | Max. | Unit |
|---------------------|---|--|------|------|------|------|
| $V_1$               | Output voltage                                      |  |      | 5.0  |      | V    |
|                     | Output voltage tolerance active mode                | $I_{\text{LOAD}} = 4\text{ mA}$ to $100\text{ mA}$ ;<br>$V_S = 13.5\text{ V}$        | -2   |      | 2    | %    |
| $V_{\text{hc1}}$    | Output voltage tolerance; active mode; high current | $I_{\text{LOAD}} = 100\text{ mA}$ to $250\text{ mA}$ ;<br>$V_S = 13.5\text{ V}$      | -3   |      | 3    | %    |
|                     |   | $I_{\text{LOAD}} = 250\text{ mA}$ ;<br>$V_S = 13.5\text{ V}$                         | -5   |      | 5    | %    |
| $V_{\text{STB1}}$   | Output voltage tolerance $V_{1\_standby}$ mode      | $I_{\text{LOAD}} = 0\text{ }\mu\text{A}$ to $4\text{ mA}$ ;<br>$V_S = 13.5\text{ V}$ | -2   |      | 4    | %    |
| $V_{\text{DP1}}$    | Drop-out voltage                                    | $I_{\text{LOAD}} = 50\text{ mA}$ ; $V_S = 5\text{ V}$                                |      | 0.2  | 0.4  | V    |
|                     |   | $I_{\text{LOAD}} = 100\text{ mA}$ ; $V_S = 4.5\text{ V}$                             |      | 0.2  | 0.5  | V    |
|                     |   | $I_{\text{LOAD}} = 100\text{ mA}$ ; $V_S = 5\text{ V}$                               |      | 0.3  | 0.5  | V    |
|                     |   | $I_{\text{LOAD}} = 150\text{ mA}$ ; $V_S = 4.5\text{ V}$                             |      | 0.45 | 0.6  | V    |
|                     |   | $I_{\text{LOAD}} = 150\text{ mA}$ ; $V_S = 5.0\text{ V}$                             |      | 0.45 | 0.6  | V    |
| $I_{\text{CC1}}$    | Output current in active mode                       | Max. continuous load current   |      |      | 250  | mA   |
| $I_{\text{CCmax1}}$ | Short circuit output current                        | Current limitation   | 340  | 600  | 900  | mA   |



Table 17. Voltage regulator  $V_1$  (continued)

| Symbol         | Parameter                                      | Test condition    | Min.                | Typ. | Max. | Unit          |
|----------------|--|-------------------|---------------------|------|------|---------------|
| $C_{load1}$    | Load capacitor 1                               | Ceramic (+/- 20%) | 0.22 <sup>(1)</sup> |      |      | $\mu\text{F}$ |
| $t_{TSD}$      | $V_1$ deactivation time after thermal shutdown |                   |                     | 1    |      | sec           |
| $I_{CMP\_ris}$ | Current comp. rising threshold                 | Rising current    | 1.0                 | 2.5  | 4.0  | mA            |
| $I_{CMP\_fal}$ | Current comp. falling threshold                | Falling current   | 0.8                 | 1.95 | 3.1  | mA            |
| $I_{CMP\_hys}$ | Current comp. hysteresis                       |                   |                     | 0.5  |      | mA            |
| $V_{1fail}$    | $V_1$ fail threshold                           | $V_1$ forced      |                     | 2    |      | V             |
| $t_{V1fail}$   | $V_1$ fail filter time                         |                   |                     | 2    |      | $\mu\text{s}$ |
| $t_{V1short}$  | $V_1$ short filter time                        |                   |                     | 4    |      | ms            |

1. Nominal capacitor value required for stability of the regulator. Tested with 220nF ceramic (+/- 20%). Capacitor must be located close to the regulator output pin.

### 5.5.5 Voltage regulator $V_2$

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.  $4.5\text{ V} \leq V_S \leq 28\text{ V}$ ;  $T_j = -40^\circ\text{C}$  to  $130^\circ\text{C}$ , unless otherwise specified.

Table 18. Voltage regulator  $V_2$ 

| Symbol       | Parameter   | Test condition   | Min.                | Typ. | Max. | Unit          |
|--------------|---|--|---------------------|------|------|---------------|
| $V_2$        | Output voltage                                      |  |                     | 5.0  |      | V             |
| $V_2$        | Output voltage tolerance; active mode               | $I_{LOAD} = 1\text{ mA to }50\text{ mA}$ ;<br>$V_S = 13.5\text{ V}$  | -3                  |      | 3    | %             |
| $V_{hc1}$    | Output voltage tolerance; active mode               | $I_{LOAD} = 50\text{ mA to }80\text{ mA}$ ;<br>$V_S = 13.5\text{ V}$ | -4                  |      | 4    | %             |
| $V_2$        | Output voltage tolerance; active mode; high current | $I_{LOAD} = 100\text{ mA}$ ; $V_S = 13.5\text{ V}$                   | -6                  |      | 6    | %             |
| $V_{STB2}$   | Output voltage tolerance<br>$V_{1\_standby}$ mode   | $I_{LOAD} = 1\text{ mA}$ ; $V_S = 13.5\text{ V}$                     | -6.5                |      | 6.5  | %             |
| $V_{DP2}$    | Drop-out voltage                                    | $I_{LOAD} = 25\text{ mA}$ ; $V_S = 5.25\text{ V}$                    |                     | 0.3  | 0.4  | V             |
|              |   | $I_{LOAD} = 50\text{ mA}$ ; $V_S = 5.25\text{ V}$                    |                     | 0.4  | 0.7  | V             |
| $I_{CC2}$    | Output current in active mode                       | Max. continuous load current   |                     |      | 100  | mA            |
| $I_{CCmax2}$ | Short circuit output current                        | Current limitation   | 150                 | 280  | 450  | mA            |
| $C_{load}$   | Load capacitor                                      | Ceramic (+/- 20%)  | 0.22 <sup>(1)</sup> |      |      | $\mu\text{F}$ |
| $V_{2fail}$  | $V_2$ fail threshold                                | $V_2$ forced   |                     | 2    |      | V             |

Table 18. Voltage regulator  $V_2$  (continued)

| Symbol        | Parameter               | Test condition | Min. | Typ. | Max. | Unit          |
|---------------|-------------------------|----------------|------|------|------|---------------|
| $t_{V2fail}$  | $V_2$ fail filter time  |                |      | 2    |      | $\mu\text{s}$ |
| $t_{V2short}$ | $V_2$ short filter time |                |      | 4    |      | ms            |

1. Nominal capacitor value required for stability of the regulator. Tested with 220 nF ceramic (+/- 20%). Capacitor must be located close to the regulator output pin

### 5.5.6 Reset output

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.  $4.0\text{ V} < V_S \leq 28\text{ V}$ ;  $T_j = -40^\circ\text{C}$  to  $130^\circ\text{C}$ , unless otherwise specified.

Table 19. Reset output

| Symbol      | Parameter                      | Test condition                                 | Min. | Typ. | Max. | Unit             |
|-------------|--------------------------------|--|------|------|------|------------------|
| $V_{RT1}$   | Reset threshold voltage 1      | $V_{V1}$ decreasing                            | 3.7  | 3.9  | 4.1  | V                |
| $V_{RT2}$   | Reset threshold voltage 2      | $V_{V1}$ decreasing                            | 4.2  | 4.3  | 4.45 | V                |
| $V_{RT3}$   | Reset threshold voltage 3      | $V_{V1}$ decreasing                            | 4.25 | 4.4  | 4.55 | V                |
| $V_{RT4}$   | Reset threshold voltage 4      | $V_{V1}$ decreasing                            | 4.5  | 4.60 | 4.75 | V                |
|             |                                | $V_{V1}$ increasing                            | 4.7  | 4.8  | 4.9  | V                |
| $V_{RESET}$ | Reset pin low output voltage   | $V_1 > 1\text{ V}$ ; $I_{RESET} = 5\text{ mA}$ |      | 0.2  | 0.4  | V                |
| $R_{RESET}$ | Reset pull up int. resistor    |  | 80   | 110  | 150  | $\text{k}\Omega$ |
| $t_{RR}$    | Reset reaction time            | $I_{LOAD} = 1\text{ mA}$                       | 6    |      | 40   | $\mu\text{s}$    |
| $t_{UV1}$   | $V_1$ undervoltage filter time |  |      | 16   |      | $\mu\text{s}$    |
| Trd         | Reset pulse duration           |  | 1.46 | 2.0  | 2.5  | ms               |

### 5.5.7 Watchdog

$4.5\text{ V} < V_S < 28\text{ V}$ ;  $4.8\text{ V} < V_1 < 5.2\text{ V}$ ;  $T_j = -40^\circ\text{C}$  to  $130^\circ\text{C}$ , unless otherwise specified, see [Figure 31](#) and [Figure 32](#).

Table 20. Watchdog

| Symbol     | Parameter              | Test condition | Min.  | Typ. | Max.  | Unit |
|------------|------------------------|----------------|-------|------|-------|------|
| $t_{LW}$   | Long open window       |                | 48.75 | 65   | 81.25 | ms   |
| $T_{EFW1}$ | Early failure window 1 |                |       |      | 4.5   | ms   |
| $T_{LFW1}$ | Late failure window 1  |                | 20    |      |       | ms   |
| $T_{SW1}$  | Safe window 1          |                | 7.5   |      | 12    | ms   |
| $T_{EFW2}$ | Early failure window 2 |                |       |      | 22.3  | ms   |
| $T_{LFW2}$ | Late failure window 2  |                | 100   |      |       | ms   |
| $T_{SW2}$  | Safe window 2          |                | 37.5  |      | 60    | ms   |
| $T_{EFW3}$ | Early failure window 3 |                |       |      | 45    | ms   |

Table 20. Watchdog (continued)

| Symbol     | Parameter              | Test condition | Min. | Typ. | Max. | Unit |
|------------|------------------------|----------------|------|------|------|------|
| $T_{LFW3}$ | Late failure window 3  |                | 200  |      |      | ms   |
| $T_{SW3}$  | Safe window 3          |                | 75   |      | 120  | ms   |
| $T_{EFW4}$ | Early failure window 4 |                |      |      | 90   | ms   |
| $T_{LFW4}$ | Late failure window 4  |                | 400  |      |      | ms   |
| $T_{SW4}$  | Safe window 4          |                | 150  |      | 240  | ms   |

Figure 31. Watchdog timing (long, early, late and safe window)

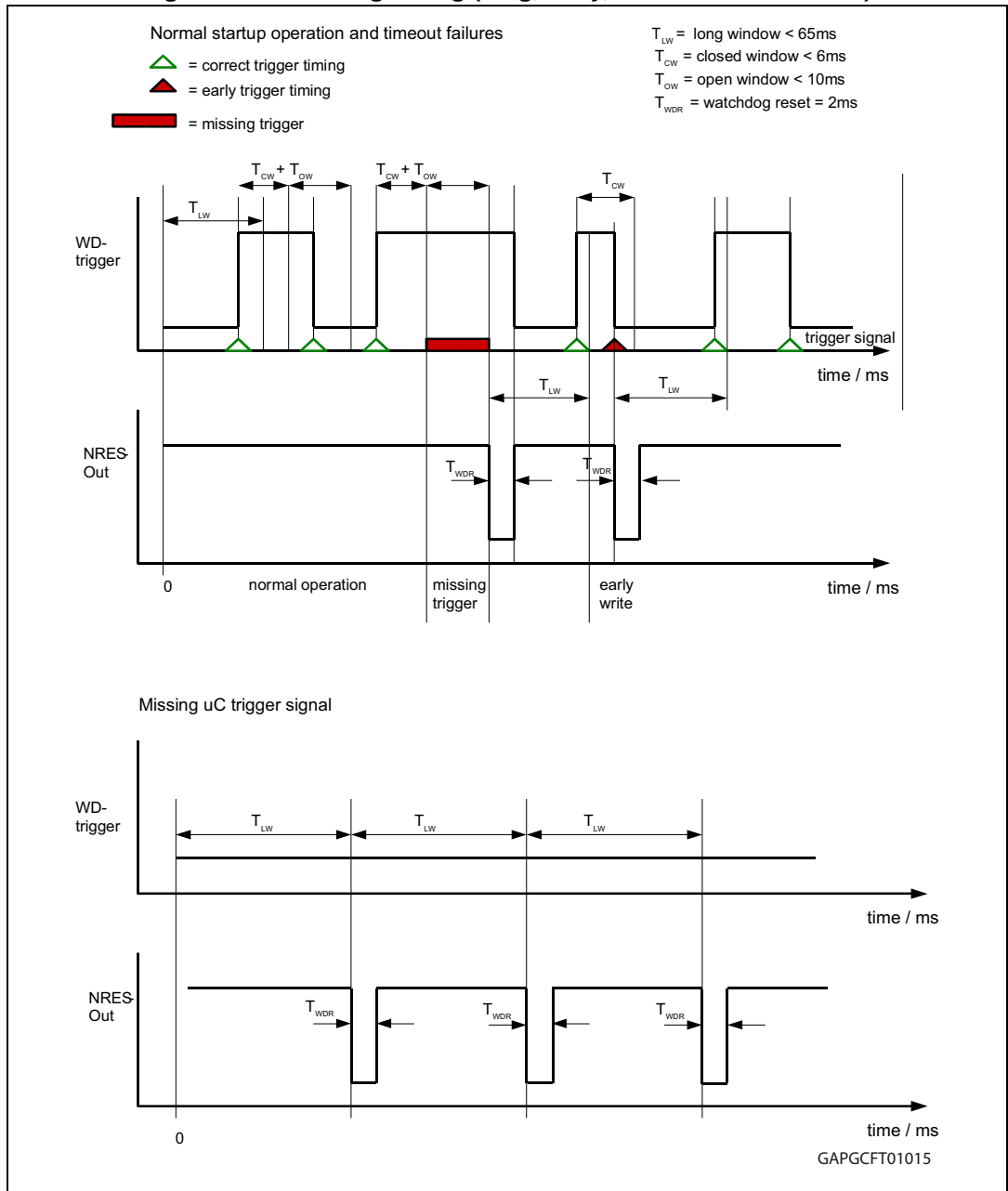
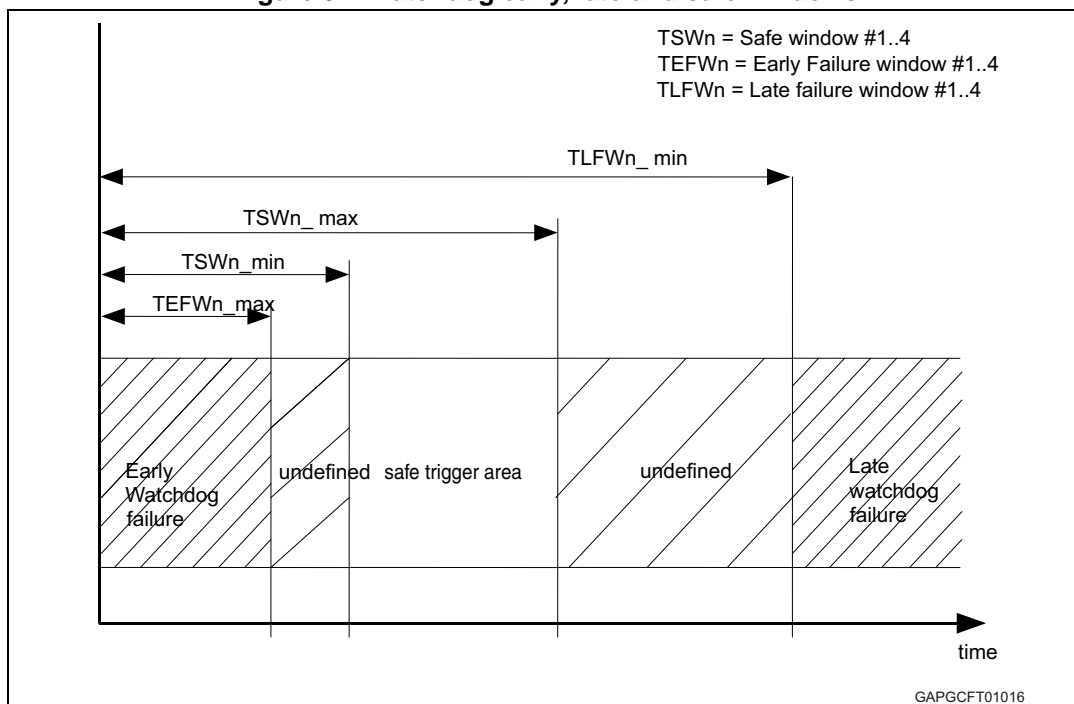


Figure 32. Watchdog early, late and safe windows



### 5.5.8 High side outputs

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.  $6\text{ V} \leq V_S \leq 18\text{ V}$ ;  $4.8\text{ V} \leq V_1 \leq 5.2\text{ V}$ ;  $T_j = -40^\circ\text{C}$  to  $130^\circ\text{C}$ , unless otherwise specified.

Table 21. Output (OUT\_HS)

| Symbol         | Parameter  | Test condition            | Min. | Typ.            | Max. | Unit                   |
|----------------|--|---------------------------|------|-----------------|------|------------------------|
| $R_{DS(on)}$   | Static drain source on-resistance<br>( $I_{OUT\_HS} = 150\text{ mA}$ ) | $T_j = 25^\circ\text{C}$  |      | 1.0             | 2.0  | $\Omega$               |
|                |  | $T_j = 125^\circ\text{C}$ |      | 1.6             | 3    | $\Omega$               |
| $t_{d(on)}$    | Switch on delay time   | $0.2 V_S$                 | 5    | 35              | 60   | $\mu\text{s}$          |
| $t_{d(off)}$   | Switch off delay time  | $0.8 V_S$                 | 40   | 95              | 150  | $\mu\text{s}$          |
| $t_{SCF}$      | Short circuit filter time  | Tested by scan chain      |      | $64 * T_{OSC}$  |      |                        |
| $t_{d\_ARHS}$  | Auto recovery filter time  | Tested by scan chain      |      | $400 * T_{OSC}$ |      |                        |
| $dV_{OUT}/dt$  | Slew rate  |                           | 0.18 | 0.5             | 0.8  | $\text{V}/\mu\text{s}$ |
| $I_{OUT}$      | Short circuit shut down current  |                           | 480  | 900             | 1320 | mA                     |
| $I_{OLD}$      | Open load detection current  |                           | 40   | 80              | 120  | mA                     |
| $t_{OLDT}$     | Open load detection time   | Tested by scan chain      |      | $64 * T_{OSC}$  |      |                        |
| $I_{FW}^{(1)}$ | Loss of GND current (ESD structure)                                    |                           | 100  |                 |      | mA                     |

1. Parameter guaranteed by design.

Table 22. Outputs (OUT1...4)

| Symbol         | Parameter  | Test condition                                     | Min. | Typ.           | Max. | Unit             |
|----------------|--|--|------|----------------|------|------------------|
| $R_{DS(ON)}$   | Static drain source on-resistance ( $I_{OUT\_HS} = 150 \text{ mA}$ ) | $I_{LOAD} = 60 \text{ mA}; T_j = 25^\circ\text{C}$ |      | 7              | 13   | $\Omega$         |
| $I_{OUT}$      | Short circuit shut down current                                      | $8 \text{ V} < V_S < 16 \text{ V}$                 | 140  | 235            | 350  | mA               |
| $I_{OLD}$      | Open load detection current  |  | 0.9  | 2              | 4.5  | mA               |
| $dV_{OUT}/dt$  | Slew rate  |  | 0.2  | 0.5            | 0.8  | V/ $\mu\text{s}$ |
| $t_{d(on)}$    | Switch ON delay time   | $0.2 V_S$  | 5    | 35             | 60   | $\mu\text{s}$    |
| $t_{d(off)}$   | Switch OFF delay time  | $0.8 V_S$  | 30   | 95             | 150  | $\mu\text{s}$    |
| $t_{SCF}$      | Short circuit filter time  | Tested by scan chain                               |      | $64 * T_{OSC}$ |      |                  |
| $I_{FW}^{(1)}$ | Loss of GND current (ESD structure)                                  |  | 100  |                |      | mA               |
| $t_{OLDT}$     | Open load detection time   | Tested by scan chain                               |      | $64 * T_{OSC}$ |      |                  |

1. Parameter guaranteed by design.

### 5.5.9 Relay drivers

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.  $6 \text{ V} \leq V_S \leq 18 \text{ V}$ ;  $4.8 \text{ V} \leq V_1 \leq 5.2 \text{ V}$ ;  $T_j = -40$  to  $130^\circ\text{C}$ , unless otherwise specified.

Table 23. Relay drivers

| Symbol        | Parameter                            | Test condition  | Min. | Typ.           | Max. | Unit             |
|---------------|--------------------------------------|---|------|----------------|------|------------------|
| $R_{DS(on)}$  | DC output resistance                 | $I_{LOAD} = 100 \text{ mA}$ at $T_j = 25^\circ\text{C}$ |      | 2              | 3    | $\Omega$         |
| $I_{OUT}$     | Short circuit shut down current      | $8 \text{ V} < V_S < 16 \text{ V}$                      | 250  | 375            | 500  | mA               |
| $V_Z$         | Output clamp voltage <sup>(1)</sup>  | $I_{LOAD} = 100 \text{ mA}$                             | 40   |                | 48   | V                |
| $t_{ONHL}$    | Turn on delay time to 10% $V_{OUT}$  |   | 5    | 50             | 100  | $\mu\text{s}$    |
| $t_{OFFLH}$   | Turn off delay time to 90% $V_{OUT}$ |   | 5    | 50             | 100  | $\mu\text{s}$    |
| $t_{SCF}$     | Short circuit filter time            | Tested by scan chain                                    |      | $64 * T_{OSC}$ |      |                  |
| $dV_{OUT}/dt$ | Slew rate                            |   | 0.2  | 2              | 4    | V/ $\mu\text{s}$ |

1. The output is capable to switch off relay coils with the impedance of  $R_L = 160 \Omega$ ;  $L = 300 \text{ mH}$  ( $R_L = 220 \Omega$ ;  $L = 420 \text{ mH}$ ); at  $V_S = 40 \text{ V}$  (Load dump condition)

### 5.5.10 Wake up inputs (WU1 ... WU3)

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.  $6\text{ V} \leq V_S \leq 18\text{ V}$ ;  $T_j = -40$  to  $130^\circ\text{C}$ , unless otherwise specified.

**Table 24. Wake-up inputs**

| Symbol          | Parameter   | Test condition  | Min.       | Typ.           | Max.       | Unit             |
|-----------------|---|---|------------|----------------|------------|------------------|
| $V_{WUthp}$     | Wake-up negative edge threshold voltage   |   | $0.4 V_S$  | $0.45 V_S$     | $0.5 V_S$  | V                |
| $V_{WUthn}$     | Wake-up positive edge threshold voltage   |   | $0.5 V_S$  | $0.55 V_S$     | $0.6 V_S$  | V                |
| $V_{HYST}$      | Hysteresis  |   | $0.05 V_S$ | $0.1 V_S$      | $0.15 V_S$ | V                |
| $t_{WU\_stat}$  | Static wake filter time   |   |            | $64 * T_{OSC}$ |            | $\mu\text{s}$    |
| $I_{WU\_stdby}$ | Input current in standby mode   | $V_{WU} < 1\text{ V}$ or<br>$V_{WU} > (V_S - 1.5\text{ V})$ | 9          | 15             | 28         | $\mu\text{A}$    |
| $R_{WU\_act}$   | Input resistor to GND in active mode and in standby mode during wake-up input sensing |   | 80         | 160            | 300        | $\text{k}\Omega$ |
| $t_{WU\_cyc}$   | Cyclic wake filter time   |   |            | 16             |            | $\mu\text{s}$    |

### 5.5.11 High speed CAN transceiver<sup>(d)</sup>

Selective wake functionality according to ISO 11898-6

**Table 25. CAN communication operating range**

| Symbol     | Parameter  | Test condition                  | Min. | Typ. | Max. | Unit |
|------------|--|---------------------------------|------|------|------|------|
| $V_{SCOM}$ | Supply voltage operating range for CAN communication | Active mode, $V_1 = V_{CANSUP}$ | 5.5  | —    | 18   | V    |

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.  $6\text{ V} \leq V_S \leq 18\text{ V}$ ;  $4.8\text{ V} \leq V_{CANSUP} \leq 5.2\text{ V}$ ;  $T_{junction} = -40^\circ\text{C}$  to  $130^\circ\text{C}$ , unless otherwise specified.  $-12\text{ V} = (\text{CANH} + \text{CANL}) / 2 = 12\text{ V}$ .

**Table 26. CAN transmit data input: pin TxDC**

| Symbol         | Parameter                     | Test condition                  | Min. | Typ. | Max. | Unit             |
|----------------|-------------------------------|---------------------------------|------|------|------|------------------|
| $V_{TXDCLOW}$  | Input voltage dominant level  | Active mode, $V_1 = 5\text{ V}$ | 1.35 | 1.8  |      | V                |
| $V_{TXDCHIGH}$ | Input voltage recessive level | Active mode, $V_1 = 5\text{ V}$ |      | 2.5  | 3    | V                |
| $V_{TXDCHYS}$  | $V_{TXDCHIGH} - V_{TXDCLOW}$  | Active mode, $V_1 = 5\text{ V}$ | 0.7  | 1    |      | V                |
| $R_{TXDCPU}$   | TxDC pull up resistor         | Active Mode, $V_1 = 5\text{ V}$ | 10   | 20   | 35   | $\text{k}\Omega$ |

d. ISO 11898-2 and ISO 11898-5 compliant.  
SAE J2284 compliant.

Table 27. CAN receive data output: pin RxDC

| Symbol         | Parameter                      | Test condition                         | Min. | Typ. | Max. | Unit |
|----------------|--------------------------------|--|------|------|------|------|
| $V_{RXDCLOW}$  | Output voltage dominant level  | Active mode, $V_1 = 5\text{ V}$ ; 2 mA |      | 0.2  | 0.5  | V    |
| $V_{RXDCHIGH}$ | Output voltage recessive level | Active mode, $V_1 = 5\text{ V}$ ; 2 mA | 4.5  |      |      | V    |

Table 28. CAN transmitter and receiver: pins CANH and CANL

| Symbol              | Parameter  | Test condition  | Min.                  | Typ.         | Max.                  | Unit |
|---------------------|--|---|-----------------------|--------------|-----------------------|------|
| $V_{CANHdom}$       | CANH voltage level in dominant state   | Active mode;<br>$V_{TXDC} = V_{TXDCLOW}$ ;<br>$R_L = 65\ \Omega$ ; $R_L = 50\ \Omega$                     | 2.75                  |              | 4.5                   | V    |
| $V_{CANLdom}$       | CANL voltage level in dominant state   | Active mode;<br>$V_{TXDC} = V_{TXDCLOW}$ ;<br>$R_L = 65\ \Omega$ ; $R_L = 50\ \Omega$                     | 0.5                   |              | 2.25                  | V    |
| $V_{DIFF,domOUT}$   | Differential output voltage in dominant state: $V_{CANHdom} - V_{CANLdom}$                   | Active mode;<br>$V_{TXDC} = V_{TXDCLOW}$ ;<br>$R_L = 65\ \Omega$ ; $R_L = 50\ \Omega$                     | 1.5                   |              | 3                     | V    |
| $V_{CM}^{(1)}$      | Driver symmetry:<br>$V_{CANHdom} + V_{CANLdom}$  | Active mode;<br>$V_{TXDC} = V_{TXDCLOW}$ ;<br>$f_{TXDC} = 250\text{kHz}$ ;<br>rectangular, 50% duty cycle | 0.9 *<br>$V_{CANSUP}$ | $V_{CANSUP}$ | 1.1 *<br>$V_{CANSUP}$ | V    |
| $V_{CANHrec}$       | CANH voltage level in recessive state (Normal Mode)  | Active mode;<br>$V_{TXDC} = V_{TXDCHIGH}$ ;<br>No load  | 2                     | 2.5          | 3                     | V    |
| $V_{CANLrec}$       | CANL voltage level in recessive state (Normal Mode)  | Active mode;<br>$V_{TXDC} = V_{TXDCHIGH}$ ;<br>No load  | 2                     | 2.5          | 3                     | V    |
| $V_{CANHrecLP}$     | CANH voltage level in recessive state (Low Power Mode)                                       | $V_{1\_standby}$ mode;<br>$V_{TXDC} = V_{TXDCHIGH}$ ;<br>No load  | -0.1                  | 0            | 0.1                   | V    |
| $V_{CANLrecLP}$     | CANL voltage level in recessive state (Low Power Mode)                                       | $V_{1\_standby}$ mode;<br>$V_{TXDC} = V_{TXDCHIGH}$ ;<br>No load  | -0.1                  | 0            | 0.1                   | V    |
| $V_{DIFF,recOUT}$   | Differential output voltage in recessive state (Normal Mode):<br>$V_{CANHrec} - V_{CANLrec}$ | Active mode;<br>$V_{TXDC} = V_{TXDCHIGH}$ ;<br>No load  | -50                   |              | 50                    | mV   |
| $V_{DIFF,recOUTLP}$ | Differential output voltage in recessive state (Low Power Mode): $V_{CANHrec} - V_{CANLrec}$ | $V_{1\_standby}$ mode;<br>$V_{TXDC} = V_{TXDCHIGH}$ ;<br>No load  | -50                   |              | 50                    | mV   |

**Table 28. CAN transmitter and receiver: pins CANH and CANL (continued)**

| Symbol               | Parameter                             | Test condition   | Min. | Typ. | Max. | Unit             |
|----------------------|---------------------------------------|--|------|------|------|------------------|
| $V_{CANHL,CM}$       | Common mode Bus voltage               | Measured with respect to the ground of each CAN node   | -12  |      | 12   | V                |
| $I_{OCANH,dom(0V)}$  | CANH output current in dominant state | Active mode;<br>$V_{TXDC} = V_{TXDCLOW}$ ;<br>$V_{CANH} = 0\text{ V}$  | -160 | -75  | -45  | mA               |
| $I_{OCANL,dom(5V)}$  | CANL output current in dominant state | Active mode;<br>$V_{TXDC} = V_{TXDCLOW}$ ;<br>$V_{CANL} = 5\text{ V}$  | 45   | 75   | 160  | mA               |
| $I_{OCANH,dom(40V)}$ | CANH output current in dominant state | Active mode;<br>$V_{TXDC} = V_{TXDCLOW}$ ;<br>$V_{CANH} = 40\text{ V}$ ;<br>$V_{CANL} = 0\text{ V}$ ;<br>$V_S = 40\text{ V}$   | 0    | 2    | 5    | mA               |
| $I_{OCANL,dom(40V)}$ | CANL output current in dominant state | Active mode;<br>$V_{TXDC} = V_{TXDCLOW}$ ;<br>$V_{CANL} = 40\text{ V}$ ;<br>$V_{CANH} = 0\text{ V}$ ;<br>$V_S = 40\text{ V}$   | 47   | 75   | 160  | mA               |
| $I_{leakage,CANH}$   | Input leakage current                 | Unpowered device;<br>$V_{BUS} = 5\text{ V}$ ;<br>– $V_{cansupply}$ connect $0\ \Omega$ to GND<br>– $V_{cansupply}$ connect $47\text{ k}\Omega$ to GND <sup>(2)</sup> | -10  | —    | 10   | $\mu\text{A}$    |
| $I_{leakage,CANL}$   | Input leakage current                 | Unpowered device;<br>$V_{BUS} = 5\text{ V}$ ;<br>– $V_{cansupply}$ connect $0\ \Omega$ to GND<br>– $V_{cansupply}$ connect $47\text{ k}\Omega$ to GND <sup>(2)</sup> | -10  | —    | 10   | $\mu\text{A}$    |
| $R_{in}$             | Internal resistance                   | Active mode &<br>$V_{1\_standby}$ mode;<br>$V_{TXDC} = V_{TXDCHIGH}$ ;<br>No load  | 20   | 27.5 | 38   | $\text{k}\Omega$ |
| $R_{in,matching}$    | Internal Resistor matching CANH,CANL  | Active mode &<br>$V_{1\_standby}$ mode;<br>$V_{TXDC} = V_{TXDCHIGH}$ ;<br>No load;<br>$R_{in(CANH)} - R_{in(CANL)}$  |      |      | 3    | %                |
| $R_{in,diff}$        | Differential internal resistance      | Active mode &<br>$V_{1\_standby}$ mode;<br>$V_{TXDC} = V_{TXDCHIGH}$ ;<br>No load  | 50   | 60   | 75   | $\text{k}\Omega$ |
| $C_{in}$             | Internal capacitance                  | Guaranteed by design   |      | 20   | 40   | pF               |



Table 28. CAN transmitter and receiver: pins CANH and CANL (continued)

| Symbol              | Parameter  | Test condition        | Min. | Typ. | Max. | Unit |
|---------------------|--|-----------------------|------|------|------|------|
| $C_{in,diff}$       | Differential internal capacitance  | Guaranteed by design  |      | 10   | 20   | pF   |
| $V_{THdom}^{(1)}$   | Differential receiver threshold voltage recessive to dominant state (Normal Mode)    | Active mode           |      |      | 0.9  | V    |
| $V_{THdomLP}^{(1)}$ | Differential receiver threshold voltage recessive to dominant state (Low Power Mode) | $V_{1\_standby}$ mode |      |      | 1.15 | V    |
| $V_{THrec}^{(1)}$   | Differential receiver threshold voltage dominant to recessive state (Normal Mode)    | Active mode           | 0.5  |      |      | V    |
| $V_{THrecLP}^{(1)}$ | Differential receiver threshold voltage dominant to recessive state (Low Power Mode) | $V_{1\_standby}$ mode | 0.4  |      |      | V    |

1. Parameter evaluated with specific  $R_{test} = 60 \Omega$ , guaranteed by characterization.

2. Guaranteed by design.

Table 29. CAN transceiver timing

| Symbol          | Parameter                                    | Test condition  | Min. | Typ. | Max. | Unit          |
|-----------------|--|---|------|------|------|---------------|
| $t_{TXpd,hl}$   | Propagation delay TxDC to RxDC (high to low) | Active mode; $R_L = 60 \Omega$ ; $C_L = 100 \text{ pF}$ ; $C_{RXDC} = 15 \text{ pF}$ ; $f_{TXDC} = 250 \text{ kHz}$ |      |      | 255  | ns            |
| $t_{TXpd,lh}$   | Propagation delay TxDC to RxDC (low to high) | Active mode; $R_L = 60 \Omega$ ; $C_L = 100 \text{ pF}$ ; $C_{RXDC} = 15 \text{ pF}$ ; $f_{TXDC} = 250 \text{ kHz}$ |      |      | 255  | ns            |
| $t_{filter}$    | Wake up filter time                          |   | 0.5  |      | 5    | $\mu\text{s}$ |
| $t_{dom(TxDC)}$ | TxDC dominant time-out                       | Tested by scan and oscillator   | 0.8  | 2    | 5    | ms            |
| $t_{CAN}$       | CAN permanent dominant time-out              |   |      | 700  |      | $\mu\text{s}$ |
| $t_{silence}$   | CAN timeout                                  |   | 600  | 700  | 1200 | ms            |

Table 29. CAN transceiver timing

| Symbol             | Parameter  | Test condition  | Min. | Typ. | Max. | Unit          |
|--------------------|--|---|------|------|------|---------------|
| $t_{\text{BIAS}}$  | Bias reaction time   | $R_L = 60 \Omega$ ; $C_L = 100 \text{ pF}$ ;<br>$C_{\text{GND}} = 100 \text{ pF}$ |      |      | 200  | $\mu\text{s}$ |
| $t_{V1\text{swn}}$ | $V_1$ switch-on time after reception of a valid WUF in $V_{\text{Bat-standby}}$ Mode |   |      |      | 50   | $\mu\text{s}$ |

### 5.5.12 LIN transceiver<sup>(e)</sup>

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.  $6\text{ V} \leq V_S \leq 18\text{ V}$ ;  $4.8\text{ V} \leq V_1 \leq 5.2\text{ V}$ ;  $T_{\text{junction}} = -40^\circ\text{C}$  to  $130^\circ\text{C}$ , unless otherwise specified.

**Table 30. LIN transmit data input: pin TxD**

| Symbol               | Parameter                                | Test condition                  | Min. | Typ. | Max. | Unit       |
|----------------------|--|---------------------------------|------|------|------|------------|
| $V_{\text{TXDLOW}}$  | Input voltage dominant level             | Active mode; $V_1 = 5\text{ V}$ | 1,35 | 1.8  |      | V          |
| $V_{\text{TXDHIGH}}$ | Input voltage recessive level            | Active mode; $V_1 = 5\text{ V}$ |      | 2.5  | 3    | V          |
| $V_{\text{TXDHYS}}$  | $V_{\text{TXDHIGH}} - V_{\text{TXDLOW}}$ | Active mode; $V_1 = 5\text{ V}$ | 0.7  | 1    |      | V          |
| $R_{\text{TXDPU}}$   | TXD pull up resistor                     | Active Mode; $V_1 = 5\text{ V}$ | 10   | 20   | 35   | k $\Omega$ |

**Table 31. LIN receive data output: pin RxD**

| Symbol               | Parameter                      | Test condition                         | Min. | Typ. | Max. | Unit |
|----------------------|--------------------------------|--|------|------|------|------|
| $V_{\text{RXDLOW}}$  | Output voltage dominant level  | Active mode; $V_1 = 5\text{ V}$ ; 2 mA |      | 0.2  | 0.5  | V    |
| $V_{\text{RXDHIGH}}$ | Output voltage recessive level | Active mode; $V_1 = 5\text{ V}$ ; 2 mA | 4.5  |      |      | V    |

**Table 32. LIN transmitter and receiver: pin LIN**

| Symbol              | Parameter  | Test condition | Min.          | Typ.         | Max.          | Unit |
|---------------------|--|----------------|---------------|--------------|---------------|------|
| $V_{\text{THdom}}$  | Receiver threshold voltage recessive to dominant state                     |                | $0.4 V_S$     | $0.45 V_S$   | $0.5 V_S$     | V    |
| $V_{\text{Busdom}}$ | Receiver dominant state  |                |               |              | $0.4 V_S$     | V    |
| $V_{\text{THrec}}$  | Receiver threshold voltage dominant to recessive state                     |                | $0.5^* V_S$   | $0.55^* V_S$ | $0.6^* V_S$   | V    |
| $V_{\text{Busrec}}$ | Receiver recessive state   |                | $0.6 V_S$     |              |               | V    |
| $V_{\text{THhys}}$  | Receiver threshold hysteresis: $V_{\text{THrec}} - V_{\text{THdom}}$       |                | $0.07^* V_S$  | $0.1^* V_S$  | $0.175^* V_S$ | V    |
| $V_{\text{THcnt}}$  | Receiver tolerance center value: $(V_{\text{THrec}} + V_{\text{THdom}})/2$ |                | $0.475^* V_S$ | $0.5^* V_S$  | $0.525^* V_S$ | V    |
| $V_{\text{THwkup}}$ | Receiver wakeup threshold voltage  |                | 1.0           | 1.5          | 2             | V    |

e. LIN 2.1 compliant for Baud rates up to 20 kBit/s.  
SAE J2602 compatible.

Table 32. LIN transmitter and receiver: pin LIN (continued)

| Symbol              | Parameter  | Test condition   | Min.        | Typ.           | Max.        | Unit       |
|---------------------|--|--|-------------|----------------|-------------|------------|
| $V_{THwkdown}$      | Receiver wakeup threshold voltage                            |  | $V_S - 3.5$ | $V_S - 2.5$    | $V_S - 1.5$ | V          |
| $t_{linbus}$        | Dominant time for wakeup via bus                             | Sleep mode; Edge: rec-dom  |             | $64 * T_{OSC}$ |             | $\mu s$    |
| $I_{LINDomSC}$      | Transmitter input current limit in dominant state            | $V_{TXD} = V_{TXDLOW}$ ;<br>$V_{LIN} = V_{BATMAX} = 18 V$  | 40          | 100            | 180         | mA         |
| $I_{bus\_PAS\_dom}$ | Input leakage current at the receiver incl. pull-up resistor | $V_{TXD} = V_{TXDHIGH}$ ; $V_{LIN} = 0 V$ ;<br>$V_{BAT} = 12 V^{(1)}$  | -1          |                |             | mA         |
| $I_{bus\_PAS\_rec}$ | Transmitter input current in recessive state                 | In stanby Modes;<br>$V_{TXD} = V_{TXDHIGH}$ ; $V_{LIN} > 8 V$ ;<br>$V_{BAT} < 18 V$ ; $V_{LIN} \geq V_{BAT}$ |             |                | 20          | $\mu A$    |
| $I_{bus\_NO\_GND}$  | Input current if loss of GND at Device                       | $GND = V_S$ ; $0 V < V_{LIN} < 18 V$ ;<br>$V_{BAT} = 12 V$   | -1          |                | 1           | mA         |
| $I_{bus}$           | Input current if loss of $V_{BAT}$ at Device                 | $GND = V_S$ ; $0 V < V_{LIN} < 18 V$   |             |                | 100         | $\mu A$    |
| $V_{LINdom}$        | LIN voltage level in dominant state                          | Active mode;<br>$V_{TXD} = V_{TXDLOW}$ ; $I_{LIN} = 40 mA$   |             |                | 1.2         | V          |
| $V_{LINrec}$        | LIN voltage level in recessive state                         | Active mode;<br>$V_{TXD} = V_{TXDHIGH}$ ; $I_{LIN} = 10 \mu A$   | $0.8 * V_S$ |                | 1           | V          |
| $R_{LINup}$         | LIN output pull up resistor                                  | $V_{LIN} = 0 V$  | 20          | 40             | 60          | k $\Omega$ |
| $C_{LIN}$           | LIN input capacitance  |  |             |                | 90          | pF         |

1. Slave mode.

Table 33. LIN transceiver timing

| Symbol          | Parameter   | Test condition   | Min. | Typ. | Max. | Unit    |
|-----------------|---|--|------|------|------|---------|
| $t_{RXpd}$      | Receiver propagation delay time                                       | $t_{RXpd} = \max(t_{RXpdr}, t_{RXpdf})$ ;<br>$t_{RXpdf} = t(0.5 V_{RXD}) - t(0.45 V_{LIN})$ ;<br>$t_{RXpdr} = t(0.5 V_{RXD}) - t(0.55 V_{LIN})$ ;<br>$V_S = 12 V$ ; $C_{RXD} = 20 pF$ ;<br>$R_{bus} = 1 k\Omega$ ; $C_{bus} = 1 nF$ ;<br>$R_{bus} = 660 \Omega$ ; $C_{bus} = 6.8 nF$ ;<br>$R_{bus} = 500 \Omega$ ; $C_{bus} = 10 nF$ |      |      | 6    | $\mu s$ |
| $t_{RXpd\_sym}$ | Symmetry of receiver propagation delay time (rising vs. falling edge) | $t_{RXpd\_sym} = t_{RXpdr} - t_{RXpdf}$ ;<br>$V_S = 12 V$ ; $R_{bus} = 1 k\Omega$ ;<br>$C_{bus} = 1 nF$ ; $C_{RXD} = 20 pF$  | -2   |      | 2    | $\mu s$ |

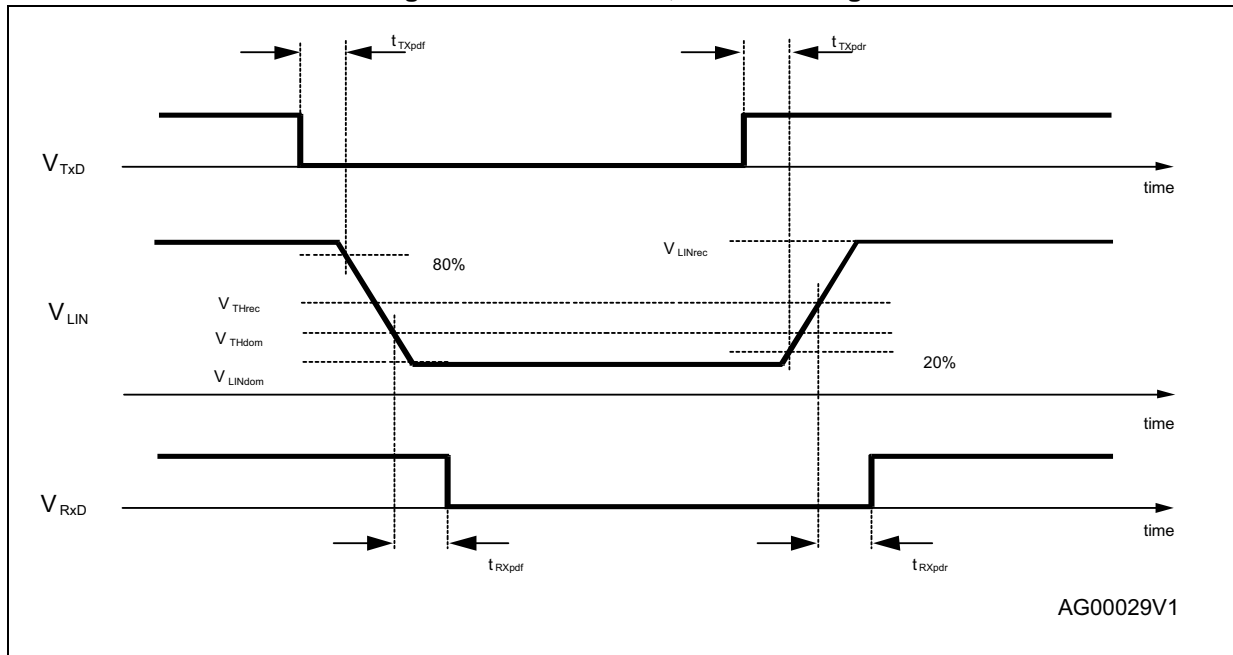
Table 33. LIN transceiver timing (continued)

| Symbol          | Parameter                           | Test condition  | Min.  | Typ. | Max.  | Unit    |
|-----------------|-------------------------------------|---|-------|------|-------|---------|
| D1              | Duty Cycle 1                        | $TH_{Rec(max)} = 0.744 * V_S$ ;<br>$TH_{Dom(max)} = 0.581 * V_S$ ;<br>$V_S = 7 V$ to $18 V$ ; $t_{bit} = 50 \mu s$ ;<br>$D1 = t_{bus\_rec(min)} / (2 * t_{bit})$ ;<br>$R_{bus} = 1 k\Omega$ ; $C_{bus} = 1 nF$ ;<br>$R_{bus} = 660 \Omega$ ; $C_{bus} = 6.8 nF$ ;<br>$R_{bus} = 500 \Omega$ ; $C_{bus} = 10 nF$   | 0.396 |      |       |         |
| D2              | Duty Cycle 2                        | $TH_{Rec(min)} = 0.422 * V_S$ ;<br>$TH_{Dom(min)} = 0.284 * V_S$ ;<br>$V_S = 7.6 V$ to $18 V$ ; $t_{bit} = 50 \mu s$ ;<br>$D2 = t_{bus\_rec(max)} / (2 * t_{bit})$ ;<br>$R_{bus} = 1 k\Omega$ ; $C_{bus} = 1 nF$ ;<br>$R_{bus} = 660 \Omega$ ; $C_{bus} = 6.8 nF$ ;<br>$R_{bus} = 500 \Omega$ ; $C_{bus} = 10 nF$ |       |      | 0.581 |         |
| D3              | Duty Cycle 3                        | $TH_{Rec(max)} = 0.778 * V_S$ ;<br>$TH_{Dom(max)} = 0.616 * V_S$ ;<br>$V_S = 7 V$ to $18 V$ ; $t_{bit} = 96 \mu s$ ;<br>$D3 = t_{bus\_rec(min)} / (2 * t_{bit})$ ;<br>$R_{bus} = 1 k\Omega$ ; $C_{bus} = 1 nF$ ;<br>$R_{bus} = 660 \Omega$ ; $C_{bus} = 6.8 nF$ ;<br>$R_{bus} = 500 \Omega$ ; $C_{bus} = 10 nF$   | 0.417 |      |       |         |
| D4              | Duty Cycle 4                        | $TH_{Rec(min)} = 0.389 * V_S$ ;<br>$TH_{Dom(min)} = 0.251 * V_S$ ;<br>$V_S = 7.6 V$ to $18 V$ ; $t_{bit} = 96 \mu s$ ;<br>$D4 = t_{bus\_rec(max)} / (2 * t_{bit})$ ;<br>$R_{bus} = 1 k\Omega$ ; $C_{bus} = 1 nF$ ;<br>$R_{bus} = 660 \Omega$ ; $C_{bus} = 6.8 nF$ ;<br>$R_{bus} = 500 \Omega$ ; $C_{bus} = 10 nF$ |       |      | 0.590 |         |
| $t_{dom(TXDL)}$ | TXDL dominant time-out              |   |       | 12   |       | ms      |
| $t_{LIN}$       | LIN permanent recessive time-out    |   |       | 40   |       | $\mu s$ |
| $T_{dom(bus)}$  | LIN Bus permanent dominant time-out |   |       | 12   |       | ms      |

Table 34. LIN pull-up: pin LINPU

| Symbol       | Parameter       | Test condition | Min. | Typ. | Max. | Unit     |
|--------------|-----------------|----------------|------|------|------|----------|
| $R_{DS(on)}$ | ON resistance   |                | —    | 10.5 | 16   | $\Omega$ |
| $I_{leak}$   | Leakage current |                | —    |      | 1    | $\mu A$  |

Figure 33. LIN transmit, receive timing



### 5.5.13 Operational amplifier

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.  $6\text{ V} \leq V_S \leq 18\text{ V}$ ;  $T_j = -40^\circ\text{C}$  to  $130^\circ\text{C}$ , unless otherwise specified.

Table 35. Operational amplifier

| Symbol             | Parameter                   | Test condition                    | Min.        | Typ. | Max.  | Unit       |
|--------------------|-----------------------------|-----------------------------------|-------------|------|-------|------------|
| GBW                | GBW product                 |                                   | 1           | 3.5  | 7.0   | MHz        |
| AVOL <sub>DC</sub> | DC open loop gain           |                                   | 80          |      |       | dB         |
| PSRR               | Power supply rejection      | DC, $V_{IN} = 150\text{ mV}$      | 80          |      |       | dB         |
| $V_{off}$          | Input offset voltage        |                                   | -5          |      | +5    | mV         |
| $V_{ICR}$          | Common mode input range     |                                   | -0.2        | 0    | 3     | V          |
| $V_{OH}$           | Output voltage range high   | $I_{LOAD} = 1\text{ mA}$ to GND   | $V_S - 0.2$ |      | $V_S$ | V          |
| $V_{OL}$           | Output voltage range low    | $I_{LOAD} = 1\text{ mA}$ to $V_S$ | 0           |      | 0.2   | V          |
| $I_{Lim+}$         | Output current limitation + | DC                                | 10          | 15   | 30    | mA         |
| $I_{lim-}$         | Output current limitation - | DC                                | -10         | -15  | -30   | mA         |
| SR+                | Slew rate positive          |                                   | 1           | 4    | 10    | V/ $\mu$ s |
| SR-                | Slew rate negative          |                                   | -1          | -4   | -10   | V/ $\mu$ s |

Note: The operational amplifier is on-chip stabilized for external capacitive loads  $C_L \leq 25\text{ pF}$  (all operating conditions)

### 5.5.14 SPI

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.

$6\text{ V} < V_S < 18\text{ V}$ ;  $4.5\text{ V} < V_1 < 5.3\text{ V}$ ; all outputs open;  $T_j = -40^\circ\text{C}$  to  $130^\circ\text{C}$ , unless otherwise specified.

**Table 36. Input: CSN**

| Symbol               | Parameter                                | Test condition                  | Min. | Typ. | Max. | Unit       |
|----------------------|--|---------------------------------|------|------|------|------------|
| $V_{\text{CSNLOW}}$  | Input voltage low level                  | Normal mode, $V_1 = 5\text{ V}$ | 1.35 | 1.8  |      | V          |
| $V_{\text{CSNHIGH}}$ | Input voltage high level                 | Normal mode, $V_1 = 5\text{ V}$ |      | 2    | 2.9  | V          |
| $V_{\text{CSNHYS}}$  | $V_{\text{CSNHIGH}} - V_{\text{CSNLOW}}$ | Normal mode, $V_1 = 5\text{ V}$ | 0.6  | 1.0  | 1.5  | V          |
| $I_{\text{CSNPU}}$   | CSN pull up resistor                     | Normal mode, $V_1 = 5\text{ V}$ | 10   | 20   | 35   | k $\Omega$ |

**Table 37. Inputs: CLK, DI**

| Symbol                | Parameter  | Test condition  | Min. | Typ. | Max. | Unit          |
|-----------------------|--|---|------|------|------|---------------|
| $t_{\text{set}}$      | Delay time from standby to active mode                         | Switching from standby to active mode. Time until output drivers are enabled after CSN going to high. |      | 160  | 300  | $\mu\text{s}$ |
| $V_{\text{INL}}$      | Input low level  | $V_1 = 5\text{ V}$  | 1.35 | 2.05 | 2.75 | V             |
| $V_{\text{INH}}$      | Input high level   | $V_1 = 5\text{ V}$  | 1.9  | 2.8  | 3.7  | V             |
| $V_{\text{INHyst}}$   | Input hysteresis   | $V_1 = 5\text{ V}$  | 0.4  | 0.75 | 1.5  | V             |
| $I_{\text{in}}$       | Pull down current at input                                     | $V_{\text{IN}} = 1.5\text{ V}$  | 5    | 30   | 60   | $\mu\text{A}$ |
| $C_{\text{in}}^{(1)}$ | Input capacitance at input CSN, CLK, DI and PWM <sub>1,2</sub> | $0\text{ V} < V_1 < 5.3\text{ V}$   |      | 10   | 15   | pF            |
| $f_{\text{CLK}}$      | SPI input frequency at CLK                                     |   |      |      | 1    | MHz           |

1. Value of input capacity is not measured in production test. Parameter guaranteed by design.

**Table 38. DI timing<sup>(1)</sup>**

| Symbol               | Parameter  | Test condition     | Min. | Typ. | Max. | Unit |
|----------------------|--|--------------------|------|------|------|------|
| $t_{\text{CLK}}$     | clock period                                       | $V_1 = 5\text{ V}$ | 1000 | —    |      | ns   |
| $t_{\text{CLKH}}$    | clock high time                                    | $V_1 = 5\text{ V}$ | 400  | —    |      | ns   |
| $t_{\text{CLKL}}$    | clock low time                                     | $V_1 = 5\text{ V}$ | 400  | —    |      | ns   |
| $t_{\text{set CSN}}$ | CSN setup time, CSN low before rising edge of CLK  | $V_1 = 5\text{ V}$ | 400  | —    |      | ns   |
| $t_{\text{set CLK}}$ | CLK setup time, CLK high before rising edge of CSN | $V_1 = 5\text{ V}$ | 400  | —    |      | ns   |
| $t_{\text{set DI}}$  | DI setup time                                      | $V_1 = 5\text{ V}$ | 200  | —    |      | ns   |

Table 38. DI timing<sup>(1)</sup> (continued)

| Symbol               | Parameter                              | Test condition      | Min. | Typ. | Max. | Unit |
|----------------------|--|---------------------|------|------|------|------|
| $t_{\text{hold DI}}$ | DI hold time                           | $V_1 = 5 \text{ V}$ | 200  | —    |      | ns   |
| $t_{\text{r in}}$    | rise time of input signal DI, CLK, CSN | $V_1 = 5 \text{ V}$ |      | —    | 100  | ns   |
| $t_{\text{f in}}$    | fall time of input signal DI, CLK, CSN | $V_1 = 5 \text{ V}$ |      | —    | 100  | ns   |

1. See [Figure 35: SPI input timing](#).

Table 39. Output: DO

| Symbol            | Parameter                  | Test condition   | Min. | Typ. | Max. | Unit          |
|-------------------|----------------------------|--|------|------|------|---------------|
| $V_{\text{DOL}}$  | output low level           | $V_1 = 5 \text{ V}; I_{\text{D}} = -4 \text{ mA}$                    |      |      | 0.5  | V             |
| $V_{\text{DOH}}$  | output high level          | $V = 5 \text{ V}; I_{\text{D}} = 4 \text{ mA}$                       | 4.5  |      |      | V             |
| $I_{\text{DOLK}}$ | tristate leakage current   | $V_{\text{CSN}} = V_1; 0 \text{ V} < V_{\text{DO}} < V_1$            | -10  |      | 10   | $\mu\text{A}$ |
| $C_{\text{DO}}$   | tristate input capacitance | $V_{\text{CSN}} = V_1;$<br>$0 \text{ V} < V_1 < 5.3 \text{ V}^{(1)}$ |      | 10   | 15   | pF            |

1. Value of input capacity is not measured in production test. Parameter guaranteed by design.

Table 40. DO timing<sup>(1)</sup>

| Symbol                    | Parameter                                   | Test condition   | Min. | Typ. | Max. | Unit |
|---------------------------|---|--|------|------|------|------|
| $t_{\text{r DO}}$         | DO rise time                                | $C_{\text{L}} = 100 \text{ pF}; I_{\text{LOAD}} = -1 \text{ mA}$                           | —    | 50   | 100  | ns   |
| $t_{\text{f DO}}$         | DO fall time                                | $C_{\text{L}} = 100 \text{ pF}; I_{\text{LOAD}} = 1 \text{ mA}$                            | —    | 50   | 100  | ns   |
| $t_{\text{en DO tri L}}$  | DO enable time from tristate to low level   | $C_{\text{L}} = 100 \text{ pF}; I_{\text{LOAD}} = 1 \text{ mA};$<br>pull-up load to $V_1$  | —    | 50   | 250  | ns   |
| $t_{\text{dis DO L tri}}$ | DO disable time from low level to tristate  | $C_{\text{L}} = 100 \text{ pF}; I_{\text{LOAD}} = 4 \text{ mA};$<br>pull-up load to $V_1$  | —    | 50   | 250  | ns   |
| $t_{\text{en DO tri H}}$  | DO enable time from tristate to high level  | $C_{\text{L}} = 100 \text{ pF}; I_{\text{LOAD}} = -1 \text{ mA};$<br>pull-down load to GND | —    | 50   | 250  | ns   |
| $t_{\text{dis DO H tri}}$ | DO disable time from high level to tristate | $C_{\text{L}} = 100 \text{ pF}; I_{\text{LOAD}} = -4 \text{ mA};$<br>pull-down load to GND | —    | 50   | 250  | ns   |
| $t_{\text{d DO}}$         | DO delay time                               | $V_{\text{DO}} < 0.3 V_1; V_{\text{DO}} > 0.7 V_1;$<br>$C_{\text{L}} = 100 \text{ pF}$     | —    | 50   | 250  | ns   |

1. See [Figure 36: SPI output timing \(part 1\)](#).

Table 41. CSN timing<sup>(1)</sup>

| Symbol                   | Parameter                        | Test condition                            | Min. | Typ. | Max. | Unit          |
|--------------------------|----------------------------------|---|------|------|------|---------------|
| $t_{\text{CSN\_HI,min}}$ | Minimum CSN HI time, active mode | Transfer of SPI-command to Input Register | 6    |      |      | $\mu\text{s}$ |
| $t_{\text{CSNfail}}$     | CSN low timeout                  |   | 20   | 35   | 50   | ms            |

1. See [Figure 37: SPI CSN - output timing](#).



The voltages are referred to ground and currents are assumed positive, when the current flows into the pin.  $6\text{ V} \leq V_S \leq 18\text{ V}$ ;  $4.8\text{ V} \leq V_1 \leq 5.2\text{ V}$ ; all outputs open;  $T_j = -40^\circ\text{C}$  to  $130^\circ\text{C}$ , unless otherwise specified

**Table 42. RXDL/NINT, RXDC/NINT timing**

| Symbol                 | Parameter                | Test condition | Min. | Typ. | Max. | Unit          |
|------------------------|--------------------------|----------------|------|------|------|---------------|
| $t_{\text{Interrupt}}$ | Interrupt pulse duration |                | —    | 56   | —    | $\mu\text{s}$ |

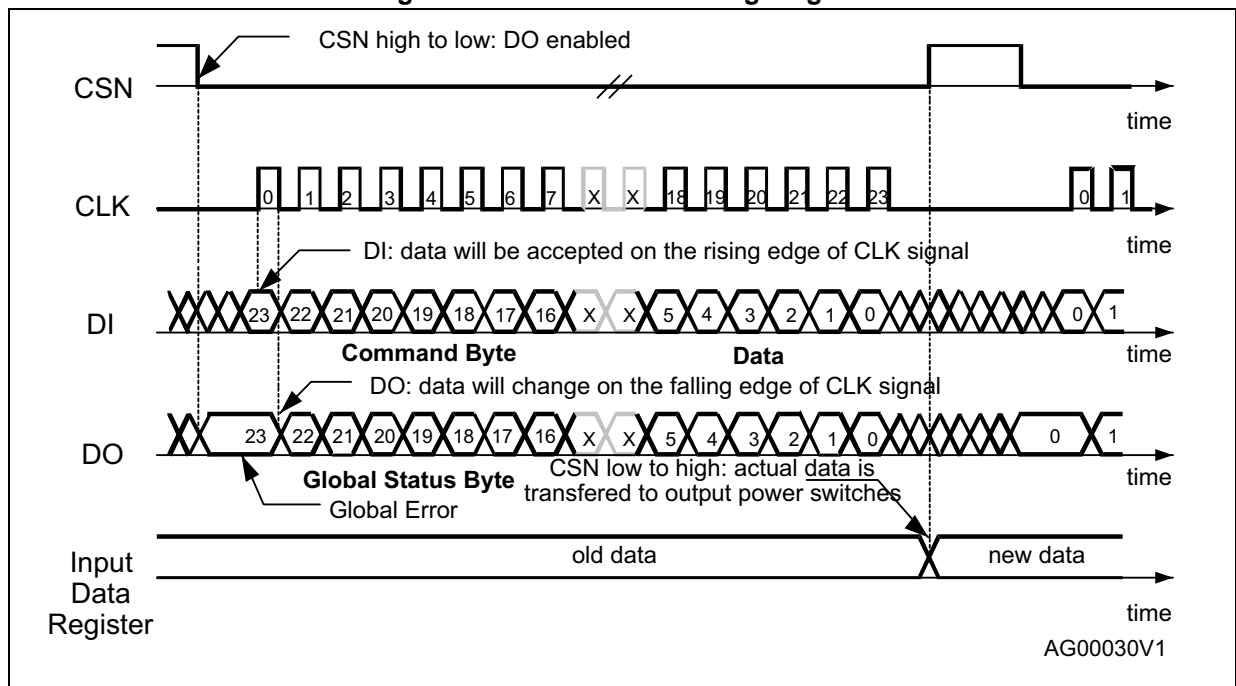
**5.5.15 Inputs TxDC and TxDL for Flash Mode**

$6\text{ V} \leq V_S \leq 18\text{ V}$ ;  $4.5\text{ V} \leq V_1 \leq 5.3\text{ V}$ ;  $T_j = -40^\circ\text{C}$  to  $130^\circ\text{C}$ ; voltages are referred to PGND, all outputs open

**Table 43. Inputs: TxDC and TxDL for Flash Mode**

| Symbol                | Parameter  | Test condition     | Min. | Typ. | Max. | Unit |
|-----------------------|--|--------------------|------|------|------|------|
| $V_{\text{flashL}}$   | Input low level ( $V_{\text{TXDC/L}}$ for exit from Flash Mode)        | $V_1 = 5\text{ V}$ | 7.1  | 8.4  | 9.0  | V    |
| $V_{\text{flashH}}$   | Input high level ( $V_{\text{TXDC/L}}$ for transition into Flash Mode) | $V_1 = 5\text{ V}$ | 8.3  | 9.4  | 10.0 | V    |
| $V_{\text{flashHYS}}$ | Input voltage hysteresis   | $V_1 = 5\text{ V}$ | 0.8  | 1.0  | 1.2  | V    |

**Figure 34. SPI - transfer timing diagram**



The SPI can be driven by a micro controller with its SPI peripheral running in following mode: CPOL = 0 and CPHA = 0.

For this mode input data is sampled by the low to high transition of the clock CLK, and output data is changed from the high to low transition of CLK.

Figure 35. SPI input timing

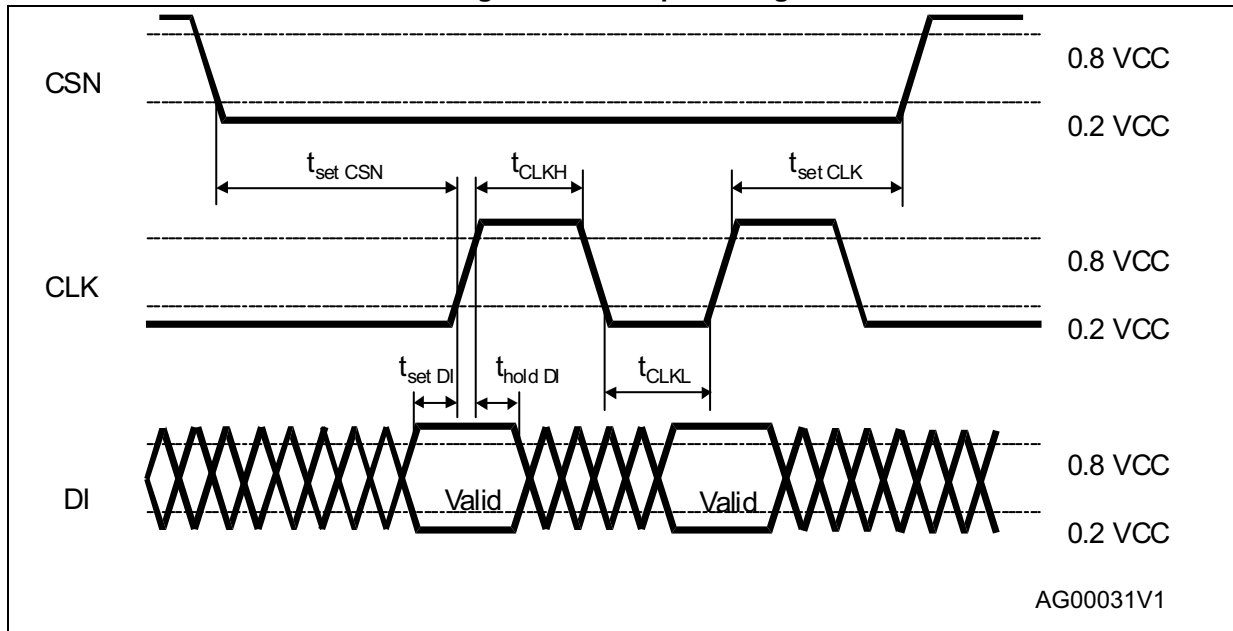


Figure 36. SPI output timing (part 1)

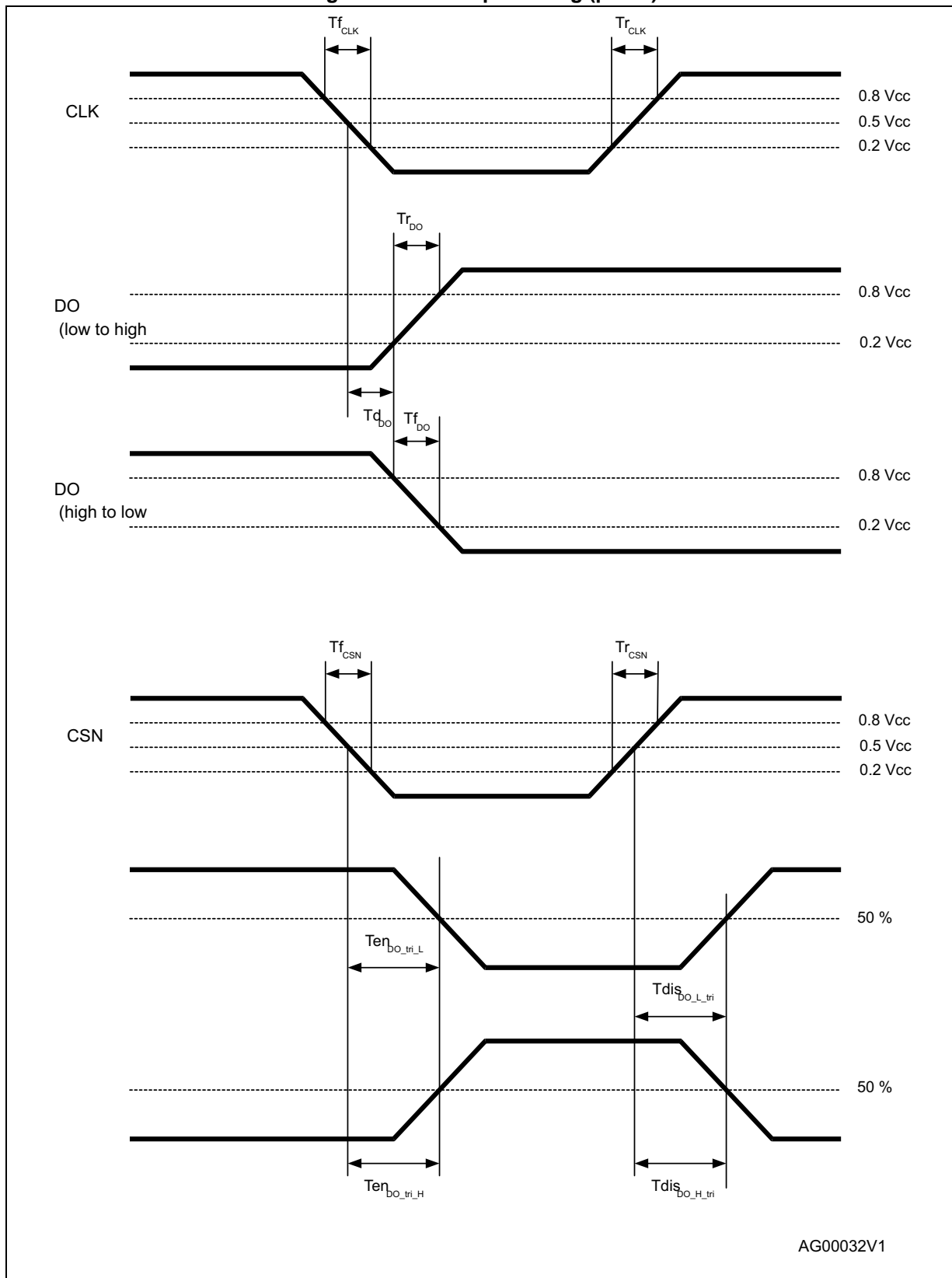


Figure 37. SPI CSN - output timing

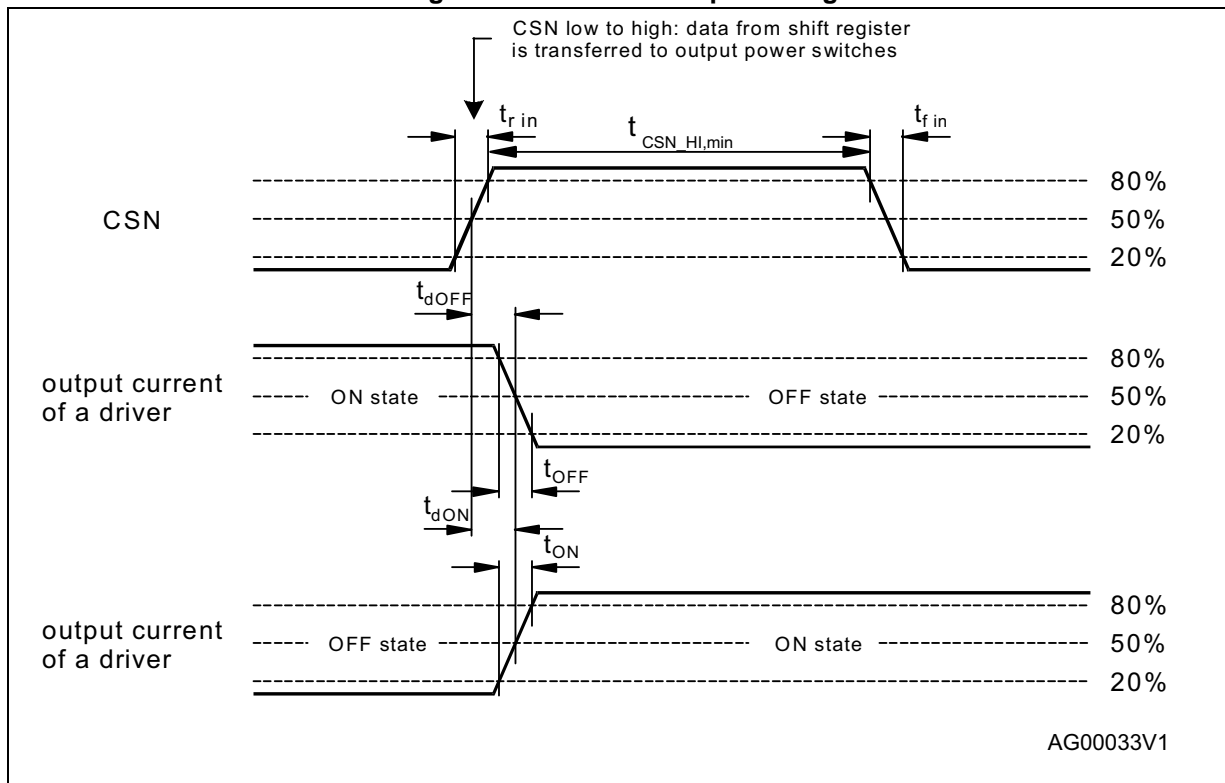
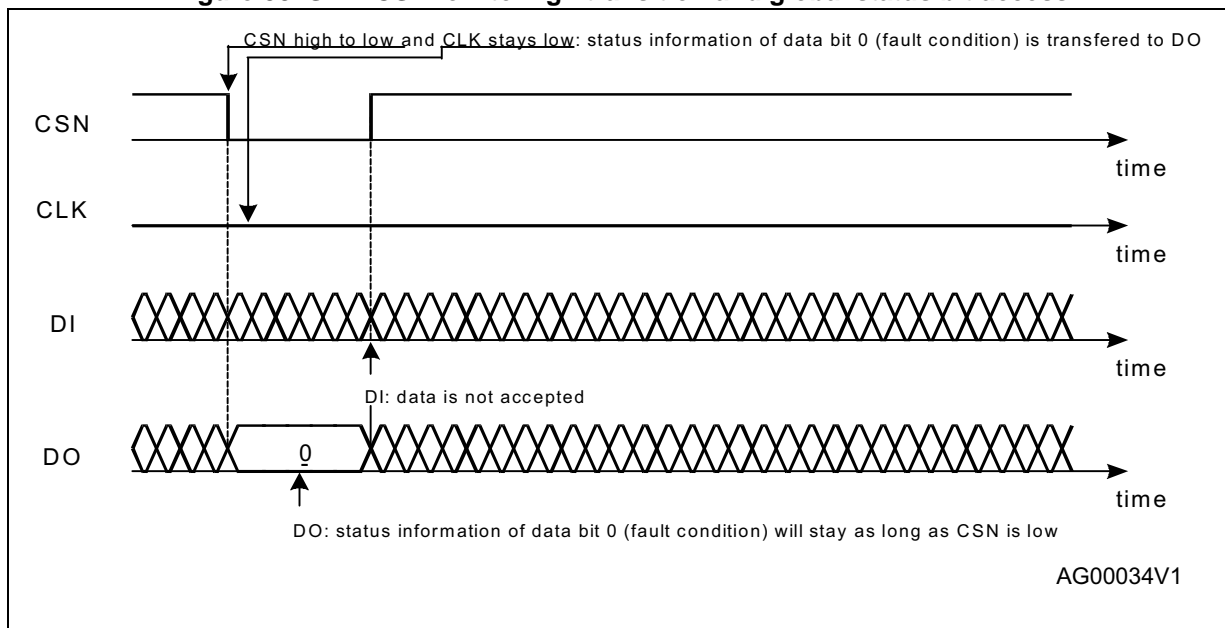


Figure 38. SPI - CSN low to high transition and global status bit access



## 6 ST SPI

### 6.1 SPI communication flow

#### 6.1.1 General description

The SPI communication is based on a standard SPI interface structure using CSN (Chip Select Not), SDI (Serial Data In), SDO (Serial Data Out/Error) and SCK (Serial Clock) signal lines.

At device start-up the master reads the *<SPI-frame-ID>* register (ROM address 3EH) of the slave device. This 8-bit register indicates the SPI frame length (24bit) and the availability of additional features.

Each communication frame consists of an instruction byte which is followed by two data bytes.

The data returned on SDO within the same frame always starts with the *<Global Status>* register. It provides general status information about the device. It is followed by two data bytes (i. e. 'In-frame-response').

For Write cycles the *<Global Status>* register is followed by the previous content of the addressed register.

For Read cycles the *<Global Status>* register is followed by the content of the addressed register.

A Write command is only accepted as a valid command by the device if the counted number of clocks is exact 24, otherwise the command is rejected.

#### Command Byte

Each communication frame starts with a command byte. It consists of an operating code which specifies the type of operation (*<Write>*, *<Read>*, *<Read and Clear>*, *<Read Device Information>*) and a 6 bit address. If less than 6 address bits are required, the remaining bits are unused but are reserved.

**Table 44. Command Byte**

| MSB     |     |         |    |    |    |    |    | LSB |
|---------|-----|---------|----|----|----|----|----|-----|
| Op Code |     | Address |    |    |    |    |    |     |
| OC1     | OC0 | A5      | A4 | A3 | A2 | A1 | A0 |     |

OCx: Operating Code

Ax: Address

## 6.1.2 Operating code definition

Table 45. Operating code definition

| OC1 | OC0 | Meaning                   |
|-----|-----|---------------------------|
| 0   | 0   | <Write Mode>              |
| 0   | 1   | <Read Mode>               |
| 1   | 0   | <Read and Clear Status>   |
| 1   | 1   | <Read Device Information> |

The <Write Mode> <Read Mode> and <Read and Clear Status> operations allow access to the RAM of the device, i. e. to write to control registers or read status information.

A <Read and Clear Status> operation addressed to a device specific status register reads back and subsequently clear this status register.

A <Read and Clear Status> operation with address 3FH clears all status registers (including the Global Status Register). Configuration Register is read by this operation.

<Read Device Information> allows access to the ROM area which contains device related information such as the product family, product name, silicon version, register width and availability of a watchdog.

More detailed descriptions of the Device Information are available in 'Read Device Information'.

## 6.1.3 Global Status Register

Table 46. Global status register

| Bit 7                   | Bit 6      | Bit 5                          | Bit 4 | Bit 3 | Bit 2               | Bit 1                       | Bit 0     |
|-------------------------|------------|--------------------------------|-------|-------|---------------------|-----------------------------|-----------|
| Global error flag (GEF) | Comm error | Not (chip reset OR comm error) | TSD2  | TSD1  | V <sub>1</sub> Fail | V <sub>S</sub> Fail (OV/UV) | Fail safe |

## 6.1.4 Configuration register<sup>(f)</sup>

The <Configuration> register is accessible at RAM address 3FH.

For the Config Register, the 8 bits are located in the low byte (LSB).

The Configuration Register is implemented for compliance purpose to ST SPI Standard.

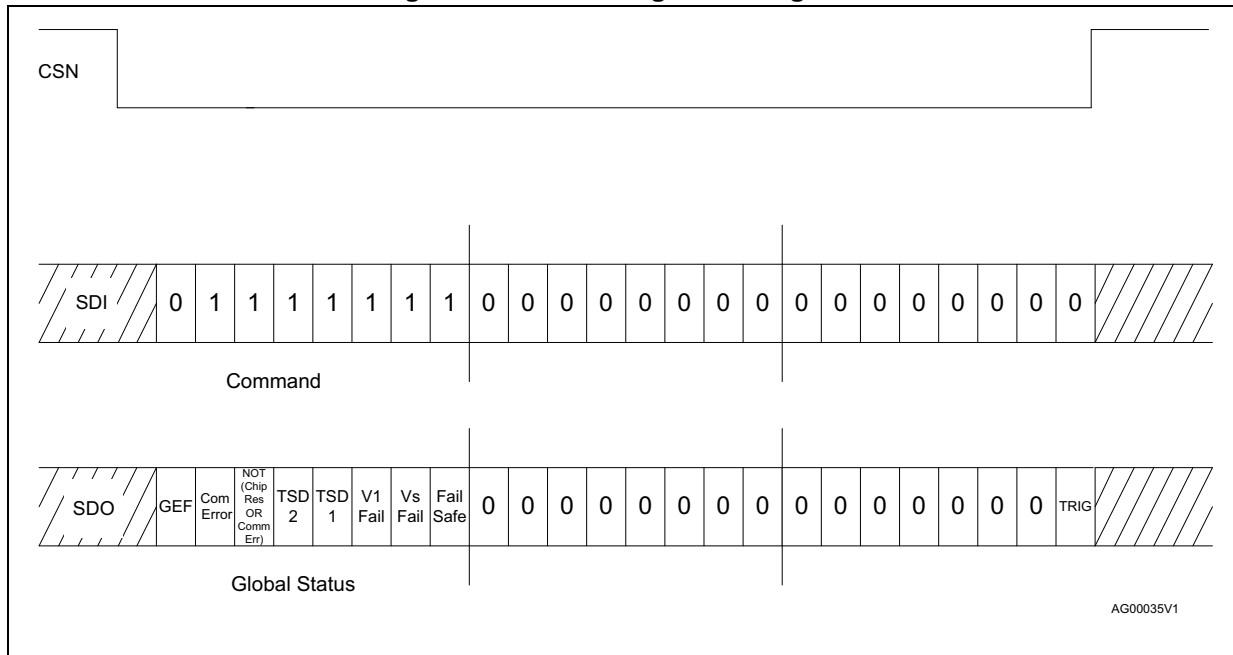
Table 47. Configuration register

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0      |
|-------|-------|-------|-------|-------|-------|-------|------------|
| 0     | 0     | 0     | 0     | 0     | 0     | 0     | WD trigger |

<WD Trigger>: This Bit is reserved to serve the watchdog.

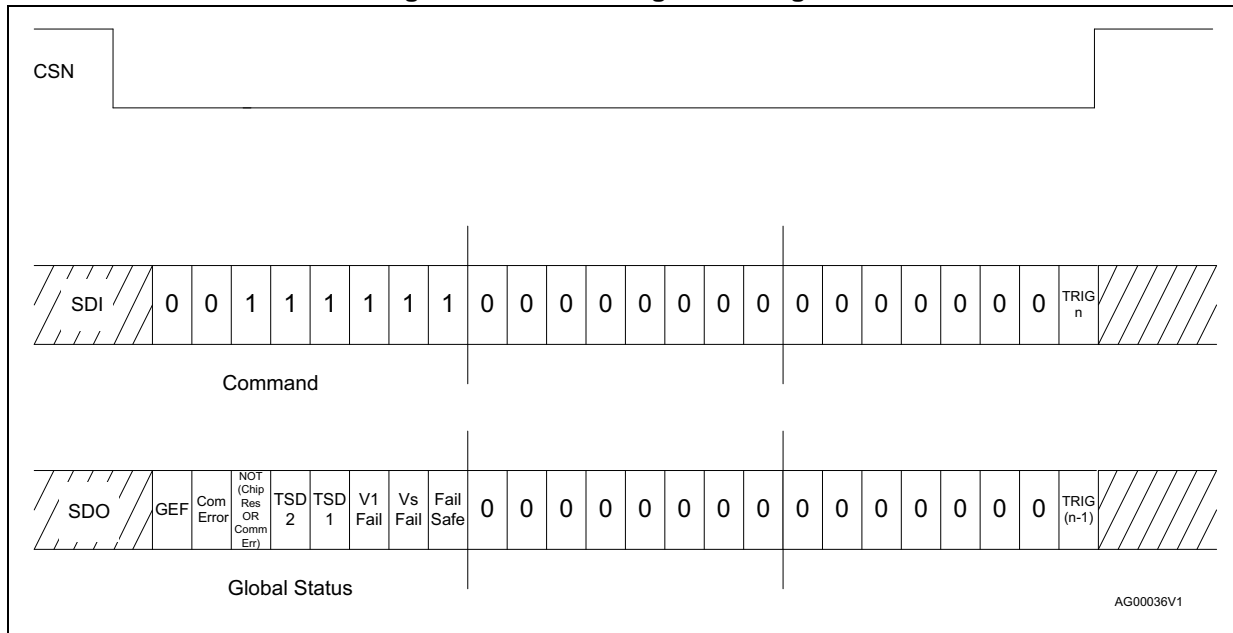
f. See [Section 6.2](#) for details.

Figure 39. Read configuration register



1. The configuration register is implemented for compliance with ST standard SPI 3.0 and contains only the watchdog trigger bit at D0.

Figure 40. Write configuration register



1. The configuration register is implemented for compliance with ST standard SPI 3.0 and contains only the watchdog trigger bit at D0.

### 6.1.5 Address mapping

Table 48. Address mapping

| RAM Address | Description        | Access | ROM Address | Description       | Access |
|-------------|--------------------|--------|-------------|-------------------|--------|
| 3FH         | <Configuration>    | R/W    | 3FH         | Reserved          | N/A    |
| ...         | ...                | ...    | 3EH         | <SPI frame ID>    | R      |
| 13H         | Status Register 3  | R      | ...         | Unused            | N/A    |
| 12H         | Status Register 2  | R      |             |                   |        |
| 11H         | Status Register 1  | R      |             |                   |        |
| ...         | ...                | ...    |             |                   |        |
| 06H         | Control Register 6 | R/W    |             |                   |        |
| 05H         | Control Register 5 | R/W    |             |                   |        |
| 04H         | Control Register 4 | R/W    | 03H         | <product code 2>  | R      |
| 03H         | Control Register 3 | R/W    | 02H         | <product code 1>  | R      |
| 02H         | Control Register 2 | R/W    | 01H         | <silicon version> | R      |
| 01H         | Control Register 1 | R/W    | 00H         | <ID Header>       | R      |
| 00H         | Reserved           | R/W    |             |                   |        |

The RAM memory area consists of 16 bit registers.

For the device information (ROM memory area) the eight most significant bits of the memory cell are used. The remaining 8 are zero.

All unused RAM and ROM addresses are read as '0'.

*Note:* The register definition for RAM address 00H is unused. A register value of all 0 must cause the device to enter a Fail-Safe state (interpreted as 'SDI stuck to GND' failure).

*Note:* ROM address 3FH is unused. An attempt to access this address must be recognized as a communication error ('SDI stuck to V<sub>CC</sub>' failure) and must cause the device to enter a Fail-Safe state.

### 6.1.6 Write operation

The write operation starts with a Command Byte followed by 2, data bytes. The number of data bytes is specified in the <SPI-frame-ID>.

#### Write command format

Table 49. Write command format: command byte

| MSB     |   |         |    |    |    |    |    | LSB |
|---------|---|---------|----|----|----|----|----|-----|
| Op Code |   | Address |    |    |    |    |    |     |
| 0       | 0 | A5      | A4 | A3 | A2 | A1 | A0 |     |



**Table 50. Write command format: data byte 1**

| MSB |     |     |     |     |     |    | LSB |
|-----|-----|-----|-----|-----|-----|----|-----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8  |

**Table 51. Write command format: data byte 2**

| MSB |    |    |    |    |    |    | LSB |
|-----|----|----|----|----|----|----|-----|
| D7  | D6 | D5 | D4 | D3 | D2 | D1 | D0  |

OC0, OC1: operating code (00 for 'write' mode)

A0 to A5: address bits

An attempt to write 00H at RAM address 00H is recognized as a failure (SDI stuck to GND). The device enters a Fail-Safe state.

### 6.1.7 Format of data shifted out at SDO during Write cycle

**Table 52. Format of data shifted out at SDO during write cycle: global status register**

| Bit 7                   | Bit 6               | Bit 5                          | Bit 4 | Bit 3 | Bit 2               | Bit 1                       | Bit 0     |
|-------------------------|---------------------|--------------------------------|-------|-------|---------------------|-----------------------------|-----------|
| Global error flag (GEF) | Communication error | Not (chip reset or comm error) | TSD2  | TSD1  | V <sub>1</sub> Fail | V <sub>S</sub> Fail (OV/UV) | Fail safe |

**Table 53. Format of data shifted out at SDO during write cycle: data byte 1**

| MSB | Previous content of addressed register |     |     |     |     |    | LSB |
|-----|--|-----|-----|-----|-----|----|-----|
| D15 | D14                                    | D13 | D12 | D11 | D10 | D9 | D8  |

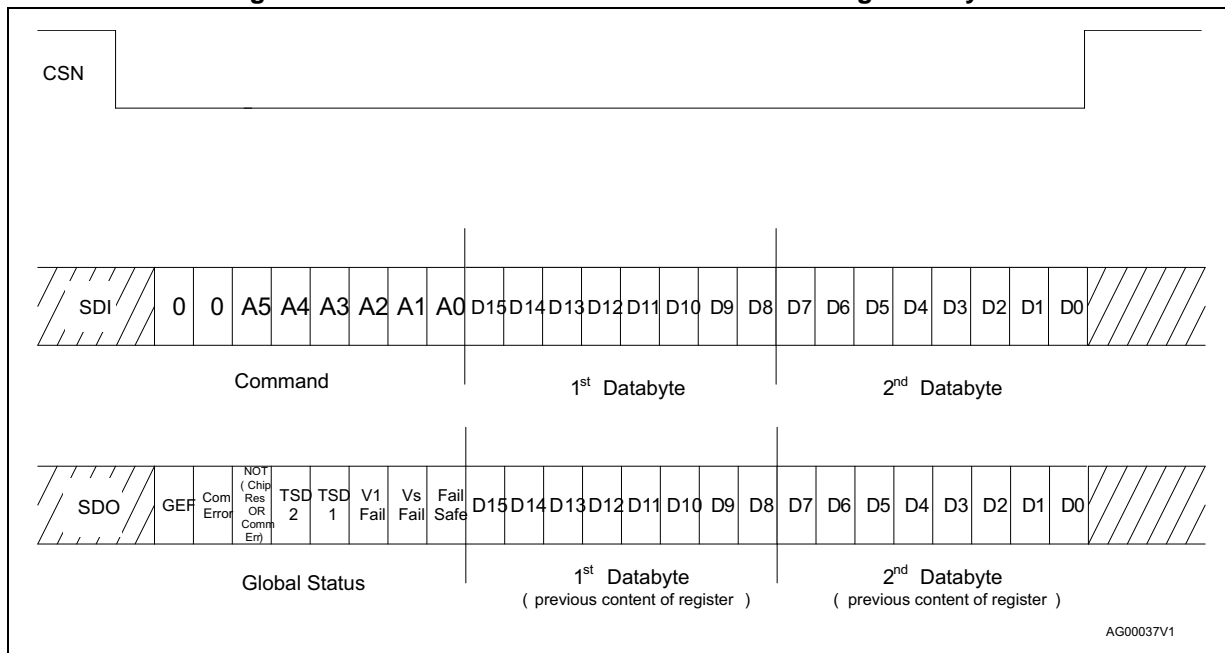
**Table 54. Format of data shifted out at SDO during write cycle: data byte 2**

| MSB | Previous content of addressed register |    |    |    |    |    | LSB |
|-----|--|----|----|----|----|----|-----|
| D7  | D6                                     | D5 | D4 | D3 | D2 | D1 | D0  |

Failures are indicated by activating the corresponding bit of the <Global Status> register.

The returned data byte(s) represent(s) the previous content of the accessed register

Figure 41. Format of data shifted out at SDO during write cycle



### 6.1.8 Read operation

Table 55. Read command format: command byte

| MSB     |   |         |    |    |    |    | LSB |
|---------|---|---------|----|----|----|----|-----|
| Op Code |   | Address |    |    |    |    |     |
| 0       | 1 | A5      | A4 | A3 | A2 | A1 | A0  |

Table 56. Read command format: data byte 1

| MSB |   |   |   |   |   |   | LSB |
|-----|---|---|---|---|---|---|-----|
| 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0   |

Table 57. Read command format: data byte 2

| MSB |   |   |   |   |   |   | LSB |
|-----|---|---|---|---|---|---|-----|
| 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0   |

OC0, OC1: operating code (01 for 'read' mode)

A0 to A5: Address Bits

### 6.1.9 Format of data shifted out at SDO during Read cycle

**Table 58. Format of data shifted out at SDO during read cycle: global status register**

| Bit 7                   | Bit 6               | Bit 5                          | Bit 4 | Bit 3 | Bit 2               | Bit 1                       | Bit 0     |
|-------------------------|---------------------|--------------------------------|-------|-------|---------------------|-----------------------------|-----------|
| Global error flag (GEF) | Communication error | Not (chip reset OR comm error) | TSD2  | TSD1  | V <sub>1</sub> Fail | V <sub>S</sub> Fail (OV/UV) | Fail safe |

**Table 59. Format of data shifted out at SDO during read cycle: data byte 1**

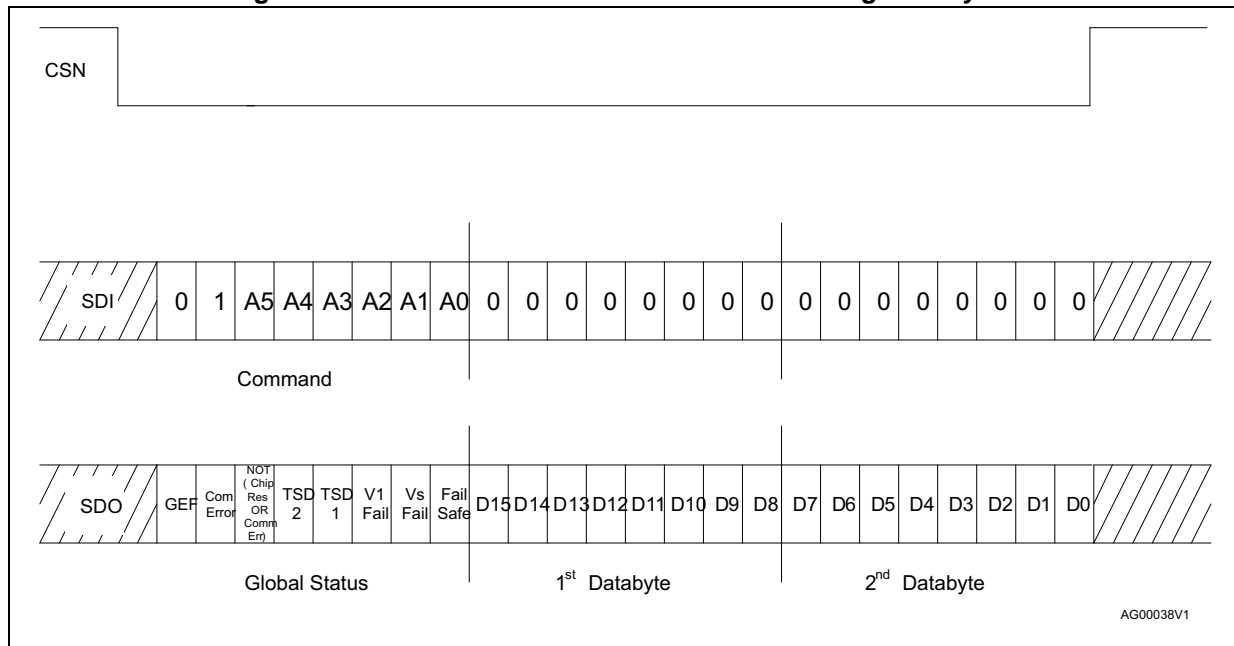
| MSB | Previous content of addressed register |     |     |     |     |    | LSB |
|-----|--|-----|-----|-----|-----|----|-----|
| D15 | D14                                    | D13 | D12 | D11 | D10 | D9 | D8  |

**Table 60. Format of data shifted out at SDO during read cycle: data byte 2**

| MSB | Previous content of addressed register |    |    |    |    |    | LSB |
|-----|--|----|----|----|----|----|-----|
| D7  | D6                                     | D5 | D4 | D3 | D2 | D1 | D0  |

Failures are indicated by activating the corresponding bit of the <Global Status> register. The returned data byte(s) represent(s) the content of the register to be read.

**Figure 42. Format of data shifted out at SDO during read cycle**



### 6.1.10 Read and Clear Status Operation

The 'Read and Clear Status' operation starts with a Command Byte followed 2 data bytes. The number of data bytes is specified in the <SPI-frame-ID>. The content of the data bytes is 'don't care'. The content of the addressed Status Register is transferred to SDO within the same frame ('in-frame response') and is subsequently cleared.

A 'Read and Clear Status' operation with address 3FH clears all Status registers (incl. the <Global Status> register). The Configuration Register is read by this operation.

**Table 61. Read and clear status command format: command byte**

| MSB     |   |         |    |    |    |    | LSB |
|---------|---|---------|----|----|----|----|-----|
| Op Code |   | Address |    |    |    |    |     |
| 1       | 0 | A5      | A4 | A3 | A2 | A1 | A0  |

**Table 62. Read and clear status command format: data byte 1**

| MSB |   |   |   |   |   |   | LSB |
|-----|---|---|---|---|---|---|-----|
| 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0   |

**Table 63. Read and clear status command format: data byte 2**

| MSB |   |   |   |   |   |   | LSB |
|-----|---|---|---|---|---|---|-----|
| 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0   |

OC0, OC1: operating code (10 for 'read and clear status' mode)

A0 to A5: address bits

#### Format of data shifted out at SDO during 'Read and Clear Status' operation

**Table 64. Format of data shifted out at SDO during read and clear status: global status register**

| Bit 7                   | Bit 6               | Bit 5                          | Bit 4 | Bit 3 | Bit 2               | Bit 1                       | Bit 0     |
|-------------------------|---------------------|--------------------------------|-------|-------|---------------------|-----------------------------|-----------|
| Global error flag (GEF) | Communication error | Not (chip reset OR comm error) | TSD2  | TSD1  | V <sub>1</sub> Fail | V <sub>S</sub> Fail (OV/UV) | Fail safe |

**Table 65. Format of data shifted out at SDO during read and clear status: data byte 1**

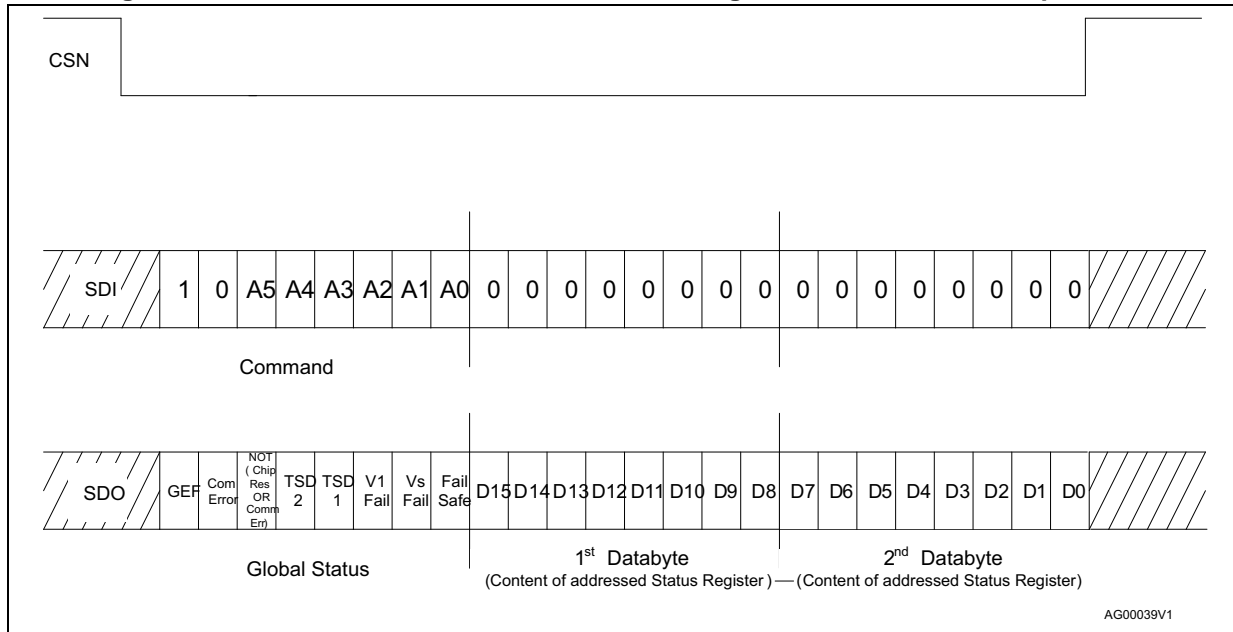
| MSB | Previous content of addressed register |     |     |     |     |    | LSB |
|-----|--|-----|-----|-----|-----|----|-----|
| D15 | D14                                    | D13 | D12 | D11 | D10 | D9 | D8  |

**Table 66. Format of data shifted out at SDO during read and clear status: data byte 2**

| MSB | Previous content of addressed register |    |    |    |    |    | LSB |
|-----|--|----|----|----|----|----|-----|
| D7  | D6                                     | D5 | D4 | D3 | D2 | D1 | D0  |

Failures are indicated by activating the corresponding bit of the <Global Status> register.  
 The returned data byte(s) represent(s) the content of the register to be read.

**Figure 43. Format of data shifted out at SDO during read and clear status operation**



### 6.1.11 Read device information

The device information is stored at the ROM addresses defined below and is read using the respective operating code.

**Table 67. Read device information**

| Op Code |     | ROM address | Device information  | Value  |
|---------|-----|-------------|---|--------|
| OC1     | OC0 |             |   |        |
| 1       | 1   | 3FH         | Reserved  | 00     |
| 1       | 1   | 3EH         | <SPI frame ID><br>Includes frame width and availability of watchdog | 42 Hex |
| 1       | 1   | 04H to 3DH  | unused  | 00     |
| 1       | 1   | 03H         | <product code 2><br>Unique product identifier                       | 27h    |
| 1       | 1   | 02H         | <product code 1><br>Unique product identifier                       | 4Bh    |
| 1       | 1   | 01H         | <silicon version><br>Indicates Design Version                       | 05h    |
| 1       | 1   | 00H         | <ID Header><br>Device family max address of device information      | 43 Hex |

The <ID-Header> (ROM address 00H) indicates the product family and specifies the highest address which contains product information

**Table 68. ID-header**

| Bit 7             | Bit 6 | Bit 5   | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------------|-------|---|-------|-------|-------|-------|-------|
| 0                 | 1     | 0   | 0     | 0     | 0     | 1     | 1     |
| Family Identifier |       | Highest address containing device information |       |       |       |       |       |

<Family Identifier>: 01 Hex (BCD)

<Highest address>: 03 Hex

**Table 69. Family identifier**

| Bit 7 | Bit 6 | Meaning        |
|-------|-------|----------------|
| 0     | 0     | VIpower        |
| 0     | 1     | BCD            |
| 1     | 0     | VIpower hybrid |
| 1     | 1     | —              |

The <Product Code 1> (ROM address 02H) and <Product Code 2> (ROM address 03H) represents a unique code to identify the product name.

<Product Code 1>: 4BHex

<Product Code 2>: 27 Hex

The <Silicon Version> (ROM address 01H) provides information about the silicon version according to the table below:

**Table 70. Silicon version identifier**

| Bit 7    | Bit 6 | Bit 5 | Bit 4 | Bit 3           | Bit 2 | Bit 1 | Bit 0 |
|----------|-------|-------|-------|-----------------|-------|-------|-------|
| Reserved |       |       |       | Silicon version |       |       |       |

The <SPI-frame-ID> (ROM address 3EH) provides information about the register width (1, 2, 3 bytes) and the availability of 'Burst Mode Read' and watchdog.

**Table 71. SPI-frame-ID**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2  | Bit 1  | Bit 0  |
|-------|-------|-------|-------|-------|--------|--------|--------|
| 0     | 1     | 0     | 0     | 0     | 0      | 1      | 0      |
| BR    | WD    | X     | X     | X     | 32-bit | 24-bit | 16-bit |

BR: Burst-Mode read (1 = Burst-Mode read is supported)

WD: Watchdog (1 = available, 0 = not available)

32-, 24-, 16-bit: width of SPI frame

<Burst Mode>: not supported

<Watchdog>: available

<Frame width>: 24 bit

## 6.2 SPI registers

### 6.2.1 Overview command byte

Table 72. SPI register: command byte

| Read/write |   | Address |   |   |   |   |   |
|------------|---|---------|---|---|---|---|---|
| x          | x | x       | x | x | x | x | x |

Table 73. SPI register: mode selection

| Read/write |   | Mode selection   |
|------------|---|------------------|
| 0          | 0 | Write            |
| 0          | 1 | Read             |
| 1          | 0 | Read and clear   |
| 1          | 1 | Read device info |

Table 74. SPI register: CTRL register selection

| CTRL register 1...6 |   |   |   |   |   | CTRL register selection |
|---------------------|---|---|---|---|---|-------------------------|
| 0                   | 0 | 0 | 0 | 0 | 1 | CTRL register1          |
| 0                   | 0 | 0 | 0 | 1 | 0 | CTRL register2          |
| 0                   | 0 | 0 | 0 | 1 | 1 | CTRL register3          |
| 0                   | 0 | 0 | 1 | 0 | 0 | CTRL register4          |
| 0                   | 0 | 0 | 1 | 0 | 1 | CTRL register5          |
| 0                   | 0 | 0 | 1 | 1 | 0 | CTRL register6          |
| 0                   | 0 | 0 | 1 | 1 | 1 | CTRL register7          |
| 0                   | 0 | 1 | 0 | 0 | 0 | CTRL register8          |
| 0                   | 0 | 1 | 0 | 0 | 1 | CTRL Register9          |
| 0                   | 0 | 1 | 0 | 1 | 0 | CTRL Register10         |
| 0                   | 0 | 1 | 0 | 1 | 1 | CTRL Register11         |
| 0                   | 0 | 1 | 1 | 0 | 0 | CTRL Register12         |
| 0                   | 0 | 1 | 1 | 0 | 1 | CTRL Register13         |
| 0                   | 0 | 1 | 1 | 1 | 0 | CTRL Register14         |
| 0                   | 0 | 1 | 1 | 1 | 1 | CTRL Register15         |
| 0                   | 1 | 0 | 0 | 0 | 0 | CTRL Register16         |

**Table 74. SPI register: CTRL register selection (continued)**

| CTRL register 1...6 |   |   |   |   |   | CTRL register selection |
|---------------------|---|---|---|---|---|-------------------------|
| 1                   | 0 | 0 | 0 | 1 | 0 | CTRL Register34         |
| 1                   | 0 | 0 | 0 | 1 | 1 | CTRL Register35         |
| 1                   | 1 | 1 | 1 | 1 | 1 | Configuration Register  |

**Table 75. SPI register: STAT register selection**

| STAT register. 1...3 |   |   |   |   |   | STAT register selection |
|----------------------|---|---|---|---|---|-------------------------|
| 0                    | 1 | 0 | 0 | 0 | 1 | STAT register1          |
| 0                    | 1 | 0 | 0 | 1 | 0 | STAT register2          |
| 0                    | 1 | 0 | 0 | 1 | 1 | STAT register3          |
| 0                    | 1 | 0 | 1 | 0 | 0 | STAT Register4          |
| 0                    | 1 | 0 | 1 | 0 | 1 | STAT Register5          |

### 6.2.2 Overview control register

**Table 76. Overview of control register data bytes**

|          | 1 <sup>st</sup> data byte <15:8> |       |          |          |           |          |          |          | 2 <sup>nd</sup> data byte <7:0> |           |           |           |          |          |         |        |
|----------|----------------------------------|-------|----------|----------|-----------|----------|----------|----------|---------------------------------|-----------|-----------|-----------|----------|----------|---------|--------|
|          | <b>Control register 1, data</b>  |       |          |          |           |          |          |          |                                 |           |           |           |          |          |         |        |
| Default  | 0                                | 0     | 0        | 0        | 0         | 0        | 0        | 0        | 0                               | 0         | 0         | 0         | 0        | 0        | 0       | 0      |
| Function | OUTH3                            | OUTH3 | OUT4     | OUT4     | OUTH3_EXT | OUT3     | OUT2     | OUT1     | REL2                            | REL1      | V2        | V2        | Parity   | Stby sel | Go Stby | Trig   |
| Group    | HS control                       |       |          |          |           |          |          |          | LS Output, V2 and mode control  |           |           |           |          |          |         |        |
|          | <b>Control register 2, data</b>  |       |          |          |           |          |          |          |                                 |           |           |           |          |          |         |        |
| Default  | 0                                | 0     | 0        | 0        | 0         | 0        | 0        | 0        | 0                               | 0         | 0         | 0         | 0        | 1        | 1       | 1      |
| Function | Reserved                         |       | WU3_Filt | WU3_Filt | WU2_Filt  | WU2_Filt | WU1_Filt | WU1_Filt | Reserved                        | WU3_Pu/Pd | WU2_Pu/Pd | WU1_Pu/Pd | Reserved | WU3_EN   | WU2_EN  | WU1_EN |
| Group    | Wake-up control                  |       |          |          |           |          |          |          | Wake-up control                 |           |           |           |          |          |         |        |





Table 76. Overview of control register data bytes (continued)

|                                 | 1 <sup>st</sup> data byte <15:8> |               |               |               |               |                      |               |               | 2 <sup>nd</sup> data byte <7:0>      |              |                 |              |              |              |               |               |
|---------------------------------|----------------------------------|---------------|---------------|---------------|---------------|----------------------|---------------|---------------|--------------------------------------|--------------|-----------------|--------------|--------------|--------------|---------------|---------------|
| <b>Control register 3, data</b> |                                  |               |               |               |               |                      |               |               |                                      |              |                 |              |              |              |               |               |
| Default                         | 0                                | 0             | 0             | 0             | 0             | 0                    | 0             | 0             | 0                                    | 0            | 0               | 0            | 1            | 1            | 0             | 0             |
| Function                        | Reserved                         | T1_On         | T1_Per_MSB    | T1_Per_LSB    | Reserved      | T2_On                | T2_Per_MSB    | T2_Per_LSB    | Reserved                             |              | WD_time_MSB     | WD_time_LSB  | LIN_WU_En    | CAN_WU_En    | Wake_Timer_En | Wake_Time_Sel |
| Group                           | Timer Settings                   |               |               |               |               |                      |               |               | Watchdog and cyclic wake up settings |              |                 |              |              |              |               |               |
| <b>Control register 4, data</b> |                                  |               |               |               |               |                      |               |               |                                      |              |                 |              |              |              |               |               |
| Default                         | 0                                | 0             | 0             | 1             | 0             | 1                    | 0             | 0             | 1                                    | 1            | 1               | 0            | 0            | 0            | 0             | 0             |
| Function                        | Reserved                         | ICMP          | OUTHS_rec_en  | VLOCK_OUT_EN  | Reserved      | LS_OV/UV_shutdown_en | V1Reset_Level | V1Reset_Level | LIN_Pu_En                            | Reserved     | Lin_TxD_Tout_En | CAN_ACT      | CAN_Loop_En  | Reserved     |               | CAN_Rec_Only  |
| Group                           | Control (other)                  |               |               |               |               |                      |               |               | Transceiver settings                 |              |                 |              |              |              |               |               |
| <b>Control register 5, data</b> |                                  |               |               |               |               |                      |               |               |                                      |              |                 |              |              |              |               |               |
| Default                         | 0                                | 1             | 1             | 1             | 1             | 1                    | 1             | 1             | 0                                    | 0            | 0               | 0            | 0            | 0            | 0             | 0             |
| Function                        | Reserved                         | PWM2_OFF_DC_6 | PWM2_OFF_DC_5 | PWM2_OFF_DC_4 | PWM2_OFF_DC_3 | PWM2_OFF_DC_2        | PWM2_OFF_DC_1 | PWM2_OFF_DC_0 | PWM Freq                             | PWM1_ON_DC_6 | PWM1_ON_DC_5    | PWM1_ON_DC_4 | PWM1_ON_DC_3 | PWM1_ON_DC_2 | PWM1_ON_DC_1  | PWM1_ON_DC_0  |
| Group                           | PWM2 setting                     |               |               |               |               |                      |               |               | PWM1 setting                         |              |                 |              |              |              |               |               |
| <b>Control register 6, data</b> |                                  |               |               |               |               |                      |               |               |                                      |              |                 |              |              |              |               |               |
| Default                         | 0                                | 1             | 1             | 1             | 1             | 1                    | 1             | 1             | 0                                    | 0            | 0               | 0            | 0            | 0            | 0             | 0             |
| Function                        | Reserved                         | PWM4_OFF_DC_6 | PWM4_OFF_DC_5 | PWM4_OFF_DC_4 | PWM4_OFF_DC_3 | PWM4_OFF_DC_2        | PWM4_OFF_DC_1 | PWM4_OFF_DC_0 | Reserved                             | PWM3_ON_DC_6 | PWM3_ON_DC_5    | PWM3_ON_DC_4 | PWM3_ON_DC_3 | PWM3_ON_DC_2 | PWM3_ON_DC_1  | PWM3_ON_DC_0  |
| Group                           | PWM4 setting                     |               |               |               |               |                      |               |               | PWM3 setting                         |              |                 |              |              |              |               |               |

**Table 76. Overview of control register data bytes (continued)**

|                                  | 1 <sup>st</sup> data byte <15:8> |           |           |           |           |           |          |          | 2 <sup>nd</sup> data byte <7:0> |          |          |          |          |          |           |           |
|----------------------------------|----------------------------------|-----------|-----------|-----------|-----------|-----------|----------|----------|---------------------------------|----------|----------|----------|----------|----------|-----------|-----------|
| <b>Control register 7, data</b>  |                                  |           |           |           |           |           |          |          |                                 |          |          |          |          |          |           |           |
| Default                          | 0                                | 0         | 0         | 0         | 0         | 0         | 0        | 0        | 0                               | 0        | 0        | 0        | 0        | 0        | 0         | 0         |
| Function                         | EXT_ID_15                        | EXT_ID_14 | EXT_ID_13 | EXT_ID_12 | EXT_ID_11 | EXT_ID_10 | EXT_ID_9 | EXT_ID_8 | EXT_ID_7                        | EXT_ID_6 | EXT_ID_5 | EXT_ID_4 | EXT_ID_3 | EXT_ID_2 | EXT_ID_1  | EXT_ID_0  |
| Group                            | Selective Wakeup Settings        |           |           |           |           |           |          |          |                                 |          |          |          |          |          |           |           |
| <b>Control register 8, data</b>  |                                  |           |           |           |           |           |          |          |                                 |          |          |          |          |          |           |           |
| Default                          | 0                                | 0         | 0         | 0         | 0         | 0         | 0        | 0        | 0                               | 0        | 0        | 0        | 0        | 0        | 0         | 0         |
| Function                         | Reserved                         |           |           | ID_10     | ID_9      | ID_8      | ID_7     | ID_6     | ID_5                            | ID_4     | ID_3     | ID_2     | ID_1     | ID_0     | EXT_ID_17 | EXT_ID_16 |
| Group                            | Selective Wakeup Settings        |           |           |           |           |           |          |          |                                 |          |          |          |          |          |           |           |
| <b>Control register 9, data</b>  |                                  |           |           |           |           |           |          |          |                                 |          |          |          |          |          |           |           |
| Default                          | 0                                | 0         | 0         | 0         | 0         | 0         | 0        | 0        | 0                               | 0        | 0        | 0        | 0        | 0        | 0         | 0         |
| Function                         | Reserved                         |           |           |           |           |           |          |          |                                 |          |          | CAN_IDE  | DLC_3    | DLC_2    | DLC_1     | DLC_0     |
| Group                            | Selective Wakeup Settings        |           |           |           |           |           |          |          |                                 |          |          |          |          |          |           |           |
| <b>Control register 10, data</b> |                                  |           |           |           |           |           |          |          |                                 |          |          |          |          |          |           |           |
| Default                          | 0                                | 0         | 0         | 0         | 0         | 0         | 0        | 0        | 0                               | 0        | 0        | 0        | 0        | 0        | 0         | 0         |
| Function                         | Data Byte 2                      |           |           |           |           |           |          |          | Data Byte 1                     |          |          |          |          |          |           |           |
| Group                            | Selective Wakeup Settings        |           |           |           |           |           |          |          |                                 |          |          |          |          |          |           |           |
| <b>Control register 11, data</b> |                                  |           |           |           |           |           |          |          |                                 |          |          |          |          |          |           |           |
| Default                          | 0                                | 0         | 0         | 0         | 0         | 0         | 0        | 0        | 0                               | 0        | 0        | 0        | 0        | 0        | 0         | 0         |
| Function                         | Data Byte 4                      |           |           |           |           |           |          |          | Data Byte 3                     |          |          |          |          |          |           |           |
| Group                            | Selective Wakeup Settings        |           |           |           |           |           |          |          |                                 |          |          |          |          |          |           |           |
| <b>Control register 12, data</b> |                                  |           |           |           |           |           |          |          |                                 |          |          |          |          |          |           |           |
| Default                          | 0                                | 0         | 0         | 0         | 0         | 0         | 0        | 0        | 0                               | 0        | 0        | 0        | 0        | 0        | 0         | 0         |
| Function                         | Data Byte 6                      |           |           |           |           |           |          |          | Data Byte 5                     |          |          |          |          |          |           |           |
| Group                            | Selective Wakeup Settings        |           |           |           |           |           |          |          |                                 |          |          |          |          |          |           |           |

Table 76. Overview of control register data bytes (continued)

|                                  | 1 <sup>st</sup> data byte <15:8> |                |                |                |                |                |               |               | 2 <sup>nd</sup> data byte <7:0> |               |               |               |               |               |                |                |
|----------------------------------|----------------------------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|---------------------------------|---------------|---------------|---------------|---------------|---------------|----------------|----------------|
| <b>Control register 13, data</b> |                                  |                |                |                |                |                |               |               |                                 |               |               |               |               |               |                |                |
| Default                          | 0                                | 0              | 0              | 0              | 0              | 0              | 0             | 0             | 0                               | 0             | 0             | 0             | 0             | 0             | 0              |                |
| Function                         | Data Byte 8                      |                |                |                |                |                |               |               | Data Byte 7                     |               |               |               |               |               |                |                |
| Group                            | Selective Wakeup Settings        |                |                |                |                |                |               |               |                                 |               |               |               |               |               |                |                |
| <b>Control register 14, data</b> |                                  |                |                |                |                |                |               |               |                                 |               |               |               |               |               |                |                |
| Default                          | 0                                | 0              | 0              | 0              | 0              | 0              | 0             | 0             | 0                               | 0             | 0             | 0             | 0             | 0             | 0              |                |
| Function                         | EXT_ID_Mask_15                   | EXT_ID_Mask_14 | EXT_ID_Mask_13 | EXT_ID_Mask_12 | EXT_ID_Mask_11 | EXT_ID_Mask_10 | EXT_ID_Mask_9 | EXT_ID_Mask_8 | EXT_ID_Mask_7                   | EXT_ID_Mask_6 | EXT_ID_Mask_5 | EXT_ID_Mask_4 | EXT_ID_Mask_3 | EXT_ID_Mask_2 | EXT_ID_Mask_1  | EXT_ID_Mask_0  |
| Group                            | Selective Wakeup Settings        |                |                |                |                |                |               |               |                                 |               |               |               |               |               |                |                |
| <b>Control register 15, data</b> |                                  |                |                |                |                |                |               |               |                                 |               |               |               |               |               |                |                |
| Defaults                         | 0                                | 0              | 0              | 0              | 0              | 0              | 0             | 0             | 0                               | 0             | 0             | 0             | 0             | 0             | 0              |                |
| Function                         | Reserved                         |                |                | ID_Mask_10     | ID_Mask_9      | ID_Mask_8      | ID_Mask_7     | ID_Mask_6     | ID_Mask_5                       | ID_Mask_4     | ID_Mask_3     | ID_Mask_2     | ID_Mask_1     | ID_Mask_0     | EXT_ID_Mask_17 | EXT_ID_Mask_16 |
| Group                            | Selective Wakeup Settings        |                |                |                |                |                |               |               |                                 |               |               |               |               |               |                |                |
| <b>Control register 16, data</b> |                                  |                |                |                |                |                |               |               |                                 |               |               |               |               |               |                |                |
| Defaults                         | 0                                | 0              | 0              | 0              | 0              | 0              | 0             | 0             | 0                               | 0             | 0             | 0             | 0             | 0             | 0              |                |
| Function                         | CR16_30                          | CR16_21        | CR16_20        | CR16_14        | CR16_13        | CR16_12        | CR16_11       | CR16_10       | Reserved                        | Samp 2        | Samp 1        | Samp 0        | Reserved      | BR1           | BR2            | SW_EN          |
| Group                            | Selective Wakeup Settings        |                |                |                |                |                |               |               |                                 |               |               |               |               |               |                |                |
| <b>Control register 34, data</b> |                                  |                |                |                |                |                |               |               |                                 |               |               |               |               |               |                |                |
| Defaults                         | 0                                | 0              | 0              | 0              | 0              | 0              | 0             | 0             | 0                               | 0             | 0             | 0             | 0             | 0             | 0              | 1              |
| Function                         | Reserved                         |                |                |                |                |                |               |               |                                 |               |               |               |               |               |                | WD_EN          |
| <b>Control Register 35, data</b> |                                  |                |                |                |                |                |               |               |                                 |               |               |               |               |               |                |                |
| Defaults                         | 0                                | 0              | 0              | 0              | 0              | 0              | 0             | 0             | 0                               | 1             | 1             | 0             | 1             | 1             | 0              |                |
| Function                         | Reserved                         |                |                |                |                |                |               |               |                                 | CR35_25       | CR35_24       | CR35_23       | CR35_22       | CR35_21       | CR35_20        | CR35_10        |

**Table 76. Overview of control register data bytes (continued)**

|                              | 1 <sup>st</sup> data byte <15:8> |   |   |   |   |   |   |   | 2 <sup>nd</sup> data byte <7:0> |   |   |   |   |   |      |  |
|------------------------------|----------------------------------|---|---|---|---|---|---|---|---------------------------------|---|---|---|---|---|------|--|
| Configuration Register, data |                                  |   |   |   |   |   |   |   |                                 |   |   |   |   |   |      |  |
| Defaults                     | 0                                | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0 | 0 | 0    |  |
| Function                     | Reserved                         |   |   |   |   |   |   |   |                                 |   |   |   |   |   | TRIG |  |

Note: Reserved bit must be kept at their default values.  
 Writing to other register address is not allowed

**6.2.3 Control Register 1**

**Table 77. Control register 1: command and data bytes**

| Command byte |   |         |   |   |   |   |   | 1 <sup>st</sup> data byte | 2 <sup>nd</sup> data byte |
|--------------|---|---------|---|---|---|---|---|---------------------------|---------------------------|
| Read/write   |   | Address |   |   |   |   |   |                           |                           |
| x            | x | 0       | 0 | 0 | 0 | 0 | 1 | Data, 8bit                | Data, 8 bit               |

**Table 78. Control register 1, data bytes**

|          | 1 <sup>st</sup> data byte <15:8> |         |        |        |           |      |      |      | 2 <sup>nd</sup> data byte <7:0> |      |      |      |        |          |         |      |
|----------|----------------------------------|---------|--------|--------|-----------|------|------|------|---------------------------------|------|------|------|--------|----------|---------|------|
| Defaults | 0                                | 0       | 0      | 0      | 0         | 0    | 0    | 0    | 0                               | 0    | 0    | 0    | 0      | 0        | 0       | 0    |
| Function | OUTHS_2                          | OUTHS_1 | OUT4_2 | OUT4_1 | OUTHS_EXT | OUT3 | OUT2 | OUT1 | REL2                            | REL1 | V2_2 | V2_1 | Parity | STBY_SEL | GO_STBY | Trig |
| Group    | HS control                       |         |        |        |           |      |      |      | LS Output, V2 and mode control  |      |      |      |        |          |         |      |

**Table 79. Control register 1, bits**

| Bit | Name  | Comment                 |         |         |                           |  |
|-----|-------|-------------------------|---------|---------|---------------------------|--|
| 15  | OUTHS | Select mode of OUTHS    |         |         |                           |  |
| 14  |       | OUTHS_EXT               | OUTHS_2 | OUTHS_1 | Mode                      |  |
|     |       | 0                       | 0       | 0       | HS off                    |  |
|     |       | 0                       | 0       | 1       | HS cyclic on with timer 1 |  |
|     |       | 0                       | 1       | 0       | HS controlled by PWM4     |  |
|     |       | 0                       | 1       | 1       | HS cyclic on with Timer 2 |  |
|     |       | 1                       | 1       | 0       | PWM3                      |  |
|     |       | 1                       | x       | 1       | HS on                     |  |
|     |       | Active and standby mode |         |         |                           |  |



**Table 79. Control register 1, bits (continued)**

| Bit | Name     | Comment                               |               |                           |
|-----|----------|---------------------------------------|---------------|---------------------------|
| 13  | OUT4     | Select mode of OUT4                   |               |                           |
| 12  |          | <b>OUT4_2</b>                         | <b>OUT4_1</b> | <b>Mode</b>               |
|     |          | 0                                     | 0             | HS off                    |
|     |          | 0                                     | 1             | HS on                     |
|     |          | 1                                     | 0             | HS controlled by PWM4     |
|     |          | 1                                     | 1             | HS cyclic on with Timer 2 |
|     |          | Active and standby mode               |               |                           |
| 11  | OUTH_EXT | Extended function of OUTHS; see OUTHS |               |                           |
| 10  | OUT3     | Select mode of OUT3                   |               |                           |
|     |          | <b>OUT3</b>                           |               | <b>Mode</b>               |
|     |          | 0                                     | Select FSO    | Active and standby mode   |
|     |          | 1                                     | Select PWM3   |                           |
| 9   | OUT2     | Select mode of OUT2                   |               |                           |
|     |          | <b>OUT2</b>                           |               | <b>Mode</b>               |
|     |          | 0                                     | Select PWM2   | Active and standby mode   |
|     |          | 1                                     | Select timer2 |                           |
| 8   | OUT1     | Select mode of OUT1                   |               |                           |
|     |          | <b>OUT1</b>                           |               | <b>Mode</b>               |
|     |          | 0                                     | Select PWM1   | Active and standby mode   |
|     |          | 1                                     | Select timer1 |                           |

**Table 79. Control register 1, bits (continued)**

| Bit    | Name           | Comment   |                        |   |                                |
|--------|----------------|---|------------------------|---|--------------------------------|
| 7      | REL2           | Select mode of REL2   |                        |   |                                |
|        |                | <b>REL2</b>   |                        | <b>Mode</b>   |                                |
|        |                | 0   | REL2 off               | Active and standby mode   |                                |
|        |                | 1   | REL2 on                | Active mode   |                                |
| 6      | REL1           | Select mode of REL1   |                        |   |                                |
|        |                | <b>REL1</b>   |                        | <b>Mode</b>   |                                |
|        |                | 0   | REL1 off               | Active and standby mode   |                                |
|        |                | 1   | REL1 on                | Active mode   |                                |
| 5<br>4 | V <sub>2</sub> | <b>V<sub>2_2</sub></b>  | <b>V<sub>2_1</sub></b> |   |                                |
|        |                | 0   | 0                      | V <sub>2</sub> OFF in all modes   |                                |
|        |                | 0   | 1                      | V <sub>2</sub> ON in active mode; OFF in V <sub>1</sub> /V <sub>Bat_standby</sub> mode        |                                |
|        |                | 1   | 0                      | V <sub>2</sub> ON in Active/V <sub>1-standby</sub> mode; OFF in V <sub>Bat_standby</sub> mode |                                |
|        |                | 1   | 1                      | V <sub>2</sub> ON in all modes  |                                |
|        |                |   |                        |   |                                |
| 3      | Parity         | The Stby_sel and Go_stby bits are protected by a parity check   |                        |   |                                |
|        |                | The bits Stby_sel, Go_stby and Parity must represent an even number of '1', otherwise the command is ignored and the Communication Error bit is set in the Global Status Register. Following are the valid settings |                        |   |                                |
|        |                | <b>Parity</b>   | <b>STBY_SEL</b>        | <b>GO_STBY</b>  | <b>Command</b>                 |
|        |                | 0   | 1                      | 1   | Go to V <sub>1-standby</sub>   |
|        |                | 1   | 0                      | 1   | Go to V <sub>Bat_standby</sub> |
|        |                | 0   | 0                      | 0   | No transition to standby       |
|        |                | 1   | 1                      | 0   | No transition to standby       |

**Table 79. Control register 1, bits (continued)**

| Bit | Name     | Comment                  |                               |
|-----|----------|--------------------------|-------------------------------|
| 2   | STBY_SEL | Select standby mode      |                               |
|     |          | 0                        | V <sub>Bat_standby</sub> mode |
|     |          | 1                        | V <sub>1_standby</sub> mode   |
| 1   | GO_STBY  | Execute standby mode     |                               |
|     |          | 0                        | No action                     |
|     |          | 1                        | Execute standby mode          |
| 0   | TRIG     | Trigger Bit for Watchdog |                               |

**6.2.4 Control Register 2**

**Table 80. Control register 2: command and data bytes**

| Command byte |         | 1 <sup>st</sup> data byte |   |   |   |   |   | 2 <sup>nd</sup> data byte |  |  |             |
|--------------|---------|---------------------------|---|---|---|---|---|---------------------------|--|--|-------------|
| Read/write   | Address |                           |   |   |   |   |   |                           |  |  |             |
| x            | x       | 0                         | 0 | 0 | 0 | 1 | 0 | Data, 8bit                |  |  | Data, 8 bit |

**Table 81. Control register 2, data bytes**

|          | 1 <sup>st</sup> data byte <15:8> |              |              |              |              |              |              | 2 <sup>nd</sup> data byte <7:0> |           |           |           |          |        |        |        |   |
|----------|----------------------------------|--------------|--------------|--------------|--------------|--------------|--------------|---------------------------------|-----------|-----------|-----------|----------|--------|--------|--------|---|
| Defaults | 0                                | 0            | 0            | 0            | 0            | 0            | 0            | 0                               | 0         | 0         | 0         | 0        | 0      | 1      | 1      | 1 |
| Function | Reserved                         | WU3_Filt_MSB | WU3_Filt_LSB | WU2_Filt_MSB | WU2_Filt_LSB | WU1_Filt_MSB | WU1_Filt_LSB | Reserved                        | WU3_Pu/Pd | WU2_Pu/Pd | WU1_Pu/Pd | Reserved | WU3_EN | WU2_EN | WU1_EN |   |
| Group    | Wakeup control                   |              |              |              |              |              |              | Wakeup control                  |           |           |           |          |        |        |        |   |

**Table 82. Control register 2, bits**

| Bit | Name     | Comment                 |
|-----|----------|-------------------------|
| 15  | Reserved | Must be kept at default |
| 14  | Reserved | Must be kept at default |

**Table 82. Control register 2, bits (continued)**

| Bit    | Name      | Comment                            |            |   |
|--------|-----------|------------------------------------|------------|---|
| 13, 12 | WU3_Filt  | Wakeup filter configuration        |            |   |
| 11, 10 | WU2_Filt  | <b>MSB</b>                         | <b>LSB</b> |   |
| 9, 8   | WU1_Filt  | 0                                  | 0          | Static, 64 $\mu$ s                      |
|        |           | 0                                  | 1          | Enabled with timer 2; 80 $\mu$ s blank  |
|        |           | 1                                  | 0          | Enabled with timer 2; 800 $\mu$ s blank |
|        |           | 1                                  | 1          | Enabled with timer 1; 800 $\mu$ s blank |
| 7      | Reserved  | Must be kept at default            |            |   |
| 6      | WU3_Pu/Pd | Pull up or pull down configuration |            |   |
| 5      | WU2_Pu/Pd | 0                                  | Pull down  |   |
| 4      | WU1_Pu/Pd | 1                                  | Pull up    |   |
| 3      | Reserved  | Must be kept at default            |            |   |
| 2      | WU3_EN    | Enable Wake up source              |            |   |
| 1      | WU2_EN    | 0                                  | Disable    |   |
| 0      | WU1_EN    | 1                                  | Enable     |   |

**6.2.5 Control Register 3**

**Table 83. Control register 3: command and data bytes**

| Command byte |   |         |   |   |   |   |   | 1 <sup>st</sup> data byte | 2 <sup>nd</sup> data byte |
|--------------|---|---------|---|---|---|---|---|---------------------------|---------------------------|
| Read/write   |   | Address |   |   |   |   |   |                           |                           |
| x            | x | 0       | 0 | 0 | 0 | 1 | 1 | Data, 8bit                | Data, 8 bit               |

**Table 84. Control register 3, data bytes**

|          | 1 <sup>st</sup> data byte <15:8> |       |            |            |          |       |            |            | 2 <sup>nd</sup> data byte <7:0>      |             |             |           |           |               |                   |   |
|----------|----------------------------------|-------|------------|------------|----------|-------|------------|------------|--------------------------------------|-------------|-------------|-----------|-----------|---------------|-------------------|---|
| Defaults | 0                                | 0     | 0          | 0          | 0        | 0     | 0          | 0          | 0                                    | 0           | 0           | 0         | 1         | 1             | 0                 | 0 |
| Function | Reserved                         | T1_On | T1_Per_MSB | T1_Per_LSB | Reserved | T2_On | T2_Per_MSB | T2_Per_LSB | Reserved                             | WD_time_MSB | WD_time_LSB | LIN_WU_En | CAN_WU_En | Wake_timer_en | Wake_timer_select |   |
| Group    | Timer Settings                   |       |            |            |          |       |            |            | Watchdog and cyclic wake up settings |             |             |           |           |               |                   |   |





Table 85. Control register 3, bits

| Bit | Name       | Comment  |     |        |   |       |   |       |   |   |       |   |   |       |   |   |        |
|-----|------------|--|-----|--------|---|-------|---|-------|---|---|-------|---|---|-------|---|---|--------|
| 15  | Reserved   | Must be kept at default  |     |        |   |       |   |       |   |   |       |   |   |       |   |   |        |
| 14  | T1_On      | Timer 1 "ON" time selections<br><table border="1"> <tr> <td>0</td> <td>10 ms</td> </tr> <tr> <td>1</td> <td>20 ms</td> </tr> </table>  | 0   | 10 ms  | 1 | 20 ms |   |       |   |   |       |   |   |       |   |   |        |
| 0   | 10 ms      |  |     |        |   |       |   |       |   |   |       |   |   |       |   |   |        |
| 1   | 20 ms      |  |     |        |   |       |   |       |   |   |       |   |   |       |   |   |        |
| 13  | T1_Per_MSB | Timer 1 period selection<br><br><table border="1"> <thead> <tr> <th>MSB</th> <th>LSB</th> <th></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1 s</td> </tr> <tr> <td>0</td> <td>1</td> <td>2 s</td> </tr> <tr> <td>1</td> <td>0</td> <td>3 s</td> </tr> <tr> <td>1</td> <td>1</td> <td>4 s</td> </tr> </tbody> </table><br>Timer 1 is restarted with a valid write command to control register 3          | MSB | LSB    |   | 0     | 0 | 1 s   | 0 | 1 | 2 s   | 1 | 0 | 3 s   | 1 | 1 | 4 s    |
| MSB | LSB        |  |     |        |   |       |   |       |   |   |       |   |   |       |   |   |        |
| 0   | 0          | 1 s  |     |        |   |       |   |       |   |   |       |   |   |       |   |   |        |
| 0   | 1          | 2 s  |     |        |   |       |   |       |   |   |       |   |   |       |   |   |        |
| 1   | 0          | 3 s  |     |        |   |       |   |       |   |   |       |   |   |       |   |   |        |
| 1   | 1          | 4 s  |     |        |   |       |   |       |   |   |       |   |   |       |   |   |        |
| 12  | T1_Per_LSB |  |     |        |   |       |   |       |   |   |       |   |   |       |   |   |        |
| 11  | Reserved   | Must be kept at default  |     |        |   |       |   |       |   |   |       |   |   |       |   |   |        |
| 10  | T2_On      | Timer 2 "ON" time selection<br><table border="1"> <tr> <td>0</td> <td>0.1 ms</td> </tr> <tr> <td>1</td> <td>1 ms</td> </tr> </table>   | 0   | 0.1 ms | 1 | 1 ms  |   |       |   |   |       |   |   |       |   |   |        |
| 0   | 0.1 ms     |  |     |        |   |       |   |       |   |   |       |   |   |       |   |   |        |
| 1   | 1 ms       |  |     |        |   |       |   |       |   |   |       |   |   |       |   |   |        |
| 9   | T2_Per_MSB | Timer 2 period selection<br><br><table border="1"> <thead> <tr> <th>MSB</th> <th>LSB</th> <th></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>10 ms</td> </tr> <tr> <td>0</td> <td>1</td> <td>20 ms</td> </tr> <tr> <td>1</td> <td>0</td> <td>50 ms</td> </tr> <tr> <td>1</td> <td>1</td> <td>200 ms</td> </tr> </tbody> </table><br>Timer 2 is restarted with a valid write command to control register 3 | MSB | LSB    |   | 0     | 0 | 10 ms | 0 | 1 | 20 ms | 1 | 0 | 50 ms | 1 | 1 | 200 ms |
| MSB | LSB        |  |     |        |   |       |   |       |   |   |       |   |   |       |   |   |        |
| 0   | 0          | 10 ms  |     |        |   |       |   |       |   |   |       |   |   |       |   |   |        |
| 0   | 1          | 20 ms  |     |        |   |       |   |       |   |   |       |   |   |       |   |   |        |
| 1   | 0          | 50 ms  |     |        |   |       |   |       |   |   |       |   |   |       |   |   |        |
| 1   | 1          | 200 ms   |     |        |   |       |   |       |   |   |       |   |   |       |   |   |        |
| 8   | T2_Per_LSB |  |     |        |   |       |   |       |   |   |       |   |   |       |   |   |        |
| 7   | Reserved   | Must be kept at default  |     |        |   |       |   |       |   |   |       |   |   |       |   |   |        |
| 6   | Reserved   | Must be kept at default  |     |        |   |       |   |       |   |   |       |   |   |       |   |   |        |

**Table 85. Control register 3, bits (continued)**

| Bit | Name              | Comment  |            |            |       |
|-----|-------------------|--|------------|------------|-------|
| 5   | WD_time_MSB       | Trigger window selection   |            |            |       |
| 4   | WD_time_LSB       |  |            |            |       |
|     |                   |  | <b>MSB</b> | <b>LSB</b> |       |
|     |                   |  | 0          | 0          | 10 ms |
|     |                   |  | 0          | 1          | 50 ms |
|     |                   | 1  | 0          | 100 ms     |       |
|     |                   | 1  | 1          | 200 ms     |       |
| 3   | LIN_WU_En         | Enable LIN as wake up source   |            |            |       |
|     |                   | 0  | Disabled   |            |       |
|     |                   | 1  | Enabled    |            |       |
| 2   | CAN_WU_En         | Enable CAN as wake up source   |            |            |       |
|     |                   | 0  | Disabled   |            |       |
|     |                   | 1  | Enabled    |            |       |
| 1   | Wake_timer_En     | Enable wake up by timer from V <sub>1_standby</sub> mode (Interrupt) or V <sub>Bat_standby</sub> Mode (NRESET) |            |            |       |
|     |                   | 0  | Disabled   |            |       |
|     |                   | 1  | Enabled    |            |       |
| 0   | Wake_timer_select | Timer selection for timer interrupt / wake-up of $\mu$ C by timer  |            |            |       |
|     |                   | 0  | Timer 2    |            |       |
|     |                   | 1  | Timer 1    |            |       |

**6.2.6 Control Register 4**

**Table 86. Control register 4: command and data bytes**

| Command byte |   |         |   |   |   |   |   | 1 <sup>st</sup> data byte | 2 <sup>nd</sup> data byte |
|--------------|---|---------|---|---|---|---|---|---------------------------|---------------------------|
| Read/write   |   | Address |   |   |   |   |   |                           |                           |
| x            | x | 0       | 0 | 0 | 1 | 0 | 0 | Data, 8bit                | Data, 8 bit               |

**Table 87. Control register 4, data bytes**

|          | 1 <sup>st</sup> data byte <15:8> |      |              |              |          |                      |                 |                 | 2 <sup>nd</sup> data byte <7:0> |          |                 |         |             |          |   |              |
|----------|----------------------------------|------|--------------|--------------|----------|----------------------|-----------------|-----------------|---------------------------------|----------|-----------------|---------|-------------|----------|---|--------------|
| Defaults | 0                                | 0    | 0            | 1            | 0        | 1                    | 0               | 0               | 1                               | 1        | 1               | 0       | 0           | 0        | 0 | 0            |
| Function | Reserved                         | ICMP | OUTHS_rec_en | VLOCK_OUT_EN | Reserved | LS_OV/UV_shutdown_en | V1Reset_level_2 | V1Reset_level_1 | LIN_PU_EN                       | Reserved | Lin_TxD_Tout_En | CAN_ACT | CAN_Loop_En | Reserved |   | CAN_Rec_only |
| Group    | Control (other)                  |      |              |              |          |                      |                 |                 | Transceiver settings            |          |                 |         |             |          |   |              |

**Table 88. Control register 4, bits**

| Bit | Name                 | Comment  |
|-----|----------------------|--|
| 15  | Reserved             | Must be kept at default  |
| 14  | ICMP                 | V <sub>1</sub> load current supervision  |
|     |                      | 0      Enabled; Watchdog is disabled in V <sub>1</sub> Standby when the V <sub>1loadcurrent</sub> < I <sub>cmphreshold</sub> |
|     |                      | 1      Disabled; Watchdog is automatically disabled when V <sub>1</sub> standby is entered                                   |
| 13  | OUTHS_rec_en         | Overcurrent Auto recovery mode for OUTHS   |
|     |                      | 0      Disabled  |
|     |                      | 1      Enabled   |
| 12  | VLOCK_OUT_EN         | Voltage lock out: OV/UV status   |
|     |                      | 0      Overvoltage/undervoltage status recovers automatically when condition disappears                                      |
|     |                      | 1      Overvoltage/undervoltage status is latched until a read and clear command is performed                                |
| 11  | Reserved             | Must be kept at default  |
| 10  | LS_OV/UV_shutdown_en | Shutdown of low-side drivers in case of overvoltage/undervoltage   |
|     |                      | 0      No shutdown of low-sides in case of overvoltage/undervoltage  |
|     |                      | 1      Shutdown low-sides in case of overvoltage/undervoltage  |

Table 88. Control register 4, bits (continued)

| Bit             | Name  | Comment   |   |                       |                 |   |   |   |       |   |   |        |   |   |       |   |   |       |
|-----------------|---|---|---|-----------------------|-----------------|---|---|---|-------|---|---|--------|---|---|-------|---|---|-------|
| 9               | V1Reset_level_1   | Select reset level  |   |                       |                 |   |   |   |       |   |   |        |   |   |       |   |   |       |
| 8               | V1Reset_level_2   |   |   |                       |                 |   |   |   |       |   |   |        |   |   |       |   |   |       |
|                 |   |   | <table border="1"> <thead> <tr> <th>V1Reset_level_2</th> <th>V1Reset_level_1</th> <th>V1 reset level</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>4.6 V</td> </tr> <tr> <td>0</td> <td>1</td> <td>4.35 V</td> </tr> <tr> <td>1</td> <td>0</td> <td>4.1 V</td> </tr> <tr> <td>1</td> <td>1</td> <td>3.8 V</td> </tr> </tbody> </table> | V1Reset_level_2       | V1Reset_level_1 | V1 reset level  | 0 | 0 | 4.6 V | 0 | 1 | 4.35 V | 1 | 0 | 4.1 V | 1 | 1 | 3.8 V |
| V1Reset_level_2 | V1Reset_level_1   |   | V1 reset level  |                       |                 |   |   |   |       |   |   |        |   |   |       |   |   |       |
| 0               | 0   |   | 4.6 V   |                       |                 |   |   |   |       |   |   |        |   |   |       |   |   |       |
| 0               | 1   |   | 4.35 V  |                       |                 |   |   |   |       |   |   |        |   |   |       |   |   |       |
| 1               | 0   | 4.1 V   |   |                       |                 |   |   |   |       |   |   |        |   |   |       |   |   |       |
| 1               | 1   | 3.8 V   |   |                       |                 |   |   |   |       |   |   |        |   |   |       |   |   |       |
|                 |   |   |   |                       |                 |   |   |   |       |   |   |        |   |   |       |   |   |       |
|                 |   |   |   |                       |                 |   |   |   |       |   |   |        |   |   |       |   |   |       |
|                 |   |   |   |                       |                 |   |   |   |       |   |   |        |   |   |       |   |   |       |
| 7               | LIN_PU_EN   | <p>Enable internal LIN pull up</p> <table border="1"> <tbody> <tr> <td>0</td> <td>No LIN master pull-up</td> </tr> <tr> <td>1</td> <td>LIN master pull-up</td> </tr> </tbody> </table>  | 0   | No LIN master pull-up | 1               | LIN master pull-up  |   |   |       |   |   |        |   |   |       |   |   |       |
| 0               | No LIN master pull-up   |   |   |                       |                 |   |   |   |       |   |   |        |   |   |       |   |   |       |
| 1               | LIN master pull-up  |   |   |                       |                 |   |   |   |       |   |   |        |   |   |       |   |   |       |
| 6               | Reserved  | Must be kept at default   |   |                       |                 |   |   |   |       |   |   |        |   |   |       |   |   |       |
| 5               | Lin_TxD_Tout_En   | <p>Enable / disable monitoring via TxD</p> <table border="1"> <tbody> <tr> <td>0</td> <td>No TxD monitoring</td> </tr> <tr> <td>1</td> <td>TxD monitoring; LIN transmitter is switched off if TXDL is dominant for <math>t &gt; 12</math> ms</td> </tr> </tbody> </table>   | 0   | No TxD monitoring     | 1               | TxD monitoring; LIN transmitter is switched off if TXDL is dominant for $t > 12$ ms |   |   |       |   |   |        |   |   |       |   |   |       |
| 0               | No TxD monitoring   |   |   |                       |                 |   |   |   |       |   |   |        |   |   |       |   |   |       |
| 1               | TxD monitoring; LIN transmitter is switched off if TXDL is dominant for $t > 12$ ms |   |   |                       |                 |   |   |   |       |   |   |        |   |   |       |   |   |       |
| 4               | CAN_ACT   | <p>Activate CAN transceiver</p> <p>Controls the CAN transceiver mode transition between 'CAN Trx Standby' Mode and 'Trx Normal' mode.</p> <p>The bit CAN_ACT is automatically reset to '0' when the device enters <math>V_{1\_standby}</math> Mode or <math>V_{Bat\_standby}</math> Mode.</p> <table border="1"> <tbody> <tr> <td>0</td> <td>CAN Trx Standby Mode</td> </tr> <tr> <td>1</td> <td>Trx Normal Mode</td> </tr> </tbody> </table> <p>See <a href="#">Section 2.9.1</a> for details.</p> | 0   | CAN Trx Standby Mode  | 1               | Trx Normal Mode   |   |   |       |   |   |        |   |   |       |   |   |       |
| 0               | CAN Trx Standby Mode  |   |   |                       |                 |   |   |   |       |   |   |        |   |   |       |   |   |       |
| 1               | Trx Normal Mode   |   |   |                       |                 |   |   |   |       |   |   |        |   |   |       |   |   |       |
| 3               | CAN_Loop_En   | <p>Enable looping of CANTX to CANRXD</p> <table border="1"> <tbody> <tr> <td>0</td> <td>No looping</td> </tr> <tr> <td>1</td> <td>TXDC is looped to RXDC</td> </tr> </tbody> </table>   | 0   | No looping            | 1               | TXDC is looped to RXDC  |   |   |       |   |   |        |   |   |       |   |   |       |
| 0               | No looping  |   |   |                       |                 |   |   |   |       |   |   |        |   |   |       |   |   |       |
| 1               | TXDC is looped to RXDC  |   |   |                       |                 |   |   |   |       |   |   |        |   |   |       |   |   |       |
| 2               | Reserved  | Must be kept at default   |   |                       |                 |   |   |   |       |   |   |        |   |   |       |   |   |       |
| 1               | Reserved  | Must be kept at default   |   |                       |                 |   |   |   |       |   |   |        |   |   |       |   |   |       |

**Table 88. Control register 4, bits (continued)**

| Bit | Name         | Comment                      |                          |             |
|-----|--------------|------------------------------|--------------------------|-------------|
| 0   | CAN_Rec_only | Enable CAN receive only mode |                          |             |
|     |              | 0                            | CAN in transceiver mode  | Active mode |
|     |              | 1                            | CAN in receive only mode |             |

**6.2.7 Control Register 5**

**Table 89. Control register 5: command and data bytes**

| Command byte |   |         |   |   |   |   |   | 1 <sup>st</sup> data byte | 2 <sup>nd</sup> data byte |
|--------------|---|---------|---|---|---|---|---|---------------------------|---------------------------|
| Read/write   |   | Address |   |   |   |   |   |                           |                           |
| x            | x | 0       | 0 | 0 | 1 | 0 | 1 | Data, 8bit                | Data, 8 bit               |

**Table 90. Control register 5, data bytes**

|          | 1 <sup>st</sup> data byte <15:8> |               |               |               |               |               |               |               | 2 <sup>nd</sup> data byte <7:0> |              |              |              |              |              |              |              |
|----------|----------------------------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------------------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Defaults | 0                                | 1             | 1             | 1             | 1             | 1             | 1             | 1             | 0                               | 0            | 0            | 0            | 0            | 0            | 0            | 0            |
| Function | Reserved                         | PWM2_OFF_DC_6 | PWM2_OFF_DC_5 | PWM2_OFF_DC_4 | PWM2_OFF_DC_3 | PWM2_OFF_DC_2 | PWM2_OFF_DC_1 | PWM2_OFF_DC_0 | PWM_Freq                        | PWM1_ON_DC_6 | PWM1_ON_DC_5 | PWM1_ON_DC_4 | PWM1_ON_DC_3 | PWM1_ON_DC_2 | PWM1_ON_DC_1 | PWM1_ON_DC_0 |
| Group    | PWM2 setting                     |               |               |               |               |               |               |               | PWM1 setting                    |              |              |              |              |              |              |              |

Table 91. Control register 5, bits

| Bit | Name          | Comment                 |                      |                      |                      |                      |                      |                      |                        |
|-----|---------------|-------------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|------------------------|
| 15  | Reserved      | Must be kept at default |                      |                      |                      |                      |                      |                      |                        |
| 14  | PWM2_OFF_DC_6 | PWM2 duty cycle         |                      |                      |                      |                      |                      |                      |                        |
| 13  | PWM2_OFF_DC_5 | <b>PWM2 OFF_DC_6</b>    | <b>PWM2 OFF_DC_5</b> | <b>PWM2 OFF_DC_4</b> | <b>PWM2 OFF_DC_3</b> | <b>PWM2 OFF_DC_2</b> | <b>PWM2 OFF_DC_1</b> | <b>PWM2 OFF_DC_0</b> | <b>PWM2 duty cycle</b> |
| 12  | PWM2_OFF_DC_4 | 1                       | 1                    | 1                    | 1                    | 1                    | 1                    | 1                    | 0%, HS OFF             |
| 11  | PWM2_OFF_DC_3 | 1                       | 1                    | 1                    | 1                    | 1                    | 1                    | 0                    | 200/128 %              |
| 10  | PWM2_OFF_DC_2 | 1                       | 1                    | 1                    | 1                    | 1                    | 1                    | 1                    | 300/128 %              |
| 9   | PWM2_OFF_DC_1 | ...                     |                      |                      |                      |                      |                      |                      |                        |
| 8   | PWM2_OFF_DC_0 | 0                       | 0                    | 0                    | 0                    | 0                    | 1                    | 0                    | 12600/128 %            |
|     |               | 0                       | 0                    | 0                    | 0                    | 0                    | 0                    | 1                    | 12700/128 %            |
|     |               | 0                       | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 100% HS ON             |
| 7   | PWM_FREQ      | Select PWM frequency    |                      |                      |                      |                      |                      |                      |                        |
|     |               | 0                       | 128 Hz               |                      |                      |                      |                      |                      |                        |
|     |               | 1                       | 256 Hz               |                      |                      |                      |                      |                      |                        |
| 6   | PWM1_ON_DC_6  | PWM1 duty cycle         |                      |                      |                      |                      |                      |                      |                        |
| 5   | PWM1_ON_DC_5  | <b>PWM1 ON_DC_6</b>     | <b>PWM1 ON_DC_5</b>  | <b>PWM1 ON_DC_4</b>  | <b>PWM1 ON_DC_3</b>  | <b>PWM1 ON_DC_2</b>  | <b>PWM1 ON_DC_1</b>  | <b>PWM1 ON_DC_0</b>  | <b>PWM1 duty cycle</b> |
| 4   | PWM1_ON_DC_4  | 1                       | 1                    | 1                    | 1                    | 1                    | 1                    | 1                    | 100%, HS ON            |
| 3   | PWM1_ON_DC_3  | 1                       | 1                    | 1                    | 1                    | 1                    | 1                    | 0                    | 12600/128 %            |
| 2   | PWM1_ON_DC_2  | 1                       | 1                    | 1                    | 1                    | 1                    | 1                    | 1                    | 12500/128 %            |
| 1   | PWM1_ON_DC_1  | ...                     |                      |                      |                      |                      |                      |                      |                        |
| 0   | PWM1_ON_DC_0  | 0                       | 0                    | 0                    | 0                    | 0                    | 1                    | 0                    | 200/128 %              |
|     |               | 0                       | 0                    | 0                    | 0                    | 0                    | 0                    | 1                    | 100/128 %              |
|     |               | 0                       | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0% HS OFF              |

6.2.8 Control Register 6

Table 92. Control register 6: command and data bytes

| Command byte |   |         |   |   |   |   |   | 1 <sup>st</sup> data byte | 2 <sup>nd</sup> data byte |
|--------------|---|---------|---|---|---|---|---|---------------------------|---------------------------|
| Read/write   |   | Address |   |   |   |   |   |                           |                           |
| x            | x | 0       | 0 | 0 | 1 | 1 | 0 | Data, 8bit                | Data, 8 bit               |

Table 93. Control register 6, data bytes

|          | 1 <sup>st</sup> data byte <15:8> |               |               |               |               |               |               |               | 2 <sup>nd</sup> data byte <7:0> |              |              |              |              |              |              |              |
|----------|----------------------------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------------------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Defaults | 0                                | 1             | 1             | 1             | 1             | 1             | 1             | 1             | 0                               | 0            | 0            | 0            | 0            | 0            | 0            | 0            |
| Function | Reserved                         | PWM4_OFF_DC_6 | PWM4_OFF_DC_5 | PWM4_OFF_DC_4 | PWM4_OFF_DC_3 | PWM4_OFF_DC_2 | PWM4_OFF_DC_1 | PWM4_OFF_DC_0 | Reserved                        | PWM3_ON_DC_6 | PWM3_ON_DC_5 | PWM3_ON_DC_4 | PWM3_ON_DC_3 | PWM3_ON_DC_2 | PWM3_ON_DC_1 | PWM3_ON_DC_0 |
| Group    | PWM4 setting                     |               |               |               |               |               |               |               | PWM3 setting                    |              |              |              |              |              |              |              |

Table 94. Control register 6, bits

| Bit | Name          | Comment                 |                      |                      |                      |                      |                      |                      |                        |  |
|-----|---------------|-------------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|------------------------|--|
| 15  | Reserved      | Must be kept at default |                      |                      |                      |                      |                      |                      |                        |  |
| 14  | PWM4_OFF_DC_6 | PWM4 duty cycle         |                      |                      |                      |                      |                      |                      |                        |  |
| 13  | PWM4_OFF_DC_5 | <b>PWM4 OFF_DC_6</b>    | <b>PWM4 OFF_DC_5</b> | <b>PWM4 OFF_DC_4</b> | <b>PWM4 OFF_DC_3</b> | <b>PWM4 OFF_DC_2</b> | <b>PWM4 OFF_DC_1</b> | <b>PWM4 OFF_DC_0</b> | <b>PWM4 duty cycle</b> |  |
| 12  | PWM4_OFF_DC_4 | 1                       | 1                    | 1                    | 1                    | 1                    | 1                    | 1                    | 0%, HS OFF             |  |
| 11  | PWM4_OFF_DC_3 | 1                       | 1                    | 1                    | 1                    | 1                    | 1                    | 0                    | 200/128 %              |  |
| 10  | PWM4_OFF_DC_2 | 1                       | 1                    | 1                    | 1                    | 1                    | 1                    | 1                    | 300/128 %              |  |
| 9   | PWM4_OFF_DC_1 | ...                     |                      |                      |                      |                      |                      |                      |                        |  |
| 8   | PWM4_OFF_DC_0 | 0                       | 0                    | 0                    | 0                    | 0                    | 1                    | 0                    | 12600/128 %            |  |
|     |               | 0                       | 0                    | 0                    | 0                    | 0                    | 0                    | 1                    | 12700/128 %            |  |
|     |               | 0                       | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 100% HS ON             |  |
| 7   | Reserved      | Must be kept at default |                      |                      |                      |                      |                      |                      |                        |  |

Table 94. Control register 6, bits (continued)

| Bit | Name         | Comment         |              |              |              |              |              |              |                 |
|-----|--------------|-----------------|--------------|--------------|--------------|--------------|--------------|--------------|-----------------|
| 6   | PWM3_ON_DC_6 | PWM3 duty cycle |              |              |              |              |              |              |                 |
| 5   | PWM3_ON_DC_5 | PWM3 ON_DC_6    | PWM3 ON_DC_5 | PWM3 ON_DC_4 | PWM3 ON_DC_3 | PWM3 ON_DC_2 | PWM3 ON_DC_1 | PWM3 ON_DC_0 | PWM3 duty cycle |
| 4   | PWM3_ON_DC_4 | 1               | 1            | 1            | 1            | 1            | 1            | 1            | 100%, HS ON     |
| 3   | PWM3_ON_DC_3 | 1               | 1            | 1            | 1            | 1            | 1            | 0            | 12600/128 %     |
| 2   | PWM3_ON_DC_2 | 1               | 1            | 1            | 1            | 1            | 1            | 1            | 12500/128 %     |
| 1   | PWM3_ON_DC_1 | ...             |              |              |              |              |              |              |                 |
| 0   | PWM3_ON_DC_0 | 0               | 0            | 0            | 0            | 0            | 1            | 0            | 200/128 %       |
|     |              | 0               | 0            | 0            | 0            | 0            | 0            | 1            | 100/128 %       |
|     |              | 0               | 0            | 0            | 0            | 0            | 0            | 0            | 0% HS OFF       |



### 6.2.9 Control Register 7

**Table 95. Control register 7: command and data bytes**

| Command byte |   |         |   |   |   |   |   | 1 <sup>st</sup> data byte | 2 <sup>nd</sup> data byte |
|--------------|---|---------|---|---|---|---|---|---------------------------|---------------------------|
| Read/write   |   | Address |   |   |   |   |   |                           |                           |
| x            | x | 0       | 0 | 0 | 1 | 1 | 1 | Data, 8bit                | Data, 8 bit               |

**Table 96. Control register 7, data bytes**

|          | 1 <sup>st</sup> data byte <15:8> |           |           |           |           |           |          |          | 2 <sup>nd</sup> data byte <7:0> |          |          |          |          |          |          |          |
|----------|----------------------------------|-----------|-----------|-----------|-----------|-----------|----------|----------|---------------------------------|----------|----------|----------|----------|----------|----------|----------|
| Defaults | 0                                | 0         | 0         | 0         | 0         | 0         | 0        | 0        | 0                               | 0        | 0        | 0        | 0        | 0        | 0        | 0        |
| Function | EXT_ID_15                        | EXT_ID_14 | EXT_ID_13 | EXT_ID_12 | EXT_ID_11 | EXT_ID_10 | EXT_ID_9 | EXT_ID_8 | EXT_ID_7                        | EXT_ID_6 | EXT_ID_5 | EXT_ID_4 | EXT_ID_3 | EXT_ID_2 | EXT_ID_1 | EXT_ID_0 |
| Group    | Selective Wakeup Settings        |           |           |           |           |           |          |          |                                 |          |          |          |          |          |          |          |

**Table 97. Control register 7, bits**

| Bit | Name      | Comment   |
|-----|-----------|---|
| 15  | EXT_ID_15 | Extended CAN Identifier<br>Definition of which Extended CAN Identifier will wake up<br>To run matching on Extended CAN Identifier also CAN IDE (Control Register 9 must be set) |
| 14  | EXT_ID_14 |   |
| 13  | EXT_ID_13 |   |
| 12  | EXT_ID_12 |   |
| 11  | EXT_ID_11 |   |
| 10  | EXT_ID_10 |   |
| 9   | EXT_ID_9  |   |
| 8   | EXT_ID_8  |   |
| 7   | EXT_ID_7  |   |
| 6   | EXT_ID_6  |   |
| 5   | EXT_ID_5  |   |
| 4   | EXT_ID_4  |   |
| 3   | EXT_ID_3  |   |
| 2   | EXT_ID_2  |   |
| 1   | EXT_ID_1  |   |
| 0   | EXT_ID_0  |   |

6.2.10 Control Register 8

Table 98. Control register 8: command and data bytes

| Command byte |   |         |   |   |   |   |   | 1 <sup>st</sup> data byte | 2 <sup>nd</sup> data byte |
|--------------|---|---------|---|---|---|---|---|---------------------------|---------------------------|
| Read/write   |   | Address |   |   |   |   |   |                           |                           |
| x            | x | 0       | 0 | 1 | 0 | 0 | 0 | Data, 8 bit               | Data, 8 bit               |

Table 99. Control register 8, data bytes

|          | 1 <sup>st</sup> data byte <15:8> |   |   |       |      |      |      |      | 2 <sup>nd</sup> data byte <7:0> |      |      |      |      |      |           |           |
|----------|----------------------------------|---|---|-------|------|------|------|------|---------------------------------|------|------|------|------|------|-----------|-----------|
| Defaults | 0                                | 0 | 0 | 0     | 0    | 0    | 0    | 0    | 0                               | 0    | 0    | 0    | 0    | 0    | 0         | 0         |
| Function | Reserved                         |   |   | ID_10 | ID_9 | ID_8 | ID_7 | ID_6 | ID_5                            | ID_4 | ID_3 | ID_2 | ID_1 | ID_0 | EXT_ID_17 | EXT_ID_16 |
| Group    | Selective Wakeup Settings        |   |   |       |      |      |      |      |                                 |      |      |      |      |      |           |           |

Table 100. Control register 8, bits

| Bit | Name      | Comment  |
|-----|-----------|--|
| 15  | Reserved  | Must be kept at default  |
| 14  | Reserved  |  |
| 13  | Reserved  |  |
| 12  | ID_10     | Standard CAN Identifier<br>Definition of which Standard CAN Identifier will wake up  |
| 11  | ID_9      |  |
| 10  | ID_8      |  |
| 9   | ID_7      |  |
| 8   | ID_6      |  |
| 7   | ID_5      |  |
| 6   | ID_4      |  |
| 5   | ID_3      |  |
| 4   | ID_2      |  |
| 3   | ID_1      |  |
| 2   | ID_0      |  |
| 1   | EXT_ID_17 | Extended CAN Identifier  |
| 0   | EXT_ID_16 | Definition of which Extended CAN Identifier will wake up<br>To run matching on Extended CAN Identifier also CAN IDE (Control Register 9 must be set) |

6.2.11 Control Register 9

Table 101. Control register 9: command and data bytes

| Command byte |   |         |   |   |   |   |   | 1 <sup>st</sup> data byte | 2 <sup>nd</sup> data byte |
|--------------|---|---------|---|---|---|---|---|---------------------------|---------------------------|
| Read/write   |   | Address |   |   |   |   |   |                           |                           |
| x            | x | 0       | 0 | 1 | 0 | 0 | 1 | Data, 8 bit               | Data, 8 bit               |

Table 102. Control register 9, data bytes

|          | 1 <sup>st</sup> data byte <15:8> |   |   |   |   |   |   |   | 2 <sup>nd</sup> data byte <7:0> |   |         |       |       |       |       |
|----------|----------------------------------|---|---|---|---|---|---|---|---------------------------------|---|---------|-------|-------|-------|-------|
| Defaults | 0                                | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               | 0 | 0       | 0     | 0     | 0     | 0     |
| Function | Reserved                         |   |   |   |   |   |   |   |                                 |   | CAN_IDE | DLC_3 | DLC_2 | DLC_1 | DLC_0 |
| Group    | Selective Wakeup Settings        |   |   |   |   |   |   |   |                                 |   |         |       |       |       |       |

Table 103. Control register 9, bits

| Bit | Name     | Comment  |
|-----|----------|--|
| 15  | Reserved | Must be kept at default  |
| 14  | Reserved |  |
| 13  | Reserved |  |
| 12  | Reserved |  |
| 11  | Reserved |  |
| 10  | Reserved |  |
| 9   | Reserved |  |
| 8   | Reserved |  |
| 7   | Reserved |  |
| 6   | Reserved |  |
| 5   | Reserved |  |
| 4   | CAN_IDE  | CAN IDE bit  |
|     |          | 1   CAN Identifier Matching based on CAN Extended Message Format   |
|     |          | 0   CAN Identifier matching based on CAN Standard Message Format   |
| 3   | DLC_3    | Data Length Code<br>Defines the amount of Data Bytes used for the data matching.<br>Possible values up to 8 Byte according to CAN message format |
| 2   | DLC_2    |  |
| 1   | DLC_1    |  |
| 0   | DLC_0    |  |

### 6.2.12 Control Register 10

**Table 104. Control register 10: command and data bytes**

| Command byte |   |         |   |   |   |   |   | 1 <sup>st</sup> data byte | 2 <sup>nd</sup> data byte |
|--------------|---|---------|---|---|---|---|---|---------------------------|---------------------------|
| Read/write   |   | Address |   |   |   |   |   |                           |                           |
| x            | x | 0       | 0 | 1 | 0 | 1 | 0 | Data, 8 bit               | Data, 8 bit               |

**Table 105. Control register 10, data bytes**

|          | 1 <sup>st</sup> data byte <15:8> |   |   |   |   |   |   |   | 2 <sup>nd</sup> data byte <7:0> |   |   |   |   |   |   |   |
|----------|----------------------------------|---|---|---|---|---|---|---|---------------------------------|---|---|---|---|---|---|---|
| Defaults | 0                                | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Function | Data Byte2                       |   |   |   |   |   |   |   | Data Byte1                      |   |   |   |   |   |   |   |
| Group    | Selective Wakeup Settings        |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |

**Table 106. Control register 10, bits**

| Bit    | Name       | Comment                      |
|--------|------------|------------------------------|
| 15 - 8 | Data Byte2 | Data field for data matching |
| 7 - 0  | Data Byte1 | Data field for data matching |

### 6.2.13 Control Register 11

**Table 107. Control register 11: command and data bytes**

| Command byte |   |         |   |   |   |   |   | 1 <sup>st</sup> data byte | 2 <sup>nd</sup> data byte |
|--------------|---|---------|---|---|---|---|---|---------------------------|---------------------------|
| Read/write   |   | Address |   |   |   |   |   |                           |                           |
| x            | x | 0       | 0 | 1 | 0 | 1 | 1 | Data, 8 bit               | Data, 8 bit               |

**Table 108. Control register 11, data bytes**

|          | 1 <sup>st</sup> data byte <15:8> |   |   |   |   |   |   |   | 2 <sup>nd</sup> data byte <7:0> |   |   |   |   |   |   |   |
|----------|----------------------------------|---|---|---|---|---|---|---|---------------------------------|---|---|---|---|---|---|---|
| Defaults | 0                                | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Function | Data Byte4                       |   |   |   |   |   |   |   | Data Byte3                      |   |   |   |   |   |   |   |
| Group    | Selective Wakeup Settings        |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |

**Table 109. Control register 11, bits**

| Bit    | Name       | Comment                      |
|--------|------------|------------------------------|
| 15 - 8 | Data Byte4 | Data field for data matching |
| 7 - 0  | Data Byte3 | Data field for data matching |

## 6.2.14 Control Register 12

**Table 110. Control register 12: command and data bytes**

| Command byte |   |         |   |   |   |   |   | 1 <sup>st</sup> data byte | 2 <sup>nd</sup> data byte |
|--------------|---|---------|---|---|---|---|---|---------------------------|---------------------------|
| Read/write   |   | Address |   |   |   |   |   |                           |                           |
| x            | x | 0       | 0 | 1 | 1 | 0 | 0 | Data, 8 bit               | Data, 8 bit               |

**Table 111. Control register 12, data bytes**

|          | 1 <sup>st</sup> data byte <15:8> |   |   |   |   |   |   |   | 2 <sup>nd</sup> data byte <7:0> |   |   |   |   |   |   |   |
|----------|----------------------------------|---|---|---|---|---|---|---|---------------------------------|---|---|---|---|---|---|---|
| Defaults | 0                                | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Function | Data Byte6                       |   |   |   |   |   |   |   | Data Byte5                      |   |   |   |   |   |   |   |
| Group    | Selective Wakeup Settings        |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |

**Table 112. Control register 12, bits**

| Bit    | Name       | Comment                      |
|--------|------------|------------------------------|
| 15 - 8 | Data Byte6 | Data field for data matching |
| 7 - 0  | Data Byte5 | Data field for data matching |

## 6.2.15 Control Register 13

**Table 113. Control register 13: command and data bytes**

| Command byte |   |         |   |   |   |   |   | 1 <sup>st</sup> data byte | 2 <sup>nd</sup> data byte |
|--------------|---|---------|---|---|---|---|---|---------------------------|---------------------------|
| Read/write   |   | Address |   |   |   |   |   |                           |                           |
| x            | x | 0       | 0 | 1 | 1 | 0 | 1 | Data, 8 bit               | Data, 8 bit               |

**Table 114. Control register 13, data bytes**

|          | 1 <sup>st</sup> data byte <15:8> |   |   |   |   |   |   |   | 2 <sup>nd</sup> data byte <7:0> |   |   |   |   |   |   |   |
|----------|----------------------------------|---|---|---|---|---|---|---|---------------------------------|---|---|---|---|---|---|---|
| Defaults | 0                                | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Function | Data Byte8                       |   |   |   |   |   |   |   | Data Byte7                      |   |   |   |   |   |   |   |
| Group    | Selective Wakeup Settings        |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |

**Table 115. Control register 13, bits**

| Bit    | Name       | Comment                      |
|--------|------------|------------------------------|
| 15 - 8 | Data Byte8 | Data field for data matching |
| 7 - 0  | Data Byte7 | Data field for data matching |

6.2.16 Control Register 14

Table 116. Control register 14: command and data bytes

| Command byte |   |         |   |   |   |   |   | 1 <sup>st</sup> data byte | 2 <sup>nd</sup> data byte |
|--------------|---|---------|---|---|---|---|---|---------------------------|---------------------------|
| Read/write   |   | Address |   |   |   |   |   |                           |                           |
| x            | x | 0       | 0 | 1 | 1 | 1 | 0 | Data, 8 bit               | Data, 8 bit               |

Table 117. Control register 14, data bytes

|          | 1 <sup>st</sup> data byte <15:8> |               |               |               |               |               |              |              | 2 <sup>nd</sup> data byte <7:0> |              |              |              |              |              |              |              |
|----------|----------------------------------|---------------|---------------|---------------|---------------|---------------|--------------|--------------|---------------------------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Defaults | 0                                | 0             | 0             | 0             | 0             | 0             | 0            | 0            | 0                               | 0            | 0            | 0            | 0            | 0            | 0            | 0            |
| Function | EXT_ID_MSK_15                    | EXT_ID_MSK_14 | EXT_ID_MSK_13 | EXT_ID_MSK_12 | EXT_ID_MSK_11 | EXT_ID_MSK_10 | EXT_ID_MSK_9 | EXT_ID_MSK_8 | EXT_ID_MSK_7                    | EXT_ID_MSK_6 | EXT_ID_MSK_5 | EXT_ID_MSK_4 | EXT_ID_MSK_3 | EXT_ID_MSK_2 | EXT_ID_MSK_1 | EXT_ID_MSK_0 |
| Group    | Selective Wakeup Settings        |               |               |               |               |               |              |              |                                 |              |              |              |              |              |              |              |

Table 118. Control register 14, bits

| Bit | Name          | Comment  |   |
|-----|---------------|--|---|
| 15  | EXT_ID_MSK_15 | Masking Bits for Extended CAN Identifier   |   |
| 14  | EXT_ID_MSK_14 | 1  | Extended CAN Identifier Bit is ignored for matching |
| 13  | EXT_ID_MSK_13 | 0  | Extended CAN Identifier Bit is matched              |
| 12  | EXT_ID_MSK_12 | To run matching on Extended CAN Identifier also CAN_IDE (Control Register 9 must be set) |   |
| 11  | EXT_ID_MSK_11 |  |   |
| 10  | EXT_ID_MSK_10 |  |   |
| 9   | EXT_ID_MSK_9  |  |   |
| 8   | EXT_ID_MSK_8  |  |   |
| 7   | EXT_ID_MSK_7  |  |   |
| 6   | EXT_ID_MSK_6  |  |   |
| 5   | EXT_ID_MSK_5  |  |   |
| 4   | EXT_ID_MSK_4  |  |   |
| 3   | EXT_ID_MSK_3  |  |   |
| 2   | EXT_ID_MSK_2  |  |   |
| 1   | EXT_ID_MSK_1  |  |   |
| 0   | EXT_ID_MSK_0  |  |   |

6.2.17 Control Register 15

Table 119. Control register 15: command and data bytes

| Command byte |   |         |   |   |   |   |   | 1 <sup>st</sup> data byte | 2 <sup>nd</sup> data byte |
|--------------|---|---------|---|---|---|---|---|---------------------------|---------------------------|
| Read/write   |   | Address |   |   |   |   |   |                           |                           |
| x            | x | 0       | 0 | 1 | 1 | 1 | 1 | Data, 8bit                | Data, 8 bit               |

Table 120. Control register 15, data bytes

|          | 1 <sup>st</sup> data byte <15:8> |   |   |           |          |          |          |          | 2 <sup>nd</sup> data byte <7:0> |          |          |          |          |          |               |               |
|----------|----------------------------------|---|---|-----------|----------|----------|----------|----------|---------------------------------|----------|----------|----------|----------|----------|---------------|---------------|
| Defaults | 0                                | 0 | 0 | 0         | 0        | 0        | 0        | 0        | 0                               | 0        | 0        | 0        | 0        | 0        | 0             | 0             |
| Function | Reserved                         |   |   | ID_MSK_10 | ID_MSK_9 | ID_MSK_8 | ID_MSK_7 | ID_MSK_6 | ID_MSK_5                        | ID_MSK_4 | ID_MSK_3 | ID_MSK_2 | ID_MSK_1 | ID_MSK_0 | EXT_ID_MSK_17 | EXT_ID_MSK_16 |
| Group    | Selective Wakeup Settings        |   |   |           |          |          |          |          |                                 |          |          |          |          |          |               |               |

Table 121. Control register 15, bits

| Bit  | Name          | Comment                                  |   |
|--|---------------|--|---|
| 15   | Reserved      | Must be kept at default                  |   |
| 14   | Reserved      |  |   |
| 13   | Reserved      |  |   |
| 12   | ID_MSK_10     | Masking Bits for Standard CAN Identifier |   |
| 11   | ID_MSK_9      | 1  | Standard CAN Identifier Bit is ignored for matching |
| 10   | ID_MSK_8      | 0  | Standard CAN Identifier Bit is matched              |
| 9  | ID_MSK_7      |  |   |
| 8  | ID_MSK_6      |  |   |
| 7  | ID_MSK_5      |  |   |
| 6  | ID_MSK_4      |  |   |
| 5  | ID_MSK_3      |  |   |
| 4  | ID_MSK_2      |  |   |
| 3  | ID_MSK_1      |  |   |
| 2  | ID_MSK_0      |  |   |
| 1  | EXT_ID_MSK_17 | Masking Bits for Extended CAN Identifier |   |
| 0  | EXT_ID_MSK_16 | 1  | Extended CAN Identifier Bit is ignored for matching |
|  |               | 0  | Extended CAN Identifier Bit is matched              |
| To run matching on Extended CAN Identifier also CAN_IDE (Control Register 9 must be set) |               |  |   |

6.2.18 Control Register 16

Table 122. Control register 16: command and data bytes

| Command byte |   |         |   |   |   |   |   | 1 <sup>st</sup> data byte | 2 <sup>nd</sup> data byte |
|--------------|---|---------|---|---|---|---|---|---------------------------|---------------------------|
| Read/write   |   | Address |   |   |   |   |   |                           |                           |
| x            | x | 0       | 1 | 0 | 0 | 0 | 0 | Data, 8 bit               | Data, 8 bit               |

Table 123. Control register 16, data bytes

|          | 1 <sup>st</sup> data byte <15:8> |         |         |         |         |         |         |         | 2 <sup>nd</sup> data byte <7:0> |          |          |          |          |      |      |       |
|----------|----------------------------------|---------|---------|---------|---------|---------|---------|---------|---------------------------------|----------|----------|----------|----------|------|------|-------|
| Defaults | 0                                | 0       | 0       | 0       | 0       | 0       | 0       | 0       | 0                               | 0        | 0        | 0        | 0        | 0    | 0    | 0     |
| Function | CR16_30                          | CR16_21 | CR16_20 | CR16_14 | CR16_13 | CR16_12 | CR16_11 | CR16_10 | Reserved                        | Sample_2 | Sample_1 | Sample_0 | Reserved | BR_1 | BR_0 | SW_EN |
| Group    | Selective Wakeup Settings        |         |         |         |         |         |         |         |                                 |          |          |          |          |      |      |       |

Table 124. Control register 16, bits

| Bit | Name                   | Comment                 |                 |                 |   |  |
|-----|------------------------|-------------------------|-----------------|-----------------|---|--|
| 15  | CR16_30 <sup>(1)</sup> | Must be kept at default |                 |                 |   |  |
| 14  | CR16_21                |                         |                 |                 |   |  |
| 13  | CR16_20                |                         |                 |                 |   |  |
| 12  | CR16_14                |                         |                 |                 |   |  |
| 11  | CR16_13                |                         |                 |                 |   |  |
| 10  | CR16_12                |                         |                 |                 |   |  |
| 9   | CR16_11                |                         |                 |                 |   |  |
| 8   | CR16_10                |                         |                 |                 |   |  |
| 7   | Reserved               | Must be kept at default |                 |                 |   |  |
| 6   | Sample_2               | Sample point            |                 |                 |   |  |
| 5   | Sample_1               | <b>Sample_2</b>         | <b>Sample_1</b> | <b>Sample_0</b> | <b>Sample point</b>                           |  |
| 4   | Sample_0               | 0                       | 0               | 0               | 71.5 %  |  |
|     |                        | 0                       | 0               | 1               | 73.5 %  |  |
|     |                        | 0                       | 1               | 0               | 75.5 %  |  |
|     |                        | 0                       | 1               | 1               | 77.5 %  |  |
|     |                        | 1                       | 0               | 0               | 79.5 %  |  |
|     |                        | 1                       | 0               | 1               | 81.5 % (Optimum sample point <sup>(2)</sup> ) |  |
|     |                        | 1                       | 1               | 0               | 83.5 %  |  |
|     |                        | 1                       | 1               | 1               | 85.5 %  |  |



Table 124. Control register 16, bits (continued)

| Bit | Name                 | Comment                           |                          |   |
|-----|----------------------|-----------------------------------|--------------------------|---|
| 3   | Reserved             | Must be kept at default           |                          |   |
| 2   | BR_1                 | CAN baud rate                     |                          |   |
| 1   | BR_0                 | <b>BR_1</b>                       | <b>BR_0</b>              | <b>Baud rate</b>  |
|     |                      | 0                                 | 0                        | 500 kbit/s  |
|     |                      | 0                                 | 1                        | 250 kbit/s  |
|     |                      | 1                                 | 0                        | Oscillator stopped (see <a href="#">Oscillator monitoring</a> ) |
|     |                      | 1                                 | 1                        | 125 kbit/s  |
| 0   | SW_EN <sup>(3)</sup> | Selective Wakeup Enable           |                          |   |
|     |                      | 0                                 | No selective wakeup      |   |
|     |                      | 1                                 | Selective wakeup enabled |   |
|     |                      | See <a href="#">Section 2.9.2</a> |                          |   |

1. Changing the default configuration of CR16 (bits 1 to 15) is only possible when selective wake is disabled (SW\_EN = 0). Setting SW\_EN = 0 is always possible. Setting SW\_EN = 1 must follow the procedure as described in [Section 2.9.2](#).
2. The sampling point bits [6:4] have to be programmed to "101" (81.5%) before enabling the selective wakeup feature.
3. SW\_EN enables CAN WUF independently from the status of CAN\_WAKE\_EN.

6.2.19 Control Register 34

Table 125. Control register 34: command and data bytes

| Command byte |   |         |   |   |   |   |   | 1 <sup>st</sup> data byte | 2 <sup>nd</sup> data byte |
|--------------|---|---------|---|---|---|---|---|---------------------------|---------------------------|
| Read/write   |   | Address |   |   |   |   |   |                           |                           |
| x            | x | 1       | 0 | 0 | 0 | 1 | 0 | Data, 8 bit               | Data, 8 bit               |

Table 126. Control register 34, data bytes

|          | 1 <sup>st</sup> data byte <15:8> |   |   |   |   |   |   |   | 2 <sup>nd</sup> data byte <7:0> |   |   |   |   |   |       |   |
|----------|----------------------------------|---|---|---|---|---|---|---|---------------------------------|---|---|---|---|---|-------|---|
| Defaults | 0                                | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0 | 0 | 0     | 1 |
| Function | Reserved                         |   |   |   |   |   |   |   |                                 |   |   |   |   |   | WD_EN |   |
| Group    | Selective Wakeup Settings        |   |   |   |   |   |   |   |                                 |   |   |   |   |   |       |   |

Table 127. Control register 34, bits

| Bit | Name              | Comment   |   |                   |   |                  |
|-----|-------------------|---|---|-------------------|---|------------------|
| 15  | Reserved          | Must be kept at default   |   |                   |   |                  |
| 14  | Reserved          |   |   |                   |   |                  |
| 13  | Reserved          |   |   |                   |   |                  |
| 12  | Reserved          |   |   |                   |   |                  |
| 11  | Reserved          |   |   |                   |   |                  |
| 10  | Reserved          |   |   |                   |   |                  |
| 9   | Reserved          |   |   |                   |   |                  |
| 8   | Reserved          |   |   |                   |   |                  |
| 7   | Reserved          |   |   |                   |   |                  |
| 6   | Reserved          |   |   |                   |   |                  |
| 5   | Reserved          |   |   |                   |   |                  |
| 4   | Reserved          |   |   |                   |   |                  |
| 3   | Reserved          |   |   |                   |   |                  |
| 2   | Reserved          |   |   |                   |   |                  |
| 1   | Reserved          |   |   |                   |   |                  |
| 0   | WD_EN             | Watchdog enabled bit<br><table border="1" style="width: 100%;"> <tr> <td style="width: 50px; text-align: center;">0</td> <td>Watchdog disabled</td> </tr> <tr> <td style="text-align: center;">1</td> <td>Watchdog enabled</td> </tr> </table> Writing to this bit is only possible during CAN Flash Mode ( $V_{TxDL} > V_{Flash}$ ). See <a href="#">Section 2.2.2: Flash Mode</a> . | 0 | Watchdog disabled | 1 | Watchdog enabled |
| 0   | Watchdog disabled |   |   |                   |   |                  |
| 1   | Watchdog enabled  |   |   |                   |   |                  |

6.2.20 Control Register 35

Table 128. Control register 35: command and data bytes

| Command byte |   |         |   |   |   |   |   | 1 <sup>st</sup> data byte | 2 <sup>nd</sup> data byte |
|--------------|---|---------|---|---|---|---|---|---------------------------|---------------------------|
| Read/write   |   | Address |   |   |   |   |   |                           |                           |
| x            | x | 1       | 0 | 0 | 0 | 1 | 1 | Data, 8 bit               | Data, 8 bit               |

Table 129. Control register 35, data bytes

|          | 1 <sup>st</sup> data byte <15:8> |   |   |   |   |   |   |   | 2 <sup>nd</sup> data byte <7:0> |         |         |         |         |         |         |   |
|----------|----------------------------------|---|---|---|---|---|---|---|---------------------------------|---------|---------|---------|---------|---------|---------|---|
| Defaults | 0                                | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               | 0       | 1       | 1       | 0       | 1       | 1       | 0 |
| Function | Reserved                         |   |   |   |   |   |   |   | CR35_25                         | CR35_24 | CR35_23 | CR35_22 | CR35_21 | CR35_20 | CR35_10 |   |
| Group    | Selective Wakeup Settings        |   |   |   |   |   |   |   |                                 |         |         |         |         |         |         |   |

Table 130. Control register 35, bits

| Bit | Name     | Comment                 |                         |
|-----|----------|-------------------------|-------------------------|
| 15  | Reserved |                         |                         |
| 14  | Reserved |                         |                         |
| 13  | Reserved |                         |                         |
| 12  | Reserved |                         |                         |
| 11  | Reserved | Must be kept at default |                         |
| 10  | Reserved |                         |                         |
| 9   | Reserved |                         |                         |
| 8   | Reserved |                         |                         |
| 7   | Reserved |                         |                         |
| 6   | CR35_25  |                         | Must be kept at default |
| 5   | CR35_24  |                         |                         |
| 4   | CR35_23  |                         |                         |
| 3   | CR35_22  |                         |                         |
| 2   | CR35_21  |                         |                         |
| 1   | CR35_20  |                         |                         |
| 0   | CR35_10  | Must be kept at default |                         |

6.2.21 Overview status register

Table 131. Overview of status register data bytes

|          |  | 1 <sup>st</sup> data byte <15:8>            |           |              |              |          |            |            | 2 <sup>nd</sup> data byte <7:0> |                |              |                  |              |                  |                         |                |                  |
|----------|--|---|-----------|--------------|--------------|----------|------------|------------|---------------------------------|----------------|--------------|------------------|--------------|------------------|-------------------------|----------------|------------------|
|          |  | <b>Status register 1, data &lt;15:0&gt;</b> |           |              |              |          |            |            |                                 |                |              |                  |              |                  |                         |                |                  |
| Function |  | OL_HS                                       | OL_OUT4   | OL_OUT3      | OL_OUT2      | OL_OUT1  | UV         | V2_fail    | V2_short                        | OV             | OC_HS        | OC_OUT4          | OC_OUT3      | OC_OUT2          | OC_OUT1                 | OC_REL2        | OC_REL1          |
| Group    |  | Diagnosis 1                                 |           |              |              |          |            |            | Diagnosis 2                     |                |              |                  |              |                  |                         |                |                  |
|          |  | <b>Status register 2, data &lt;15:0&gt;</b> |           |              |              |          |            |            |                                 |                |              |                  |              |                  |                         |                |                  |
| Function |  | WU3_state                                   | WU2_state | WU1_state    | WU3_wake     | WU2_wake | WU1_Wake   | Wake_CAN   | Wake_LIN                        | Wake_Timer_int | LIN_perm_dom | LIN_TxD_perm_dom | LIN_perm_rec | CAN_RxD_perm_rec | CAN_perm_rec            | CAN_perm_dom   | CAN_TxD_perm_dom |
| Group    |  | Diagnosis 3                                 |           |              |              |          |            |            | Diagnosis 4                     |                |              |                  |              |                  |                         |                |                  |
|          |  | <b>Status register 3, data &lt;15:0&gt;</b> |           |              |              |          |            |            |                                 |                |              |                  |              |                  |                         |                |                  |
| Function |  | TSD1  | TW        | Device_state | Device_state | V1_fail  | V1_restart | V1_restart | V1_restart                      | WD_fail        | WD_fail      | WD_fail          | WD_fail      | Forced_sleep_WD  | Forced_sleep_TSD2_SHTV1 | WD_timer_state | WD_timer_state   |
| Group    |  | Diagnosis 5                                 |           |              |              |          |            |            | Diagnosis 6                     |                |              |                  |              |                  |                         |                |                  |
|          |  | <b>Status register 4, data &lt;15:0&gt;</b> |           |              |              |          |            |            |                                 |                |              |                  |              |                  |                         |                |                  |
| Function |  | SWRD_15                                     | SWRD_14   | SWRD_13      | SWRD_12      | SWRD_11  | SWRD_10    | SWRD_9     | SWR_D 8                         | SWRD_7         | SYS_ERR      | TX_SYNC          | CAN_TO       | WUP              | WUF                     | CAN_silent     | FD_ERR           |
| Group    |  | Diagnosis 7                                 |           |              |              |          |            |            | Diagnosis 8                     |                |              |                  |              |                  |                         |                |                  |
|          |  | <b>Status register 5, data &lt;15:0&gt;</b> |           |              |              |          |            |            |                                 |                |              |                  |              |                  |                         |                |                  |
| Function |  | Reserved                                    |           | FECNT_4      | FECNT_3      | FECNT_2  | FECNT_1    | FECNT_0    | OSC_FAIL                        | Reserved       |              | Osc_Mon          |              |                  |                         |                |                  |
| Group    |  | Diagnosis 9                                 |           |              |              |          |            |            | Diagnosis 10                    |                |              |                  |              |                  |                         |                |                  |



## 6.2.22 Global status register

The Global Error Flag is set once the watchdog failure counter (SR3<7:4>) is unequal to 0 (see also [Section 2.5: Fail Safe Mode](#)).

**Table 132. Global status register**

|  | Bit 7                            | Bit 6                              | Bit 5   | Bit 4               | Bit 3 | Bit 2   | Bit 1                                      | Bit 0                    | Hex value |
|--|----------------------------------|------------------------------------|---|---------------------|-------|---------|--|--------------------------|-----------|
|  | Global error flag <sup>(1)</sup> | Communication error <sup>(2)</sup> | NOT (chip reset or comm error) <sup>(3)</sup> | TSD2 <sup>(4)</sup> | TSD1  | V1 Fail | V <sub>S</sub> Fail (OV/UV) <sup>(5)</sup> | Fail safe <sup>(6)</sup> |           |
| Active high/low  | High                             | High                               | Low   | High                | High  | High    | High                                       | High                     |           |
| Default value in Normal Mode - after correct WD trigger or after Read & Clear on Error Flags | 0                                | 0                                  | 1   | 0                   | 0     | 0       | 0  | 0                        | 20        |
| Power ON   | 1                                | 0                                  | 0   | 0                   | 0     | 0       | 0  | 0                        | 80        |
| Power ON weak battery <sup>(7)</sup>   | 1                                | 0                                  | 0   | 0                   | 0     | 0       | 1  | 0                        | 82        |
| Communication error  | 1                                | 1                                  | 0   | 0                   | 0     | 0       | 0  | 0                        | C0        |
| V <sub>S</sub> overvoltage or undervoltage   | 1                                | 0                                  | 1   | 0                   | 0     | 0       | 1  | 0                        | A2        |
| WD failure   | 1                                | 0                                  | 1   | 0                   | 0     | 0       | 0  | 1                        | A1        |
| SPI Error (DI Stuck)   | 1                                | 0                                  | 1   | 0                   | 0     | 0       | 0  | 1                        | A1        |
| TSD1   | 1                                | 0                                  | 1   | 0                   | 1     | 0       | 0  | 0                        | A8        |
| TSD2   | 1                                | 0                                  | 1   | 1                   | 1     | 0       | 0  | 1                        | B9        |
| V1 Fail  | 1                                | 0                                  | 1   | 0                   | 0     | 1       | 0  | 0                        | A4        |
| Other Device Failure <sup>(8)</sup>  | 1                                | 0                                  | 1   | 0                   | 0     | 0       | 0  | 0                        | A0        |

- The following Status Bits are reported in the Global Error Flag:  
Global Status Register: Bits 6-0  
Status Register 1: Bits 10-0  
Status Register 3: Bits 15, 11, 7-2
- Communication Error: invalid number of CLOCK cycles during CSN low or failed parity check on standby command.
- Cleared with CLR command on SR3.
- Cleared with "READ and CLEAR" on SR3 (-> TSD1)
- Diagnosis bit only, V<sub>S</sub> Fail is not a Fail-Safe event; cleared by Read&Clear. Bit is automatically cleared at (V<sub>S</sub> > V<sub>SUV</sub>) and (V<sub>S</sub> < V<sub>SOV</sub>) if Vlock\_out\_en = 0
- Cleared with a valid WD trigger (WD fail) or by clearing the corresponding status register related to failure. It is recommended that the microcontroller does not enter standby mode, if a fail-safe event is indicated in the Global Status Register. The selective wake-up configuration in CR 7 to 15 has to be re-written before sending the standby command.
- Slow V<sub>S</sub> ramp-up (V<sub>S</sub> undervoltage is filtered with 64µs after power-on reset)
- The Global Error Flag is raised due to a failure condition which is not reported in the Global Status Register. The Failure is reported in the Status Registers 1-5

6.2.23 Status Register 1

Table 133. Status register 1: command and data bytes

| Command byte |   |         |   |   |   |   |   | 1 <sup>st</sup> data byte | 2 <sup>nd</sup> data byte |
|--------------|---|---------|---|---|---|---|---|---------------------------|---------------------------|
| Read/write   |   | Address |   |   |   |   |   | Bit <15:8>                | Bit <7:0>                 |
| x            | x | 0       | 1 | 0 | 0 | 0 | 1 | Data, 8bit                | Data, 8 bit               |

Table 134. Status register 1, data bytes

|          | 1 <sup>st</sup> data byte <15:8> |         |         |         |         |    |         |          | 2 <sup>nd</sup> data byte <7:0> |       |         |         |         |         |         |         |
|----------|----------------------------------|---------|---------|---------|---------|----|---------|----------|---------------------------------|-------|---------|---------|---------|---------|---------|---------|
| Function | OL_HS                            | OL_OUT4 | OL_OUT3 | OL_OUT2 | OL_OUT1 | UV | V2_fail | V2_short | OV                              | OC_HS | OC_OUT4 | OC_OUT3 | OC_OUT2 | OC_OUT1 | OC_REL2 | OC_REL1 |
| Group    | Diagnosis 1                      |         |         |         |         |    |         |          | Diagnosis 2                     |       |         |         |         |         |         |         |

Table 135. Status register 1, bits

| Bit | Name     | Comment   | Information storage                            |  |
|-----|----------|---|--|--|
| 15  | OL_HS    | Open-load event occurred since last read out  | Bit is latched until a “read and clear” access |  |
| 14  | OL_OUT4  |   |  |  |
| 13  | OL_OUT3  |   |  |  |
| 12  | OL_OUT2  |   |  |  |
| 11  | OL_OUT1  |   |  |  |
| 10  | UV       | Under voltage event on V <sub>S</sub> occurred since last read out  | <b>VLOCKOUTEN (CR4)</b>                        | <b>Information storage</b>                       |
|     |          |   | 0  | automatically reset when UV condition disappears |
|     |          |   | 1  | Bit is latched until a “read and clear” access   |
|     |          |   |  |  |
| 9   | V2_fail  | V <sub>2</sub> fail (V <sub>2</sub> < 2 V for t > 2 μs) event occurred since last readout                 | Bit is latched until a “Read and clear” access |  |
| 8   | V2_short | V <sub>2</sub> short (V <sub>2</sub> < 2 V for t > 4ms during start up) event occurred since last readout | Bit is latched until a “Read and clear” access |  |

Table 135. Status register 1, bits (continued)

| Bit | Name    | Comment  | Information storage                            |  |
|-----|---------|--|--|--|
| 7   | OV      | Over voltage event on $V_S$ occurred since last read out | <b>VLOCKOUTEN (CR4)</b>                        |  |
|     |         |  | <b>Information storage</b>                     |  |
|     |         |  | 0  | automatically reset when OV condition disappears |
|     |         |  | 1  | Bit is latched until a “read and clear” access   |
| 6   | OC_HS   | Over current event occurred since last read out          | Bit is latched until a “read and clear” access |  |
| 5   | OC_OUT4 |  |  |  |
| 4   | OC_OUT3 |  |  |  |
| 3   | OC_OUT2 |  |  |  |
| 2   | OC_OUT1 |  |  |  |
| 1   | OC_REL2 |  |  |  |
| 0   | OC_REL1 |  |  |  |

6.2.24 Status Register 2

Table 136. Status register 2: command and data bytes

| Command byte |   |         |   |   |   |   |   | 1 <sup>st</sup> data byte | 2 <sup>nd</sup> data byte |
|--------------|---|---------|---|---|---|---|---|---------------------------|---------------------------|
| Read/write   |   | Address |   |   |   |   |   | Bit <15:8>                | Bit <7:0>                 |
| x            | x | 0       | 1 | 0 | 0 | 1 | 0 | Data, 8bit                | Data, 8 bit               |

Table 137. Status register 2, data bytes

|          | 1 <sup>st</sup> data byte <15:8> |           |           |          |          |          |          |          |                | 2 <sup>nd</sup> data byte <7:0> |                  |              |                  |              |              |                  |
|----------|----------------------------------|-----------|-----------|----------|----------|----------|----------|----------|----------------|---------------------------------|------------------|--------------|------------------|--------------|--------------|------------------|
| Function | WU3_state                        | WU2_state | WU1_state | WU3_wake | WU2_wake | WU1_wake | Wake_CAN | Wake_LIN | Wake_Timer_int | LIN_perm_dom                    | LIN_TxD_perm_dom | LIN_perm_rec | CAN_RxD_perm_rec | CAN_perm_rec | CAN_perm_dom | CAN_TxD_perm_dom |
| Group    | Diagnosis 3                      |           |           |          |          |          |          |          |                | Diagnosis 4                     |                  |              |                  |              |              |                  |

Table 138. Status register 2, bits

| Bit | Name                    | Comment                              | Information storage                              |
|-----|-------------------------|--------------------------------------|--|
| 15  | WU3_state               | State of WUx input;                  | "Live bits" not clearable                        |
| 14  | WU2_state               |                                      |  |
| 13  | WU1_state               |                                      |  |
| 12  | WU3_wake                | Shows wake up source ('1' = wake-up) | Bits are latched until a "Read and clear" access |
| 11  | WU2_wake                |                                      |  |
| 10  | WU1_wake                |                                      |  |
| 9   | WAKE_CAN <sup>(1)</sup> |                                      |  |
| 8   | WAKE_LIN                |                                      |  |
| 7   | Wake_TIMER_int          |                                      |  |





**Table 138. Status register 2, bits (continued)**

| Bit | Name             | Comment  | Information storage                              |
|-----|------------------|--|--|
| 6   | LIN_perm_DOM     | LIN bus is dominant for t > 12 ms                                  | Bits are latched until a “Read and clear” access |
| 5   | LIN_TxD_perm_DOM | TxDL pin is dominant for t > 12 ms; Transmitter is disabled        |  |
| 4   | LIN_perm_REC     | LIN bus does not follow TxDL within 40 μs; Transmitter is disabled |  |
| 3   | CAN_RxD_perm_rec | RxDC has not followed TxDC for 4 times; Transmitter is disabled    |  |
| 2   | CAN_perm_REC     | CAN has not followed TxDC for 4 times; Transmitter is disabled     |  |
| 1   | CAN_perm_DOM     | CAN bus is dominant for t > 700 μs                                 |  |
| 0   | CAN_TxD_perm_DOM | TxDC pin is dominant for t > 700 μs; Transmitter is disabled       |  |

1. The bit is set only if CAN\_WU\_EN = 1; the bit does not indicate a wake-up by CAN wake-up frame (WUF).

### 6.2.25 Status Register 3

**Table 139. Status register 3: command and data bytes**

| Command byte |   |         |   |   |   |   |   | 1 <sup>st</sup> data byte | 2 <sup>nd</sup> data byte |
|--------------|---|---------|---|---|---|---|---|---------------------------|---------------------------|
| Read/write   |   | Address |   |   |   |   |   | Bit <15:8>                | Bit <7:0>                 |
| x            | x | 0       | 1 | 0 | 0 | 1 | 1 | Data, 8bit                | Data, 8 bit               |

**Table 140. Status register 3, data bytes**

|          | 1 <sup>st</sup> data byte <15:8> |    |                |                |         |              |              |              | 2 <sup>nd</sup> data byte <7:0> |           |           |           |                 |                         |                  |                  |
|----------|----------------------------------|----|----------------|----------------|---------|--------------|--------------|--------------|---------------------------------|-----------|-----------|-----------|-----------------|-------------------------|------------------|------------------|
| Function | TSD1                             | TW | Device_state_1 | Device_state_0 | V1_fail | V1_restart_2 | V1_restart_1 | V1_restart_0 | WD_fail_3                       | WD_fail_2 | WD_fail_1 | WD_fail_0 | Forced_sleep_WD | Forced_sleep_TSD2_SHTV1 | WD_timer_state_1 | WD_timer_state_0 |
| Group    | Diagnosis 5                      |    |                |                |         |              |              |              | Diagnosis 6                     |           |           |           |                 |                         |                  |                  |

**Table 141. Status register 3, bits**

| Bit | Name | Comment   | Information storage                            |
|-----|------|---|--|
| 15  | TSD1 | Thermal warning / shutdown1 occurred since last readout | Bit is latched until a “read and clear access” |
| 14  | TW   |   |  |

**Table 141. Status register 3, bits (continued)**

| Bit | Name                                | Comment   | Information storage   |  |                                     |
|-----|-------------------------------------|---|---|--|-------------------------------------|
| 13  | Device_state                        | State from which the device woke up   |   | Bit is latched until a “read and clear access” after a “read and clear access”, the device state is updated. After a wake up, device state is:<br>01: V <sub>1_standby</sub><br>or<br>10: V <sub>Bat_standby</sub> |                                     |
| 12  |                                     | Device state_2  | Device state_1  |  | State from which the device woke up |
|     |                                     | 0   | 0   |  | Active                              |
|     |                                     | 0   | 1   |  | V <sub>1_standby</sub>              |
|     |                                     | 1   | 0   |  | V <sub>Bat_standby</sub>            |
|     |                                     | 1   | 1   |  | Flash                               |
| 11  | V1_fail                             | V <sub>1</sub> fail (V <sub>1</sub> < 2 V for t > 2 μs) event occurred since last read out  | Bit is latched until a “read and clear access”  |  |                                     |
| 10  | V1_restart_2                        | Number of TSD2 events which caused a restart of V <sub>1</sub> regulator (7 TSD2 events forces the device into V <sub>Bat_standby</sub> ) | Bits are not clearable; is cleared automatically if no additional TSD2 event occurs within 1 min. |  |                                     |
| 9   | V1_restart_1                        |   |   |  |                                     |
| 8   | V1_restart_0                        |   |   |  |                                     |
| 7   | WD_fail_3                           | Number of missing watchdog triggers (15 missing watchdog trigger forces the device into V <sub>Bat_standby</sub> )                        | Bits are not clearable; is cleared with a proper Watchdog trigger                                 |  |                                     |
| 6   | WD_fail_2                           |   |   |  |                                     |
| 5   | WD_fail_1                           |   |   |  |                                     |
| 4   | WD_fail_0                           |   |   |  |                                     |
| 3   | Forced_sleep_WD                     | Device was forced to V <sub>Bat_standby</sub> mode because of multiple watchdog errors  | Bits are latched until a read and clear access  |  |                                     |
| 2   | Forced_sleep_TSD2_SHTV <sub>1</sub> | Device was forced to V <sub>Bat_standby</sub> or multiple thermal shutdown events or a short on V <sub>1</sub> during startup.            |   |  |                                     |
| 1   | WD_timer_state_1                    | Status of watchdog counter of selected watchdog timing  | Bits are not clearable  |  |                                     |
| 0   | WD_timer_state_0                    |   |   |  |                                     |
|     | WD_timer_state_1                    |   |   | WD_timer_state_0   | Counter                             |
|     | 0                                   |   |   | 0  | 0 – 33%                             |
|     | 0                                   |   |   | 1  | 33 – 66%                            |
|     | 1                                   | 1   | 66 – 100%   |  |                                     |

## 6.2.26 Status Register 4

Table 142. Status register 4: command and data bytes

| Command byte |   |         |   |   |   |   |   | 1 <sup>st</sup> data byte | 2 <sup>nd</sup> data byte |
|--------------|---|---------|---|---|---|---|---|---------------------------|---------------------------|
| Read/write   |   | Address |   |   |   |   |   | Bit <15:8>                | Bit <7:0>                 |
| x            | x | 0       | 1 | 0 | 1 | 0 | 0 | Data, 8bit                | Data, 8 bit               |

Table 143. Status register 4, data bytes

|          | 1 <sup>st</sup> data byte <15:8> |         |         |         |         |         |        |        | 2 <sup>nd</sup> data byte <7:0> |         |         |        |     |     |            |        |
|----------|----------------------------------|---------|---------|---------|---------|---------|--------|--------|---------------------------------|---------|---------|--------|-----|-----|------------|--------|
| Function | SWRD_15                          | SWRD_14 | SWRD_13 | SWRD_12 | SWRD_11 | SWRD_10 | SWRD_9 | SWRD_8 | SWRD_7                          | SYS_ERR | TX_SYNC | CAN_TO | WUP | WUF | CAN_silent | FD_ERR |
| Group    | Diagnosis 5                      |         |         |         |         |         |        |        | Diagnosis 6                     |         |         |        |     |     |            |        |

Table 144. Status register 4, bits

| Bit | Name    | Comment  | Information storage   |
|-----|---------|--|---|
| 15  | SWRD_15 | Status flag for Read operation to Selective Wakeup relevant Registers<br>0: Read not done<br>1: Read done<br>See also <a href="#">Section 2.10: Serial Peripheral Interface (ST SPI Standard 3.0)</a>                              | Automatically cleared by a write  |
| 14  | SWRD_14 |  |   |
| 13  | SWRD_13 |  |   |
| 12  | SWRD_12 |  |   |
| 11  | SWRD_11 |  |   |
| 10  | SWRD_10 |  |   |
| 9   | SWRD_9  |  |   |
| 8   | SWRD_8  |  |   |
| 7   | SWRD_7  |  |   |
| 6   | SYS_ERR | This bit is a logical OR combination of NOT(SWRD_x) OR OSC_Fail OR FD_ERR<br>The selective wake feature cannot be enabled (SW_EN = 1) if SYS_ERR = 1<br>In case of a SYS_ERR the selective wake-up feature is disabled (SW_EN = 0) | Live bit be updated while the change of SWRD_x, OSC_Fail and FD_ERR.<br>If SWRD_x are all 1, OSC_Fail is 0 and FD_ERR is 0, this bit is 0, otherwise this bit is 1. |
| 5   | TX_SYNC | Status flag for Synchronous Reference oscillator of the Transceiver. Indicates that the last received frame was decoded correctly<br>0: Not synchron<br>1: Synchron  | Live bit updated after each sent CAN frame  |

Table 144. Status register 4, bits (continued)

| Bit | Name       | Comment   | Information storage                          |
|-----|------------|---|--|
| 4   | CAN_TO     | CAN timeout, bit is set if there is no communication on the bus for longer than $t_{\text{silence}}$<br>$V_{\text{bat\_standby}}$ Mode: CAN_TO indicates that there was a transition from PN_TRX_selective_sleep to TRX_SLEEP<br>During TRX_STBY Mode (CAN_ACT = 0, Active Mode and $V_{1\_standby}$ Mode <sup>(1)</sup> ) this bit indicates a CAN communication timeout. An interrupt on RxDC/NINT is generated in this case. | Bit is latched until a read and clear access |
| 3   | WUP        | Wake up flag for Remote Wake up pattern   | Bit is latched until a read and clear access |
| 2   | WUF        | Wake up flag for Remote Wake up Frame   | Bit is latched until a read and clear access |
| 1   | CAN_Silent | Online monitoring bit to see if there is silence on the bus for longer than $t_{\text{silence}}$<br>This flag shows the actual status of the CAN bus (activity/silence). A microcontroller in Stop Mode may check this flag periodically  | Auto cleared and set                         |
| 0   | FD_ERR     | Frame Detect Error.<br>This bit is set at overflow of the Frame Error Counter (FECNT) in SR5<br>In case of a Frame Detect Error, the device will wake up from PN_Trx_selective_sleep  | Bit is latched until a read and clear access |

1. It is recommended to clear the bit CAN\_TO prior to transition into  $V_{1\_standby}$  mode.

## 6.2.27 Status Register 5

Table 145. Status register 5: command and data bytes

| Command byte |   |         |   |   |   |   |   | 1 <sup>st</sup> data byte | 2 <sup>nd</sup> data byte |
|--------------|---|---------|---|---|---|---|---|---------------------------|---------------------------|
| Read/write   |   | Address |   |   |   |   |   | Bit <15:8>                | Bit <7:0>                 |
| x            | x | 0       | 1 | 0 | 1 | 0 | 1 | Data, 8bit                | Data, 8 bit               |

Table 146. Status register 5, data bytes

|          | 1 <sup>st</sup> data byte <15:8> |         |         |         |         |         | 2 <sup>nd</sup> data byte <7:0> |          |         |         |         |         |         |
|----------|----------------------------------|---------|---------|---------|---------|---------|---------------------------------|----------|---------|---------|---------|---------|---------|
| Function | Reserved                         | FECNT_4 | FECNT_3 | FECNT_2 | FECNT_1 | FECNT_0 | OSC_FAIL                        | Reserved | Osc_mon | Osc_mon | Osc_mon | Osc_mon | Osc_mon |
| Group    | Diagnosis 5                      |         |         |         |         |         | Diagnosis 6                     |          |         |         |         |         |         |

Table 147. Status register 5, bits

| Bit   | Name     | Comment   | Information storage                          |
|-------|----------|---|--|
| 15    | Reserved | Must be kept at default   |  |
| 14    | Reserved |   |  |
| 13    | Reserved |   |  |
| 12    | FECNT_4  | Frame Detect Error Counter  | Live bit updated after each sent CAN frame   |
| 11    | FECNT_3  | This counter is increased by 1 in case a frame was not received/decoded correctly (CRC error, stuff-bit error, form error). |  |
| 10    | FECNT_2  | The counter is decreased by 1 with every frame which is decoded correctly   |  |
| 9     | FECNT_1  | If FECNT = 31, the next erroneous frame will wake-up the device, set FDERR = 1 and reset FECNTx = 0                         |  |
| 8     | FECNT_0  |   |  |
| 7     | OSC_FAIL | OSC Failure Flag (used device internally)   | Bit is latched until a read and clear access |
| 6     | Reserved | Must be kept at default   |  |
| 5     | Reserved |   |  |
| 4 - 0 | Osc_mon  | Monitoring of internal oscillator (used internally)   | Live bit updated after each sent CAN frame   |

## 7 Package information

### 7.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 7.2 PowerSSO-36 mechanical data

Figure 44. PowerSSO-36 package dimensions

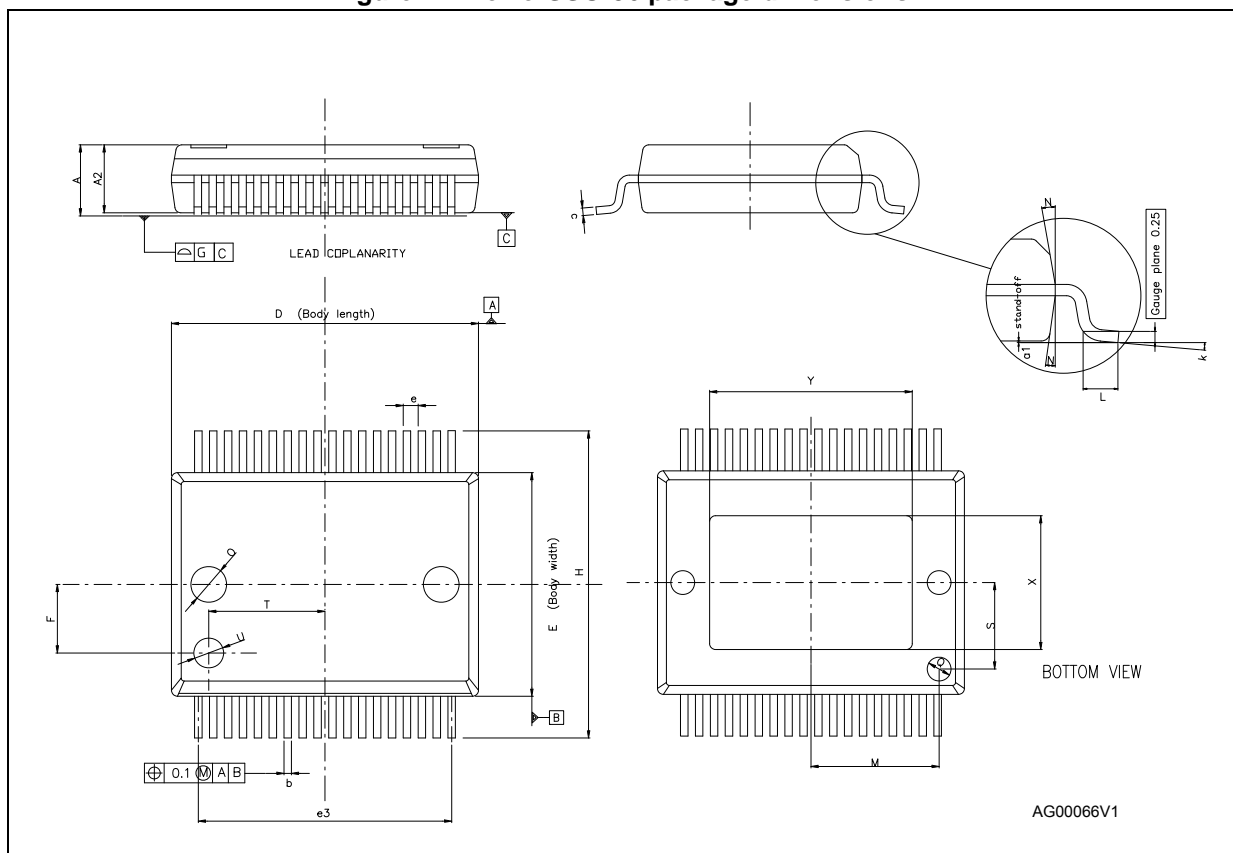


Table 148. PowerSSO-36 mechanical data

| Symbol | Millimeters |      |        |
|--------|-------------|------|--------|
|        | Min.        | Typ. | Max.   |
| A      | -           | -    | 2.45   |
| A2     | 2.15        | -    | 2.35   |
| a1     | 0           | -    | 0.1    |
| b      | 0.18        | -    | 0.36   |
| c      | 0.23        | -    | 0.32   |
| D      | 10.10       | -    | 10.50  |
| E      | 7.4         | -    | 7.6    |
| e      | -           | 0.5  | -      |
| e3     | -           | 8.5  | -      |
| F      | -           | 2.3  | -      |
| G      | -           | -    | 0.1    |
| G1     | -           | -    | 0.06   |
| H      | 10.1        | -    | 10.5   |
| h      | -           | -    | 0.4    |
| k      | 0°          | -    | 8°     |
| L      | 0.55        | -    | 0.85   |
| M      | -           | 4.3  | -      |
| N      | -           | -    | 10 deg |
| O      | -           | 1.2  | -      |
| Q      | -           | 0.8  | -      |
| S      | -           | 2.9  | -      |
| T      | -           | 3.65 | -      |
| U      | -           | 1.0  | -      |
| X      | 4.1         | -    | 4.7    |
| Y      | 6.5         | -    | 7.1    |

## 8 Revision history

**Table 149. Document revision history**

| Date        | Revision | Changes  |
|-------------|----------|--|
| 10-Jun-2013 | 1        | Initial release.   |
| 19-Sep-2013 | 2        | Updated Disclaimer.  |
| 03-Mar-2014 | 3        | <p>Updated <a href="#">Section 2.2.5: Interrupt</a><br/>           Added <a href="#">Section : Oscillator monitoring</a><br/>           Updated <a href="#">Section 2.9.4: Wake up by CAN</a><br/> <a href="#">Table 14: Supply and supply monitoring</a><br/>           – <math>V_{\text{hyst\_UV}}</math>: updated values<br/> <a href="#">Table 28: CAN transmitter and receiver: pins CANH and CANL:</a><br/>           – <math>V_{\text{CANHdom}}</math>, <math>V_{\text{CANLdom}}</math>, <math>V_{\text{DIFF,domOUT}}</math>: updated test condition<br/>           – <math>V_{\text{CM}}</math>: updated test condition and added note<br/>           – <math>V_{\text{THdom}}</math>, <math>V_{\text{THdomLP}}</math>, <math>V_{\text{THrec}}</math>, <math>V_{\text{THrecLP}}</math>: added note<br/> <a href="#">Table 29: CAN transceiver timing:</a><br/>           – <math>t_{\text{TXpd,hl}}</math>, <math>t_{\text{TXpd,hl}}</math>: updated test condition<br/> <a href="#">Table 91: Control register 5, bits:</a><br/>           – PWM2 duty cycle, PWM1 duty cycle: updated values<br/> <a href="#">Table 94: Control register 6, bits:</a><br/>           – PWM4 duty cycle, PWM3 duty cycle: updated values<br/> <a href="#">Table 124: Control register 16, bits:</a><br/>           – SW_EN: added note<br/>           – BR_0: updated comment<br/> <a href="#">Table 138: Status register 2, bits:</a><br/>           – WAKE_CAN: added note<br/> <a href="#">Table 144: Status register 4, bits:</a><br/>           – Removed note</p> |
| 24-Apr-2014 | 4        | Updated <a href="#">Section 2.2.2: Flash Mode</a>  |



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