16-Lane 4-Port PCI Express® Switch

89HPES16T4
Data Sheet

Device Overview

The 89HPES16T4 is a member of the IDT PRECISE™ family of PCI Express® switching solutions. The PES16T4 is a 16-lane, 4-port peripheral chip that performs PCI Express packet switching with a feature set optimized for high performance applications such as servers, storage, and communications/networking. It provides connectivity and switching functions between a PCI Express upstream port and up to three downstream ports and supports switching between downstream ports.

Features

- **High Performance PCI Express Switch**
  - *Sixteen 2.5 Gbps PCI Express lanes*
  - *Four switch ports*
  - *Upstream port configurable up to x8*
  - *Downstream ports configurable up to x4*
  - *Low-latency cut-through switch architecture*
  - *Support for Max Payload Size up to 2048 bytes*
  - *One virtual channel*
  - *Eight traffic classes*
  - *PCI Express Base Specification Revision 1.1 compliant*
- **Flexible Architecture with Numerous Configuration Options**
  - *Automatic per port link width negotiation to x8, x4, x2 or x1*
  - *Automatic lane reversal on all ports*
  - *Automatic polarity inversion on all lanes*
  - *Ability to load device configuration from serial EEPROM*
- **Legacy Support**
  - *PCI compatible INTx emulation*
  - *Bus locking*
- **Highly Integrated Solution**
  - *Requires no external components*
  - *Incorporates on-chip internal memory for packet buffering and queueing*
  - *Integrates sixteen 2.5 Gbps embedded SerDes with 8B/10B encoder/decoder (no separate transceivers needed)*
- **Reliability, Availability, and Serviceability (RAS) Features**
  - *Supports ECRC and Advanced Error Reporting*
  - *Internal end-to-end parity protection on all TLPs ensures data integrity even in systems that do not implement end-to-end CRC (ECRC)*
  - *Supports PCI Express Native Hot-Plug, Hot-Swap capable I/O*
  - *Compatible with Hot-Plug I/O expanders used on PC and server motherboards*

Block Diagram

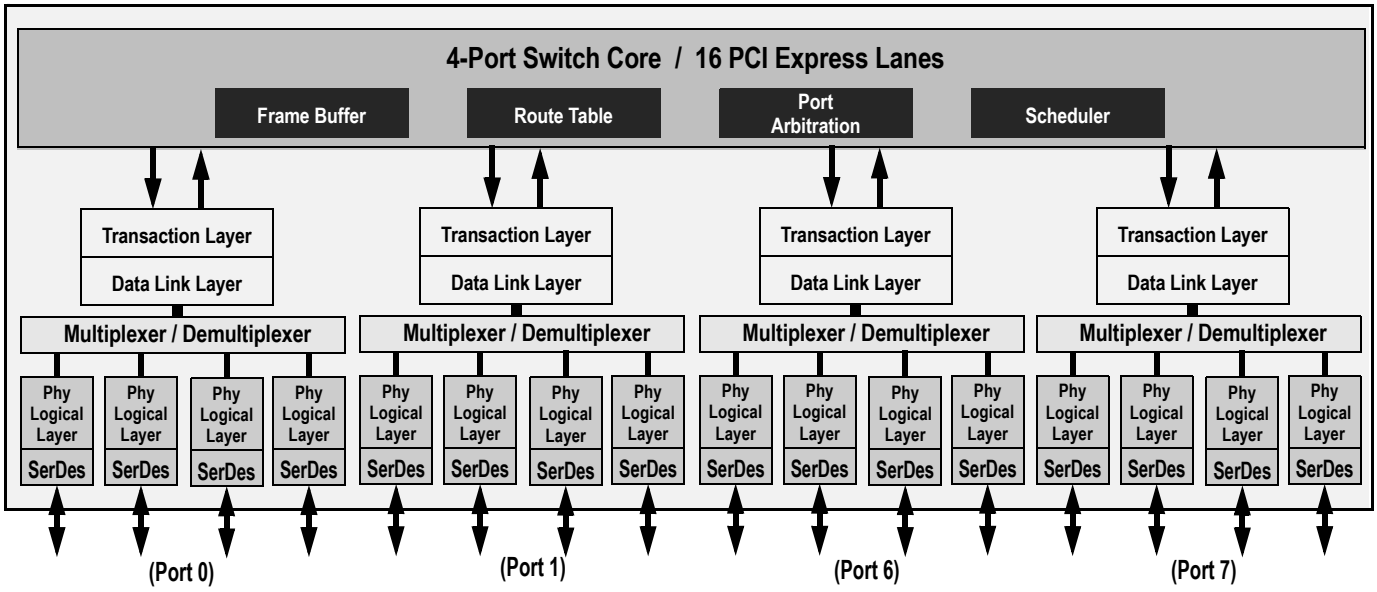

Figure 1 Internal Block Diagram

- **Power Management**
  - *Utilizes advanced low-power design techniques to achieve low typical power consumption*
  - *Supports PCI Power Management Interface specification (PCI-PM 1.1)*
    - *Supports device power management states: D0, $D3_{hot}$ and $D3_{cold}$*
  - *Unused SerDes are disabled*
- **Testability and Debug Features**
  - *Ability to read and write any internal register via the SMBus*
- **Eleven General Purpose Input/Output Pins**
  - *Each pin may be individually configured as an input or output*
  - *Each pin may be individually configured as an interrupt input*
  - *Some pins have selectable alternate functions*
- **Packaged in a 23mm x 23mm 484-ball BCG with 1mm ball spacing**

Product Description

Utilizing standard PCI Express interconnect, the PES16T4 provides the most efficient I/O connectivity solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. It provides connectivity for up to 4 ports across 16 integrated serial lanes. Each lane provides 2.5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base specification revision 1.1.

SMBus Interface

The PES16T4 contains two SMBus interfaces. The slave interface provides full access to the configuration registers in the PES16T4, allowing every configuration register in the device to be read or written by an external agent. The master interface allows the default configuration register values of the PES16T4 to be overridden following a reset with values programmed in an external serial EEPROM. The master interface is also used by an external Hot-Plug I/O expander.

Six pins make up each of the two SMBus interfaces. These pins consist of an SMBus clock pin, an SMBus data pin, and 4 SMBus address pins. In the slave interface, these address pins allow the SMBus address to which the device responds to be configured. In the master interface, these address pins allow the SMBus address of the serial configuration EEPROM from which data is loaded to be configured. The SMBus address is set up on negation of PERSTN by sampling the corresponding address pins. When the pins are sampled, the resulting address is assigned as shown in Table 1.

Bit	Slave SMBus Address	Master SMBus Address
1	SSMBADDR[1]	MSMBADDR[1]
2	SSMBADDR[2]	MSMBADDR[2]
3	SSMBADDR[3]	MSMBADDR[3]
4	0	MSMBADDR[4]
5	SSMBADDR[5]	1
6	1	0
7	1	1

Table 1 Master and Slave SMBus Address Assignment

As shown in Figure 2, the master and slave SMBuses may be used in a unified or split configuration. In the unified configuration, shown in Figure 2(a), the master and slave SMBuses are tied together and the PES16T4 acts both as a SMBus master as well as a SMBus slave on this bus. This requires that the SMBus master or processor that has access to PES16T4 registers supports SMBus arbitration. In some systems, this SMBus master interface may be implemented using general purpose I/O pins on a processor or micro controller, and may not support SMBus arbitration. To support these systems, the PES16T4 may be configured to operate in a split configuration as shown in Figure 2(b).

In the split configuration, the master and slave SMBuses operate as two independent buses and thus multi-master arbitration is never required. The PES16T4 supports reading and writing of the serial EEPROM on the master SMBus via the slave SMBus, allowing in system programming of the serial EEPROM.

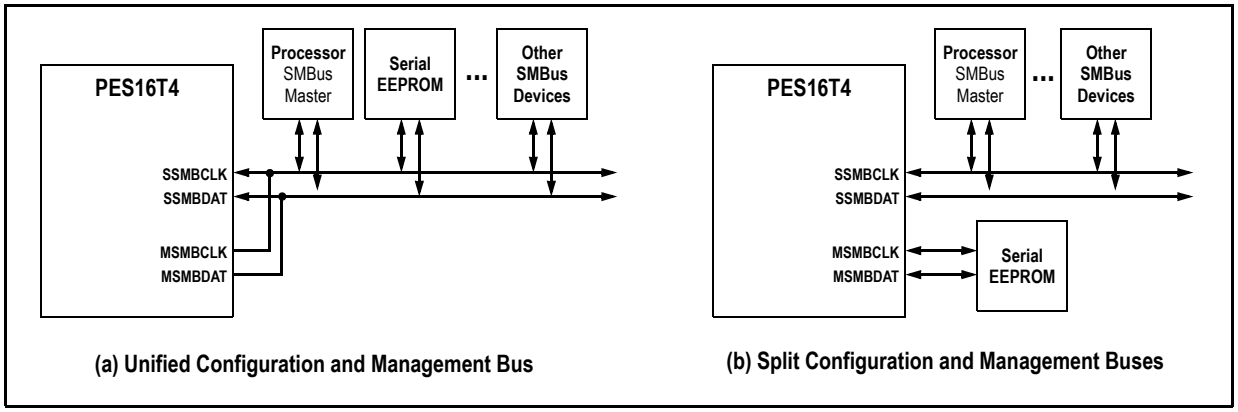

Figure 2 SMBus Interface Configuration Examples

Hot-Plug Interface

The PES16T4 supports PCI Express Hot-Plug on each downstream port. To reduce the number of pins required on the device, the PES16T4 utilizes an external I/O expander, such as that used on PC motherboards, connected to the SMBus master interface. Following reset and configuration, whenever the state of a Hot-Plug output needs to be modified, the PES16T4 generates an SMBus transaction to the I/O expander with the new value of all of the outputs. Whenever a Hot-Plug input changes, the I/O expander generates an interrupt which is received on the IOEXPINTN input pin (alternate function of GPIO) of the PES16T4. In response to an I/O expander interrupt, the PES16T4 generates an SMBus transaction to read the state of all of the Hot-Plug inputs from the I/O expander.

General Purpose Input/Output

The PES16T4 provides 11 General Purpose Input/Output (GPIO) pins that may be used by the system designer as bit I/O ports. Each GPIO pin may be configured independently as an input or output through software control. Some GPIO pins are shared with other on-chip functions. These alternate functions may be enabled via software, SMBus slave interface, or serial configuration EEPROM.

The PES16T4 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCI Express Base specification Revision 1.1. The PES16T4 can operate either as a store and forward or cut-through switch and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management to enable efficient switching and I/O connectivity for servers, storage, and embedded applications.

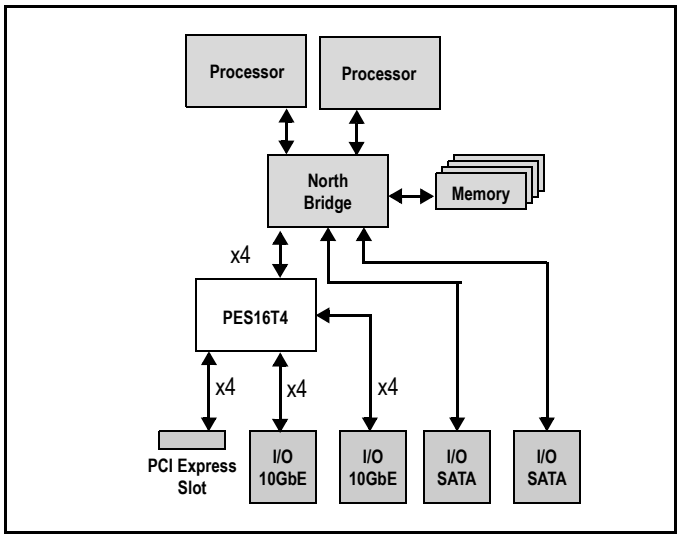

Figure 3 I/O Expansion Application

Pin Description

The following tables list the functions of the pins provided on the PES16T4. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an "N" are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

Note: In the PES16T4, the three downstream ports are labeled port 1, port 6, and port 7.

Signal	Type	Name/Description
PE0RP[3:0] PE0RN[3:0]	I	**PCI Express Port 0 Serial Data Receive.** Differential PCI Express receive pairs for port 0. Port 0 is the upstream port.
PE0TP[3:0] PE0TN[3:0]	O	**PCI Express Port 0 Serial Data Transmit.** Differential PCI Express transmit pairs for port 0. Port 0 is the upstream port.
PE1RP[3:0] PE1RN[3:0]	I	**PCI Express Port 1 Serial Data Receive.** Differential PCI Express receive pairs for port 1. When port 0 is merged with port 1, these signals become port 0 receive pairs for lanes 4 through 7.
PE1TP[3:0] PE1TN[3:0]	O	**PCI Express Port 1 Serial Data Transmit.** Differential PCI Express transmit pairs for port 1. When port 0 is merged with port 1, these signals become port 0 transmit pairs for lanes 4 through 7.
PE6RP[3:0] PE6RN[3:0]	I	**PCI Express Port 6 Serial Data Receive.** Differential PCI Express receive pairs for port 6.
PE6TP[3:0] PE6TN[3:0]	O	**PCI Express Port 6 Serial Data Transmit.** Differential PCI Express transmit pairs for port 6.
PE7RP[3:0] PE7RN[3:0]	I	**PCI Express Port 7 Serial Data Receive.** Differential PCI Express receive pairs for port 7. When port 6 is merged with port 7, these signals become port 6 receive pairs for lanes 4 through 7.
PE7TP[3:0] PE7TN[3:0]	O	**PCI Express Port 7 Serial Data Transmit.** Differential PCI Express transmit pairs for port 7. When port 6 is merged with port 7, these signals become port 6 transmit pairs for lanes 4 through 7.
P01MERGEN	I	**Port 0 and 1 Merge.** P01MERGEN is an active low signal. It is pulled low internally via a 251K ohm resistor. When this pin is low, port 0 is merged with port 1 to form a single x8 port. The Serdes lanes associated with port 1 become lanes 4 through 7 of port 0. When this pin is high, port 0 and port 1 are not merged, and each operates as a single x4 port.
P67MERGEN	I	**Port 6 and 7 Merge.** P67MERGEN is an active low signal. It is pulled low internally via a 251K ohm resistor. When this pin is low, port 6 is merged with port 7 to form a single x8 port. The Serdes lanes associated with port 7 become lanes 4 through 7 of port 6. When this pin is high, port 6 and port 7 are not merged, and each operates as a single x4 port.
PEREFCLKP[2:1] PEREFCLKN[2:1]	I	**PCI Express Reference Clock.** Differential reference clock pair input. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic and on-chip SerDes. The frequency of the differential reference clock is determined by the REFCLKM signal.
REFCLKM	I	**PCI Express Reference Clock Mode Select.** This signal selects the frequency of the reference clock input. 0x0 - 100 MHz 0x1 - 125 MHz

Table 2 PCI Express Interface Pins

Signal	Type	Name/Description
MSMBADDR[4:1]	I	**Master SMBus Address.** These pins determine the SMBus address of the serial EEPROM from which configuration information is loaded.
MSMBCLK	I/O	**Master SMBus Clock.** This bidirectional signal is used to synchronize transfers on the master SMBus. It is active and generating the clock only when the EEPROM or I/O Expanders are being accessed.
MSMBDAT	I/O	**Master SMBus Data.** This bidirectional signal is used for data on the master SMBus.
SSMBADDR[5,3:1]	I	**Slave SMBus Address.** These pins determine the SMBus address to which the slave SMBus interface responds.
SSMBCLK	I/O	**Slave SMBus Clock.** This bidirectional signal is used to synchronize transfers on the slave SMBus.
SSMBDAT	I/O	**Slave SMBus Data.** This bidirectional signal is used for data on the slave SMBus.

Table 3 SMBus Interface Pins

Signal	Type	Name/Description
GPIO[0]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[1]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[2]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[3]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[4]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN2 Alternate function pin type: Input Alternate function: I/O Expander interrupt 2 input
GPIO[5]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN3 Alternate function pin type: Input Alternate function: I/O Expander interrupt 3 input
GPIO[6]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin.
GPIO[7]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: GPEN Alternate function pin type: Output Alternate function: General Purpose Event (GPE) output

Table 4 General Purpose I/O Pins (Part 1 of 2)

Signal	Type	Name/Description
GPIO[8]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P1RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 1
GPIO[11]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P6RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 6
GPIO[12]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: P7RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 7

Table 4 General Purpose I/O Pins (Part 2 of 2)

Signal	Type	Name/Description
CCLKDS	I	**Common Clock Downstream.** When the CCLKDS pin is asserted, it indicates that a common clock is being used between the downstream device and the downstream port.
CCLKUS	I	**Common Clock Upstream.** When the CCLKUS pin is asserted, it indicates that a common clock is being used between the upstream device and the upstream port.
MSMBSMODE	I	**Master SMBus Slow Mode.** The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 KHz. This value may not be overridden.
PERSTN	I	**Fundamental Reset.** Assertion of this signal resets all logic inside PES16T4 and initiates a PCI Express fundamental reset.
RSTHALT	I	**Reset Halt.** When this signal is asserted during a PCI Express fundamental reset, PES16T4 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the SWCTL register by an SMBus master.
SWMODE[2:0]	I	**Switch Mode.** These configuration pins determine the PES16T4 switch operating mode. These pins should be static and not change after the negation of PERSTN. 0x0 - Normal switch mode 0x1 - Normal switch mode with Serial EEPROM initialization 0x2 - through 0xF Reserved

Table 5 System Pins

Signal	Type	Name/Description
JTAG_TCK	I	**JTAG Clock**. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller. JTAG_TCK is independent of the system clock with a nominal 50% duty cycle.
JTAG_TDI	I	**JTAG Data Input**. This is the serial data input to the boundary scan logic or JTAG Controller.
JTAG_TDO	O	**JTAG Data Output**. This is the serial data shifted out from the boundary scan logic or JTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TMS	I	**JTAG Mode**. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller.
JTAG_TRST_N	I	**JTAG Reset**. This active low signal asynchronously resets the boundary scan logic and JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board

Table 6 Test Pins

Signal	Type	Name/Description
V_{DD}CORE	I	**Core V_{DD}.** Power supply for core logic.
V_{DD}IO	I	**I/O V_{DD}.** LVTTL I/O buffer power supply.
V_{DD}PE	I	**PCI Express Digital Power.** PCI Express digital power used by the digital power of the SerDes.
V_{DD}APE	I	**PCI Express Analog Power.** PCI Express analog power used by the PLL and bias generator.
V_{TT}PE	I	**PCI Express Termination Power.**
V_{SS}	I	**Ground.**

Table 7 Power and Ground Pins

Pin Characteristics

Note: Some input pads of the PES16T4 do not contain internal pull-ups or pull-downs. Unused inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs which, if left floating, could adversely affect operation. Also, any input pin left floating can cause a slight increase in power consumption.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
PCI Express Interface	PE0RN[3:0]	I	CML	Serial Link		
	PE0RP[3:0]	I				
	PE0TN[3:0]	O				
	PE0TP[3:0]	O				
	PE1RN[3:0]	I				
	PE1RP[3:0]	I				
	PE1TN[3:0]	O				
	PE1TP[3:0]	O				
	PE6RN[3:0]	I				
	PE6RP[3:0]	I				
	PE6TN[3:0]	O				
	PE6TP[3:0]	O				
	PE7RN[3:0]	I				
	PE7RP[3:0]	I				
	PE7TN[3:0]	O				
	PE7TP[3:0]	O				
	PEREFCLKN[2:1]	I	LVPECL/ CML	Diff. Clock Input		Refer to Table 9
	PEREFCLKP[2:1]	I				
	REFCLKM	I	LVTTL	Input	pull-down	
SMBus	MSMBADDR[4:1]	I	LVTTL	Input	pull-up	
	MSMBCLK	I/O		STI[2]		pull-up on board
	MSMBDAT	I/O		STI		pull-up on board
	SSMBADDR[5,3:1]	I		Input	pull-up	
	SSMBCLK	I/O		STI		pull-up on board
	SSMBDAT	I/O		STI		pull-up on board
General Purpose I/O	GPIO[12,11,8:0]	I/O	LVTTL	High Drive	pull-up	
System Pins	CCLKDS	I	LVTTL	Input	pull-up	
	CCLKUS	I			pull-up	
	MSMBSMODE	I			pull-down	
	PERSTN	I				
	P01MERGEN	I			pull-down	
	P67MERGEN	I			pull-down	
	RSTHALT	I			pull-down	
	SWMODE[2:0]	I			pull-down	

Table 8 Pin Characteristics (Part 1 of 2)

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
EJTAG / JTAG	JTAG_TCK	I	LVTTL	STI	pull-up	
	JTAG_TDI	I		STI	pull-up	
	JTAG_TDO	O				
	JTAG_TMS	I		STI	pull-up	
	JTAG_TRST_N	I		STI	pull-up	External pull-down

Table 8 Pin Characteristics (Part 2 of 2)

1. Internal resistor values under typical operating conditions are 54K Ω for pull-up and 251K Ω for pull-down.
2. Schmitt Trigger Input (STI).

Logic Diagram — PES16T4

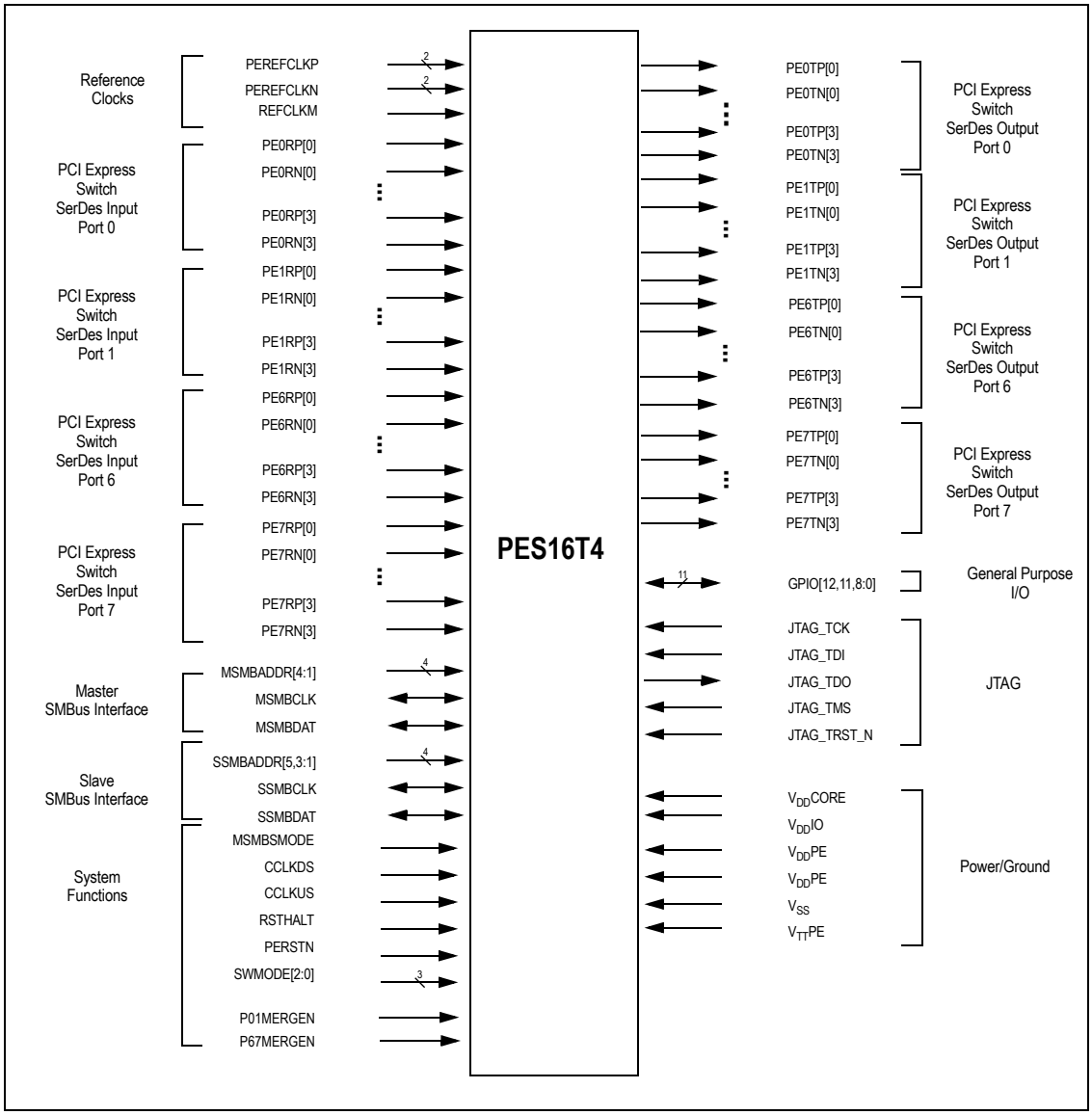

Figure 4 PES16T4 Logic Diagram

System Clock Parameters

Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 13 and 14.

Parameter	Description	Min	Typical	Max	Unit
$Refclk_{FREQ}$	Input reference clock frequency range	100		125[1]	MHz
$Refclk_{DC}$[2]	Duty cycle of input clock	40	50	60	%
T_R, T_F	Rise/Fall time of input clocks			0.2*RCUI	RCUI[3]
V_{SW}	Differential input voltage swing[4]	0.6		1.6	V
T_{jitter}	Input clock jitter (cycle-to-cycle)			125	ps
R_T	Termination Resistor		110		Ohms

Table 9 Input Clock Requirements

1. The input clock frequency will be either 100 or 125 MHz depending on signal REFCLKM.
2. ClkIn must be AC coupled. Use 0.01 — 0.1 µF ceramic capacitors.
3. RCUI (Reference Clock Unit Interval) refers to the reference clock period.
4. AC coupling required.

AC Timing Characteristics

Parameter	Description	Min[1]	Typical[1]	Max[1]	Units
PCIe Transmit					
UI	Unit Interval	399.88	400	400.12	ps
T_{TX-EYE}	Minimum Tx Eye Width	0.7	.9		UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median			0.15	UI
$T_{TX-RISE}$, $T_{TX-FALL}$	D+ / D- Tx output rise/fall time	50	90		ps
$T_{TX- IDLE-MIN}$	Minimum time in idle	50			UI
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Idle after sending an Idle ordered set			20	UI
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition from valid idle to diff data			20	UI
$T_{TX-SKEW}$	Transmitter data skew between any 2 lanes		500	1300	ps
PCIe Receive					
UI	Unit Interval	399.88	400	400.12	ps
T_{RX-EYE} (with jitter)	Minimum Receiver Eye Width (jitter tolerance)	0.4			UI
$T_{RX-EYE-MEDIUM TO MAX JITTER}$	Max time between jitter median & max deviation			0.3	UI
$T_{RX-IDLE-DET-DIFF-ENTER TIME}$	Unexpected Idle Enter Detect Threshold Integration Time			10	ms
$T_{RX-SKEW}$	Lane to lane input skew			20	ns

Table 10 PCIe AC Timing Characteristics

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 1.1

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
GPIO						
GPIO[10:0][1]	Tpw[2]	None	50	—	ns	

Table 11 GPIO AC Timing Characteristics

1. GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.

2. The values for this symbol were determined by calculation, not by testing.

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
JTAG						
JTAG_TCK	Tper_16a	none	50.0	—	ns	See Figure 5.
	Thigh_16a, Tlow_16a		10.0	25.0	ns	
JTAG_TMS[1], JTAG_TDI	Tsu_16b	JTAG_TCK rising	2.4	—	ns	
	Thld_16b		1.0	—	ns	
JTAG_TDO	Tdo_16c	JTAG_TCK falling	—	20	ns	
	Tdz_16c[2]		—	20	ns	
JTAG_TRST_N	Tpw_16d[2]	none	25.0	—	ns	

Table 12 JTAG AC Timing Characteristics

1. The JTAG specification, IEEE 1149.1, recommends that JTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when JTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

2. The values for this symbol were determined by calculation, not by testing.

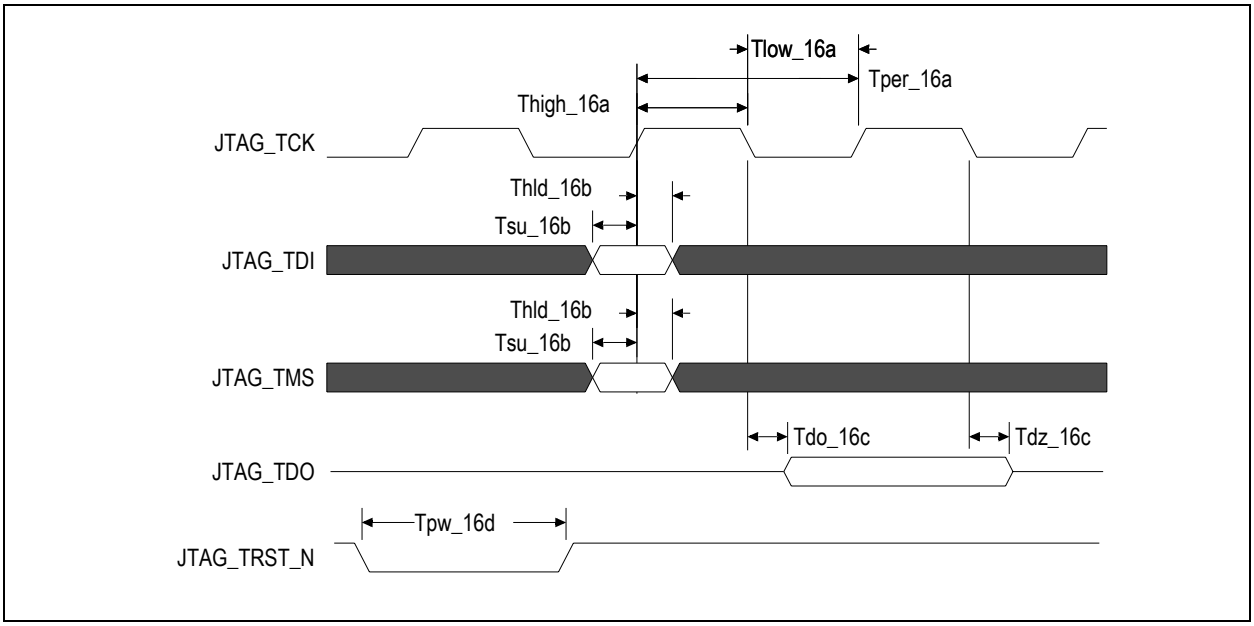

Figure 5 JTAG AC Timing Waveform

Recommended Operating Supply Voltages

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DD}CORE	Internal logic supply	0.9	1.0	1.1	V
V_{DD}I/O	I/O supply except for SerDes LVPECL/CML	3.0	3.3	3.6	V
V_{DD}PE	PCI Express Digital Power	0.9	1.0	1.1	V
V_{DD}APE	PCI Express Analog Power	0.9	1.0	1.1	V
V_{TT}PE	PCI Express Serial Data Transmit Termination Voltage	1.425	1.5	1.575	V
V_{SS}	Common ground	0	0	0	V

Table 13 PES16T4 Operating Voltages

Power-Up Sequence

This section describes the sequence in which various voltages must be applied to the part during power-up to ensure proper functionality. For the PES16T4, the power-up sequence must be as follows:

1. V_{DD}I/O — 3.3V
2. V_{DD}Core, V_{DD}PE, V_{DD}APE — 1.0V
3. V_{TT}PE — 1.5V

When powering up, each voltage level must ramp and stabilize prior to applying the next voltage in the sequence to ensure internal latch-up issues are avoided. There are no maximum time limitations in ramping to valid power levels. The power-down sequence must be in the reverse order of the power-up sequence.

Recommended Operating Temperature

Grade	Temperature
Commercial	0°C to +70°C Ambient

Table 14 PES16T4 Operating Temperatures

Power Consumption

Typical power is measured under the following conditions: 25°C Ambient, 35% total link usage on all ports, typical voltages defined in Table 13 (and also listed below).

Maximum power is measured under the following conditions: 70°C Ambient, 85% total link usage on all ports, maximum voltages defined in Table 13 (and also listed below).

Number of active Lanes per Port		Core Supply		PCIe Digital Supply		PCIe Analog Supply		PCIe Termination Supply		I/O Supply		Total	
		Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 1.5V	Max 1.575V	Typ 3.3V	Max 3.6V	Typ Power	Max Power
4/4/4/4	mA	598	756	730	873	308	342	371	436	1	1	2.2W	2.9W
	Watts	0.6	0.83	0.73	0.96	0.31	0.38	0.56	0.69	0.004	0.004		
4/4/1/1	mA	528	642	548	631	279	298	220	270	1	1	1.69W	2.2W
	Watts	0.53	0.71	0.55	0.69	0.28	0.33	0.33	0.43	0.003	0.003		

Table 15 PES16T4 Power Consumption

Thermal Considerations

This section describes thermal considerations for the PES16T4 (23mm^2 BCG484 package). The data in Table 16 below contains information that is relevant to the thermal performance of the PES16T4 switch.

Symbol	Parameter	Value	Units	Conditions
$T_{J(max)}$	Junction Temperature	125	°C	Maximum
$T_{A(max)}$	Ambient Temperature	70	°C	Maximum for commercial-rated products
$\theta_{JA(effective)}$	Effective Thermal Resistance, Junction-to-Ambient	11.5	°C/W	Zero air flow
		9.6	°C/W	1 m/S air flow
		9.0	°C/W	2 m/S air flow
θ_{JB}	Thermal Resistance, Junction-to-Board	10.9	°C/W	
θ_{JC}	Thermal Resistance, Junction-to-Case	5	°C/W	
P	Power Dissipation of the Device	2.9	Watts	Maximum

Table 16 Thermal Specifications for PES16T4, 23x23mm BCG484 Package

Note: The parameter $\theta_{JA(eff)}$ is not the *absolute* thermal resistance for the package as defined by JEDEC (JESD-51). Because resistance can vary with the number of board layers, size of the board, and airflow, $\theta_{JA(eff)}$ is the *effective* thermal resistance. The values for effective θ_{JA} given above are based on a 10-layer, standard height, full length (4.3"x12.2") PCIe add-in card.

Heat Sink

Table 17 lists heat sink requirements for the PES16T4 under three common usage scenarios. As shown in this table, a heat sink is not required in most cases.

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Air Flow	Board Size	Board Layers	Heat Sink Requirement
Zero	3.9"x6.2" (ExpressModule form factor) or larger	6 or more	No heat sink required
Zero	Any	10 or more	No heat sink required
1 m/S or more	Any	Any	No heat sink required

Table 17 Heat Sink Requirements Based on Air Flow and Board Characteristics

Thermal Usage Examples

The junction-to-ambient thermal resistance is a measure of a device's ability to dissipate heat from the die to its surroundings in the absence of a heat sink. The general formula to determine θ_{JA} is:

$$\theta_{JA} = (T_J - T_A)/P$$

Thermal reliability of a device is generally assured when the actual value of T_J in the specific system environment being considered is less than the maximum T_J specified for the device. Using an ambient temperature of 70°C and assuming a system with 1m/S airflow, the actual value of T_J is:

$$T_{J(actual)} = T_A + P * \theta_{JA(eff)} = 70^oC + 2.9W * 9.6W/^oC = 98^oC$$

The actual T_J of 98°C is well below the maximum T_J of 125°C specified for the device (shown in Table 16). Therefore, no heat sink is needed in this scenario. The formula is also useful from a system design perspective. It can be used to determine if a heat sink should be added to the device based on some desired value of T_J. For example, if for reliability purposes the desired T_J is 100°C, then the maximum allowable T_A is:

$$T_{A(allowed)} = T_{J(desired)} - (P * \theta_{JA(effective)})$$
$$T_{A(allowed)} = 100^oC - (2.9W * 9.6W/^oC) = 100^oC - 28^oC = 72^oC$$

An appropriate level of increased air flow and/or a heat sink can be added to achieve this lower ambient temperature. Please contact ssdhelp@idt.com for further assistance.

DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 13.

Note: See Table 8, Pin Characteristics, for a complete I/O listing.

I/O Type	Parameter	Description	Min[1]	Typ[1]	Max[1]	Unit	Conditions
Serial Link	**PCIe Transmit**						
	$V_{TX-DIFFp-p}$	Differential peak-to-peak output voltage	800		1200	mV	
	$V_{TX-DE-RATIO}$	De-emphasized differential output voltage	-3		-4	dB	
	$V_{TX-DC-CM}$	DC Common mode voltage	-0.1	1	3.7	V	
	$V_{TX-CM-ACP}$	RMS AC peak common mode output voltage			20	mV	
	$V_{TX-CM-DC-active-idle-delta}$	Abs delta of DC common mode voltage between L0 and idle			100	mV	
	$V_{TX-CM-DC-line-delta}$	Abs delta of DC common mode voltage between D+ and D-			25	mV	
	$V_{TX-Idle-DiffP}$	Electrical idle diff peak output			20	mV	
	$V_{TX-RCV-Detect}$	Voltage change during receiver detection			600	mV	
	$RL_{TX-DIFF}$	Transmitter Differential Return loss	12			dB	
	RL_{TX-CM}	Transmitter Common Mode Return loss	6			dB	
	$Z_{TX-DEFF-DC}$	DC Differential TX impedance	80	100	120	Ω	
	Z_{OSE}	Single ended TX Impedance	40	50	60	Ω	
	Transmitter Eye Diagram	TX Eye Height (De-emphasized bits)	505	650		mV	
	Transmitter Eye Diagram	TX Eye Height (Transition bits)	800	950		mV	
Serial Link (cont.)	**PCIe Receive**						
	$V_{RX-DIFFp-p}$	Differential input voltage (peak-to-peak)	175		1200	mV	
	$V_{RX-CM-AC}$	Receiver common-mode voltage for AC coupling			150	mV	
	$RL_{RX-DIFF}$	Receiver Differential Return Loss	15			dB	
	RL_{RX-CM}	Receiver Common Mode Return Loss	6			dB	
	$Z_{RX-DIFF-DC}$	Differential input impedance (DC)	80	100	120	Ω	
	$Z_{RX-COMM-DC}$	Single-ended input impedance	40	50	60	Ω	
	$Z_{RX-COMM-HIGH-Z-DC}$	Powered down input common mode impedance (DC)	200k	350k		Ω	
	$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65		175	mV	
PCIe REFCLK							
	C_{IN}	Input Capacitance	1.5	—		pF	

Table 18 DC Electrical Characteristics (Part 1 of 2)

I/O Type	Parameter	Description	Min[1]	Typ[1]	Max[1]	Unit	Conditions
Other I/Os							
LOW Drive Output	I_{OL}		—	2.5	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-5.5	—	mA	V_{OH} = 1.5V
High Drive Output	I_{OL}		—	12.0	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-20.0	—	mA	V_{OH} = 1.5V
Schmitt Trigger Input (STI)	V_{IL}		-0.3	—	0.8	V	—
	V_{IH}		2.0	—	$V_{DD}IO$ + 0.5	V	—
Input	V_{IL}		-0.3	—	0.8	V	—
	V_{IH}		2.0	—	$V_{DD}IO$ + 0.5	V	—
Capacitance	C_{IN}		—	—	8.5	pF	—
Leakage	Inputs		—	—	± 10	µA	$V_{DD}I/O$ (max)
	$I/O_{LEAK\ W/O}$ Pull-ups/downs		—	—	± 10	µA	$V_{DD}I/O$ (max)
	$I/O_{LEAK\ WITH}$ Pull-ups/downs		—	—	± 80	µA	$V_{DD}I/O$ (max)

Table 18 DC Electrical Characteristics (Part 2 of 2)

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 1.1.

Package Pinout — 484-BGA Signal Pinout for PES16T4

The following table lists the pin numbers and signal names for the PES16T4 device.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
A1	V_{SS}		B13	V_{SS}		D3	SSMBCLK		E15	V_{DD}PE	
A2	V_{SS}		B14	PE0TP02		D4	V_{SS}		E16	V_{DD}PE	
A3	V_{SS}		B15	V_{SS}		D5	PE1RP03		E17	V_{SS}	
A4	PE1TN03		B16	PE0TP01		D6	V_{SS}		E18	V_{DD}APE	
A5	V_{SS}		B17	V_{SS}		D7	PE1RP02		E19	V_{SS}	
A6	PE1TP02		B18	PE0TP00		D8	V_{SS}		E20	SWMODE_0	
A7	V_{SS}		B19	V_{SS}		D9	PE1RN01		E21	SWMODE_1	
A8	PE1TN01		B20	V_{SS}		D10	V_{SS}		E22	V_{DD}CORE	
A9	V_{SS}		B21	V_{SS}		D11	PE1RP00		F1	V_{SS}	
A10	PE1TP00		B22	V_{SS}		D12	V_{SS}		F2	V_{DD}IO	
A11	V_{SS}		C1	V_{DD}CORE		D13	PE0RP03		F3	V_{DD}IO	
A12	PE0TN03		C2	SSMBADDR_3		D14	V_{SS}		F4	V_{SS}	
A13	V_{SS}		C3	SSMBDAT		D15	PE0RN02		F5	V_{DD}CORE	
A14	PE0TN02		C4	V_{SS}		D16	V_{TT}PE		F6	V_{DD}IO	
A15	V_{SS}		C5	PE1RN03		D17	PE0RP01		F7	V_{SS}	
A16	PE0TN01		C6	V_{SS}		D18	V_{SS}		F8	V_{DD}PE	
A17	V_{SS}		C7	PE1RN02		D19	PE0RN00		F9	V_{DD}APE	
A18	PE0TN00		C8	V_{SS}		D20	V_{SS}		F10	V_{DD}CORE	
A19	V_{SS}		C9	PE1RP01		D21	V_{DD}IO		F11	V_{DD}PE	
A20	V_{SS}		C10	V_{SS}		D22	V_{SS}		F12	V_{DD}IO	
A21	V_{SS}		C11	PE1RN00		E1	V_{DD}CORE		F13	V_{DD}PE	
A22	V_{SS}		C12	V_{SS}		E2	SSMBADDR_1		F14	V_{DD}CORE	
B1	V_{SS}		C13	PE0RN03		E3	SSMBADDR_5		F15	V_{DD}APE	
B2	V_{DD}IO		C14	V_{SS}		E4	CCLKUS		F16	V_{DD}CORE	
B3	V_{SS}		C15	PE0RP02		E5	V_{SS}		F17	V_{DD}IO	
B4	PE1TP03		C16	V_{SS}		E6	V_{DD}PE		F18	CCLKDS	
B5	V_{SS}		C17	PE0RN01		E7	V_{TT}PE		F19	RSTHALT	
B6	PE1TN02		C18	V_{SS}		E8	V_{SS}		F20	PERSTN	
B7	V_{SS}		C19	PE0RP00		E9	V_{DD}APE		F21	SWMODE_2	
B8	PE1TP01		C20	V_{SS}		E10	V_{TT}PE		F22	V_{SS}	
B9	V_{SS}		C21	V_{DD}APE		E11	V_{DD}PE		G1	V_{DD}CORE	
B10	PE1TN00		C22	V_{DD}CORE		E12	V_{DD}PE		G2	MSMBADDR_4	
B11	V_{SS}		D1	V_{SS}		E13	V_{TT}PE		G3	MSMBCLK	
B12	PE0TP03		D2	SSMBADDR_2		E14	V_{DD}APE		G4	MSMBDAT	

Table 19 PES16T4 484-pin Signal Pin-Out (Part 1 of 4)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
G5	V_{SS}		H20	GPIO_00		K13	V_{DD}CORE		M6	V_{SS}	
G6	V_{DD}CORE		H21	GPIO_01		K14	V_{SS}		M7	V_{DD}CORE	
G7	V_{SS}		H22	V_{SS}		K15	V_{DD}CORE		M8	V_{SS}	
G8	V_{SS}		J1	V_{DD}CORE		K16	V_{SS}		M9	V_{DD}CORE	
G9	V_{SS}		J2	JTAG_TDO		K17	V_{DD}CORE		M10	V_{SS}	
G10	V_{DD}CORE		J3	JTAG_TMS		K18	V_{SS}		M11	V_{DD}CORE	
G11	V_{SS}		J4	JTAG_TRST_N		K19	GPIO_07	1	M12	V_{SS}	
G12	V_{SS}		J5	V_{SS}		K20	GPIO_06		M13	V_{DD}CORE	
G13	V_{DD}CORE		J6	V_{SS}		K21	GPIO_05	1	M14	V_{SS}	
G14	V_{SS}		J7	V_{SS}		K22	V_{SS}		M15	V_{DD}CORE	
G15	V_{SS}		J8	V_{DD}CORE		L1	V_{DD}CORE		M16	V_{SS}	
G16	V_{SS}		J9	V_{SS}		L2	V_{DD}CORE		M17	V_{DD}CORE	
G17	V_{SS}		J10	V_{DD}CORE		L3	V_{SS}		M18	V_{SS}	
G18	V_{DD}APE		J11	V_{SS}		L4	V_{DD}CORE		M19	V_{SS}	
G19	V_{SS}		J12	V_{DD}CORE		L5	V_{SS}		M20	V_{DD}IO	
G20	V_{DD}APE		J13	V_{SS}		L6	V_{DD}CORE		M21	V_{SS}	
G21	V_{DD}IO		J14	V_{SS}		L7	V_{SS}		M22	V_{SS}	
G22	V_{DD}CORE		J15	V_{SS}		L8	V_{DD}CORE		N1	PEREFCLKP1	
H1	V_{SS}		J16	V_{SS}		L9	V_{SS}		N2	V_{SS}	
H2	MSMBADDR_1		J17	V_{DD}IO		L10	V_{DD}CORE		N3	V_{DD}CORE	
H3	MSMBADDR_2		J18	V_{DD}CORE		L11	V_{SS}		N4	V_{DD}CORE	
H4	MSMBADDR_3		J19	GPIO_04	1	L12	V_{DD}CORE		N5	V_{SS}	
H5	V_{DD}CORE		J20	GPIO_03		L13	V_{SS}		N6	V_{DD}APE	
H6	V_{SS}		J21	GPIO_02		L14	V_{DD}CORE		N7	V_{SS}	
H7	V_{DD}CORE		J22	V_{DD}CORE		L15	V_{SS}		N8	V_{DD}CORE	
H8	V_{SS}		K1	V_{SS}		L16	V_{SS}		N9	V_{SS}	
H9	V_{DD}CORE		K2	V_{DD}IO		L17	V_{SS}		N10	V_{DD}CORE	
H10	V_{SS}		K3	JTAG_TDI		L18	V_{DD}CORE		N11	V_{SS}	
H11	V_{DD}CORE		K4	JTAG_TCK		L19	V_{SS}		N12	V_{DD}CORE	
H12	V_{SS}		K5	V_{DD}CORE		L20	V_{SS}		N13	V_{SS}	
H13	V_{DD}CORE		K6	V_{SS}		L21	V_{DD}IO		N14	V_{DD}CORE	
H14	V_{SS}		K7	V_{DD}CORE		L22	V_{DD}CORE		N15	V_{SS}	
H15	V_{DD}CORE		K8	V_{SS}		M1	V_{SS}		N16	V_{SS}	
H16	V_{SS}		K9	V_{DD}CORE		M2	V_{SS}		N17	V_{DD}APE	
H17	V_{DD}CORE		K10	V_{SS}		M3	V_{SS}		N18	V_{DD}CORE	
H18	V_{SS}		K11	V_{DD}CORE		M4	V_{SS}		N19	V_{DD}CORE	
H19	V_{SS}		K12	V_{SS}		M5	V_{DD}CORE		N20	V_{DD}CORE	

Table 19 PES16T4 484-pin Signal Pin-Out (Part 2 of 4)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
N21	V_{SS}		R14	V_{DD}CORE		U7	V_{DD}IO		V22	V_{DD}CORE	
N22	PEREFCLKN2		R15	V_{SS}		U8	V_{DD}PE		W1	V_{SS}	
P1	PEREFCLKN1		R16	V_{SS}		U9	V_{DD}APE		W2	V_{DD}CORE	
P2	V_{SS}		R17	V_{DD}IO		U10	V_{DD}PE		W3	V_{SS}	
P3	V_{SS}		R18	V_{DD}CORE		U11	V_{SS}		W4	V_{SS}	
P4	V_{SS}		R19	GPIO_08	1	U12	V_{DD}IO		W5	PE6RP00	
P5	V_{SS}		R20	GPIO_11	1	U13	V_{DD}PE		W6	V_{SS}	
P6	V_{SS}		R21	GPIO_12	1	U14	V_{DD}APE		W7	PE6RP01	
P7	V_{DD}CORE		R22	V_{SS}		U15	V_{SS}		W8	V_{SS}	
P8	V_{SS}		T1	V_{DD}CORE		U16	V_{DD}IO		W9	PE6RN02	
P9	V_{DD}CORE		T2	V_{SS}		U17	V_{SS}		W10	V_{SS}	
P10	V_{SS}		T3	V_{SS}		U18	V_{DD}APE		W11	PE6RP03	
P11	V_{DD}CORE		T4	V_{SS}		U19	REFCLKM		W12	V_{SS}	
P12	V_{SS}		T5	V_{SS}		U20	MSMBSMODE		W13	PE7RP00	
P13	V_{DD}CORE		T6	V_{DD}IO		U21	V_{SS}		W14	V_{SS}	
P14	V_{SS}		T7	V_{DD}CORE		U22	V_{SS}		W15	PE7RN01	
P15	V_{DD}CORE		T8	V_{SS}		V1	V_{DD}CORE		W16	V_{TT}PE	
P16	V_{SS}		T9	V_{SS}		V2	V_{SS}		W17	PE7RP02	
P17	V_{DD}CORE		T10	V_{DD}CORE		V3	V_{DD}CORE		W18	V_{SS}	
P18	V_{SS}		T11	V_{SS}		V4	V_{SS}		W19	PE7RN03	
P19	V_{SS}		T12	V_{SS}		V5	V_{SS}		W20	V_{SS}	
P20	V_{SS}		T13	V_{DD}CORE		V6	V_{DD}PE		W21	V_{DD}CORE	
P21	V_{SS}		T14	V_{SS}		V7	V_{TT}PE		W22	V_{SS}	
P22	PEREFCLKP2		T15	V_{SS}		V8	V_{SS}		Y1	V_{DD}CORE	
R1	V_{SS}		T16	V_{SS}		V9	V_{DD}APE		Y2	V_{SS}	
R2	V_{DD}APE		T17	V_{DD}CORE		V10	V_{TT}PE		Y3	V_{DD}CORE	
R3	P01MERGEN		T18	V_{SS}		V11	V_{DD}PE		Y4	V_{SS}	
R4	P67MERGEN		T19	V_{SS}		V12	V_{DD}PE		Y5	PE6RN00	
R5	V_{SS}		T20	V_{SS}		V13	V_{TT}PE		Y6	V_{SS}	
R6	V_{DD}IO		T21	V_{DD}APE		V14	V_{DD}APE		Y7	PE6RN01	
R7	V_{SS}		T22	V_{DD}CORE		V15	V_{DD}PE		Y8	V_{SS}	
R8	V_{DD}CORE		U1	V_{SS}		V16	V_{DD}PE		Y9	PE6RP02	
R9	V_{SS}		U2	V_{DD}CORE		V17	V_{SS}		Y10	V_{SS}	
R10	V_{DD}CORE		U3	V_{SS}		V18	V_{DD}APE		Y11	PE6RN03	
R11	V_{SS}		U4	V_{DD}APE		V19	V_{SS}		Y12	V_{SS}	
R12	V_{DD}CORE		U5	V_{SS}		V20	V_{SS}		Y13	PE7RN00	
R13	V_{SS}		U6	V_{DD}APE		V21	V_{SS}		Y14	V_{SS}	

Table 19 PES16T4 484-pin Signal Pin-Out (Part 3 of 4)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
Y15	PE7RP01		AA6	PE6TN01		AA19	V_{SS}		AB10	PE6TP03	
Y16	V_{SS}		AA7	V_{SS}		AA20	V_{SS}		AB11	V_{SS}	
Y17	PE7RN02		AA8	PE6TP02		AA21	V_{DD}CORE		AB12	PE7TN00	
Y18	V_{SS}		AA9	V_{SS}		AA22	V_{SS}		AB13	V_{SS}	
Y19	PE7RP03		AA10	PE6TN03		AB1	V_{SS}		AB14	PE7TN01	
Y20	V_{DD}CORE		AA11	V_{SS}		AB2	V_{SS}		AB15	V_{SS}	
Y21	V_{SS}		AA12	PE7TP00		AB3	V_{SS}		AB16	PE7TN02	
Y22	V_{DD}CORE		AA13	V_{SS}		AB4	PE6TN00		AB17	V_{SS}	
AA1	V_{SS}		AA14	PE7TP01		AB5	V_{SS}		AB18	PE7TN03	
AA2	V_{DD}CORE		AA15	V_{SS}		AB6	PE6TP01		AB19	V_{SS}	
AA3	V_{SS}		AA16	PE7TP02		AB7	V_{SS}		AB20	V_{SS}	
AA4	PE6TP00		AA17	V_{SS}		AB8	PE6TN02		AB21	V_{SS}	
AA5	V_{SS}		AA18	PE7TP03		AB9	V_{SS}		AB22	V_{SS}	

Table 19 PES16T4 484-pin Signal Pin-Out (Part 4 of 4)

Alternate Signal Functions

Pin	GPIO	Alternate
J19	GPIO_04	IOEXPINTN2
K21	GPIO_05	IOEXPINTN3
K19	GPIO_07	GPEN
R19	GPIO_08	P1RSTN
R20	GPIO_11	P6RSTN
R21	GPIO_12	P7RSTN

Table 20 PES16T4 Alternate Signal Functions

Power Pins

V_{DD}Core	V_{DD}Core	V_{DD}Core	V_{DD}Core	V_{DD}IO	V_{DD}PE	V_{DD}APE	V_{TT}PE
C1	J10	M7	R10	B2	E6	C21	D16
C22	J12	M9	R12	D21	E11	E9	E7
E1	J18	M11	R14	F2	E12	E14	E10
E22	J22	M13	R18	F3	E15	E18	E13
F5	K5	M15	T1	F6	E16	F9	V7
F10	K7	M17	T7	F12	F8	F15	V10
F14	K9	N3	T10	F17	F11	G18	V13
F16	K11	N4	T13	G21	F13	G20	W16
G1	K13	N8	T17	J17	U8	N6	
G6	K15	N10	T22	K2	U10	N17	
G10	K17	N12	U2	L21	U13	R2	
G13	L1	N14	V1	M20	V6	T21	
G22	L2	N18	V3	R6	V11	U4	
H5	L4	N19	V22	R17	V12	U6	
H7	L6	N20	W2	T6	V15	U9	
H9	L8	P7	W21	U7	V16	U14	
H11	L10	P9	Y1	U12		U18	
H13	L12	P11	Y3	U16		V9	
H15	L14	P13	Y20			V14	
H17	L18	P15	Y22			V18	
J1	L22	P17	AA2				
J8	M5	R8	AA21				

Table 21 PES16T4 Power Pins

Ground Pins

V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
A1	C16	H6	L15	P8	U3	Y16
A2	C18	H8	L16	P10	U5	Y18
A3	C20	H10	L17	P12	U11	Y21
A5	D1	H12	L19	P14	U15	AA1
A7	D4	H14	L20	P16	U17	AA3
A9	D6	H16	M1	P18	U21	AA5
A11	D8	H18	M2	P19	U22	AA7
A13	D10	H19	M3	P20	V2	AA9
A15	D12	H22	M4	P21	V4	AA11
A17	D14	J5	M6	R1	V5	AA13
A19	D18	J6	M8	R5	V8	AA15
A20	D20	J7	M10	R7	V17	AA17
A21	D22	J9	M12	R9	V19	AA19
A22	E5	J11	M14	R11	V20	AA20
B1	E8	J13	M16	R13	V21	AA22
B3	E17	J14	M18	R15	W1	AB1
B5	E19	J15	M19	R16	W3	AB2
B7	F1	J16	M21	R22	W4	AB3
B9	F4	K1	M22	T2	W6	AB5
B11	F7	K6	N2	T3	W8	AB7
B13	F22	K8	N5	T4	W10	AB9
B15	G5	K10	N7	T5	W12	AB11
B17	G7	K12	N9	T8	W14	AB13
B19	G8	K14	N11	T9	W18	AB15
B20	G9	K16	N13	T11	W20	AB17
B21	G11	K18	N15	T12	W22	AB19
B22	G12	K22	N16	T14	Y2	AB20
C4	G14	L3	N21	T15	Y4	AB21
C6	G15	L5	P2	T16	Y6	AB22
C8	G16	L7	P3	T18	Y8	
C10	G17	L9	P4	T19	Y10	
C12	G19	L11	P5	T20	Y12	
C14	H1	L13	P6	U1	Y14	

Table 22 PES16T4 Ground Pins

Signals Listed Alphabetically

Signal Name	I/O Type	Location	Signal Category
CCLKDS	I	F18	System
CCLKUS	I	E4	
GPIO_00	I/O	H20	General Purpose Input/Output
GPIO_01	I/O	H21	
GPIO_02	I/O	J21	
GPIO_03	I/O	J20	
GPIO_04	I/O	J19	
GPIO_05	I/O	K21	
GPIO_06	I/O	K20	
GPIO_07	I/O	K19	
GPIO_08	I/O	R19	
GPIO_11	I/O	R20	
GPIO_12	I/O	R21	
JTAG_TCK	I	K4	JTAG
JTAG_TDI	I	K3	
JTAG_TDO	O	J2	
JTAG_TMS	I	J3	
JTAG_TRST_N	I	J4	
MSMBADDR_1	I	H2	SMBus
MSMBADDR_2	I	H3	
MSMBADDR_3	I	H4	
MSMBADDR_4	I	G2	
MSMBCLK	I/O	G3	
MSMBDAT	I/O	G4	
MSMBSMODE	I	U20	System
P01MERGEN	I	R3	PCI Express
P67MERGEN	I	R4	
PE0RN00	I	D19	
PE0RN01	I	C17	
PE0RN02	I	D15	
PE0RN03	I	C13	
PE0RP00	I	C19	
PE0RP01	I	D17	
PE0RP02	I	C15	

Table 23 89PES16T4 Alphabetical Signal List (Part 1 of 4)

Signal Name	I/O Type	Location	Signal Category
PE0RP03	I	D13	PCI Express (Cont.)
PE0TN00	O	A18	
PE0TN01	O	A16	
PE0TN02	O	A14	
PE0TN03	O	A12	
PE0TP00	O	B18	
PE0TP01	O	B16	
PE0TP02	O	B14	
PE0TP03	O	B12	
PE1RN00	I	C11	
PE1RN01	I	D9	
PE1RN02	I	C7	
PE1RN03	I	C5	
PE1RP00	I	D11	
PE1RP01	I	C9	
PE1RP02	I	D7	
PE1RP03	I	D5	
PE1TN00	O	B10	
PE1TN01	O	A8	
PE1TN02	O	B6	
PE1TN03	O	A4	
PE1TP00	O	A10	
PE1TP01	O	B8	
PE1TP02	O	A6	
PE1TP03	O	B4	
PE6RN00	I	Y5	
PE6RN01	I	Y7	
PE6RN02	I	W9	
PE6RN03	I	Y11	
PE6RP00	I	W5	
PE6RP01	I	W7	
PE6RP02	I	Y9	
PE6RP03	I	W11	
PE6TN00	O	AB4	
PE6TN01	O	AA6	
PE6TN02	O	AB8	

Table 23 89PES16T4 Alphabetical Signal List (Part 2 of 4)

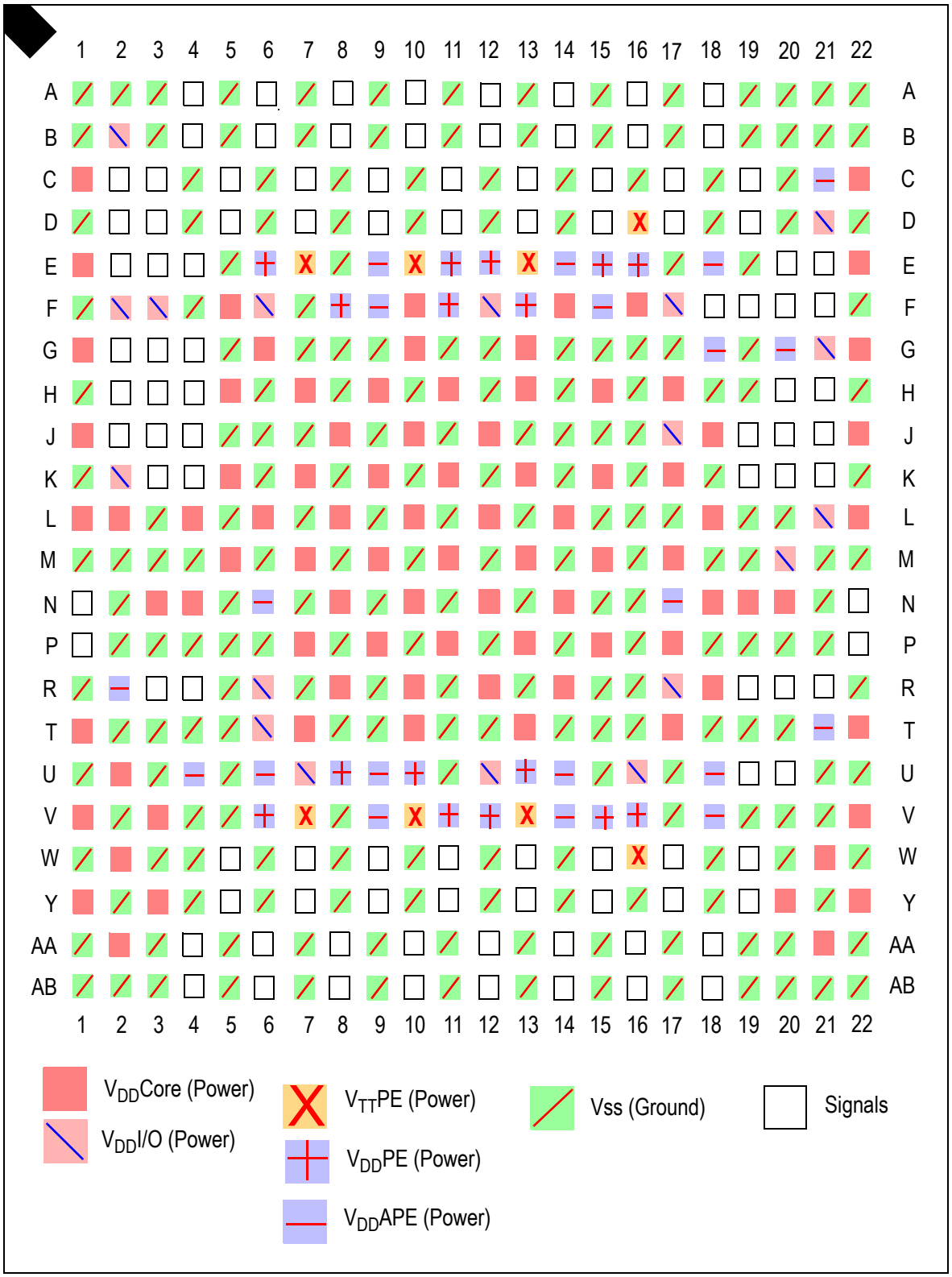
Signal Name	I/O Type	Location	Signal Category
PE6TN03	O	AA10	PCI Express (Cont.)
PE6TP00	O	AA4	
PE6TP01	O	AB6	
PE6TP02	O	AA8	
PE6TP03	O	AB10	
PE7RN00	I	Y13	
PE7RN01	I	W15	
PE7RN02	I	Y17	
PE7RN03	I	W19	
PE7RP00	I	W13	
PE7RP01	I	Y15	
PE7RP02	I	W17	
PE7RP03	I	Y19	
PE7TN00	O	AB12	
PE7TN01	O	AB14	
PE7TN02	O	AB16	
PE7TN03	O	AB18	
PE7TP00	O	AA12	
PE7TP01	O	AA14	
PE7TP02	O	AA16	
PE7TP03	O	AA18	
PEREFCLKN1	I	P1	
PEREFCLKN2	I	N22	
PEREFCLKP1	I	N1	
PEREFCLKP2	I	P22	
PERSTN	I	F20	System
REFCLKM	I	U19	PCI Express
RSTHALT	I	F19	System
SSMBADDR_1	I	E2	SMBus
SSMBADDR_2	I	D2	
SSMBADDR_3	I	C2	
SSMBADDR_5	I	E3	
SSMBCLK	I/O	D3	SMBus
SSMBDAT	I/O	C3	

Table 23 89PES16T4 Alphabetical Signal List (Part 3 of 4)

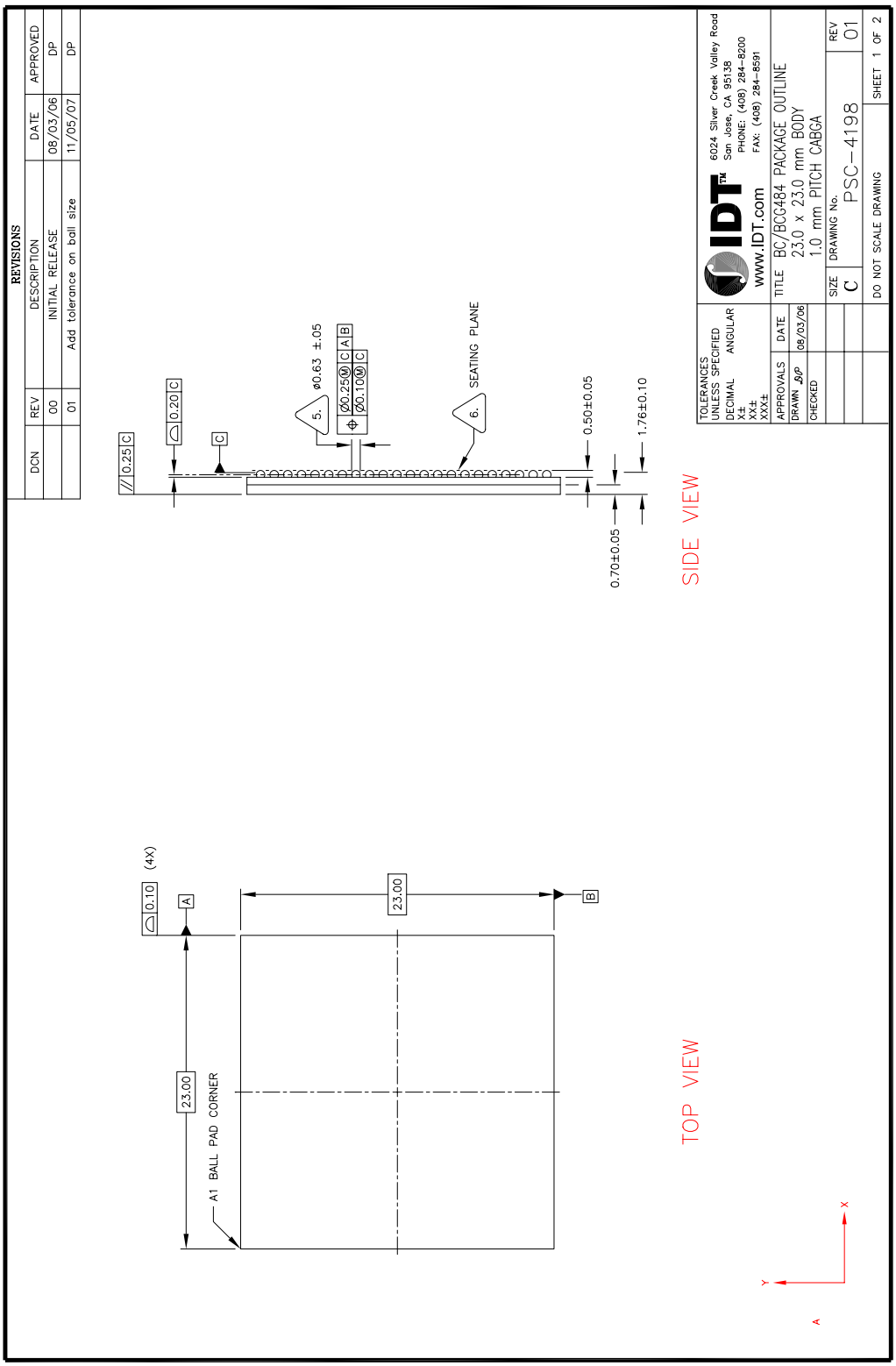
Signal Name	I/O Type	Location	Signal Category
SWMODE_0	I	E20	System
SWMODE_1	I	E21	
SWMODE_2	I	F21	
V_{DD}CORE, V_{DD}APE, V_{DD}IO, V_{DD}PE, V_{TT}PE	See Table 21 for a listing of power pins.		
V_{SS}	See Table 22 for a listing of ground pins.		

Table 23 89PES16T4 Alphabetical Signal List (Part 4 of 4)

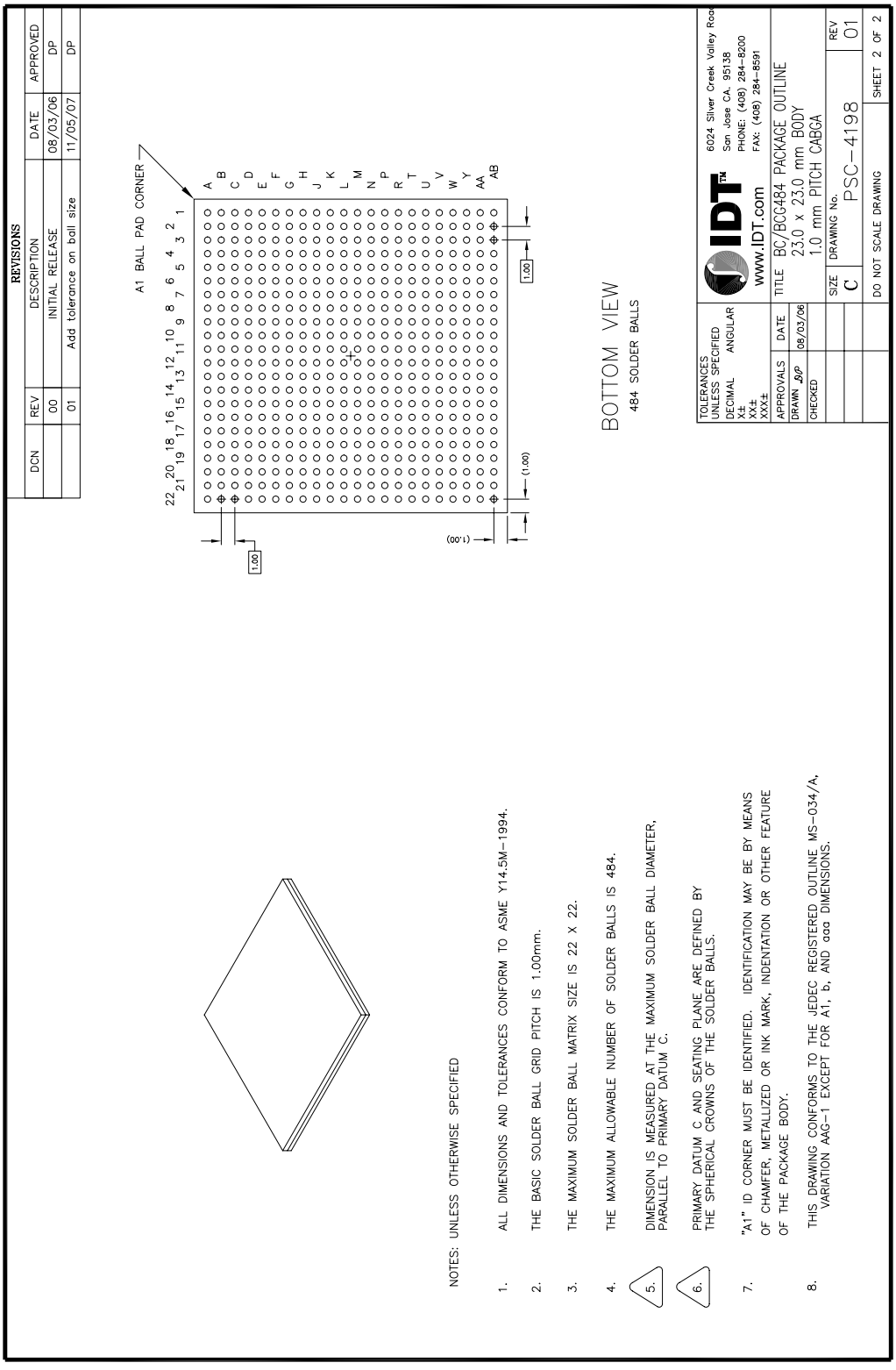
PES16T4 Pinout — Top View



PES16T4 Package Drawing — 484-Pin BC484/BCG484



PES16T4 Package Drawing — Page Two



Revision History

February 8, 2007: Initial publication.

April 4, 2007: In Table 3, revised description for MSMBCLK signal.

May 30, 2007: Changed device revision in Ordering Information from ZD to ZH.

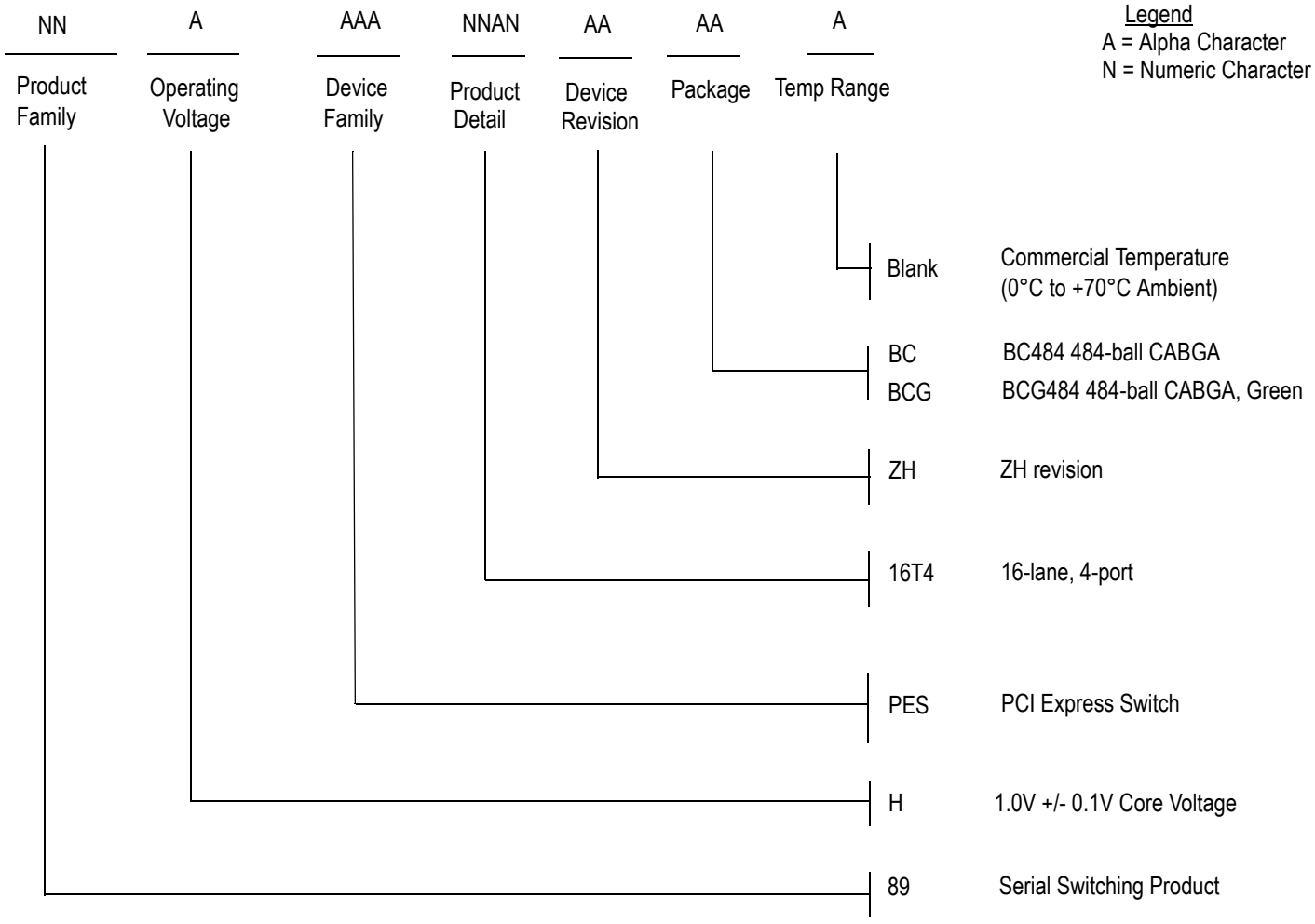
November 1, 2007: Changed package drawing to reflect correct ball/package dimensions.

November 6, 2007: Updated package drawing with solder ball tolerance added.

November 8, 2007: Added new parameter, Termination Resistor, to Table 9, Input Clock Requirements.

March 25, 2008: Added θ_{JB} and θ_{JC} parameters to Table 16, Thermal Specifications.

Ordering Information



Valid Combinations

89HPES16T4ZHBC	484-ball CABGA package, Commercial Temperature
89HPES16T4ZHBCG	484-ball Green CABGA package, Commercial Temperature

CORPORATE HEADQUARTERS
6024 Silver Creek Valley Road
San Jose, CA 95138

for SALES:
800-345-7015 or 408-284-8200
fax: 408-284-2775
www.idt.com

for Tech Support:
email: ssdhelp@idt.com
phone: 408-284-8208