ISL12058

Low Cost and Low Power I^{2}C-Bus Real Time Clock/Calendar Low Power and Low Cost RTC with Alarm Function

FN6756
Rev 1.00
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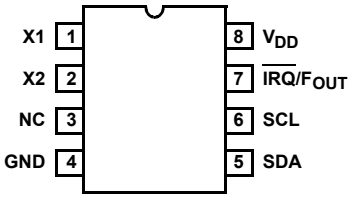
The ISL12058 device is a low power real time clock with clock/calendar, and alarm function.

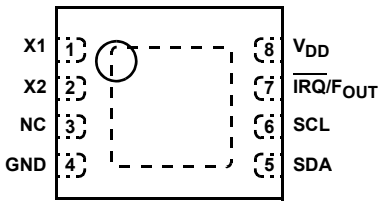
The oscillator uses an external, low-cost 32.768kHz crystal. The real time clock tracks time with separate registers for hours, minutes, and seconds. The device has calendar registers for date, month, year and day of the week. The calendar is accurate through 2099, with automatic leap year correction.

Pinouts

ISL12058
(8 LD SOIC, MSOP)
TOP VIEW



ISL12058
(8 LD 2x2 µTDFN, 8 LD 3x3 TDFN)
TOP VIEW



Features

- Real Time Clock/Calendar
  - Tracks Time in Hours, Minutes, and Seconds
  - Day of the Week, Date, Month, and Year
- 4 Selectable Frequency Outputs
- 2 Alarms
  - Settable to the Second, Minute, Hour, Day of the Week, Date, or Month
- I^{2}C Interface
  - 400kHz Data Transfer Rate
- Small Package Options
  - 8 Ld 2mmx2mm µTDFN Package
  - 8 Ld 3mmx3mm TDFN Package
  - 8 Ld MSOP Package
  - 8 Ld SOIC Package
  - Pb-Free (RoHS Compliant)
- Low Cost 3V Alternative to ISL1208 and ISL12082

Applications

- Utility Meters
- HVAC Equipment
- Audio/Video Components
- Set-Top Box/Television
- Modems
- Network Routers, Hubs, Switches, Bridges
- Cellular Infrastructure Equipment
- Fixed Broadband Wireless Equipment
- Pagers/PDA
- Point Of Sale Equipment
- Test Meters/Fixtures
- Office Automation (Copiers, Fax)
- Home Appliances
- Computer Products
- Other Industrial/Medical/Automotive

Ordering Information

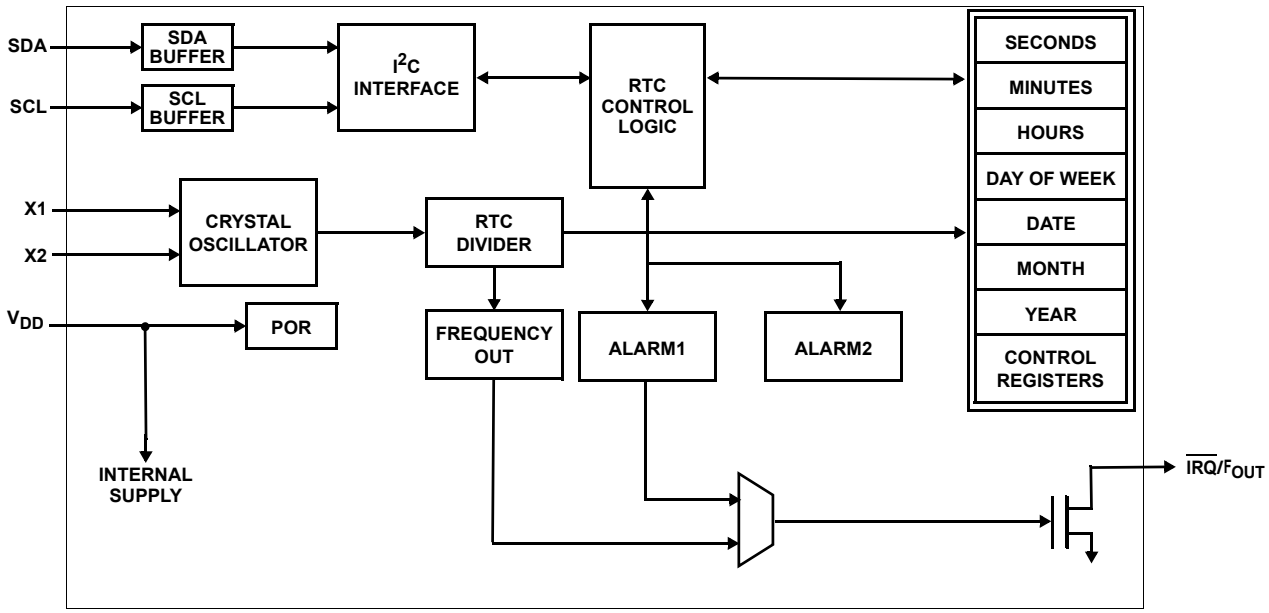
PART NUMBER	PART MARKING	V_{DD} RANGE (V)	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL12058IBZ (Note 1)	12058 IBZ	1.4 to 3.6	-40 to +85	8 Ld SOIC	M8.15
ISL12058IBZ-T* (Note 1)	12058 IBZ	1.4 to 3.6	-40 to +85	8 Ld SOIC (Tape and Reel)	M8.15
ISL12058IUZ (Note 1)	12058	1.4 to 3.6	-40 to +85	8 Ld MSOP	M8.118
ISL12058IUZ-T* (Note 1)	12058	1.4 to 3.6	-40 to +85	8 Ld MSOP (Tape and Reel)	M8.118
ISL12058IRTZ (Note 1)	2058	1.4 to 3.6	-40 to +85	8 Ld TDFN	L8.3x3I
ISL12058IRTZ-T* (Note 1)	2058	1.4 to 3.6	-40 to +85	8 Ld TDFN (Tape and Reel)	L8.3x3I
ISL12058IRUZ-T* (Note 2) **No longer available or supported**	058	1.4 to 3.6	-40 to +85	8 Ld µTDFN (Tape and Reel)	L8.2x2

*Please refer to TB347 for details on reel specifications.

NOTES:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Block Diagram



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	X1	The X1 pin is the input of an inverting amplifier and is intended to be connected to one pin of an external 32.768kHz quartz crystal.
2	X2	The X2 pin is the output of an inverting amplifier and is intended to be connected to one pin of an external 32.768kHz quartz crystal.
3	NC	No Connection. Can be connected to GND or left floating.
4	GND	Ground
5	SDA	Serial Data (SDA) is a bi-directional pin used to transfer serial data into and out of the device. It has an open drain output and may be wire OR'ed with other open drain or open collector outputs.
6	SCL	The Serial Clock (SCL) input is used to clock all serial data into and out of the device.
7	$\overline{IRQ}/F_{OUT}$	Interrupt Output /Frequency Output is a multi-functional pin that can be used as alarm interrupt or frequency output pin. The function is set via the configuration register. This pin is open drain and requires an external pull-up resistor. It has a default output of 32.768kHz at power-up.
8	V_{DD}	Power supply

Absolute Maximum Ratings

Voltage on V_{DD} Pin (respect to GND) . . . . . -0.2V to 4V
Voltage on $\overline{IRQ}/F_{OUT}$, SCL and SDA Pins (respect to GND) . . . . . -0.2V to 6V
Voltage on X1 and X2 Pins (respect to GND) . . . . . -0.2V to 4V
ESD Rating ((Per MIL-STD-883 Method 3014)
Human Body Model . . . . . >4kV
Machine Model . . . . . >350V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Lead SOIC (Note 3)	120	N/A
8 Lead MSOP (Note 3)	169	N/A
8 Lead µTDFN (Note 3)	160	N/A
8 Lead TDFN (Notes 4, 5)	52	7

Storage Temperature . . . . . -65°C to +150°C
Pb-free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

DC Operating Characteristics – RTC

Temperature = -40°C to +85°C unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 8)	TYP (Note 7)	MAX (Note 8)	UNITS	NOTES
V_{DD}	Main Power Supply		1.8		3.6	V	
V_{DDT}	Timekeeping Power Supply		1.4		1.8	V	
I_{DD1}	Standby Supply Current	V_{DD} = 3.6V		600	950	nA	6, 12
		V_{DD} = 3.0V		500		nA	
I_{DD2}	Timekeeping Current	V_{DD} = 1.8V		400	650	nA	6, 12
		V_{DD} = 1.4V		350		nA	
I_{DD3}	Supply Current With I^2C Active at Clock Speed of 400kHz	V_{DD} = 3.6V		15	40	µA	6
I_{LI}	Input Leakage Current on SCL		-100		100	nA	
I_{LO}	I/O Leakage Current on SDA		-100		100	nA	
$\overline{IRQ}/F_{OUT}$							
V_{OL}	Output Low Voltage	V_{DD} = 1.8V, I_{OL} = 3mA			0.4	V	

Serial Interface Specifications

Over the recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 8)	TYP (Note 7)	MAX (Note 8)	UNITS	NOTES
SERIAL INTERFACE SPECS							
V_{IL}	SDA and SCL Input Buffer LOW Voltage		-0.3		0.3 x V_{DD}	V	
V_{IH}	SDA and SCL Input Buffer HIGH Voltage		0.7 x V_{DD}		5.5	V	
Hysteresis	SDA and SCL Input Buffer Hysteresis			0.04 x V_{DD}		V	
V_{PULLUP}	Maximum Pull-up Voltage on SDA during I^2C Communication				V_{DD} + 2	V	11
V_{OL}	SDA Output Buffer LOW Voltage, Sinking 3mA	V_{DD} > 1.8V, V_{PULLUP} = 5.0V	0		0.4	V	
Cpin	SDA and SCL Pin Capacitance	T_A = +25°C, f = 1MHz, V_{DD} = 5V, V_{IN} = 0V, V_{OUT} = 0V			10	pF	9, 10
f_{SCL}	SCL Frequency				400	kHz	

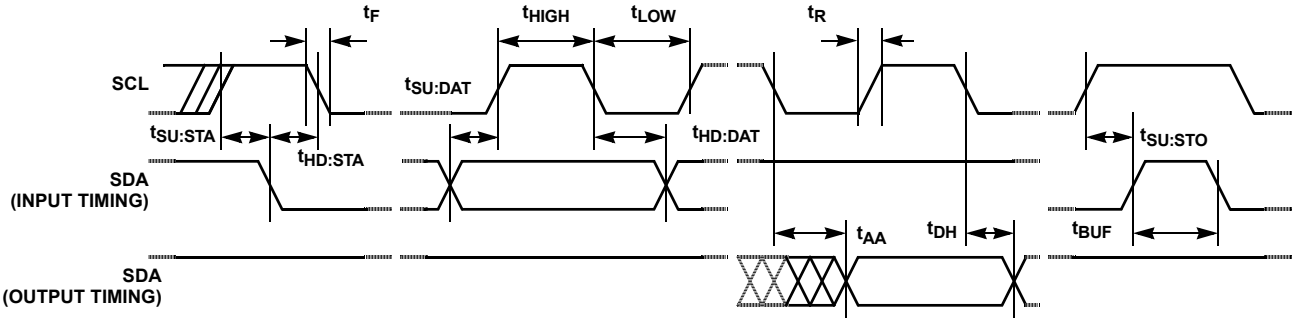
Serial Interface Specifications Over the recommended operating conditions unless otherwise specified. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 8)	TYP (Note 7)	MAX (Note 8)	UNITS	NOTES
t_{IN}	Pulse width Suppression Time at SDA and SCL Inputs	Any pulse narrower than the max spec is suppressed			50	ns	
t_{AA}	SCL Falling Edge to SDA Output Data Valid	SCL falling edge crossing 30% of V_{DD}, until SDA exits the 30% to 70% of V_{DD} window			900	ns	11
t_{BUF}	Time the Bus Must be Free Before the Start of a New Transmission	SDA crossing 70% of V_{DD} during a STOP condition, to SDA crossing 70% of V_{DD} during the following START condition	1300			ns	
t_{LOW}	Clock LOW Time	Measured at the 30% of V_{DD} crossing	1300			ns	
t_{HIGH}	Clock HIGH Time	Measured at the 70% of V_{DD} crossing	600			ns	
$t_{SU:STA}$	START Condition Setup Time	SCL rising edge to SDA falling edge. Both crossing 70% of V_{DD}	600			ns	
$t_{HD:STA}$	START Condition Hold Time	From SDA falling edge crossing 30% of V_{DD} to SCL falling edge crossing 70% of V_{DD}	600			ns	
$t_{SU:DAT}$	Input Data Setup Time	From SDA exiting the 30% to 70% of V_{DD} window, to SCL rising edge crossing 30% of V_{DD}	100			ns	
$t_{HD:DAT}$	Input Data Hold Time	From SCL falling edge crossing 30% of V_{DD} to SDA entering the 30% to 70% of V_{DD} window	0		900	ns	
$t_{SU:STO}$	STOP Condition Setup Time	From SCL rising edge crossing 70% of V_{DD}, to SDA rising edge crossing 30% of V_{DD}	600			ns	
$t_{HD:STO}$	STOP Condition Hold Time	From SDA rising edge to SCL falling edge. Both crossing 70% of V_{DD}	600			ns	
t_{DH}	Output Data Hold Time	From SCL falling edge crossing 30% of V_{DD}, until SDA enters the 30% to 70% of V_{DD} window	0			ns	
t_R	SDA and SCL Rise Time	From 30% to 70% of V_{DD}	20 + 0.1 x Cb		300	ns	9, 10
t_F	SDA and SCL Fall Time	From 70% to 30% of V_{DD}	20 + 0.1 x Cb		300	ns	9, 10, 11
Cb	Capacitive Loading of SDA or SCL	Total on-chip and off-chip	10		400	pF	9, 10
Rpu	SDA and SCL Bus Pull-Up Resistor Off-Chip	Maximum is determined by t_R and t_F. For Cb = 400pF, max is about 2kΩ to~2.5kΩ. For Cb = 40pF, max is about 15kΩ to ~20kΩ	1			kΩ	9, 10

NOTES:

6. $\overline{IRQ}/F_{OUT}$ inactive.
7. Typical values are for T = +25°C and 3.3V supply voltage.
8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
9. Limits should be considered typical and are not production tested.
10. These are I^2C specific parameters and are not production tested, however, they are used to set conditions for testing devices to validate specification.
11. Parts will work with SDA pull-up voltage above the V_{PULLUP} limit but the t_{AA} and $t_F$in the I^2C parameters are not guaranteed.
12. Specified at +25°C.

SDA vs SCL Timing



Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

EQUIVALENT AC OUTPUT LOAD CIRCUIT FOR V_{DD} = 3.0V

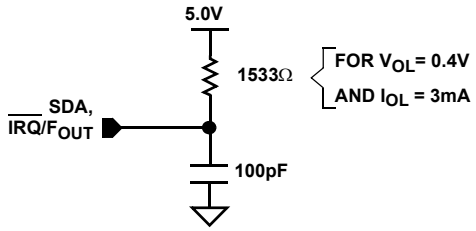


FIGURE 1. STANDARD OUTPUT LOAD FOR TESTING THE DEVICE WITH V_{DD} = 3.0V, V_{PULLUP} = 5.0V

Typical Performance Curves Temperature is +25°C unless otherwise specified

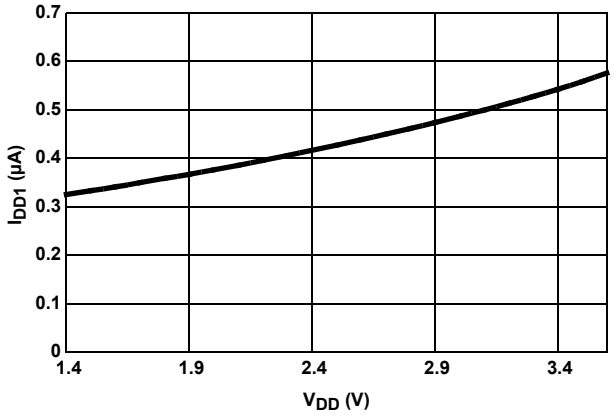


FIGURE 2. I_{DD1} vs V_{DD}

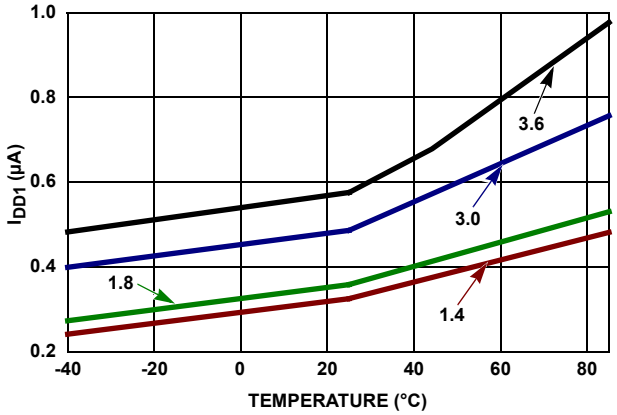


FIGURE 3. I_{DD1} vs TEMPERATURE

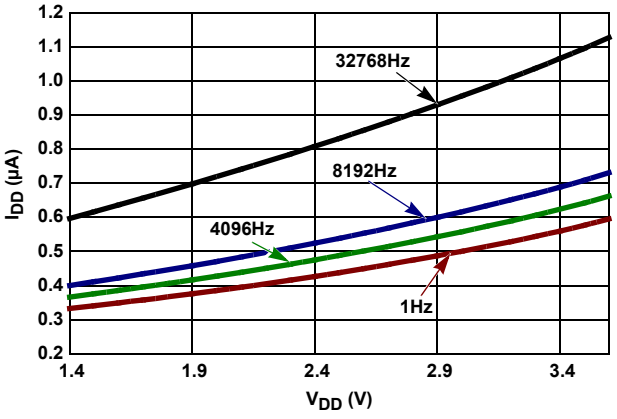


FIGURE 4. I_{DD} vs V_{DD} vs F_{OUT}

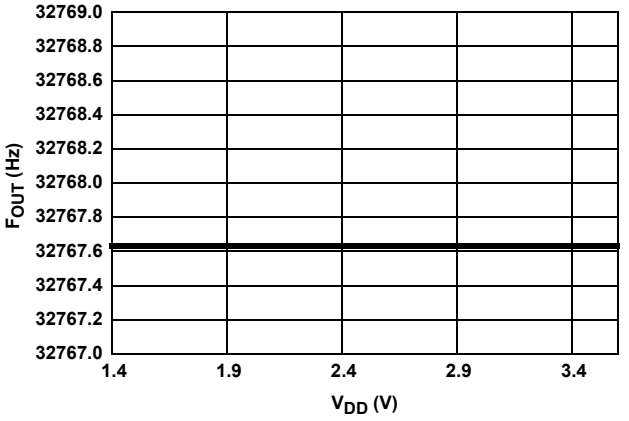


FIGURE 5. F_{OUT} vs V_{DD} WITH A TYPICAL 32.768kHZ CRYSTAL

General Description

The ISL12058 device is a low power real time clock with clock/calendar, and alarm.

The oscillator uses an external, low-cost 32.768kHz crystal. The real time clock tracks time with separate registers for hours, minutes, and seconds. The device has calendar registers for date, month, year and day of the week. The calendar is accurate through 2099, with automatic leap year correction.

The ISL12058's flexible alarm can be set to any clock/calendar value for a match. For example, every minute, every Tuesday or at 5:23 AM on March 21. The alarm status is available by checking the Status Register, or the device can be configured to provide a hardware interrupt via the $\overline{IRQ}/F_{OUT}$ pin.

Pin Descriptions

X1, X2

The X1 and X2 pins are the input and output, respectively, of an inverting amplifier. An external 32.768kHz quartz crystal is used with the ISL12058 to supply a timebase for the real time clock. Refer to Figure 6.

The device can also be driven directly from a 32.768kHz square wave source with peak to peak voltage from 0V to VDD at X1 pin with X2 pin floating.

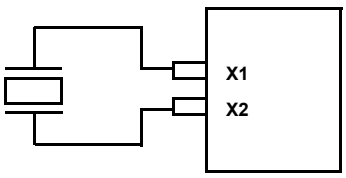


FIGURE 6. RECOMMENDED CRYSTAL CONNECTION

$\overline{IRQ}/F_{OUT}$ (Interrupt Output/Frequency Output)

This dual function pin can be used as an interrupt or frequency output pin. The $\overline{IRQ}/F_{OUT}$ mode is selected via the IRQE bit of the control register (address 08h). The $\overline{IRQ}/F_{OUT}$ is an open drain output and requires the use of a pull-up resistor, and it can accept a pull-up voltage up to 5.5V.

This pin has a default output of 32.768kHz at power-up.

- **Interrupt Mode.** The pin provides an interrupt signal output. This signal notifies a host processor that an alarm has occurred and requests action.
- **Frequency Output Mode.** The pin outputs a clock signal which is related to the crystal frequency. The frequency output is user selectable and enabled via the I^2C bus.

Serial Clock (SCL)

The SCL input is used to clock all serial data into and out of the device. The input buffer on this pin is always active (not gated). The SCL pin can accept a logic high voltage up to 5.5V.

Serial Data (SDA)

SDA is a bi-directional pin used to transfer data into and out of the device. It has an open drain output and may be ORed with other open drain or open collector outputs. The input buffer is always active (not gated) in normal mode.

An open drain output requires the use of a pull-up resistor, and it can accept a pull-up voltage up to 5.5V. The output circuitry controls the fall time of the output signal with the use of a slope controlled pull-down. The circuit is designed for 400kHz I^2C interface speeds.

NOTE: Parts will work with SDA pull-up voltage above the V_{PULLUP} limit but the t_{AA} and t_F in the I^2C parameters are not guaranteed.

V_{DD}, GND

Chip power supply and ground pins. The device will have full operation with a power supply from 1.8V to 3.6V, and timekeeping function with a power supply from 1.4V to 3.6V.

A 0.1µF decoupling capacitor is recommended on the V_{DD} pin to ground.

NC (No Connection)

The NC pin is not connected to the die. The pin can be connected to GND or left floating.

Functional Description

Real Time Clock Operation

The Real Time Clock (RTC) uses an external 32.768kHz quartz crystal to maintain an accurate internal representation of second, minute, hour, day of week, date, month, and year. The RTC also has leap-year correction. The RTC also corrects for months having fewer than 31 days and has a bit that controls 24 hour or AM/PM format. When the ISL12058 powers up after the loss of V_{DD}, the clock will not begin incrementing until at least one byte is written to the clock register.

Accuracy of the Real Time Clock

The accuracy of the Real Time Clock depends on the frequency of the quartz crystal that is used as the time base for the RTC. Since the resonant frequency of a crystal is temperature dependent, the RTC performance will also be dependent upon temperature. The frequency deviation of the crystal is a function of the turnover temperature of the crystal from the crystal's nominal frequency. For example, a ~20ppm frequency deviation translates into an accuracy of ~1 minute per month. These parameters are available from the crystal manufacturer.

Alarm Interrupt

The alarm interrupt mode is enabled by setting IRQE bit to '1' with Alarm1 enables by setting ALM1E to '1'.

The standard alarm allows for alarms of time, date, day of the week, month, and year. When a time alarm occurs, the $\overline{IRQ}/F_{OUT}$ pin will be pulled low and the alarm interrupt bit (A1F) will be set to "1".

NOTE: The A1F bit can be reset by the user or cleared automatically using the Auto Reset mode (see ARST bit, address 07h). Alarm2 does not have hardware interrupt function.

Frequency Output Mode

The ISL12058 has the option to provide a frequency output signal using the $\overline{IRQ}/F_{OUT}$ pin. The frequency output mode is set by using the FO bits to select 4 possible output frequency values from 1Hz to 32.768kHz. The IRQE bit must be set to '0' for frequency output.

I^2C Serial Interface

The ISL12058 has an I^2C serial bus interface that provides access to the real time clock registers, control and status registers and the alarm registers. The I^2C serial interface is compatible with other industry I^2C serial bus protocols using a bi-directional data signal (SDA) and a clock signal (SCL).

Register Descriptions

The registers are accessible following a slave byte of "1101111x" and reads or writes to addresses [00h:1Fh]. The defined addresses and default values are described in Table 1. Address 15h to 1Fh are not used. Reads or writes to 15h to 1Fh will not affect operation of the device but should be avoided. For Page Write and Page Read operation, the address will wrap around from address 1Fh to 00h.

REGISTER ACCESS

The contents of the registers can be modified by performing a byte or a page write operation directly to any register address.

The registers are divided into 3 sections. These are:

1. Real Time Clock (7 bytes): Address 00h to 06h.
2. Control and Status (2 bytes): Address 07h to 08h.
3. Alarm1 and Alarm2 (9 bytes): Address 0Ch to 14h.

There are no addresses above 1Fh.

TABLE 1. REGISTER MEMORY MAP

ADDR.	SECTION	REG NAME	BIT								REG	
			7	6	5	4	3	2	1	0	RANGE	DEFAULT
00h	RTC	SC	0	SC22	SC21	SC20	SC13	SC12	SC11	SC10	0 to 59	00h
01h		MN	0	MN22	MN21	MN20	MN13	MN12	MN11	MN10	0 to 59	00h
02h		HR	MIL	0	HR21	HR20	HR13	HR12	HR11	HR10	0 to 23	00h
03h		DT	0	0	DT21	DT20	DT13	DT12	DT11	DT10	1 to 31	01h
04h		MO	0	0	0	MO20	MO13	MO12	MO11	MO10	1 to 12	01h
05h		YR	YR23	YR22	YR21	YR20	YR13	YR12	YR11	YR10	0 to 99	00h
06h		DW	0	0	0	0	0	DW12	DW11	DW10	0 to 6	00h
07h	Status	SR	ARST	XSTOP	0	WRTC	OSF	A1F	A2F	PF	N/A	09h
08h	Control	INT	0	ALM1E	ALM2E	FO1	FO0	IRQE	0	A1E	N/A	18h
09h		Not Used	0	0	0	0	0	0	0	0	N/A	00h
0Ah		Not Used	0	0	0	0	0	0	0	0	N/A	00h
0Bh		Not Used	0	0	0	0	0	0	0	0	N/A	00h
0Ch	Alarm1	A1SC	A1M1	A1SC22	A1SC21	A1SC20	A1SC13	A1SC12	A1SC11	A1SC10	00 to 59	00h
0Dh		A1MN	A1M2	A1MN22	A1MN21	A1MN20	A1MN13	A1MN12	A1MN11	A1MN10	00 to 59	00h
0Eh		A1HR	A1M3	A1MIL	A1HR21	A1HR20	A1HR13	A1HR12	A1HR11	A1HR10	0 to 23	00h
0Fh		A1DT	A1M4	0	A1DT21	A1DT20	A1DT13	A1DT12	A1DT11	A1DT10	1 to 31	00h
10h		A1MO	A1M5	0	0	A1MO20	A1MO13	A1MO12	A1MO11	A1MO10	1 to 12	00h
11h		A1DW	A1M6	0	0	0	0	A1DW12	A1DW11	A1DW10	0 to 6	00h
12h	Alarm2	A2MN	A2M2	A2MN22	A2MN21	A2MN20	A2MN13	A2MN12	A2MN11	A2MN10	00 to 59	00h
13h		A2HR	A2M3	A2MIL	A2HR21	A2HR20	A2HR13	A2HR12	A2HR11	A2HR10	0 to 23	00h
14h		A2DW/$\overline{DT}$	A2M4	A2DW/$\overline{DT}$	A2DT21	A2DT20	A2DT13	A2DT12	A2DT11	A2DT10	1 to 31	00h
								A2DW12	A2DW11	A2DW10	0 to 6	00h

Address 09h to 0Bh and 15h to 1Fh are not used. Reads or writes to these registers will not affect operation of the device but should be avoided.

A register can be read by performing a random read at any address at any time. This returns the contents of that register location. Additional registers are read by performing a sequential read. For the RTC registers, the read instruction latches all clock registers into a buffer, so an update of the clock does not change the time being read. A sequential read will not result in the output of data from the memory array. At the end of a read, the master supplies a stop condition to end the operation and free the bus. After a read or write instruction, the address remains at the previous address +1 so the user can execute a current address read and continue reading the next register.

Real Time Clock Registers

Addresses [00h to 06h]

RTC REGISTERS (SC, MN, HR,DW, DT, MO, YR)

These registers depict BCD representations of the time. As such, SC (Seconds, address 00h) and MN (Minutes, address 01h) range from 0 to 59, HR (Hour, address 02h) can either be a 12-hour or 24-hour mode, DT (Date, address 03h) is 1 to 31, MO (Month, address 04h) is 1 to 12, YR (Year, address 06h) is 0 to 99, and DW (Day of the Week, address 06h) is 0 to 6.

The DW register provides a Day of the Week status and uses three bits DW2 to DW0 to represent the seven days of the week. The counter advances in the cycle 0-1-2-3-4-5-6-0-1-2-… The assignment of a numerical value to a specific day of the week is arbitrary and may be decided by the system software designer. The default value is defined as “0”.

24 HOUR TIME

If the MIL bit of the HR register is “1”, the RTC uses a 24-hour format. If the MIL bit is “0”, the RTC uses a 12-hour format and HR21 bit functions as an AM/PM indicator with a “1” representing PM. The clock defaults to 12-hour format time with HR21 = “0”.

If the A1HR and/or A2HR registers are used for alarm interrupt, the A1HR and/or A2HR registers must set to the same hour format as the HR register. For example, if the HR register is set to 24-hour format by setting the MIL bit to “1”, then the AxHR register must be set to 24-hour format with AxMIL bit set to “1”. If the hour format does not match between the HR register and the AxHR register, then the alarm interrupt will not trigger.

LEAP YEARS

Leap years add the day February 29 and are defined as those years that are divisible by 4. Years divisible by 100 are not leap years, unless they are also divisible by 400. This means that the year 2000 is a leap year, the year 2100 is not. The ISL12058 does not correct for the leap year in the year 2100.

Control and Status Registers

Addresses [07h to 0Bh]

The Control and Status Registers consist of the Status Register, Interrupt Register, and Alarm Registers.

Status Register (SR) [Address 07h]

The Status Register is located in the memory map at address 0Bh. This is a volatile register that provides either control or status of alarm interrupt and crystal oscillator enable. Refer to Table 2.

TABLE 2. STATUS REGISTER (SR)

ADDR	7	6	5	4	3	2	1	0
07h	ARST	XSTOP	0	WRTC	OSF	A1F	A2F	PF
Default	0	0	0	0	1	0	0	1

NOTE: read operation will remain set after the read operation is complete.

POWER FAILURE BIT (PF)

This bit is set to a “1” after a total power failure. This is a read only bit that is set by hardware (ISL12058 internally) when the device powers up after having lost power to the device. On power-up after a total power failure, all registers are set to their default states. The first valid write to the RTC section after a complete power failure resets the PF bit to “0” (writing one RTC register is sufficient).

ALARM1 INTERRUPT BIT (A1F)

These bits announce if the Alarm1 matches the real time clock. If there is a match, the respective bit is set to “1”. This bit is manually reset to “0” by the user. A write to this bit in the SR can only set it to “0”, not “1”.

ALARM2 INTERRUPT BIT (A2F)

These bits announce if the Alarm2 matches the real time clock. If there is a match, the respective bit is set to “1”. This bit is manually reset to “0” by the user. A write to this bit in the SR can only set it to “0”, not “1”.

OSCILLATOR FAIL BIT (OSF)

Oscillator Fail Indicator bit (OSF). This bit is set to a “1” when there is no oscillation on X1 pin. The OSF bit can only be reset by having an oscillation on X1 and manually reset to “0” to reset it.

WRITE RTC ENABLE BIT (WRTC)

The WRTC bit enables or disables write capability into the RTC Timing Registers. The factory default setting of this bit is “0”. Upon initialization or power-up, the WRTC must be set to “1” to enable the RTC. Upon the completion of a valid write (STOP), the RTC starts counting. The RTC internal 1Hz signal is synchronized to the STOP condition during a valid write cycle.

CRYSTAL OSCILLATOR ENABLE BIT (XSTOP)

This bit enables/disables the internal crystal oscillator. When the XSTOP is set to “1”, the oscillator is disabled. The XSTOP bit is set to “0” on power-up for normal operation.

AUTO RESET ENABLE BIT (ARST)

This bit enables/disables the automatic reset of the A1F and A2F status bits only. When ARST bit is set to “1”, these status bits are reset to “0” after a valid read of the respective status register (with a valid STOP condition). When the ARST is cleared to “0”, the user must manually reset the A1F and A2F bits.

Interrupt Control Register (INT) [Address 08h]

TABLE 3. INTERRUPT CONTROL REGISTER (INT)

ADDR	7	6	5	4	3	2	1	0
08h	0	ALM1E	ALM2E	FO1	FO0	IRQE	0	A1E
Default	0	0	0	1	1	0	0	0

ALARM1 INTERRUPT ENABLE BIT (A1E)

This bit enables the hardware interrupt function of ALARM1 to $\overline{IRQ}/F_{OUT}$ pin. When A1E set to ‘1’, IRQE set to ‘1’ and ALM1E set to ‘1’, the $\overline{IRQ}/F_{OUT}$ pin will pull low when the A1F bit is set by the ALARM1 interrupt.

$\overline{IRQ}/F_{OUT}$ FUNCTION SELECTION BIT (IRQE)

This bit selects the function of the $\overline{IRQ}/F_{OUT}$ pin. Refer to Table 4 for function selection of $\overline{IRQ}/F_{OUT}$ PIN.

TABLE 4. FUNCTION SELECTION OF $\overline{IRQ}/F_{OUT}$ PIN WITH A1E AND IRQE BITS

A1E	IRQE	$\overline{IRQ}/F_{OUT}$ FUNCTION
0	0	F_{OUT}
0	1	High Impedance
1	0	F_{OUT}

TABLE 4. FUNCTION SELECTION OF $\overline{IRQ}/F_{OUT}$ PIN WITH A1E AND IRQE BITS (Continued)

A1E	IRQE	$\overline{IRQ}/F_{OUT}$ FUNCTION
1	1	Alarm 1 Interrupt

FREQUENCY OUT CONTROL BITS (FO <1:0>)

These bits select the output frequency at the $\overline{IRQ}/F_{OUT}$ pin. IRQE must be set to “0” for frequency output at the $\overline{IRQ}/F_{OUT}$ pin. Refer to Table 5 for frequency selection.

TABLE 5. FREQUENCY SELECTION OF $\overline{IRQ}/F_{OUT}$ PIN WITH FO1 AND FO0 BITS

FO1	FO0	FREQUENCY, F_{OUT} (Hz)	COMMENT
1	1	32768	Free running crystal clock
1	0	8192	Free running crystal clock
0	1	4096	Free running crystal clock
0	0	1	Sync. at RTC write

ALARM ENABLE BITS (ALM1E, ALM2E)

This bit enables/disables the Alarm1 and Alarm2 function.

When the ALM1E bit is set to “1”, the Alarm1 function is enabled. When the ALM1E is cleared to “0”, the alarm function is disabled. ALM1E bit is set to “0” at power-up.

When the ALM2E bit is set to “1”, the Alarm2 function is enabled. When the ALM2E is cleared to “0”, the alarm function is disabled. ALM2E bit is set to “0” at power-up.

NOTE: The Alarm1 has hardware function via the $\overline{IRQ}/F_{OUT}$ pin. Alarm2 does not have hardware interrupt function.

Alarm1 Registers

Addresses [Address 0Ch to 11h]

The Alarm1 register bytes are set up identical to the RTC register bytes, except that the MSB of each byte functions as an enable bit (enable = “1”). These enable bits specify which alarm registers (seconds, minutes, etc) are used to make the comparison. Note that there is no alarm byte for year. When all the enable bits are set to “0” with ALM1E set to “1”, the Alarm 1 will triggered once a second.

The Alarm1 function works as a comparison between the Alarm1 registers and the RTC registers. As the RTC advances, the Alarm1 will be triggered once a match occurs between the Alarm1 registers and the RTC registers. Any one Alarm1 register, multiple registers, or all registers can be enabled for a match.

To clear an Alarm1, the A1F status bit can be set to “0” with a write or use the ARST bit auto reset function.

TABLE 6. ALARM1 INTERRUPT WITH ENABLE BITS SELECTION

A1M1	A1M2	A1M3	A1M4	A1M5	A1M6	ALARM1 Interrupt
0	0	0	0	0	0	Every Second
1	0	0	0	0	0	Match Second
0	1	0	0	0	0	Match Minute
0	0	1	0	0	0	Match Hour
0	0	0	1	0	0	Match Date
0	0	0	0	1	0	Match Month
0	0	0	0	0	1	Match Day
1	1	0	0	0	0	Match Second and Minute
1	0	1	0	0	0	Match Second and Hour
1	1	1	0	0	0	Match Second, Minute, and Hour
. . .	. . .	. . .	. . .	. . .	. . .	
0	0	0	1	1	1	Match Date, Month, and Day
1	0	0	1	1	1	Match Second, Date, Month, and Day
. . .	. .	. . .	. . .	. . .	. . .	. . .
0	1	1	1	1	1	Match MInute, Hour, Date, Month, and Day
1	1	1	1	1	1	Match Second, MInute, Hour, Date, Month, and Day

Following is example of Alarm1 Interrupt.

Example – A single alarm will occur on January 1 at 11:30am.

A. Set Alarm1 registers as follows:

ALARM1 REGISTER	BIT									DESCRIPTION
	7	6	5	4	3	2	1	0	HEX	
A1SC	0	0	0	0	0	0	0	0	00h	Seconds disabled
A1MN	1	0	1	1	0	0	0	0	B0h	Minutes set to 30, enabled
A1HR	1	0	0	1	0	0	0	1	91h	Hours set to 11, enabled
A1DT	1	0	0	0	0	0	0	1	81h	Date set to 1, enabled
A1MO	1	0	0	0	0	0	0	1	81h	Month set to 1, enabled
A1DW	0	0	0	0	0	0	0	0	00h	Day of week disabled

B. Also the ALME bit must be set as follows:

CONTROL REGISTER	BIT									DESCRIPTION
	7	6	5	4	3	2	1	0	HEX	
INT	0	1	x	x	x	1	0	1	45h	Enable Alarm1, and Alarm1 Interrupt to $\overline{IRQ}/F_{OUT}$

xx indicate other control bits and these bit can be set to 0 or 1.

After these registers are set, the Alarm1 interrupt will be generated when the RTC advances to exactly 11:30am on January 1 (after seconds changes from 59 to 00) by setting the A1F bit in the status register to “1” and also bringing the $\overline{IRQ}/F_{OUT}$ output low.

Alarm2 Registers

Addresses [Address 12h to 14h]

The Alarm2 register bytes are set up identical to the RTC register bytes except that the MSB of each byte functions as an enable bit (enable = “1”). These enable bits specify which alarm registers (minutes, hour, and date/day) are used to make the comparison. Note that there are no alarm bytes for second, month and year. When all the enable bits are set to “0” with ALM2E set to “1”, the Alarm2 will triggered once a minute when second hits “00”.

The Alarm2 function works as a comparison between the Alarm2 registers and the RTC registers. As the RTC advances, the Alarm2 will be triggered once a match occurs between the Alarm2 registers and the RTC registers. Any one Alarm2 register, multiple registers, or all registers can be enabled for a match.

To clear an Alarm2, the A2F status bit can be set to “0” with a write or use the ARST bit auto reset function.

TABLE 7. ALARM2 INTERRUPT WITH ENABLE BITS SELECTION

A2DW/$\overline{DT}$	A2M2	A2M3	A2M4	ALARM2 Interrupt
0	0	0	0	Every Minute (Second=00)
0	1	0	0	Match Minute
0	0	1	0	Match Hour
0	0	0	1	Match Date
1	0	0	1	Match Day
0	1	1	0	Match Minute and Hour
0	1	0	1	Match Minute and Date
0	0	1	1	Match Hour and Date
0	1	1	1	Match Minute, Hour, and Date
1	1	1	0	Match Minute and Hour
1	1	0	1	Match Minute and Day
1	0	1	1	Match Hour and Day
1	1	1	1	Match Minute, Hour, and Day

Following is example of Alarm2 Interrupt.

Example – A single alarm will occur on every Monday at 20:00 military time (Monday is when DW = 1).

A. Set Alarm registers as follows:

ALARM2 REGISTER	BIT									DESCRIPTION
	7	6	5	4	3	2	1	0	HEX	
A2MN	0	0	0	0	0	0	0	0	00h	Minutes disabled
A2HR	1	1	1	0	0	0	0	0	E0h	Hours set to 20, enabled
A2DW/$\overline{DT}$	1	1	0	0	0	0	0	1	C1h	Day set to Monday, enabled

After these registers are set, an alarm will be generated when the RTC advances to exactly 20:00 on Monday (after minutes changes from 59 to 00) by setting the A2F bit in the status register to “1”.

I^2C Serial Interface

The ISL12058 supports a bi-directional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL12058 operates as a slave device in all applications.

All communication over the I^2C interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 7). On power-up of the ISL12058, the SDA pin is in the input mode.

All I^2C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL12058 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 7). A START condition is ignored during the power-up sequence.

All I^2C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 7). A STOP condition at the end of a read operation or at the end of a write operation to memory only places the device in its standby mode.

An acknowledge (ACK) is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting 8 bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the 8 bits of data (see Figure 8).

The ISL12058 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL12058 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

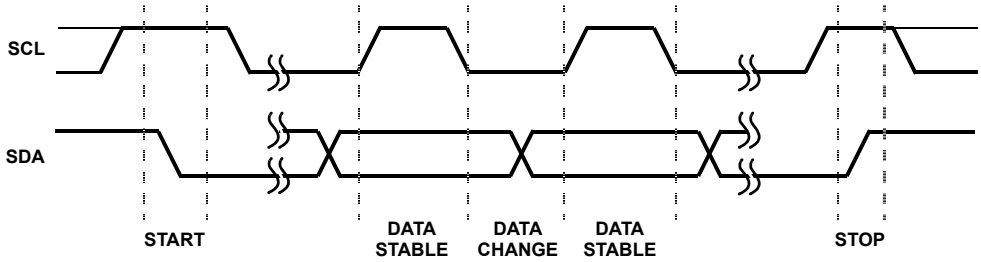


FIGURE 7. VALID DATA CHANGES, START, AND STOP CONDITIONS

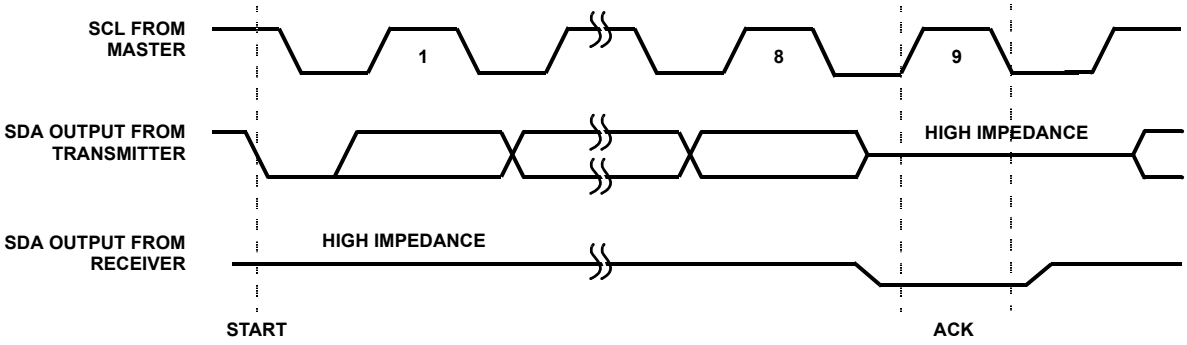


FIGURE 8. ACKNOWLEDGE RESPONSE FROM RECEIVER

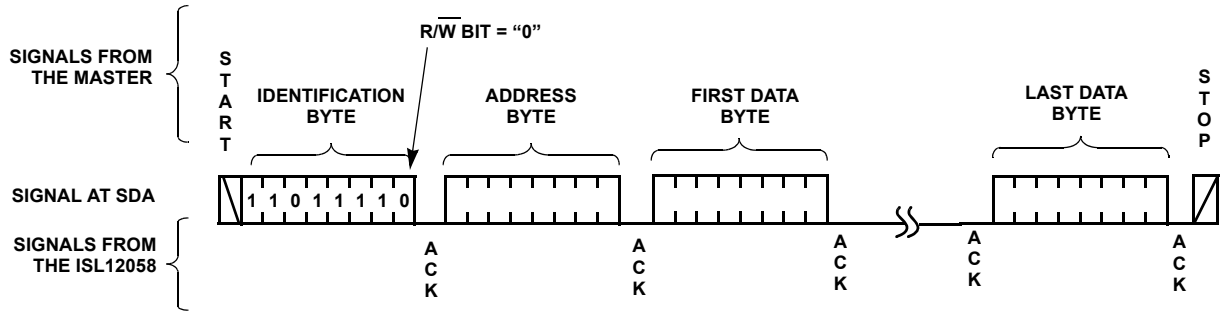


FIGURE 9. SEQUENTIAL BYTE WRITE SEQUENCE

Device Addressing

Following a start condition, the master must output a Slave Address Byte. The 7 MSBs of the Slave Address Byte are the device identifier bits, and the device identifier bits are "1101111".

The last bit of the Slave Address Byte defines a read or write operation to be performed. When this R/$\overline{W}$ bit is a "1", then a read operation is selected. A "0" selects a write operation (refer to Figure 10).

After loading the entire Slave Address Byte from the SDA bus, the ISL12058 compares the device identifier bits with "1101111". Upon a correct compare, the device outputs an acknowledge on the SDA line.

Following the Slave Address Byte is a 1 byte register address. The register address is supplied by the master device. On power-up, the internal address counter is set to address 0h, so a current address read of the RTC array starts at address 0h. When required, as part of a random read, the master must supply the 1 Word Address Bytes as shown in Figure 11.

In a random read operation, the slave byte in the "dummy write" portion must match the slave byte in the "read" section. For a random read of the Clock/Control Registers, the slave byte must be "1101111x" in both places.

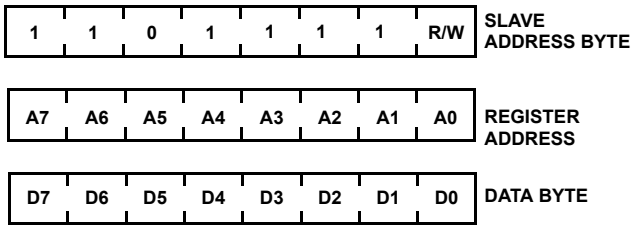


FIGURE 10. SLAVE ADDRESS, WORD ADDRESS, AND DATA BYTES

Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL12058 responds with an ACK. At this time, the I^2C interface enters a standby state.

Read Operation

A Read operation consists of a three byte instruction followed by one or more Data Bytes (see Figure 11). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/$\overline{W}$ bit set to "0", an Address Byte, a second START, and a second Identification byte with the R/$\overline{W}$ bit set to "1". After each of the three bytes, the ISL12058 responds with an ACK. Then the ISL12058 transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of each byte. The master terminates the read operation (issuing a STOP condition) following the last bit of the last Data Byte (see Figure 11).

The Data Bytes are from the memory location indicated by an internal pointer. This pointer's initial value is determined by the Address Byte in the Read operation instruction, and increments by one during transmission of each Data Byte. After reaching the memory location 1Fh, the pointer "rolls over" to 00h, and the device continues to output data for each ACK received.

Application Section

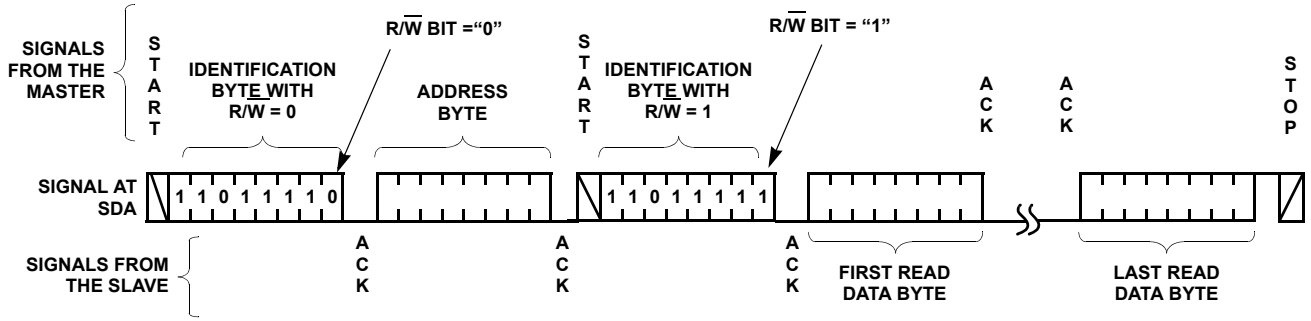


FIGURE 11. MULTIPLE BYTES READ SEQUENCE

Oscillator Crystal Requirements

The ISL12058 uses a standard 32.768kHz crystal. Either through hole or surface mount crystals can be used. Table 8 lists some recommended surface mount crystals and the parameters of each. This list is not exhaustive and other surface mount devices can be used with the ISL12058 if their specifications are very similar to the devices listed. The crystal should have a required parallel load capacitance of 12.5pF and an equivalent series resistance of less than 50k. The crystal's temperature range specification should match the application. Many crystals are rated for -10°C to +60°C (especially through-hole and tuning fork types), so an appropriate crystal should be selected if extended temperature range is required.

TABLE 8. SUGGESTED SURFACE MOUNT CRYSTALS

MANUFACTURER	PART NUMBER
Citizen	CM200S
MicroCrystal	MS3V
Raltron	RSM-200S
SaRonix	32S12
Ecliptek	ECPSM29T-32.768K
ECS	ECX-306
Fox	FSM-327

Layout Considerations

The crystal input at X1 has a very high impedance, and oscillator circuits operating at low frequencies (such as 32.768kHz) are known to pick up noise very easily if layout precautions are not followed. Most instances of erratic clocking or large accuracy errors can be traced to the susceptibility of the oscillator circuit to interference from adjacent high speed clock or data lines. Careful layout of the RTC circuit will avoid noise pickup and insure accurate clocking.

Figure 12 shows a suggested layout for the ISL12058 device using a surface mount crystal. Two main precautions should be followed:

1. Do not run the serial bus lines or any high speed logic lines in the vicinity of the crystal. These logic level lines can induce noise in the oscillator circuit to cause misclocking.
2. Add a ground trace around the crystal with one end terminated at the chip ground. This will provide termination for emitted noise in the vicinity of the RTC device.

In addition, it is a good idea to avoid a ground plane under the X1 and X2 pins and the crystal, as this will affect the load capacitance and therefore the oscillator accuracy of the circuit. If the $\overline{IRQ}/F_{OUT}$ pin is used as a clock, it should be routed away from the RTC device as well. The traces for the V_{DD} pins can be treated as a ground, and should be routed around the crystal.

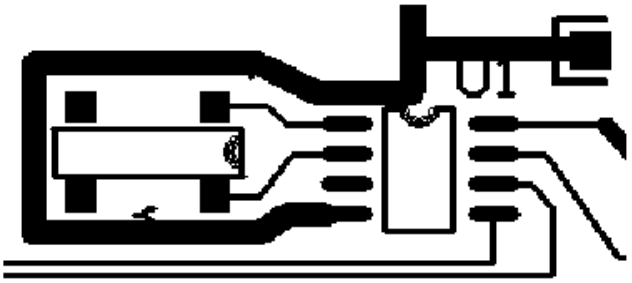


FIGURE 12. SUGGESTED LAYOUT FOR ISL12058 AND

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
December 10, 2015	FN6756.1	Added Rev History and About Intersil Verbiage. Updated Ordering Information on page 2 **Updated POD L8.2X2** to most current version. Rev changes are as follows: Added Triangles to Note referenced in POD. Tiebar Note updated From: Tiebar shown (if present) is a non-functional feature. To: Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends). **Updated POD M8.15** to most current version. Rev changes are as follows: Changed Note 1 "1982" to "1994" Changed in Typical Recommended Land Pattern the following: 2.41(0.095) to 2.20(0.087) 0.76 (0.030) to 0.60(0.023) 0.200 to 5.20(0.205) Updated to new POD format by removing table and moving dimensions onto drawing and adding land pattern **Updated POD L8.3x3I** to most current version. Rev changes are as follows: Tiebar Note updated From: Tiebar shown (if present) is a non-functional feature. To: Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends). Flipped top view and bottom view so pin 1 indicator is on bottom left in top view and bottom right in bottom view. 2. Added pin numbers 4 and 5 to bottom view. 3. Added pin 1 indicator in land pattern. +++20141002 Change Security to E. **Updated POD M8.118** to most current version. Rev changes are as follows: Corrected lead width dimension in side view 1 from "0.25 - 0.036" to "0.25 - 0.36" Updated to new intersil format by adding land pattern and moving dimensions from table onto drawing.

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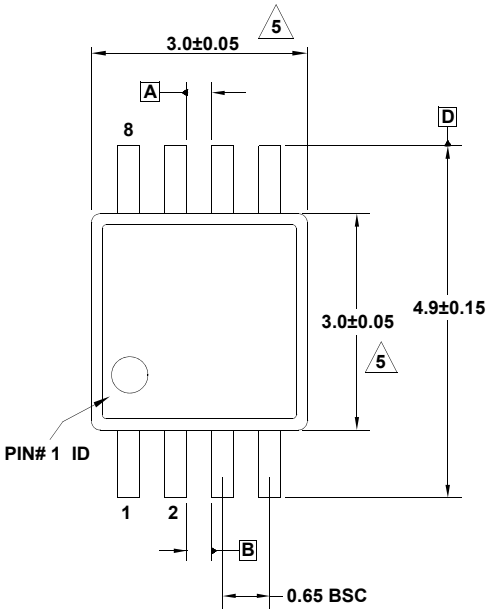
Package Outline Drawing

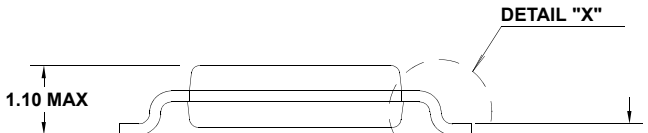
M8.118

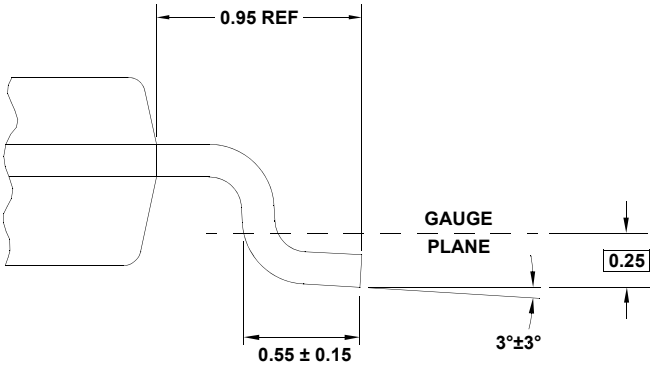
8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

Rev 4, 7/11

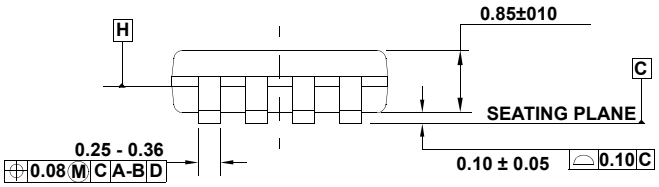


TOP VIEW

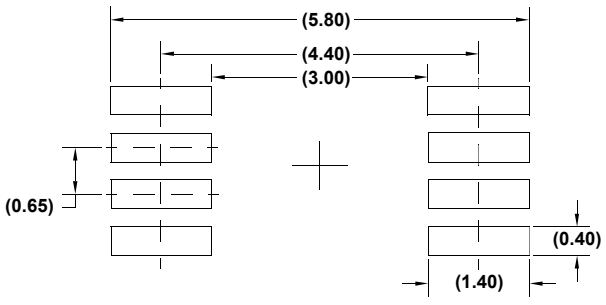




DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

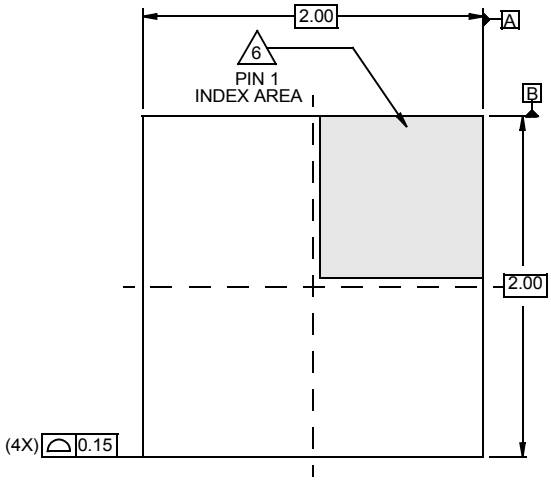
1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.

Package Outline Drawing

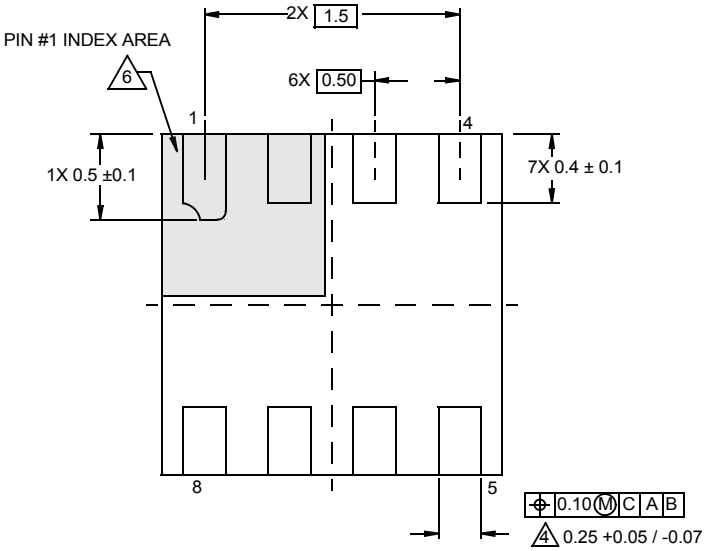
L8.2x2

8 Lead Ultra Thin Dual Flat No-Lead COL Plastic Package (UTDFN COL)

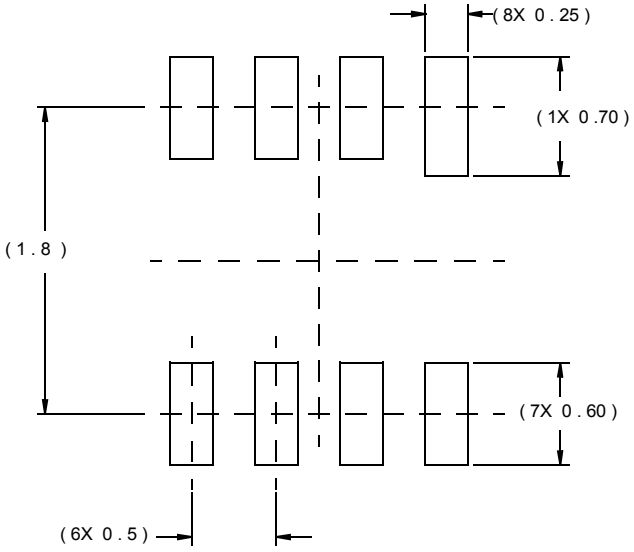
Rev 4, 05/15



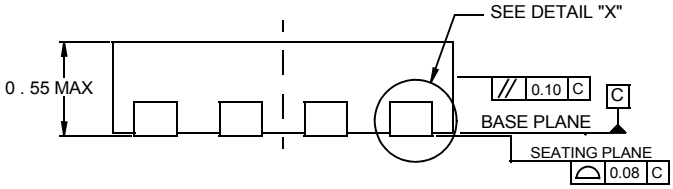
TOP VIEW



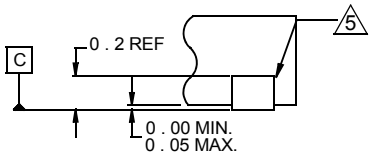
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

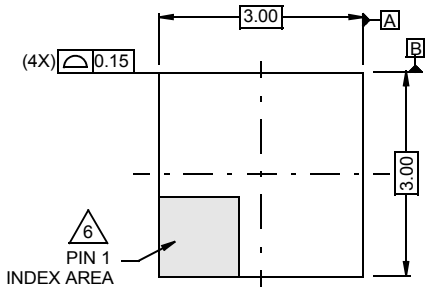
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

Package Outline Drawing

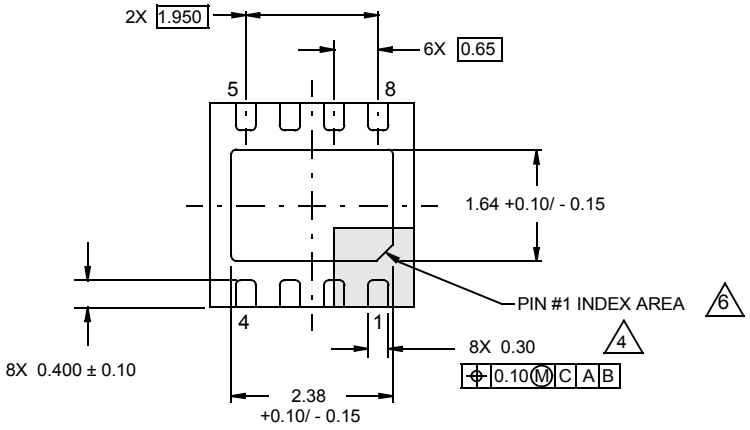
L8.3x3I

8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

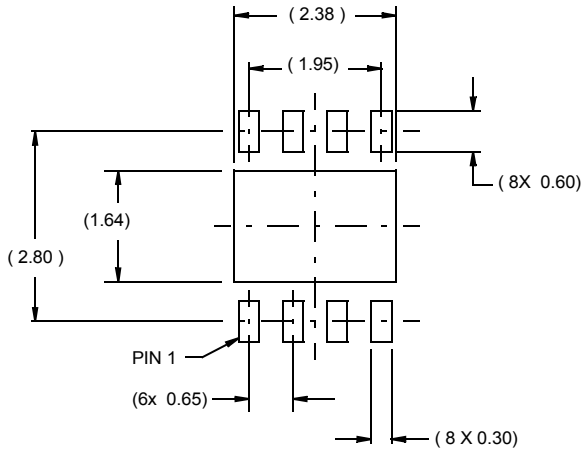
Rev 2 5/15



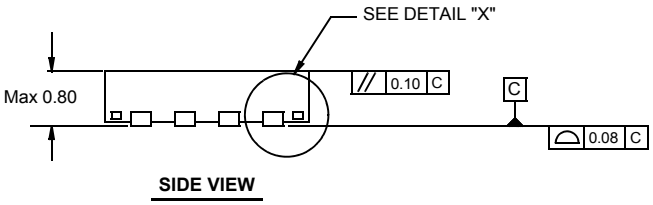
TOP VIEW



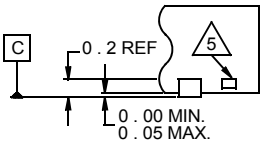
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

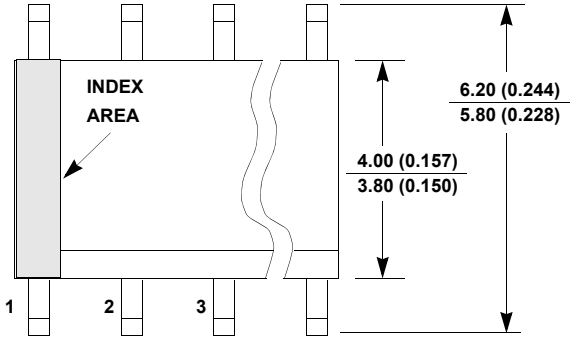
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

Package Outline Drawing

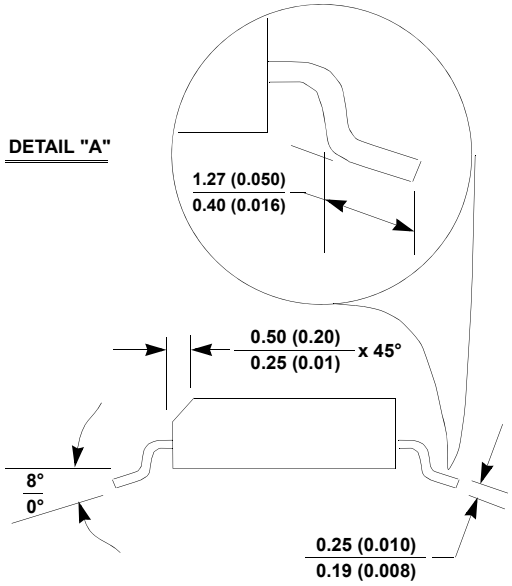
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

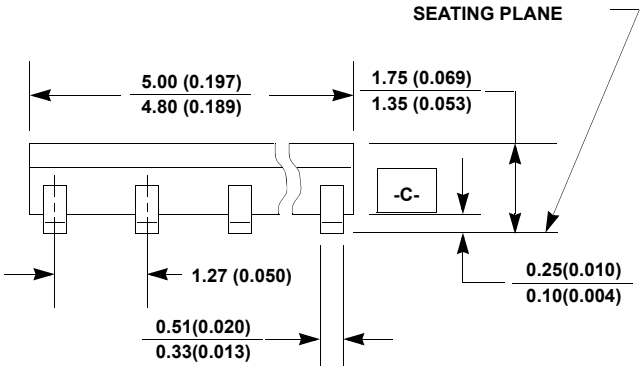
Rev 4, 1/12



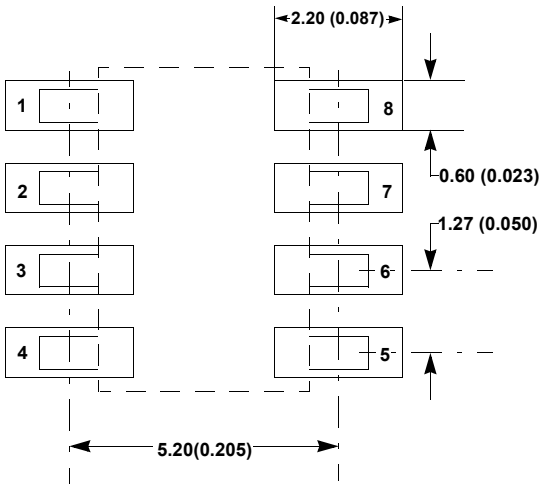
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.