

N-channel 650 V, 0.290 Ω typ., 8 A MDmesh™ M2 Power MOSFET in a PowerFLAT™ 5x6 HV package

Datasheet - preliminary data

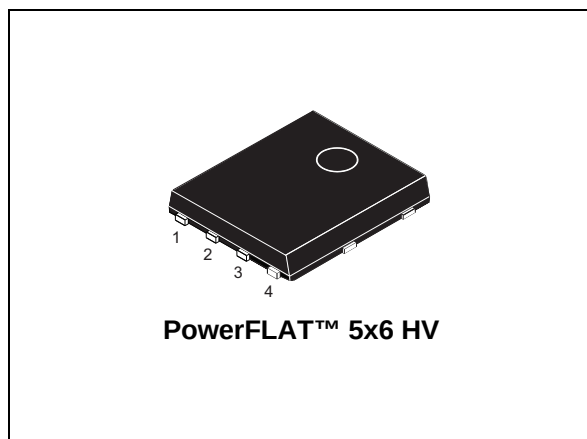
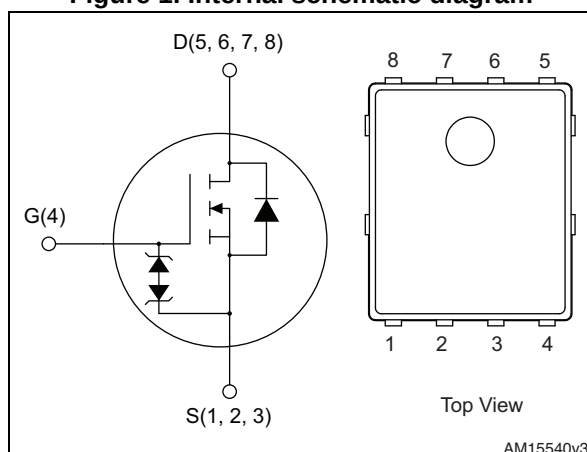


Figure 1. Internal schematic diagram



Features

Order codes	$V_{DS} @ T_{Jmax}$	$R_{DS(on)} max$	I_D
STL18N65M2	715 V	0.365 Ω	8 A

- Extremely low gate charge
- Excellent output capacitance (C_{oss}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STL18N65M2	18N65M2	PowerFLAT™ 5x6 HV	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ °C}$	8	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ °C}$	5	A
$I_{DM}^{(2)}$	Drain current (pulsed)	32	A
P_{TOT}	Total dissipation at $T_C = 25\text{ °C}$	57	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	1.8	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ °C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	120	mJ
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(4)}$	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. The value is rated according to $R_{thj-case}$ and limited by package
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 8\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DSpeak} \leq V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$
4. $V_{DS} \leq 520\text{ V}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2.2	°C/W
$R_{thj-amb}^{(1)}$	Thermal resistance junction-amb max	59	°C/W

1. When mounted on 1inch² FR-4 board, 2 oz Cu

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	650			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 650\text{ V}$			1	μA
		$V_{DS} = 650\text{ V}$, $T_C = 125\text{ °C}$			100	μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25\text{ V}$			± 10	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 4\text{ A}$		0.290	0.365	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	764	-	pF
C_{oss}	Output capacitance		-	35.5	-	pF
C_{rss}	Reverse transfer capacitance		-	1.2	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Output equivalent capacitance	$V_{DS} = 0\text{ to }520\text{ V}$, $V_{GS} = 0$	-	175.5	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	6	-	Ω
Q_g	Total gate charge	$V_{DD} = 520\text{ V}$, $I_D = 12\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 3)	-	21.5	-	nC
Q_{gs}	Gate-source charge		-	3.2	-	nC
Q_{gd}	Gate-drain charge		-	11.3	-	nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 325\text{ V}$, $I_D = 6.5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 6\text{ V}$ (see Figure 7)	-	11	-	ns
t_r	Rise time		-	7.5	-	ns
$t_{d(off)}$	Turn-on delay time		-	46	-	ns
t_f	Fall time		-	12.5	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		8	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		32	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 8\text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 12\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 4)	-	331		ns
Q_{rr}	Reverse recovery charge		-	3.4		μC
I_{RRM}	Reverse recovery current		-	20.5		A
t_{rr}	Reverse recovery time	$V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, $I_{SD} = 12\text{ A}$ $T_j = 150\text{ }^\circ\text{C}$ (see Figure 4)	-	462		ns
Q_{rr}	Reverse recovery charge		-	4.6		μC
I_{RRM}	Reverse recovery current		-	20		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

3 Test circuits

Figure 2. Switching times test circuit for resistive load

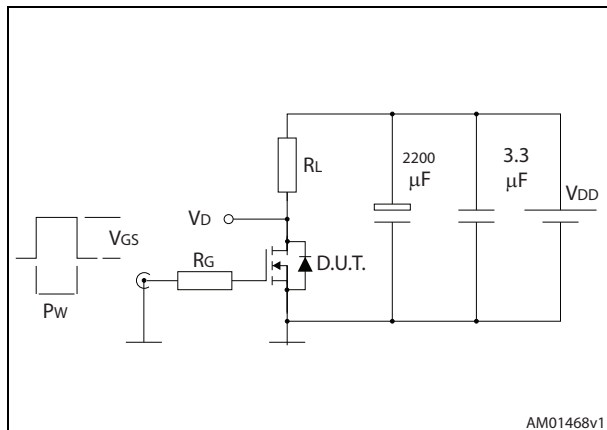


Figure 3. Gate charge test circuit

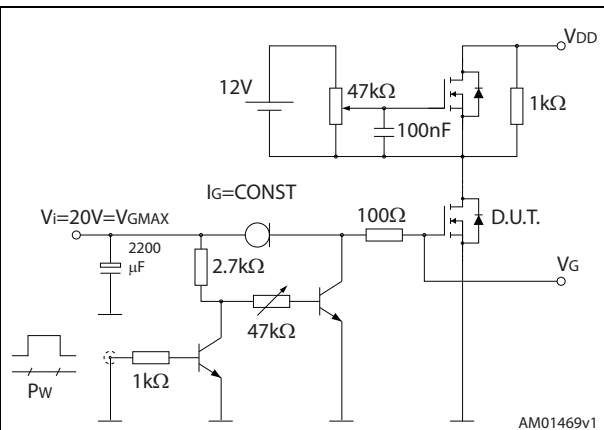


Figure 4. Test circuit for inductive load switching and diode recovery times

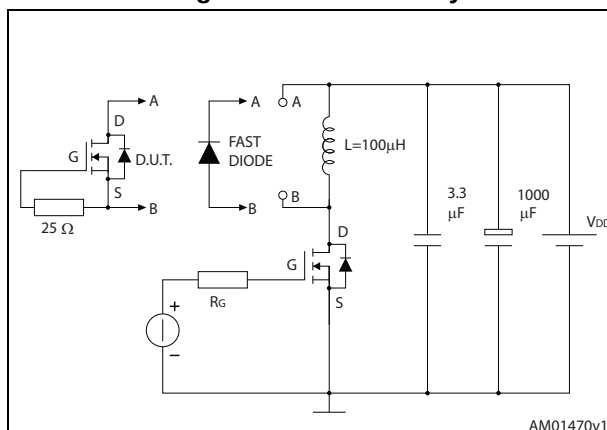


Figure 5. Unclamped inductive load test circuit

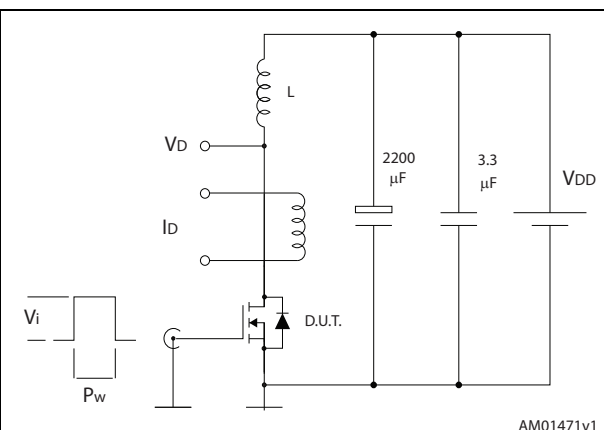


Figure 6. Unclamped inductive waveform

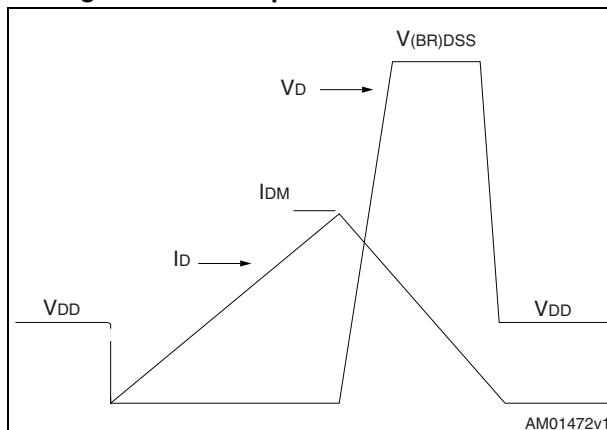
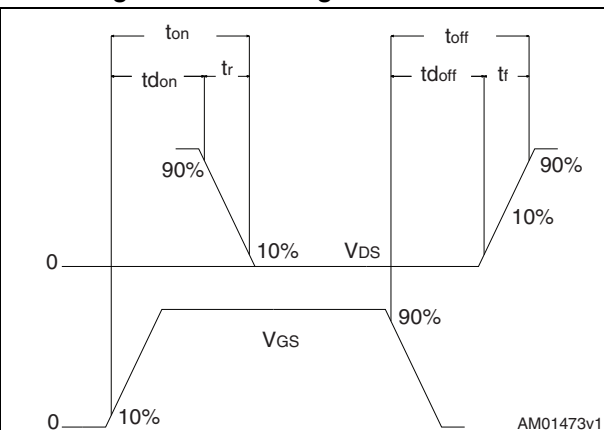


Figure 7. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Figure 8. PowerFLAT™ 5x6 HV drawing

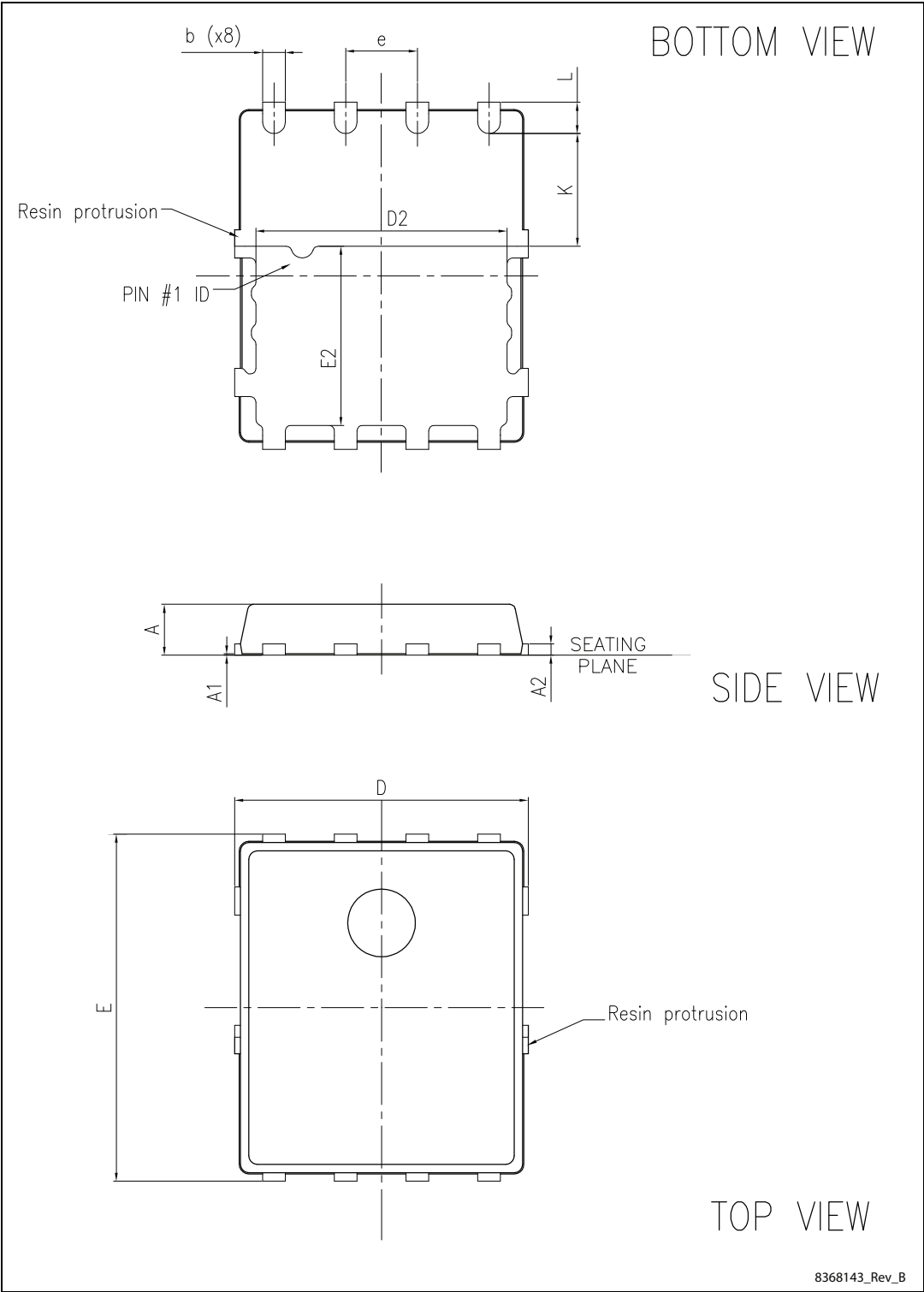
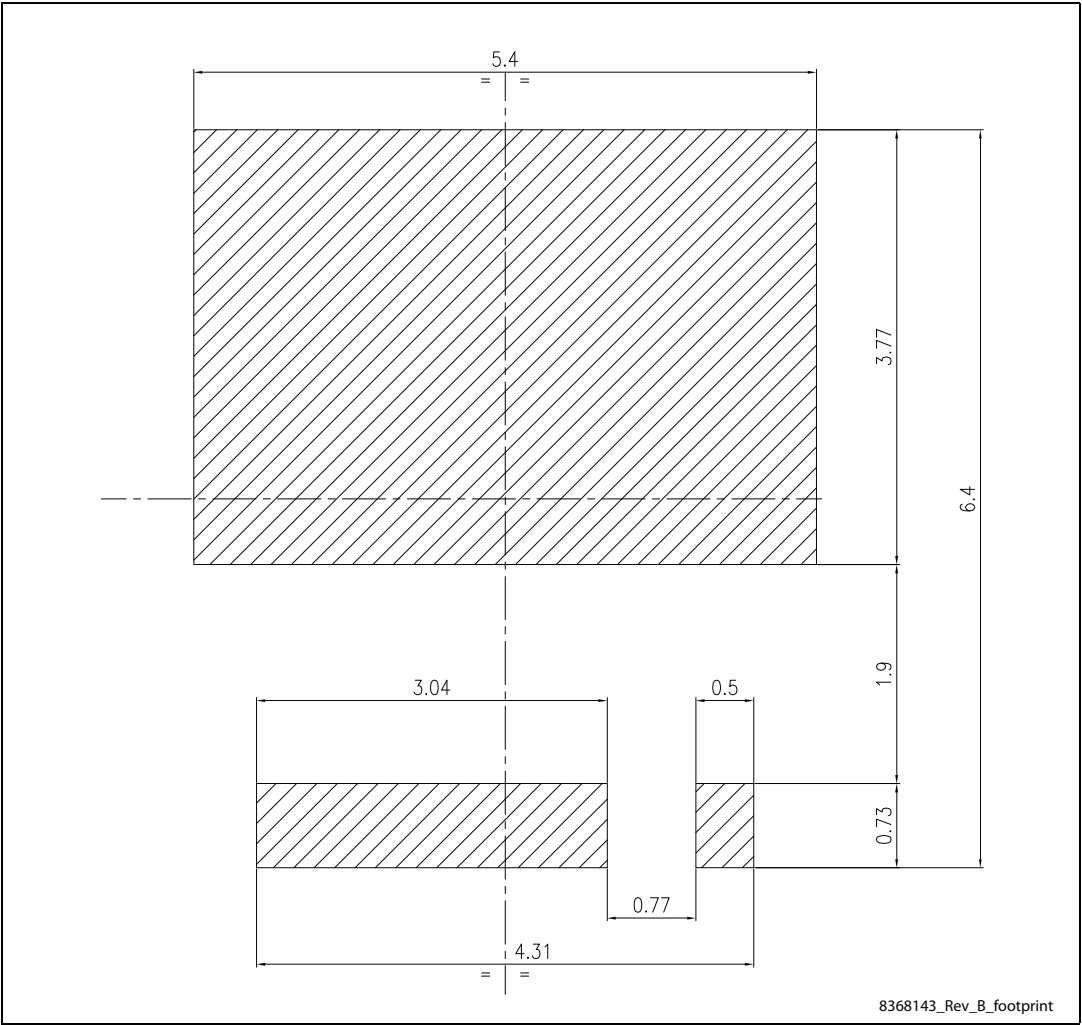


Table 8. PowerFLAT™ 5x6 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	5.95	6.15	6.35
D2	4.30	4.40	4.50
E2	3.10	3.20	3.30
e		1.27	
L	0.50	0.55	0.60
K	1.90	2.00	2.10

Figure 9. PowerFLAT™ 5x6 HV recommended footprint (dimensions are in mm)



5 Packaging mechanical data

Figure 10. PowerFLAT™ 5x6 tape^(a)

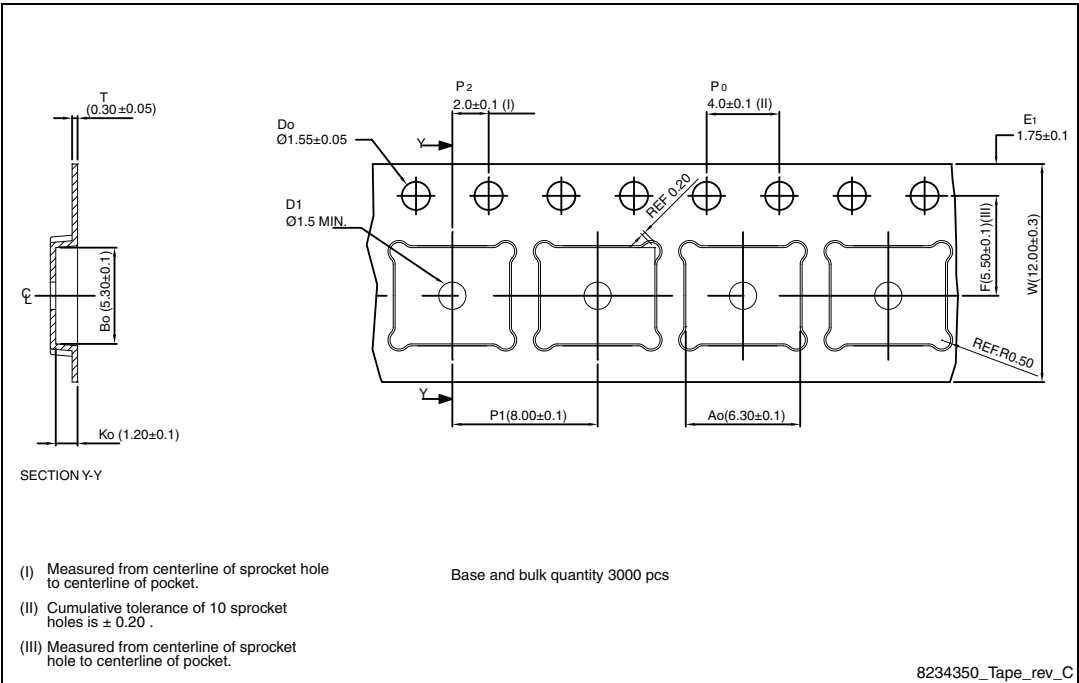
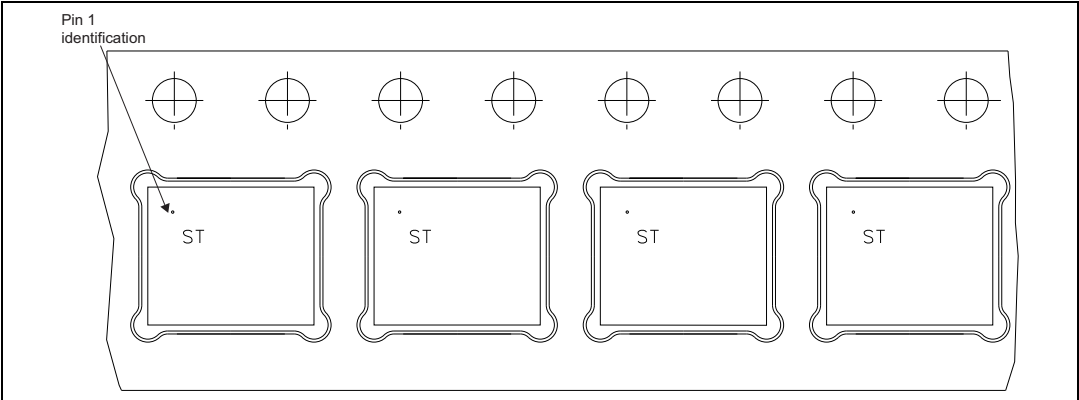
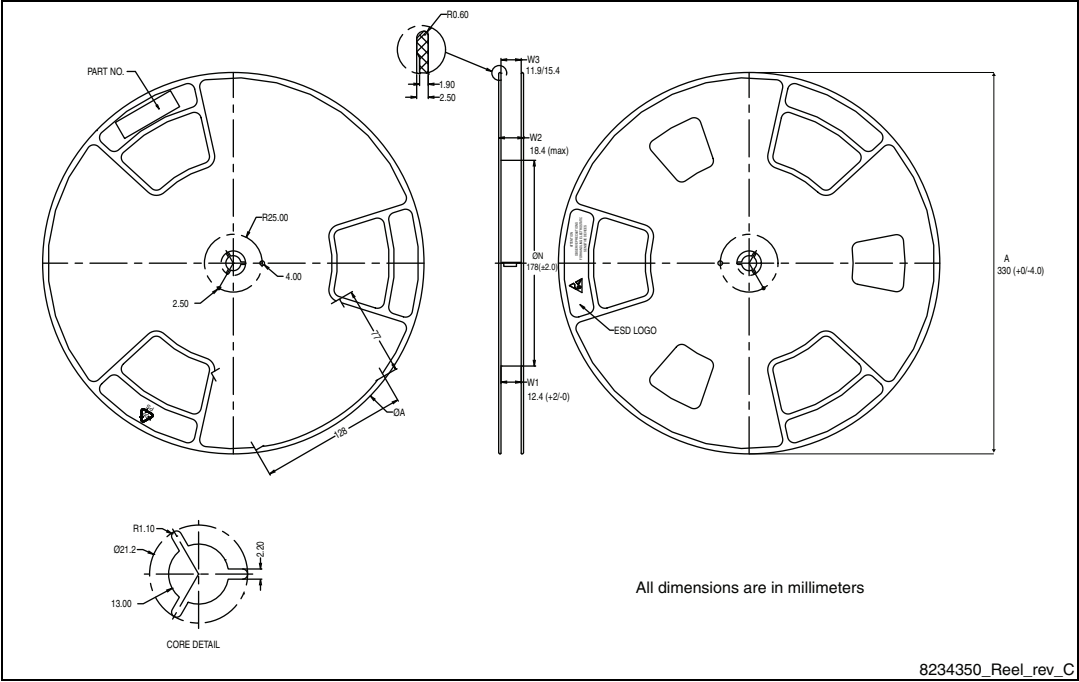


Figure 11. PowerFLAT™ 5x6 package orientation in carrier tape



a. All dimensions are in millimeters.

Figure 12. PowerFLAT™ 5x6 reel



6 Revision history

Table 9. Document revision history

Date	Revision	Changes
14-Mar-2014	1	First release.
25-Mar-2014	2	Updated title and features on cover page. Updated Table 4: On /off states and Table 5: Dynamic Inserted P _{TOT} value in Table 2: Absolute maximum ratings . Minor text changes.
02-Oct-2014	3	Updated values in Table 2: Absolute maximum ratings , Table 4: On /off states , Table 5: Dynamic , Table 6: Switching times and Table 7: Source drain diode . Updated title, features and description in cover page. Minor text changes.

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