

### FEATURES

- Bias Current Range 4 mA to 200 mA**
- Monitor Photodiode Current 50  $\mu$ A to 1200  $\mu$ A**
- Closed-Loop Control of Average Power**
- Laser FAIL and Laser DEGRADE Alarms**
- Automatic Laser Shutdown, ALS**
- Full Current Parameter Monitoring**
- 5 V Operation**
- 40°C to +85°C Temperature Range**
- 5 mm  $\times$  5 mm 32-Lead LFCSP Package**

### APPLICATIONS

**Fiber Optic Communication**

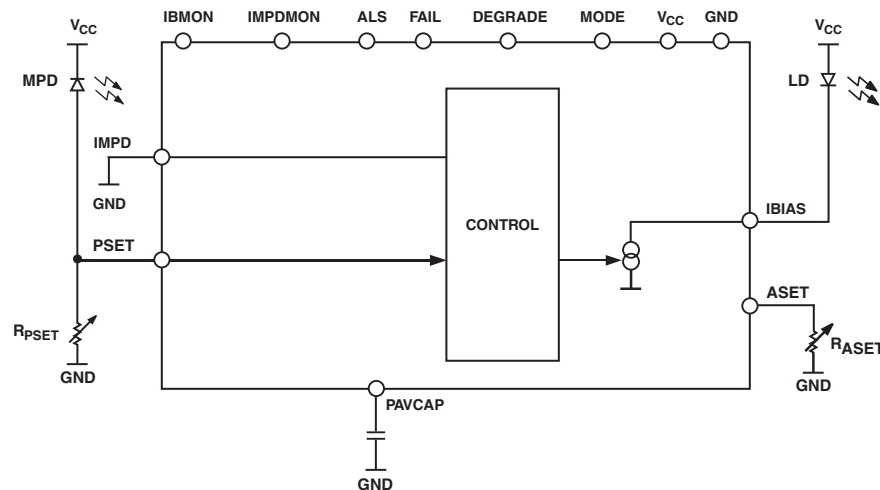
### GENERAL DESCRIPTION

The ADN2830 provides closed-loop control of the average optical power of a continuous wave (CW) laser diode (LD) after initial factory setup. The control loop adjusts the laser IBIAS to maintain a constant back facet monitor photodiode (MPD) current and thus a constant laser optical power. The external PSET resistor is adjusted during factory setup to set the desired optical power.  $R_{PSET}$  is set at  $1.23/I_{AV}$ , where  $I_{AV}$  is the MPD current corresponding to the desired optical power. Programmable alarms are provided for laser fail (end of life) and laser degrade (impending fail).

To provide monitoring of the MPD current, the MPD can be connected to the IMPD pin. In this case, the MPD current is mirrored to the IMPDMON pin to provide a monitor and internally to the PSET pin to close the control loop.

By closing the feedback using IBMON rather than an MPD connected to PSET, the device is configured to control a constant current in the laser rather than a constant optical output power.

### FUNCTIONAL BLOCK DIAGRAM



REV. A

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# ADN2830—SPECIFICATIONS ( $V_{CC} = 5\text{ V} \pm 10\%$ . All specifications $T_{MIN}$ to $T_{MAX}$ , unless otherwise noted<sup>1</sup>. Typical values as specified at 25°C.)

Parameter	Min	Typ	Max	Unit	Conditions/Comments
LASER BIAS (BIAS)					
Output Current IBIAS	4		200	mA	
Compliance Voltage	1.2		$V_{CC}$	V	
IBIAS during ALS			40	$\mu\text{A}$	
ALS Response Time		10		$\mu\text{s}$	
MONITOR PD (IMPD)					
Current	50		1200	$\mu\text{A}$	
Input Voltage			1.6	V	
POWER SET INPUT (PSET)					
Capacitance			80	pF	
Input Current	50		1200	$\mu\text{A}$	
Voltage	1.15	1.23	1.35	V	
ALARM SET (ASET)					
Allowable Resistance Range	1.2		13	k $\Omega$	
Voltage	1.15	1.23	1.35	V	
Hysteresis		5		%	
LOGIC INPUTS (ALS, MODE)					
$V_{IH}$	2.4			V	
$V_{IL}$			0.8	V	
ALARM OUTPUTS (Internal 30 k $\Omega$ Pull-Up)					
$V_{OH}$	2.4			V	
$V_{OL}$			0.4	V	
IBMON IMPDMON					
IBMON, Division Ratio		100		A/A	
IMPDMON Division Ratio		1		A/A	
Compliance Voltage	0		$V_{CC} - 1.2$	V	
SUPPLY					
$I_{CC}^2$		25		mA	IBIAS = 0
$V_{CC}$	4.5	5.0	5.5	V	

## NOTES

<sup>1</sup>Temperature range: -40°C to +85°C.

<sup>2</sup> $I_{CC}$  for power calculation is the typical  $I_{CC}$  given.

Specifications subject to change without notice.

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

(T<sub>A</sub> = 25°C, unless otherwise noted.)

V <sub>CC</sub> to GND	7 V
Digital Inputs (ALS, Mode)	-0.3 V to V <sub>CC</sub> + 0.3 V
Operating Temperature Range	
Industrial	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature (T <sub>J</sub> Max)	150°C
θ <sub>JA</sub> Thermal Impedance <sup>2</sup>	32°C/W
32-Lead LFCSP Package,	
Power Dissipation	(T <sub>J</sub> Max - T <sub>A</sub> )/θ <sub>JA</sub> mW
Lead Temperature (Soldering 10 sec)	300°C

## NOTES

<sup>1</sup>Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

<sup>2</sup>θ<sub>JA</sub> is defined when the part is soldered onto a 4-layer board.

## ORDERING GUIDE

Model	Temperature Range	Package Description
ADN2830ACP32	-40°C to +85°C	32-Lead LFCSP
ADN2830ACP32-REEL7	-40°C to +85°C	32-Lead LFCSP
ADN2830ACP32-REEL	-40°C to +85°C	32-Lead LFCSP

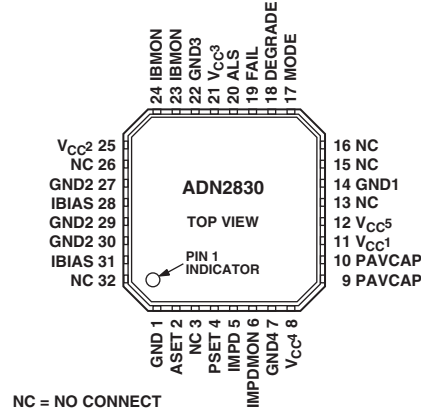
## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADN2830 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



# ADN2830

## PIN CONFIGURATION



## PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	GND	Supply Ground
2	ASET	Alarm Current Threshold Set Pin
3	NC	No Connect
4	PSET	Average Optical Power Set Pin
5	IMPD	Monitor Photodiode Input
6	IMPDMON	Mirrored Current from Monitor Photodiode—Current Source
7	GND4	Supply Ground
8	V <sub>CC</sub> 4	Supply Voltage
9	PAVCAP	Average Power Loop Capacitor
10	PAVCAP	Average Power Loop Capacitor
11	V <sub>CC</sub> 1	Supply Voltage
12	V <sub>CC</sub> 5	Supply Voltage
13	NC	No Connect
14	GND1	Supply Ground
15	NC	No Connect
16	NC	No Connect
17	MODE	Mode Select: Tied to ALS = Standalone, High = Parallel Current Booster
18	DEGRADE	DEGRADE Alarm Output
19	FAIL	FAIL Alarm Output
20	ALS	Automatic Laser Shutdown
21	V <sub>CC</sub> 3	Supply Voltage
22	GND3	Supply Ground
23	IBMON	Bias Current Monitor Output—Current Source
24	IBMON	Bias Current Monitor Output—Current Source
25	V <sub>CC</sub> 2	Supply Voltage
26	NC	No Connect
27	GND2	Supply Ground
28	IBIAS	Laser Diode Bias Current
29	GND2	Supply Ground
30	GND2	Supply Ground
31	IBIAS	Laser Diode Bias Current
32	NC	No Connect

## GENERAL

Laser diodes have current-in to light-out transfer functions as shown in Figure 1. Two key characteristics of this transfer function are the threshold current,  $I_{TH}$ , and slope in the linear region beyond the threshold current, referred to as slope efficiency (LI).

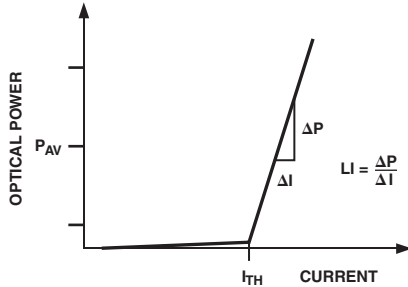


Figure 1. Laser Transfer Function

## CONTROL

A monitor photodiode (MPD) is required to control the laser diode. The MPD current is fed into the ADN2830 to control the power, continuously adjusting the bias current in response to the laser's changing threshold current and light to current (LI) slope (slope efficiency).

The ADN2830 uses automatic power control (APC) to maintain a constant power over time and temperature.

The average power is controlled by the  $R_{PSET}$  resistor connected between the PSET pin and ground. The PSET pin is kept 1.23 V above GND. For an initial setup, the  $R_{PSET}$  resistor can be calculated using the following formula.

$$R_{PSET} = \frac{1.23 V}{I_{AV}}$$

where  $I_{AV}$  is average MPD current.

Note the  $I_{PSET}$  will change from device to device. It is not required to know exact values for LI and MPD optical coupling.

## LOOP BANDWIDTH SELECTION

Capacitor values greater than 22 nF are used to set the actual loop bandwidth. This capacitor is placed between the PAVCAP pin and ground. It is important that the capacitor is a low leakage multilayer ceramic with an insulation resistance greater than 100 GΩ or a time constant of 1000 sec, whichever is less.

## ALARMS

The ADN2830 has two active high alarms, DEGRADE and FAIL. A resistor between ground and the ASET pin is used to set the current at which these alarms are raised. The current through the ASET resistor is a ratio of  $(N \times 200):1$  to the FAIL alarm threshold ( $N$  is the number of ADN2830s in parallel). The DEGRADE alarm will be raised at 90% of this level.

Example:

$$I_{FAIL} = 50 \text{ mA}, N = 1 \therefore I_{DEGRADE} = 45 \text{ mA}$$

$$I_{ASET} = \frac{I_{BLASTRIP}}{N \times 200} = \frac{50 \text{ mA}}{200} = 250 \mu\text{A}$$

$$*R_{ASET} = \frac{1.23 V}{I_{ASET}} = \frac{1.23}{250 \mu\text{A}} = 4.92 \text{ k}\Omega$$

The laser degrade alarm, DEGRADE, gives a warning of imminent laser failure if the laser diode degrades further or environmental conditions continue to stress the laser diode, e.g., increasing temperature.

The laser fail alarm, FAIL, is activated when:

- The ASET threshold is reached.
- The ALS pin is set high. This shuts off the modulation and bias currents to the laser diode, resulting in the MPD current dropping to zero.

DEGRADE will only be raised when the bias current exceeds 90% of the ASET current.

## MONITOR CURRENTS

IBMON and IMPDMON are current controlled current sources from  $V_{CC}$ . They mirror the bias and MPD current for increased monitoring functionality. An external resistor to GND gives a voltage proportional to the current monitored. If the IMPDMON function is not used, the IMPD pin must be grounded and the monitor photodiode must be tied directly to the PSET pin.

## AUTOMATIC LASER SHUTDOWN

When ALS is logic high, the bias current is turned off. Correct operation of ALS can be confirmed by the fail alarm being raised when ALS is asserted. Note that this is the only time DEGRADE will be low while FAIL is high.

## MODE

The MODE feature on the ADN2830 allows the user to operate more than one ADN2830 in parallel current boosting mode to achieve up to  $N \times 200$  mA of bias current ( $N$  is the number of ADN2830s in parallel). When using parallel boosting mode, one device is run as the master, the other as the slave. The MODE pin on the master is tied to ALS and the MODE pin on the slave is tied high (see Figure 3 for reference circuit).

## ALARM INTERFACES

The FAIL and DEGRADE outputs have an internal 30 kΩ pull-up resistor that is used to pull the digital high value to  $V_{CC}$ . However, the alarm output may be overdriven with an external resistor allowing the alarm interfacing to non- $V_{CC}$  levels. Non- $V_{CC}$  alarm output levels must be below the  $V_{CC}$  used for the ADN2830.

\*The smallest value for  $R_{ASET}$  is 1.2 kΩ, as this corresponds to the IBIAS maximum of  $N \times 200$  mA.

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## POWER CONSUMPTION

The ADN2830 die temperature must be kept below 125°C. The exposed paddle should be connected in such a manner that it is at the same potential as the ADN2830 ground pins. Power consumption can be calculated using the following formulas.

$$T_{DIE} = T_{AMBIENT} + \theta_{JA} \times P$$

$$I_{CC} = I_{CCMIN}$$

$$P = V_{CC} \times I_{CC} + (IBIAS \times V_{BIAS\_PIN})$$

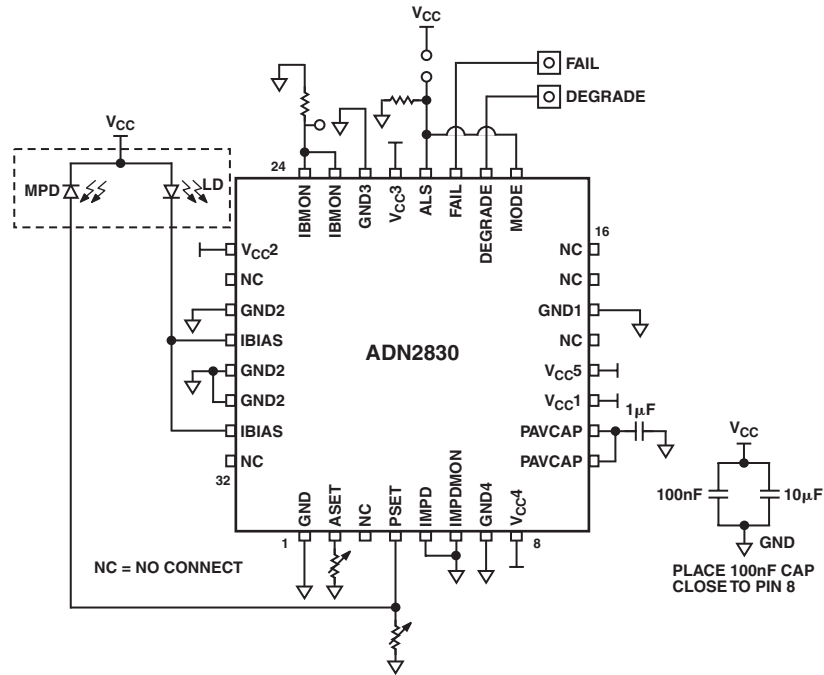


Figure 2. Test Circuit, Standalone Mode, IMPD Input Not Used

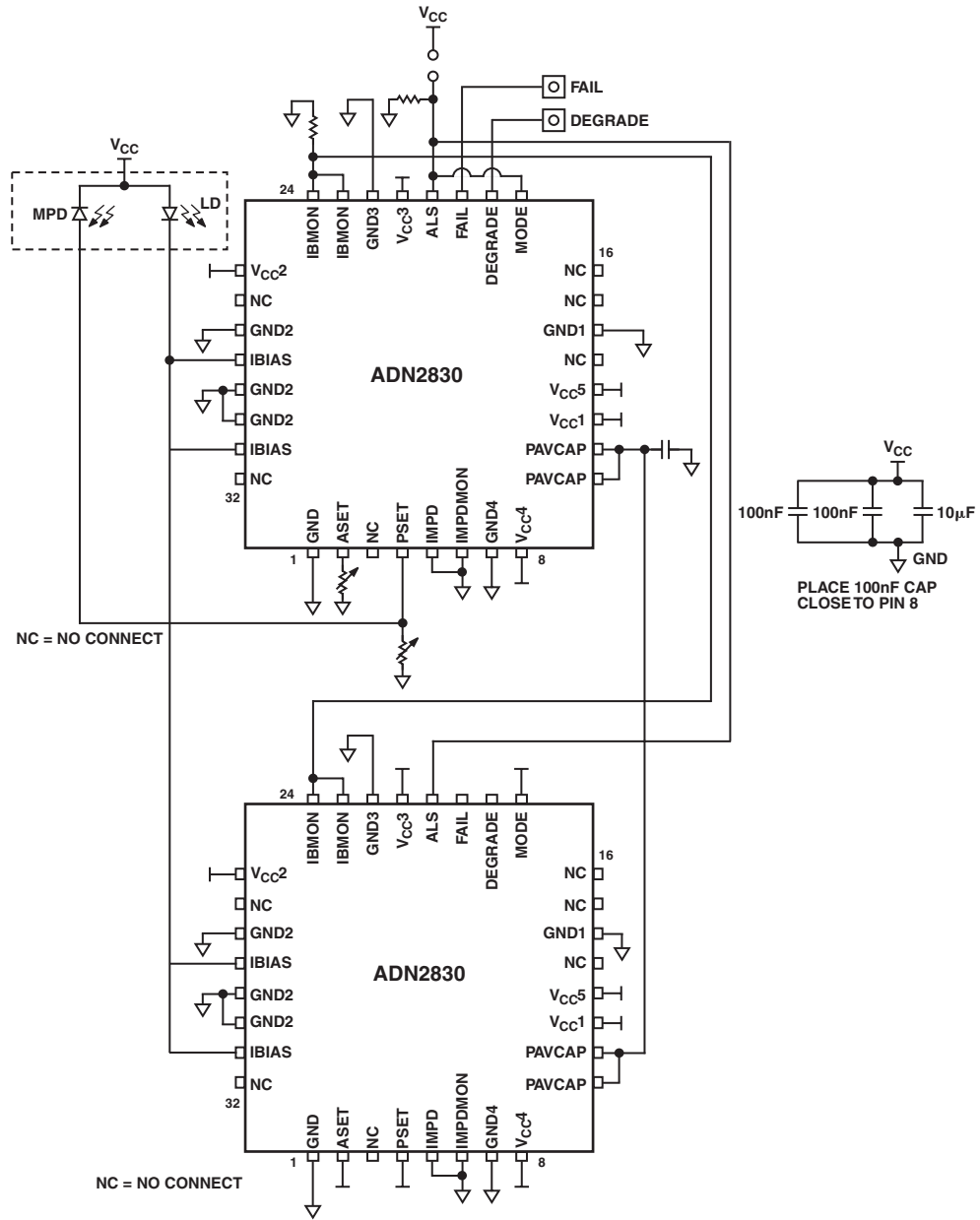
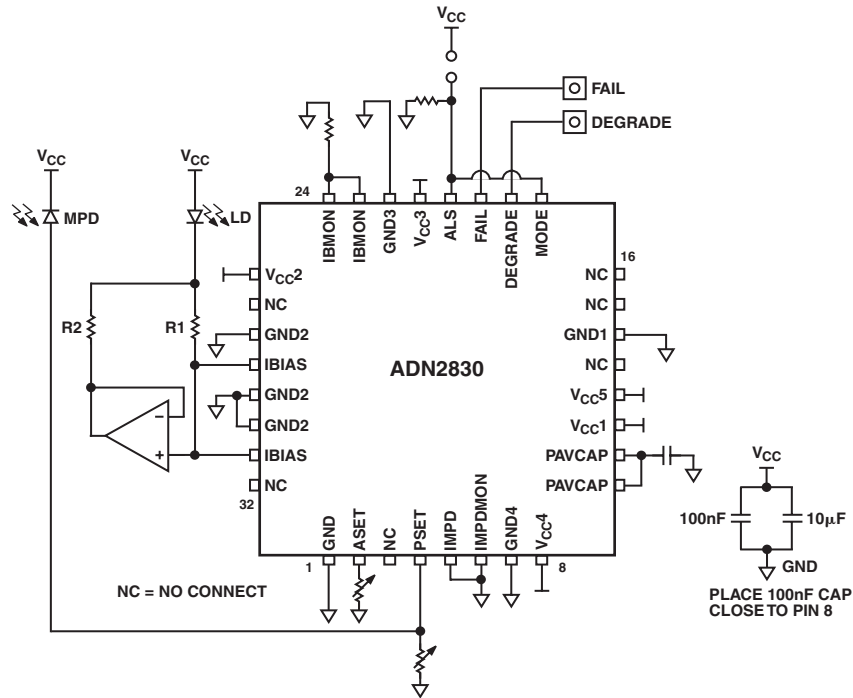


Figure 3. Test Circuit, Second ADN2830 Used in Parallel Current Boosting Mode to Achieve 400 mA Max IBIAS

# ADN2830



## NOTES

1. FOR DIGITAL CONTROL, REPLACE  $R_{PSET}$  WITH A DIGITAL POTENTIOMETER FROM ANALOG DEVICES: ADN2850 10-BIT RESOLUTION, 35 ppm/°C TC, EEPROM; AD5242 8-BIT RESOLUTION, 30 ppm/°C TC.
2. TOTAL CURRENT TO LASER =  $IBIAS + IBIAS \times R1/R2$ .
3. FOR BEST ACCURACY, SIZE  $R1$  TO HAVE A MAXIMUM VOLTAGE DROP ACROSS IT WITHIN THE HEADROOM CONSTRAINTS.
4. FOR 250 mA EXTRA  $IBIAS$  (450 mA TOTAL) FROM AMP1, USE AD8591 AMPLIFIER. AMP1 IS THE OPERATIONAL AMPLIFIER SHOWN IN THIS FIGURE.
5. FOR 350 mA EXTRA  $IBIAS$  (550 mA TOTAL) FROM AMP1, USE ANALOG DEVICES' SSM2211 AMPLIFIER. AMP1 IS THE OPERATIONAL AMPLIFIER SHOWN IN THIS FIGURE.

Figure 4. The ADN2830 Configured with Current Multiplier

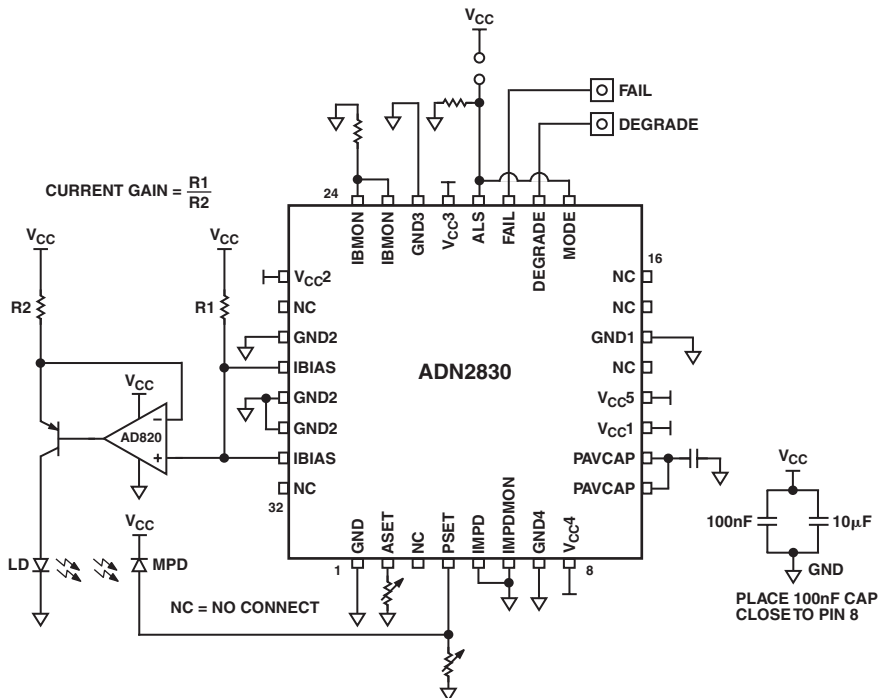


Figure 5. The ADN2830 Configured as Average Power Controller (Bias Current Sourced)



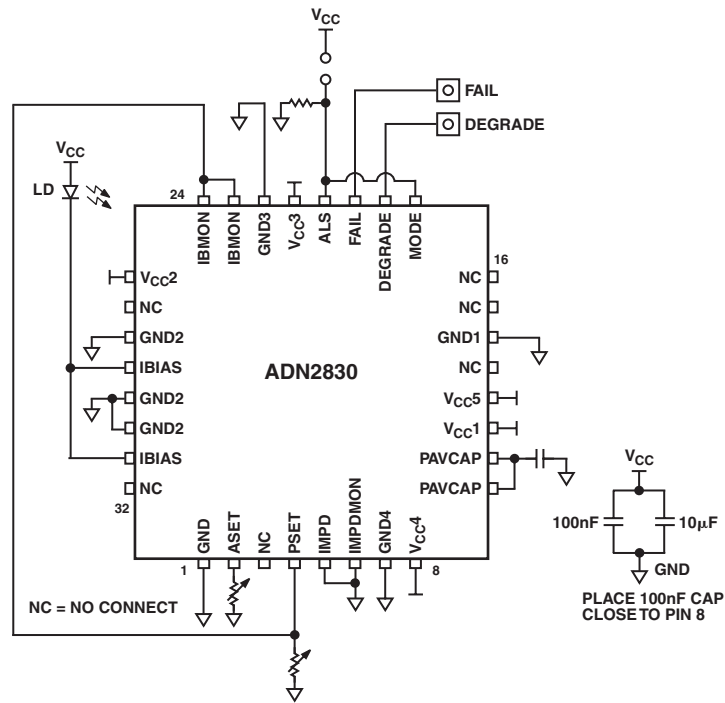
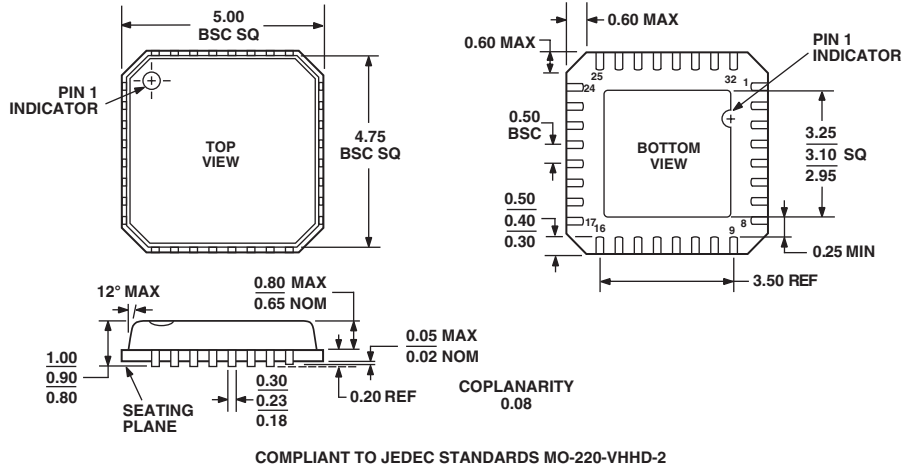


Figure 6. The ADN2830 Configured as a Controlled Current Source by Feeding Back the Bias Monitor Current to  $R_{PSET}$

# ADN2830

## OUTLINE DIMENSIONS 32-Lead Frame Chip Scale Package [LFCSP] (CP-32)

Dimensions shown in millimeters



## Revision History

Location	Page
6/03—Data Sheet changed from REV. 0 to REV. A.	
Changes to ABSOLUTE MAXIMUM RATINGS .....	3
Updated OUTLINE DIMENSIONS .....	10







Поставка электронных компонентов

**Юридический адрес организации:**  
198099, г. Санкт-Петербург, ул. Калинина, дом 2, кор. 4, лит А.  
**Фактический адрес организации:**  
198099, г. Санкт-Петербург, ул. Калинина, дом 2, кор. 4, лит А.  
ИНН 780277764  
КПП 780501001  
Р/С 40702810422510004035 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в Санкт-Петербурге К/С 30101810900000000703  
БИК 044030703  
**Телефон:** 8 (812) 309-44-11 (многоканальный)  
**Факс:** 8 (812) 309-44-11  
**Электронная почта:** [sales@timechips.ru](mailto:sales@timechips.ru)  
**Сайт:** [timechips.ru](http://timechips.ru)

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<http://www.timechips.ru/>

<http://lcd-timechips.ru/>

**Телефон: +7 (812) 309-44-11 доб. 141**

**Факс: +7 (812) 309-44-11 доб. 152**

**Моб. Тел. +7 (905) 232-40-65**

**Skype: time.chips5**

**Электронная почта: [manager1@timechips.ru](mailto:manager1@timechips.ru)**

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