High Power Negative Voltage Hot Swap Controller with Energy Monitor

FEATURES

- **Drives Two Gates for High Power Applications**
- **Configurable Parallel, Staged Start or Single Modes**
- **Protects MOSFET with SOA Timer**
- **Programmable 15mV to 30mV Current Limit Sense Voltage with 2% Accuracy and Adjustable Foldback**
- **8-Bit to 16-Bit Gear-Shift ADC with 0.5% Accuracy**
- **Monitors Voltages, Currents, Power and Energy**
- **Nonvolatile Configuration and Fault Recording**
- Floating Topology for Rugged High Voltage Operation
- Selectable Inrush Control: dV/dt or Current Limit
- I²C/SMBus or Single-Wire Broadcast Interfaces
- Min/Max ADC Measurement Logging with Alerts
- Reboots on I²C Command with Programmable Delay
- Adjustable Input UV/OV Thresholds and Hysteresis
- 44-Pin 5mm × 8mm QFN Package

APPLICATIONS

- Telecom Infrastructure
- –48V Distributed Power Systems
- Servers and Data Centers
- Power Monitors

DESCRIPTION

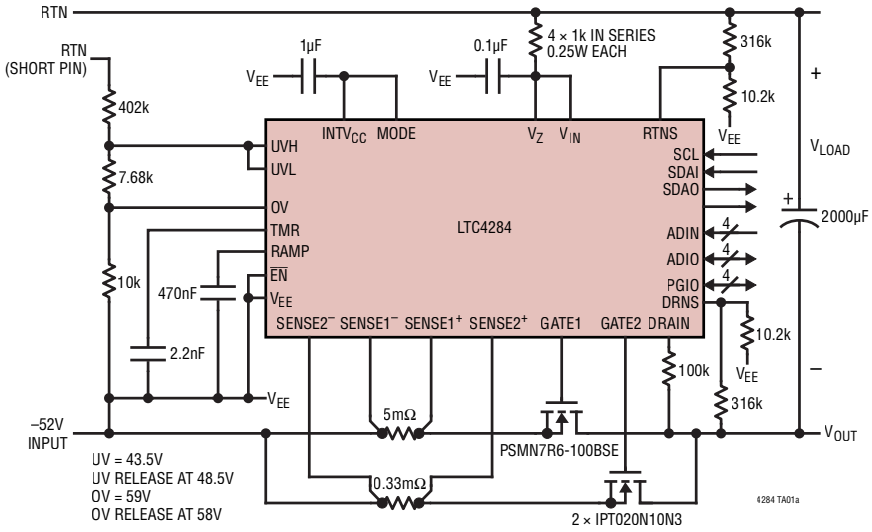
The LTC®4284 negative voltage hot swap controller drives external N-channel MOSFETs to allow a board to be safely inserted and removed from a live backplane. The dual-gate, multi-mode drivers optimize the MOSFET safe operating area (SOA) for a variety of power levels. The SOA timer limits MOSFET temperature rise for reliable protection against overstresses.

An I²C interface and onboard gear-shift ADC allow monitoring of board current, voltage, power, energy, and fault status. An available single-wire broadcast mode simplifies the interface by eliminating two isolators. The included EEPROM provides black-box capturing and nonvolatile configuration of fault behavior.

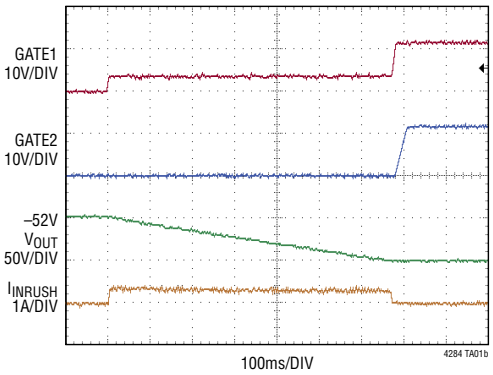
Additional features respond to input UV/OV, interrupt the host when a fault has occurred, notify when output power is good, detect insertion of a board, turn off the MOSFETs if an external supply monitor fails to indicate power good within a timeout period, and auto-reboot after a programmable delay following a host commanded turn-off.

TYPICAL APPLICATION

–52V/2500W Hot Swap Controller with Telemetry



Startup Behavior



Rev. A

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ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Supply Voltage:
- V_{IN} ..... –0.3V to 12.5V
- $INTV_{CC}$ ..... –0.3V to 5.5V

Input Voltages
- V_Z (Note 3) ..... –0.3V to 16V
- DRAIN (Note 4) ..... –0.3V to 3.2V
- EN# (Note 5) ..... –0.3V to 6V
- MODE ..... –0.3V to V_{IN} + 0.3V
- UVL, UVH ..... –0.3V to 16V
- ADC^+ , $ADC^–$, ADIN1-4, ADR0, ADR1, DRNS, OV, RTNS, SCL, SDAI, $SENSE1^+$, $SENSE1^–$, $SENSE2^+$, $SENSE2^–$, VOUTTH, WP ..... –0.3V to $INTV_{CC}$ + 0.3V

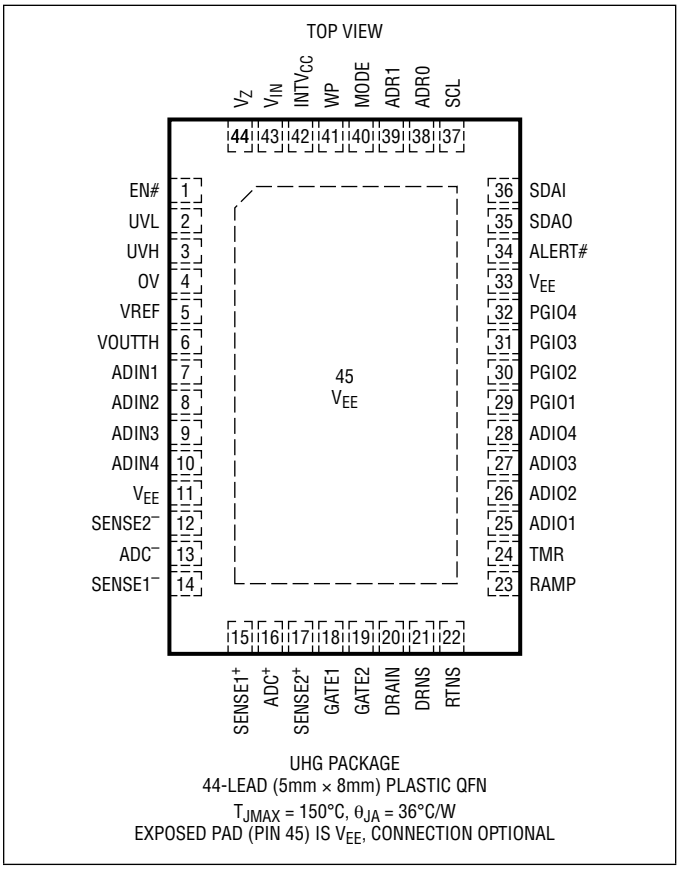
Output Voltages
- GATE1, GATE2, PGIO1-4 ..... –0.3V to V_{IN} + 0.3V
- VREF ..... –0.3V to 4.5V
- ADIO1-4, RAMP, TMR ..... –0.3V to $INTV_{CC}$ + 0.3V
- ALERT#, SDAO ..... –0.3V to 5.5V

Input Currents:
- V_Z 50mA
- DRAIN 1.5mA
- EN# 5mA

Operating Ambient Temperature Range
- LTC4284C ..... 0°C to 70°C
- LTC4284I ..... –40°C to 85°C
- LTC4284H ..... –40°C to 125°C

Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UHG PACKAGE
44-LEAD (5mm × 8mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 36°C/W
EXPOSED PAD (PIN 45) IS V_{EE}, CONNECTION OPTIONAL

ORDER INFORMATION

TUBE	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4284CUHG#PBF	LTC4284CUHG#TRPBF	4284	44-Lead (5mm × 8mm) Plastic QFN	0°C to 70°C
LTC4284IUHG#PBF	LTC4284IUHG#TRPBF	4284	44-Lead (5mm × 8mm) Plastic QFN	–40°C to 85°C
LTC4284HUHG#PBF	LTC4284HUHG#TRPBF	4284	44-Lead (5mm × 8mm) Plastic QFN	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, I_{IN} + I_{VZ} = 4mA with V_{IN} Connected to V_Z. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
V_{IN}	Shunt Regulated Voltage at V_{IN}	I_{IN} + I_{VZ} = 4mA	●	10.8	11.5	12	V
ΔV_{IN}	Load Regulation at V_{IN}	I_{IN} + I_{VZ} = 4mA to 35mA	●		250	500	mV
I_{IN}	V_{IN} Supply Current	V_{IN} = 10.5V	●		2.5	4	mA
$V_{IN(UVLO)}$	V_{IN} Undervoltage Lockout Threshold	V_{IN} Rising	●	7.5	8.1	8.6	V
$\Delta V_{IN(UVLO)}$	V_{IN} Undervoltage Lockout Hysteresis		●	0.4	0.5	0.6	V
I_{VZ}	V_Z Input Current	V_{IN} = 10.5V, V_Z = 15V	●			20	µA
$INTV_{CC}$	Internal 5V LDO Voltage	I_{LOAD} = 1mA to 30mA, I_{IN} + I_{VZ} = 35mA	●	4.75	5.05	5.35	V
$V_{CC(UVLO)}$	$INTV_{CC}$ Undervoltage Lockout Threshold	$INTV_{CC}$ Rising	●	3.65	4	4.3	V
$\Delta V_{CC(UVLO)}$	$INTV_{CC}$ Undervoltage Lockout Hysteresis		●	0.12	0.2	0.3	V
Gate Drive							
V_{GATE}	Gate Drive Voltage for GATE1,2		●	V_{IN} – 0.3	V_{IN}	V_{IN} + 0.3	V
$V_{GATE(TH)}$	Gate High Threshold for Asserting Power Good	GATE1,2 Rising	●	V_{IN} – 2.1	V_{IN} – 1.8	V_{IN} – 1.5	V
$V_{GATE(HYST)}$	Gate High Hysteresis		●	0.3	0.7	1.1	V
$I_{GATE(UP)}$	GATE1,2 Pull-Up Current	V_{GATE} = 4V	●	–40	–50	–75	µA
$I_{GATE(DN)}$	GATE1,2 Fast Pull-Down Current	$\Delta V_{SENSE1,2}$ = $V_{ILIM(FAST)}$ + 10mV, V_{GATE} = 7V	●	0.5	1.2	2	A
	GATE1,2 Current Limit Pull-Down Current	$\Delta V_{SENSE1,2}$ = V_{ILIM} + 5mV, V_{GATE} = 7V	●	12.5	25	50	mA
	GATE1,2 Turn Off Pull-Down Current	TMR, OV, EN# = High, UVL = Low, V_{GATE} = 7V	●	4	9	20	mA
On/Off Timing							
$t_{PHL(SENSE)}$	$\Delta V_{SENSE1,2}$ High to GATE1,2 Low Propagation Delay	ILIM = 0000b, $\Delta V_{SENSE1,2}$ Steps from 0mV to 100mV, V_{GATE} < 3V, GATE1,2 Open	●		60	150	ns
$t_{PHL(GATE)}$	GATE1,2 Turn Off Propagation Delay	TMR, OV, EN# = High, UVL = Low, V_{GATE} < 3V, GATE1,2 Open	●		0.5	1	µs
$t_{DL(DB)}$	Debounce Delay, Auto-Retry Delay Following Undervoltage or PGI Fault		●	115	128	141	ms
$t_{DL(PG)}$	Power Good Delay		●	230	256	282	ms
$t_{DL(PGIWD)}$	Power Good Input Watchdog Timer		●	461	512	563	ms
$t_{DL(RTRY)}$	Auto-Retry Delay Following Overcurrent, FET Bad or External Fault (Table 11)	COOLING_DL = 000b – 111b	●			±10	%
$t_{DL(RTCRST)}$	Auto-Retry Counter Reset Delay	OC_RETRY, FET_BAD_RETRY = 01b, 10b	●	14.8	16.4	18	s
$t_{DL(FETBAD)}$	FET Bad Fault Timer Delay (Table 11)	FTBD_DL = 00b – 11b	●			±10	%
$t_{DL(RBT)}$	Auto-Reboot Delay (Table 23)	After RBT_EN Bit is Set Via I^2C Interface, RBT_DL = 000b – 111b	●			±10	%
dV/dt Control							
I_{RAMP}	RAMP Output Current	Startup Only, dV/dt Control Enabled	●	–2.25	–2.5	–2.75	µA
$I_{RAMP(DN)}$	RAMP Discharge Current	V_{RAMP} = 1.2V	●	1	4	10	mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, I_{IN} + I_{VZ} = 4mA with V_{IN} Connected to V_Z. (Note 2)

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Drain Monitor								
$V_{D,PG(TH)}$	DRAIN Input Threshold for Power Good	DRAIN Falling		●	2	2.05	2.1	V
$\Delta V_{D,PG(HYST)}$	DRAIN Input Hysteresis for Power Good					20		mV
$V_{D,FET(TH)}$	DRAIN Input Threshold for FET Bad Timer and TMR Pull-Up Current (Table 11)	DRAIN Rising, V_{DTH} = 00b – 11b		●			±10	%
$\Delta V_{D,FET(HYST)}$	DRAIN Input Hysteresis with $V_{D,FET(TH)}$					10		mV
I_{DRAIN}	DRAIN Input Current	V_{DRAIN} = 200mV		●		0	±0.1	µA
		V_{DRAIN} = 2 V		●		0	±1	µA
Current Limit								
V_{ILIM}	Current Limit Voltage DAC Zero-Scale	ILIM = 0000b, C-Grade (Note 6) ILIM = 0000b, I-, H-Grade		● ●	14.7 14.5	15 15	15.3 15.5	mV mV
	Current Limit Voltage DAC Full-Scale	ILIM = 1111b, C-Grade (Note 6) ILIM = 1111b, I-, H-Grade		● ●	29.4 29	30 30	30.6 31	mV mV
	Current Limit Voltage DAC INL			●		0	±50	µV
ΔV_{ILIM}	Current Limit Voltage Mismatch between Channel 1 and Channel 2			●		0	±350	µV
$\alpha_{STARTUP}$	Current Limit Foldback Factor at Startup	RTNS = 1.8V, DRNS = 0, 1.8V	FB = 01b	●	45	50	55	%
			FB = 10b	●	16	20	24	%
			FB = 11b	●	7	10	13	%
α_{NORMAL}	Current Limit Foldback Factor in Normal Operation	RTNS = DRNS = 1.8V	FB = 01b	●	45	50	55	%
			FB = 10b	●	15	20	26	%
			FB = 11b	●	6	10	16	%
$V_{ILIM(FAST)}$	Fast Pull-Down Sense Threshold Voltage	ILIM = 0000b		●	20	30	40	mV
		ILIM = 1111b		●	47	60	70	mV
I_{SENSE}^+	SENSE1,2$^+$ Input Current	SENSE1,2$^+$ = 33mV		●		0	±1	µA
I_{SENSE}^-	SENSE1,2$^-$ Input Current	SENSE1,2$^-$ = SENSE1,2$^+$ = 0		●	–4	–10.5	–15	µA
TMR Pin Function								
$I_{TMR(UP)}$	TMR Pull-Up Current in Current Limit							
	Onset	DRNS = 0V, TMR = 1V		●	–1.5	–2	–2.5	µA
	Startup in Foldback	dV/dt Control Disabled, DRNS = 1.8V, TMR = 1V	FB = 00b	●	–192	–202	–212	µA
			FB = 01b	●	–96	–102	–108	µA
			FB = 10b	●	–39	–42	–45	µA
			FB = 11b	●	–20	–22	–24	µA
	Startup in dV/dt	dV/dt Control Enabled, DRNS = 1.8V, TMR = 1V		●	–192	–202	–212	µA
	Hard Short in Normal Operation	DRNS = 1.8V, TMR = 1V		●	–192	–202	–212	µA
$I_{TMR(DN)}$	TMR Pull-Down Current	DRAIN < $V_{D,FET(TH)}$ or Start into dV/dt Control, THERM_TMR = 0, TMR = 1V		●	1.6	2	2.3	µA
$I_{TMR(RST)}$	TMR Reset Current	EN# = High, TMR = 1V		●	3	5	8	mA
$V_{TMRH(TH)}$	TMR Fault Threshold	TMR Rising		●	2.028	2.048	2.068	V
$V_{TMRH(HYST)}$	TMR Fault Hysteresis					20		mV
$V_{TMRL(TH)}$	TMR Low Status Threshold	TMR Falling		●	80	100	120	mV
$V_{TMRL(HYST)}$	TMR Low Hysteresis					20		mV

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Input Pins								
$V_{MODE(TH)}$	MODE Input Thresholds	Threshold 1		●	0.4	0.7	1	V
		Threshold 2		●	$INTV_{CC}$ – 0.85	$INTV_{CC}$ – 0.55	$INTV_{CC}$ – 0.25	V
		Threshold 3		●	$INTV_{CC}$ + 0.5	$INTV_{CC}$ + 1.5	$INTV_{CC}$ + 2.5	V
$I_{MODE(IN)}$	Allowable Leakage in Open State	Mode 1		●			±10	µA
$V_{UVH(TH)}$	UVH Input Threshold	UVH Rising		●	2.028	2.048	2.068	V
$V_{UVL(TH)}$	UVL Input Threshold	UVL Falling		●	1.815	1.833	1.851	V
$\Delta V_{UV(HYST)}$	Built-In UV Hysteresis	UVH and UVL Tied Together		●	204	215	226	mV
$\delta V_{UV(HYST)}$	UVH, UVL Minimum Hysteresis					11		mV
$V_{UVLR(TH)}$	UVL Reset Threshold	UVL Falling		●	1	1.024	1.05	V
$\Delta V_{UVLR(HYST)}$	UVL Reset Hysteresis					21		mV
$V_{OV(TH)}$	OV Input Threshold	OV Rising		●	1.392	1.406	1.42	V
$\Delta V_{OV(HYST)}$	OV Input Hysteresis			●	10	24	38	mV
$V_{OUTL(TH)}$	V_{OUT} Low Threshold	RTNS – DRNS Falling, VOUTTH = 0.8V		●	VOUTTH – 0.06	VOUTTH	VOUTTH + 0.06	V
$\Delta V_{OUTL(HYST)}$	V_{OUT} Low Hysteresis					40		mV
$V_{EN\#(TH)}$	EN# Input Threshold	EN# Falling		●	1.248	1.28	1.312	V
$\Delta V_{EN\#(HYST)}$	EN# Input Hysteresis					18		mV
$V_{WP(TH)}$	WP Input Threshold	WP Rising		●	1.2	1.65	2.1	V
$\Delta V_{WP(HYST)}$	WP Input Hysteresis					100		mV
$V_{INPUT(TH)}$	ADIO1-4, PGIO1-4 Input Threshold	ADIO1-4, PGIO1-4 Rising		●	1.248	1.28	1.312	V
$\Delta V_{INPUT(HYST)}$	ADIO1-4, PGIO1-4 Input Hysteresis					18		mV
I_{INPUT}	DRNS, EN#, OV, RTNS, UVL, UVH, VOUTTH, WP Input Current	DRNS, EN#, OV, RTNS, UVL, UVH, VOUTTH, WP = 3V		●		0	±1	µA
Output Pins								
V_{OL}	ADIO1-4, PGIO1-4 Output Low Voltage	I = 5mA		●		0.15	0.4	V
I_{LEAK}	ADIO1-4, PGIO1-4 Leakage Current	ADIO1-4 = $INTV_{CC}$, PGIO1-4 = V_{IN}		●		0	±1	µA
V_{REF}	VREF Output Voltage	I_{VREF} = –200µA, 0, 400µA		●	1.01	1.024	1.038	V
r_{REF}	V_{REF} to ADC V_{FS} Ratio	I_{VREF} = –200µA, 0, 400µA		●	0.495	0.5	0.505	
ADC								
	Resolution (No Missing Codes) (Note 6)	RTNS, ADIN1-4, ADIO1-4, DRNS, DRAIN, (ADC^+ – ADC^-), Power	ADC = 000b	●	8			Bits
			ADC = 010b	●	10			Bits
			ADC = 100b	●	12			Bits
			ADC = 110b	●	14			Bits
			ADC = xx1b	●	14	16		Bits
		($SENSE1,2^+$ – $SENSE1,2^-$), (ADIN2 – ADIN1), (ADIN4 – ADIN3), (ADIO2 – ADIO1), (ADIO4 – ADIO3)	ADC = 000b	●	7			Bits
			ADC = 010b	●	9			Bits
			ADC = 100b	●	11			Bits
			ADC = 110b	●	13			Bits
			ADC = xx1b	●	13	15		Bits

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, I_{IN} + I_{VZ} = 4mA with V_{IN} Connected to V_Z. (Note 2)

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{FS}	Full-Scale Voltage	Single-Ended Inputs				2.048		V
		Differential Inputs				32.768		mV
LSB	LSB Step Voltage	RTNS, ADIN1-4, ADIO1-4, DRNS, DRAIN	ADC = 000b			8		mV
			ADC = 010b			2		mV
			ADC = 100b			0.5		mV
			ADC = 110b			0.125		mV
			ADC = xx1b			0.03125		mV
		$ADC^+ – ADC^–$	ADC = 000b			128		µV
			ADC = 010b			32		µV
			ADC = 100b			8		µV
			ADC = 110b			2		µV
			ADC = xx1b			0.5		µV
		$SENSE1,2^+ – SENSE1,2^–$, ADIN2 – ADIN1, ADIN4 – ADIN3, ADIO2 – ADIO1, ADIO4 – ADIO3	ADC = 000b			256		µV
			ADC = 010b			64		µV
			ADC = 100b			16		µV
			ADC = 110b			4		µV
			ADC = xx1b			1		µV
V_{OS}	Offset Error (Note 7)	Single-Ended Inputs		●		0	±0.125	% V_{FS}
		Differential Inputs		●		0	±0.25	% V_{FS}
INL	Integral Nonlinearity (Note 7)	ADIN1-4, ADIO1-4, RTNS, DRNS, DRAIN, $ADC^+ – ADC^–$		●		±0.01	±0.06	% V_{FS}
		$SENSE1,2^+ – SENSE1,2^–$, ADIN2 – ADIN1, ADIN4 – ADIN3, ADIO2 – ADIO1, ADIO4 – ADIO3		●		±0.02	±0.12	% V_{FS}
FSE	Full-Scale Error (Note 7)	Single-Ended Inputs, C-Grade (Note 6)		●			±0.5	%
		Single-Ended Inputs, I-, H-Grade		●			±0.7	%
		Differential Inputs, C-Grade (Note 6)		●			±1	%
		Differential Inputs, I-, H-Grade		●			±1.2	%
		Power, C-Grade (Note 6)		●			±1	%
		Power, I-, H-Grade		●			±1.2	%
		Energy		●			±5	%
f_{CONV}	Refresh Rate in Continuous Mode (Table 12)			●			±5	%
I_{ADC}^+	ADC^+ Input Current	ADC^+ = 33mV		●		0	±1	µA
$I_{ADC}^–$	ADC^+ Input Current	$ADC^–$ = ADC^+ = 0		●		–3	–7	µA
$R_{ADIN(SE)}$	ADIN1-4, ADIO1-4 Input Impedance, Single-Ended	V = 3V		●	3			MΩ
$I_{ADIN(SE)}$	ADIN1-4, ADIO1-4 Input Current, Single-Ended	V = 3V		●		0	±1	µA
$I_{ADIN(DIFF)}$	ADIN1, ADIN3, ADIO1, ADIO3 Input Current, Differential Mode	ADIN1, ADIN3, ADIO1, ADIO3 = 0, ADIN2, ADIN4, ADIO2, ADIO4 = 0		●		–3	–7	µA
	ADIN2, ADIN4, ADIO2, ADIO4 Input Current, Differential Mode	ADIN2, ADIN4, ADIO2, ADIO4 = 33mV		●		0	±1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, I_{IN} + I_{VZ} = 4mA with V_{IN} Connected to V_Z. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I²C Interface							
$V_{ADR(H)}$	ADR0, ADR1 Input High Threshold		●	$INTV_{CC}$ – 0.85	$INTV_{CC}$ – 0.55	$INTV_{CC}$ – 0.25	V
$V_{ADR(L)}$	ADR0, ADR1 Input Low Threshold		●	0.4	0.7	1	V
$I_{ADR(IN)}$	Allowable Leakage Current		●			±10	µA
$V_{ALERT\#(OL)}$	ALERT# Output Low Voltage	I = 5mA	●		0.15	0.4	V
$V_{SDAO(OL)}$	SDAO Output Low Voltage	I = 20mA	●		0.25	0.6	V
$I_{SDAO,ALERT\#}$	SDAO, ALERT# Input Current	SDAO, ALERT# = $INTV_{CC}$	●		0	±1	µA
$V_{SDAI,SCL(TH)}$	SDAI, SCL Input Threshold		●	1.5	1.75	2	V
$I_{SDAI,SCL}$	SDAI, SCL Input Current	SDAI, SCL = $INTV_{CC}$	●		0	±1	µA
I²C Interface Timing (Note 7)							
$f_{SCL(MAX)}$	Maximum SCL Clock Frequency			400			kHz
t_{LOW}	Minimum SCL Low Period				0.65	1.3	µs
t_{HIGH}	Minimum SCL High Period				50	600	ns
$t_{BUF(MIN)}$	Minimum Bus Free Time Between Stop/ Start Condition				0.12	1.3	µs
$t_{HD,STA(MIN)}$	Minimum Hold Time After (Repeated) Start Condition				140	600	ns
$t_{SU,STA(MIN)}$	Minimum Repeated Start Condition Set-Up Time				30	600	ns
$t_{SU,STO(MIN)}$	Minimum Stop Condition Set-Up Time				30	600	ns
$t_{HD,DATI(MIN)}$	Minimum Data Hold Time Input				–100	0	ns
$t_{HD,DATO(MIN)}$	Minimum Data Hold Time Output			300	600	900	ns
$t_{SU,DAT(MIN)}$	Minimum Data Set-Up Time Input				30	100	ns
$t_{SP(MAX)}$	Maximum Suppressed Spike Pulse Width			50	110	250	ns
t_{RST}	Stuck-Bus Reset Time	SCL or SDAO Held Low		26	30	34	ms
C_X	SCL, SDA Input Capacitance	SDAI Tied to SDAO			5	10	pF
Single-Wire Broadcast Timing							
f_{BC}	Broadcast Data Rate (Table 11)		●			±10	%
EEPROM							
	Endurance	1 Cycle = 1 Write (Notes 8, 9)	●	10,000			Cycles
	Data Retention	(Notes 8, 9)	●	20			Years
t_{WRITE}	EEPROM Write Time per Byte		●	1.2	2.2	3	ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All Currents into device pins are positive and all currents out of device pins are negative. All voltages are referenced to V_{EE} unless otherwise specified.

Note 3: When V_Z is connected to V_{IN}, an internal shunt regulator limits the voltage to a minimum of 11V. Driving the pins above 11V may damage the part. These pins can be safely biased by a higher voltage using a resistor or current source that limits the current below 50mA.

Note 4: An internal clamp limits DRAIN to a minimum of 3.2V. Driving this pin to voltages above the clamp may damage the part. The pin can be safely tied to higher voltages through a resistor that limits the current below 1.5mA.

Note 5: An internal clamp limits EN# to a minimum of 6V. Driving this pin to voltages above the clamp may damage the part. The pin can be safely tied to higher voltages through a resistor that limits the current below 5mA.

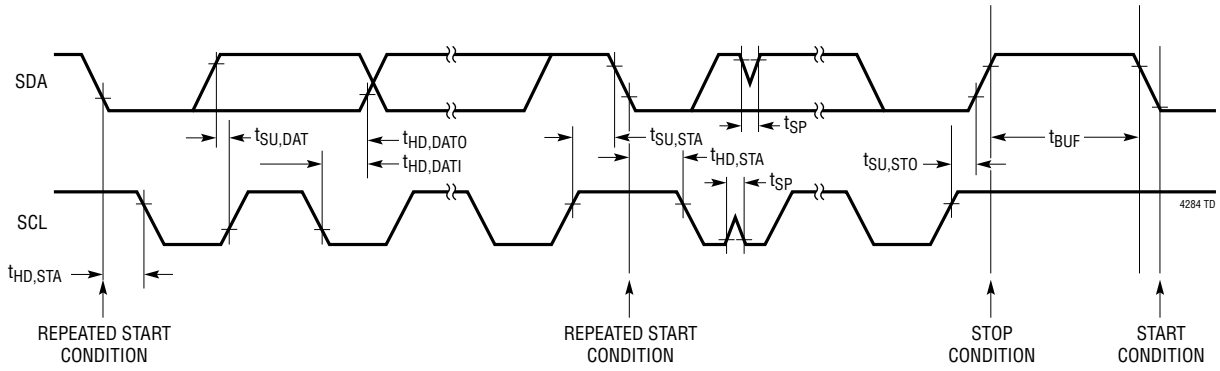
Note 6: Guaranteed by design and characterization. Not tested in production.

Note 7: Tested at 12-bit resolution and guaranteed for other resolutions by design and characterization.

Note 8: EEPROM endurance and retention are guaranteed by design, characterization and correlation with statistical process controls.

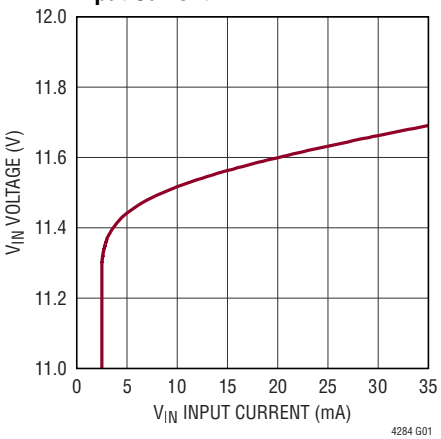
Note 9: EEPROM endurance and retention will be degraded when T_J > 85°C.

I²C TIMING DIAGRAM

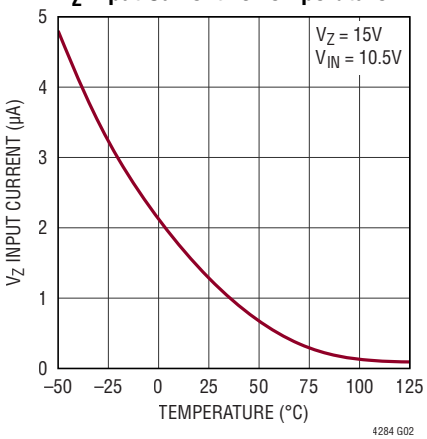


TYPICAL PERFORMANCE CHARACTERISTICS

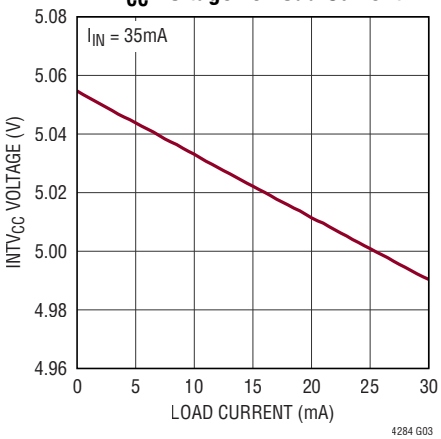
Shunt Regulator Voltage vs Input Current



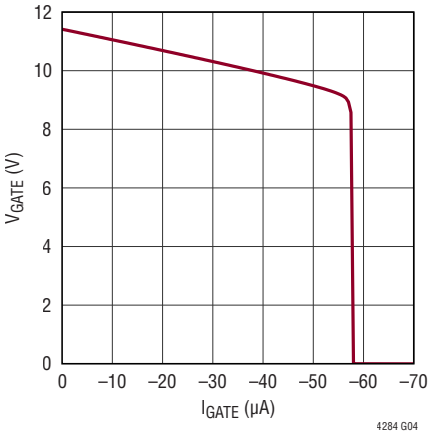
VZ Input Current vs Temperature



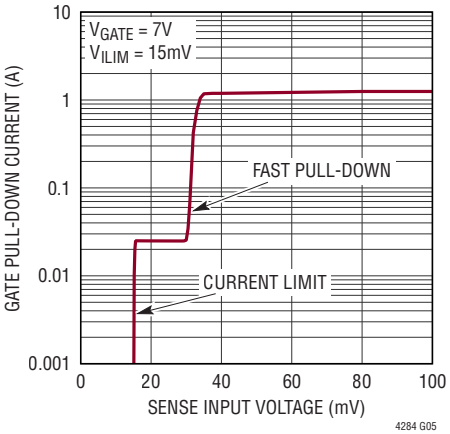
INTVCC Voltage vs Load Current



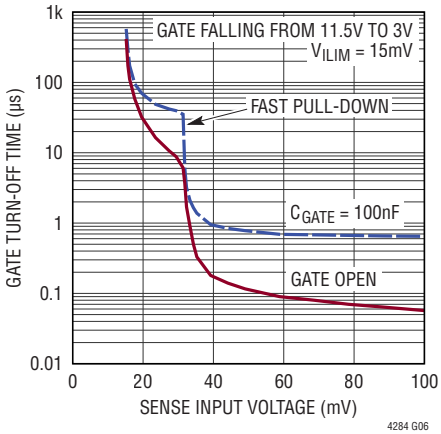
GATE Output High Voltage vs Leakage Current



GATE Pull-Down Current vs SENSE Input Voltage

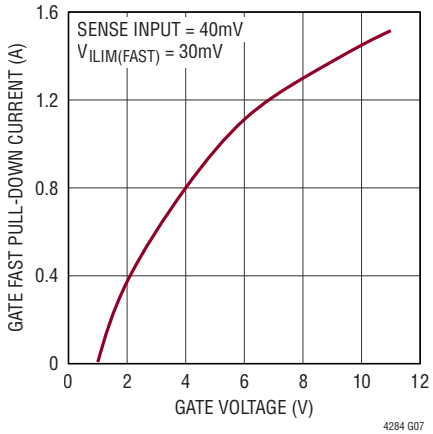


GATE Turn-Off Time vs SENSE Input Voltage

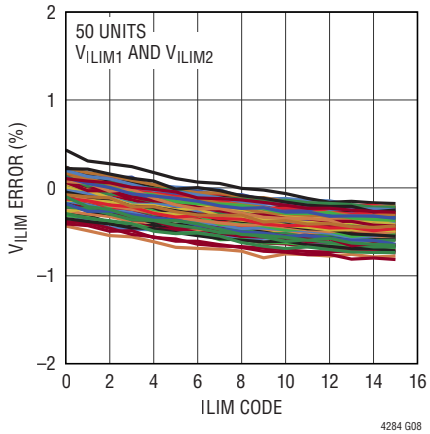


TYPICAL PERFORMANCE CHARACTERISTICS

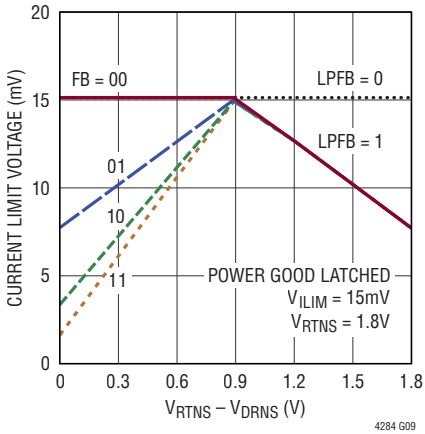
GATE Fast Pull-Down Current vs GATE Voltage



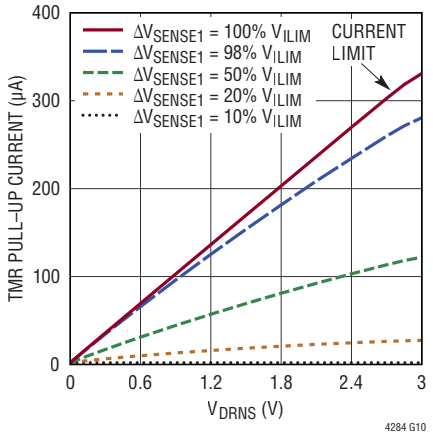
Current Limit Voltage Error vs ILIM Code



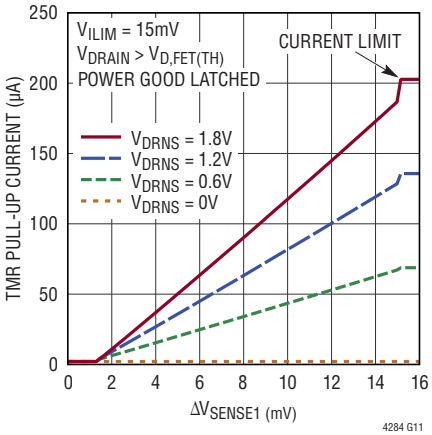
Current Limit Foldback Profiles



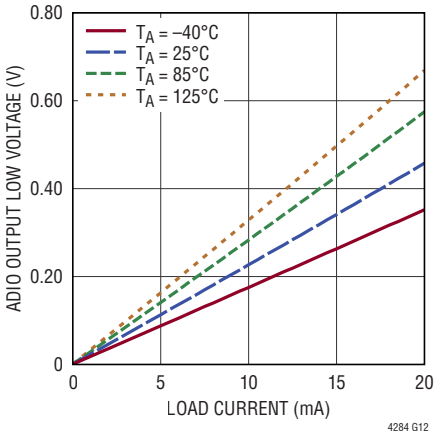
TMR Pull-Up Current vs DRNS Voltage



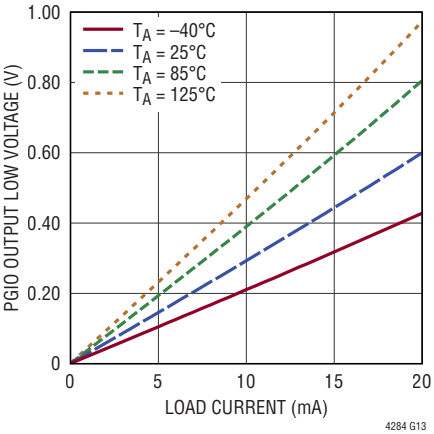
TMR Pull-Up Current vs SENSE Input Voltage



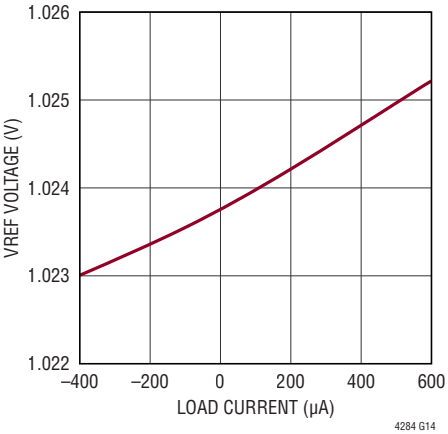
ADIO Output Low Voltage vs Load Current



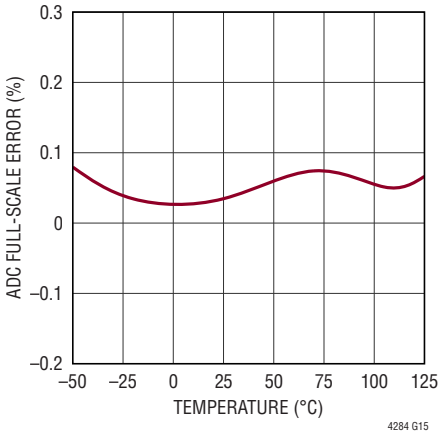
PGIO Output Low Voltage vs Load Current



VREF Output Voltage vs Load Current

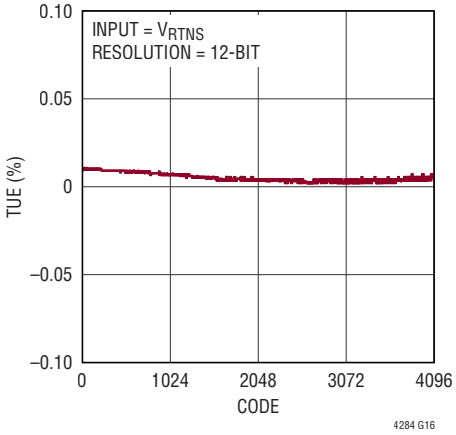


ADC Full-Scale Error vs Temperature

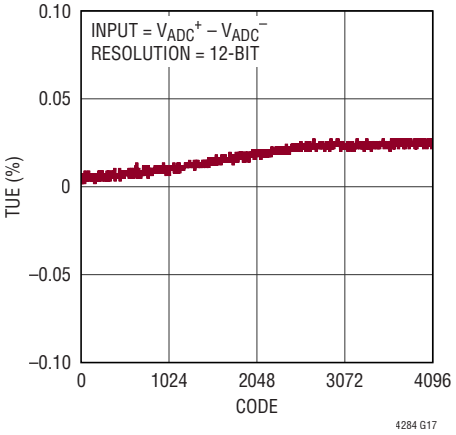


TYPICAL PERFORMANCE CHARACTERISTICS

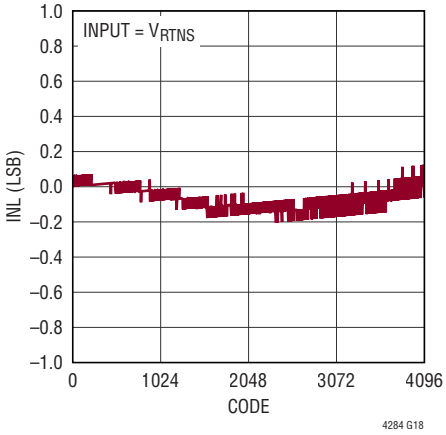
Voltage ADC Total Unadjusted Error (TUE) vs Code



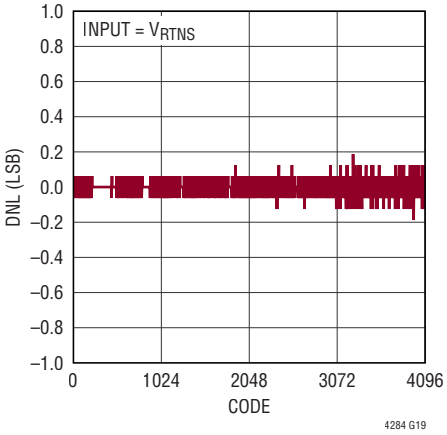
Current ADC Total Unadjusted Error (TUE) vs Code



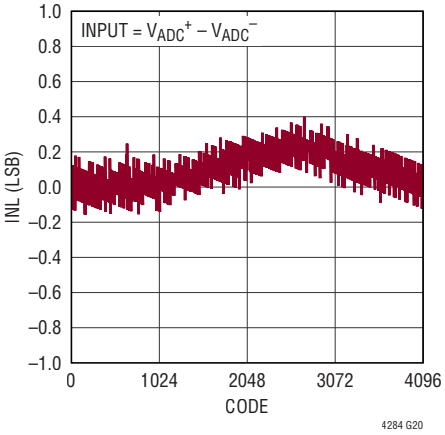
12-Bit Voltage ADC INL vs Code



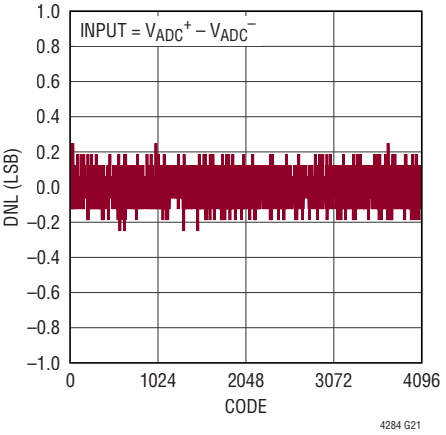
12-Bit Voltage ADC DNL vs Code



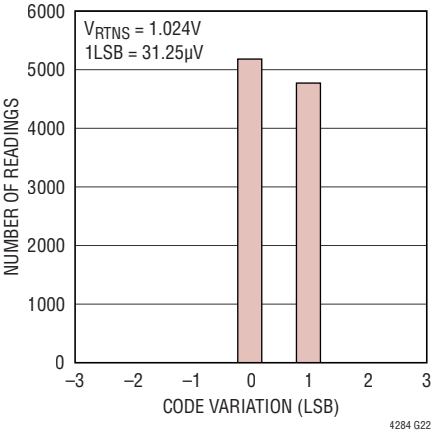
12-Bit Current ADC INL vs Code



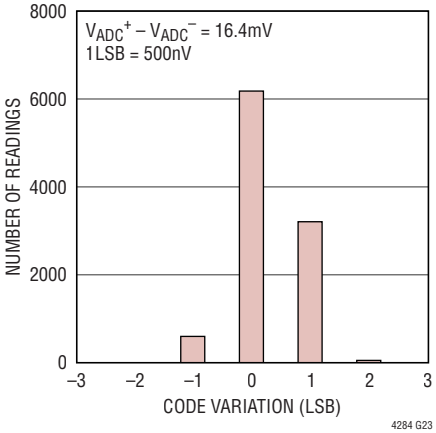
12-Bit Current ADC DNL vs Code



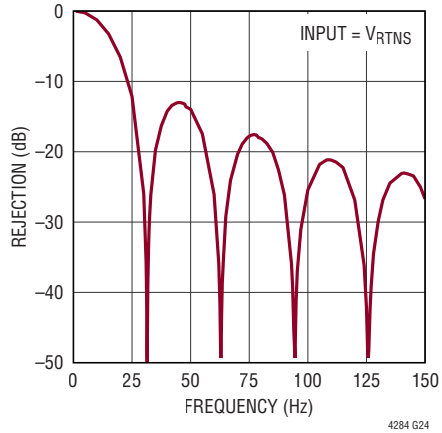
16-Bit Voltage ADC Noise Histogram



16-Bit Current ADC Noise Histogram

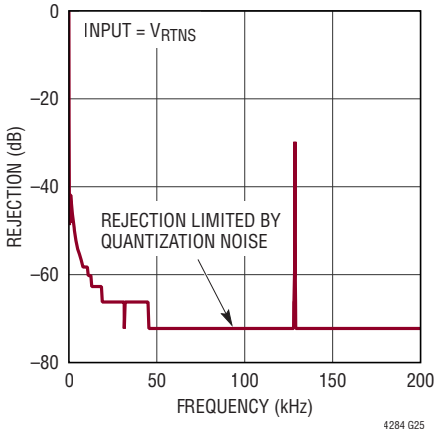


12-Bit ADC Input Signal Attenuation (Low Frequencies)

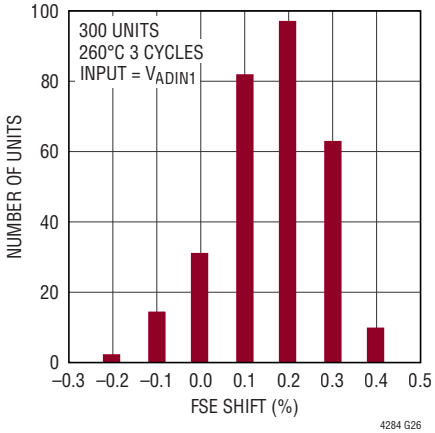


TYPICAL PERFORMANCE CHARACTERISTICS

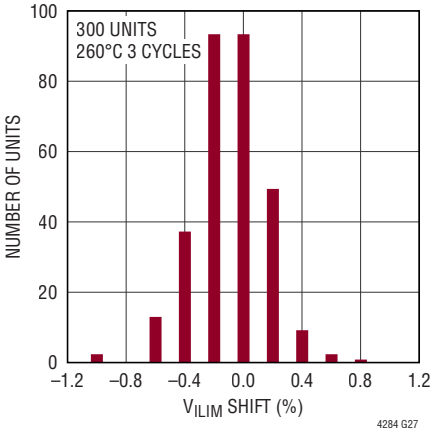
12-Bit ADC Input Signal Attenuation (Extended Frequencies)



ADC FSE Shift Due to IR Reflow



V_{ILIM} Shift Due to IR Reflow



PIN FUNCTIONS

ADC⁺ (Pin 16): Positive Current Sense Kelvin Input to ADC. Connect to the tap of an external resistive divider between SENSE1⁺ and SENSE2⁺ to measure the average between those two pins. Connect to SENSE1⁺ when using a single sense resistor. Connect to V_{EE} if unused.

ADC⁻ (Pin 13): Negative Current Sense Kelvin Input to ADC. Connect to the tap of an external resistive divider between SENSE1⁻ and SENSE2⁻ to measure the average between those two pins. Connect to SENSE1⁻ when using a single sense resistor. Connect to V_{EE} if unused.

ADIN1–ADIN4 (Pins 7–10): ADC Inputs. A single-ended voltage between 0V and 2.048V applied to each ADIN is measured by the on-chip ADC. Two differential voltages ADIN2 – ADIN1 and ADIN4 – ADIN3, if enabled, are also measured by the ADC with a full scale of 32.768mV. Connect to V_{EE} if unused.

ADIO1–ADIO4 (Pins 25–28): General Purpose Inputs/Outputs and ADC Inputs. Configurable to logic inputs and general purpose outputs (open-drain). See Table 13 for details. The single-ended voltages at ADIOs are measured by the ADC with a full scale of 2.048V. The differential voltages ADIO2 – ADIO1 and ADIO4 – ADIO3, if enabled, are also measured by the ADC with a full scale of 32.768mV. Connect to V_{EE} if unused.

ADR0, ADR1 (Pin 38, Pin 39): Serial Bus Address Inputs. Connecting to V_{EE}, OPEN or $INTV_{CC}$ configures one of nine possible addresses, with one dedicated to the single-wire broadcast mode. Do not bias with an external supply. See Table 2 in Applications Information for address decoding.

ALERT# (Pin 34): Fault Alert Output. Open-drain logic output that pulls to V_{EE} when a fault occurs to alert the host controller. A fault alert is enabled by the FAULT_ALERT and ADC_ALERT registers. See Tables 15 and 16 in Applications Information for details. Connect to V_{EE} if unused.

DRAIN (Pin 20): Drain Sense Input. Connect an external 100k resistor between this pin and the drain terminal of the N-channel MOSFET. A DRAIN voltage below 2.048V is one of the conditions to assert power good outputs and turn on GATE2 in the high stress staged start (Mode 3) or low stress staged start mode (Mode 4). When DRAIN voltage is above a voltage configurable between 72mV and 203mV, the FET Bad fault timer is started and the TMR output current is enabled when not in current limit. DRAIN is internally clamped to a minimum of 3.2V.

PIN FUNCTIONS

DRNS (Pin 21): Attenuated Drain Sense Input. Connect to the tap of an external resistive divider between the drain terminal of the N-channel MOSFET and V_{EE} to monitor the drain voltage. DRNS coupled with RTNS monitors the output voltage for the load, which controls dV/dt inrush current and current limit foldback. DRNS operates from 0 to 2.8V. Connect to V_{EE} if unused.

EN# (Pin 1): Device Enable Input. Pull low to enable the GATE outputs to turn-on after a startup debounce delay. When pulled high, both GATE1 and GATE2 are turned off. A high-to-low transition clears faults. Transitions are recorded. Requires external pull-up. Debouncing with an external capacitor is recommended when used to monitor board present. Connect to V_{EE} if unused.

Exposed Pad (Pin 45): Exposed Pad may be left open or connected to device ground (V_{EE}).

GATE1, GATE2 (Pin 18, Pin 19): N-Channel MOSFET Gate Drive Outputs. The GATEs can be configured into single driver, parallel, high stress staged start, and low stress staged start modes. See Table 1 in Application Information for details. The GATEs are pulled high by internal current sources (>40µA) when V_{IN} and $INTV_{CC}$ cross the UVLO thresholds, UV and OV conditions are satisfied, no other faults are present and the debounce delay expires. The GATE1 and GATE2 voltages higher than V_{IN} – 1.8V satisfy one of the conditions to assert power good outputs. Upon a low impedance output short, a 1.2A fast pull-down current is immediately activated.

$INTV_{CC}$ (Pin 42): 5V Internal Supply Output. The output of the internal linear regulator sources up to 30mA with an UVLO threshold of 4V. The supply powers the data converters, logic control circuitry, I^2C interface and EEPROM. Bypass with 1µF capacitor to V_{EE}. $INTV_{CC}$ is not current limited. When driving $INTV_{CC}$ with an external supply, V_{IN} and V_Z must be left open or connected to $INTV_{CC}$.

MODE (Pin 40): GATE Drive Mode Configuration Input. Its voltage decodes four operation modes of GATE1 and GATE2. Leaving MODE open enables the single driver mode (Mode 1): GATE1 and GATE2 drive a single channel of MOSFETs. Connecting MODE to V_{EE} enables the parallel mode (Mode 2): GATE1 and GATE2 drive two parallel channels of MOSFETs that turn on simultaneously to share the load current and turn off simultaneously upon overload. Connecting MODE to V_{IN} enables the high stress staged start mode (Mode 3): GATE1 drives a high SOA MOSFET that turns on first for startup and withstands the stress under overload conditions, while GATE2 drives a low $R_{DS(ON)}$ MOSFET as a bypass switch that turns on after GATE1 is fully enhanced and turns off whenever overload occurs. Connecting MODE to $INTV_{CC}$ enables the low stress staged start mode (Mode 4): the turn-on behavior of GATE1 and GATE2 is the same as Mode 3, but GATE1 drives a low SOA trickle MOSFET and the low $R_{DS(ON)}$ bypass MOSFET driven by GATE2 stays on under overload to share the stress. See Applications Information for more details.

OV (Pin 4): Overvoltage Detection Input. Connect to an external resistive divider from V_{EE}. When OV is above its threshold of 1.406V, the GATE outputs pull low to turn off the MOSFETs and an overvoltage fault is recorded. The overvoltage fault does not affect the status of the power good outputs. Connect to V_{EE} if unused.

PGIO1, PGIO2 (Pin 29, Pin 30): General Purpose Inputs/Outputs. Configurable to sequenced, inverted and non-inverted power good outputs, general purpose logic inputs and open-drain outputs. See Table 12 in Application Information for details. If the PGIO2_ACLB bit in CONTROL_1 register 0x0A is set, PGIO2 is configured as inverted current limit engagement indicator after startup. Connect to V_{EE} if unused.

PGIO3 (Pin 31): General Purpose Input/Output. Configurable to inverted and non-inverted power good watchdog input (PGI# and PGI), general purpose logic input and open-drain output. See Table 12 in Application Information for details. Connect to V_{EE} if unused.

PGIO4 (Pin 32): General Purpose Input/Output. Configurable to inverted and non-inverted external fault input (EXT_FAULTIN# and EXT_FAULTIN), general purpose logic input and open-drain output. See Table 12 in Application Information for details. Connect to $INTV_{CC}$ if unused.

PIN FUNCTIONS

RAMP (Pin 23): Ramp Control. Connect a capacitor between RAMP and V_{EE} to set inrush current in dV/dt startup mode. During the dV/dt control, RAMP acts as an attenuated output and feeds a fixed 2.5µA current through the RAMP capacitor to set the slew rate of the output voltage. The dV/dt inrush control is disabled after startup when power good signals are asserted. Leave open if unused.

RTNS (Pin 22): RTN Sense Input. Connect to the tap of an external resistive divider between RTN and V_{EE} to monitor the board input voltage. When selected, the RTNS voltage is measured by the ADC and used to calculate the input power. Monitors the output voltage for the load when coupled with DRNS, which controls dV/dt inrush current and current limit foldback. Operates from 0V to 2.8V. Connect to $INTV_{CC}$ if unused.

SCL (Pin 37): Serial Bus Clock Input. Data at SDAI is shifted in and data at SDAO is shifted out on rising edges of SCL. This is a high impedance input that is generally connected to the output of the incoming isolator driven by the SCL port of the master controller. An external pull-up resistor or current source is required. Pull up to $INTV_{CC}$ if unused.

SDAI (Pin 36): Serial Bus Data Input. This is a high impedance input used for shifting in command bits, data bits, and SDAO acknowledge bits. An external pull-up resistor or current source is required. Normally connected to the output of the incoming isolator that is driven by the SDA port of the master controller. Pull up to $INTV_{CC}$ if unused.

SDAO (Pin 35): Serial Bus Data Output. Open-drain output used for sending data back to the master controller or acknowledging a write operation. An external pull-up resistor or current source is required. Normally connected to the input of the outgoing isolator that outputs to the SDA port of the master controller. In the single-wire broadcast mode, SDAO sends out selected data that is Manchester encoded with an internal clock. The broadcast bit rate is configurable between 2Mbit/s and 32kbit/s.

SENSE1$^+$, SENSE2$^+$ (Pin 15, Pin 17): Positive Current Sense Kelvin Inputs. Connect to the high side of the current sense resistors. The active current limit amplifiers control GATE1 and GATE2 independently to limit the sense voltages SENSE1$^+$ – SENSE1$^-$ and SENSE2$^+$ – SENSE2$^-$ from 15mV to 30mV, configurable in 1mV steps. When enabled, SENSE1$^+$ – SENSE1$^-$ and SENSE2$^+$ – SENSE2$^-$ are also measured by the ADC with a full scale of 32.768mV. Connect together when using a single sense resistor. Connect SENSE2$^+$ to V_{EE} in the high stress staged start mode (Mode 3). Connect both to V_{EE} if unused.

SENSE1$^-$, SENSE2$^-$ (Pin 14, Pin 12): Negative Current Sense Kelvin Inputs. Connect to the low side of the current sense resistors.

TMR (Pin 24): Timer Current Output. The current sourced out of TMR is proportional to the power dissipation in the MOSFET driven by GATE1. If an RC network that represents the thermal behavior of the MOSFET is connected between TMR and V_{EE}, the voltage at TMR represents the real-time temperature rise of the MOSFET. When the TMR voltage reaches its threshold of 2.048V that corresponds to $T_{J(MAX)}$ of the MOSFET, both GATE1 and GATE2 pull low to turn off the MOSFETs and an overcurrent fault is logged. If a single capacitor is connected between TMR and V_{EE}, TMR sets the delay for MOSFET turn-off based on the power dissipation in the MOSFET. In this mode the 2µA pull-down current must be enabled to discharge the capacitor when the MOSFET power drops to near zero. When EN# is low, TMR is discharged by a 5mA current. Connect to V_{EE} if unused.

UVH (Pin 3): Undervoltage High Level Input. Connect to an external resistive divider from V_{EE}. If UVH rises above 2.048V and UVL is above 1.833V, the GATE outputs pull high to turn on the MOSFETs. A capacitor of at least 10nF between UVH and V_{EE} prevents transients and switching noise from affecting the UV threshold. Connect to $INTV_{CC}$ if unused.

PIN FUNCTIONS

UVL (Pin 2): Undervoltage Low Level Input. Connect to an external resistive divider from V_{EE}. If UVL drops below 1.833V and UVH is below 2.048V, the MOSFETs are turned off. Pulling below 1.024V resets faults and allows the MOSFET to turn back on when undervoltage is cleared. Connect to $INTV_{CC}$ if unused.

V_{EE} (Pin 11 and Pin 33): Negative Supply Voltage Input and Device Ground. Connect to the negative side of the power supply. The connection between any component and device ground must be made to a dedicated plane that connects directly to V_{EE}, not to the main current-carrying trace of –48V on the board.

V_{IN} (Pin 43): Positive Supply Input to the Device. Connect to V_Z directly or through an external buffer transistor driven by V_Z. The voltage at V_{IN} is internally regulated at 11.5V. An undervoltage lockout (UVLO) circuit holds the GATE1 and GATE2 outputs low until V_{IN} is above 8.1V. Bypass with at least 0.1µF capacitor to V_{EE}. If it is desired to log fault information into EEPROM upon brown-out, bypass V_{IN} with at least 68µF capacitor to V_{EE} (See Applications Information for details).

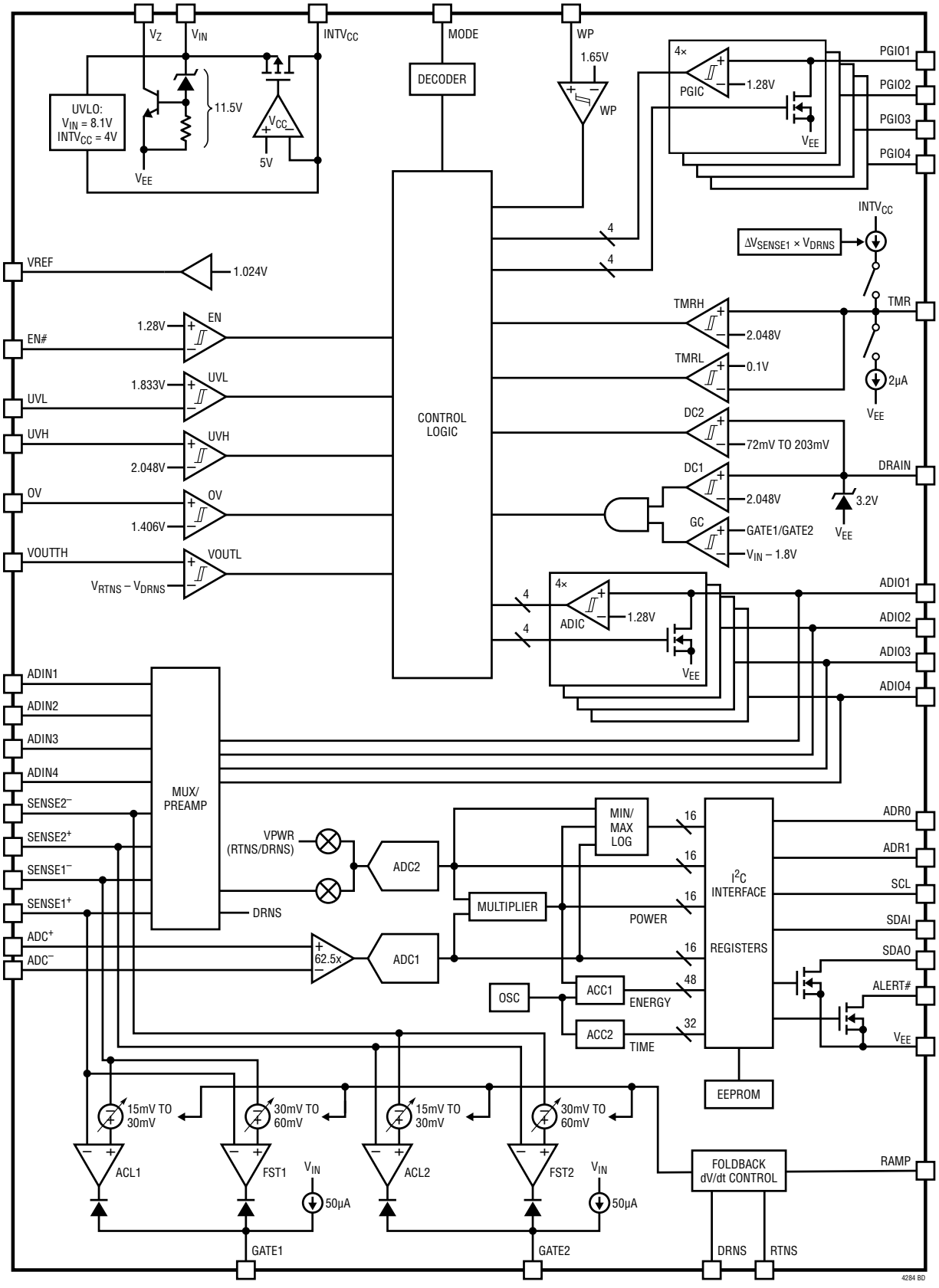
VOUTTH (Pin 6): Output Low Threshold Input. Connect to an external reference voltage for output voltage low threshold. RTNS – DRNS below VOUTTH sets the V_{OUT} low status bit. RTNS – DRNS above VOUTTH satisfies one of the conditions to assert power good outputs. Connect to V_{EE} if unused.

VREF (Pin 5): Reference Voltage Output. Regulated at 1.024V or half of the ADC full-scale. Sources up to 200µA and sinks up to 400µA. It can drive a capacitive load of up to 10nF. Leave open if unused.

V_Z (Pin 44): Shunt Regulator Input. Operates with a bias of 20µA to 30mA. Connect to the positive supply (RTN) through a dropping resistor. To supply external loads with V_{IN}, use V_Z to drive an external buffer transistor with the emitter or source connected to V_{IN}. Bypass with a 0.1µF capacitor to V_{EE}.

WP (Pin 41): EEPROM Write Protect Input. All write operations to the EEPROM except fault logging are blocked when the voltage at WP is above 1.65V.

BLOCK DIAGRAM



OPERATION

The LTC4284 is designed to turn a board's supply voltage on and off in a controlled manner, allowing the board to be safely inserted or removed from a live, high power system. The device features four distinct operation modes: single driver mode (Mode 1), parallel mode (Mode 2), high stress staged start mode (Mode 3), and low stress staged start mode (Mode 4). Each of these modes addresses specific application requirements for SOA (Safe Operating Area), $R_{DS(ON)}$, and cost.

In normal operation after a startup debounce delay, the LTC4284 turns on the external N-channel MOSFETs, passing the power to the load. The inrush control during startup is configurable between two methods. One is programmable active current limiting with an adjustable foldback factor. The other is constant dV/dt ramp control of the output voltage using a capacitor connected between RAMP and V_{EE}. The inrush current is a function of the RAMP capacitor, the load capacitor and the attenuated load voltage seen between RTNS and DRNS.

An 11.5V shunt regulator on V_{IN} powers the LTC4284 with an external dropping resistor from the system RTN node. It also provides gate drive for GATE1 and GATE2. An optional buffer transistor driven by V_Z boosts sourcing capability to supply external loads.

An internally generated 5V supply on $INTV_{CC}$ supplies the logic control circuits, communication interface, data converters and EEPROM. Prior to turning on the MOSFETs, both V_{IN} and $INTV_{CC}$ voltages must exceed their undervoltage lockout thresholds. In addition, the control inputs UVH, UVL, OV, EN#, PGIO3 and PGIO4 are monitored by comparators. The MOSFETs are held off until all startup conditions are met.

The DRAIN, RTNS – DRNS and GATE voltages are monitored to determine if power is available for the load. Two power good signals are sequenced on PGIO1 and PGIO2, each with a delay that is twice the startup debounce delay. Additionally, PGIO3 serves as a watchdog input to monitor the output of the DC/DC module. If the module output fails to come up, the LTC4284 turns off the MOSFETs. PGIO4 defaults as an external fault input (inverted). PGIO1-4 can also be configured into general purpose inputs or outputs.

An overcurrent fault at the output may result in excessive MOSFET power dissipation during Active Current Limiting (ACL). To limit this power in each channel, the ACL amplifiers regulate the $SENSE1^+ – SENSE1^-$ and $SENSE2^+ – SENSE2^-$ voltages at precise, programmable values (15mV to 30mV in 1mV steps). When the output voltage is low, power dissipation is further reduced by folding back the current limit, with the foldback ratio configurable to 10%, 20%, or 50% of nominal. In the event of a catastrophic output short when the sensed current is twice of the current limit, fast response comparators immediately pull the GATE pins down with 1.2A.

When active current limiting is engaged, TMR is pulled up by a current that is proportional to the power dissipation in the MOSFET (M1) driven by GATE1. With an RC network representing the thermal behavior of M1 connected between TMR and V_{EE}, the TMR voltage is proportional to the temperature rise in M1. When TMR voltage reaches its threshold of 2.048V (representing $T_{J(MAX)}$ of the MOSFET), the overcurrent fault is logged and both GATE1 and GATE2 turn off, allowing protection of the MOSFETs based on true SOA. TMR can also be configured to drive a single capacitor. Following the overcurrent fault, the LTC4284 can either latch off the MOSFETs or auto-retry after a cooling delay. Both the retry delay and the number of retries are configurable, too. The LTC4284 also logs and responds to other faults including overvoltage, undervoltage, FET bad, Power Good Input (PGI) fault, FET short and external fault.

Included in the LTC4284 is a pair of analog to digital converters (ADCs). The ADCs are configurable from 8-bit at 1kHz to 16-bit at 1Hz in five settings. As shown in the Block Diagram, ADC1 continuously monitors the current sense voltage between ADC^+ and ADC^-. ADC2 is synchronized to ADC1 and measures the attenuated input voltage at RTNS or the attenuated MOSFET drain voltage at DRNS plus one of the sixteen auxiliary inputs. Every time the ADCs finish taking a measurement, the current sense voltage is multiplied by the measurement of the RTNS or DRNS voltage to provide a power measurement. Every time power is measured, it is added to an energy accumulator that tracks the input energy or the energy consumption of the MOSFET. The energy accumulator

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can generate an optional alert upon overflow, and can be preset to allow it to overflow after a given amount of energy is reached. A time accumulator tallies energy increments; dividing the results of the energy accumulator by the time accumulator gives the average system power. The minimum and maximum of each ADC measurement and power are stored, and optional alerts may be generated if a measurement is above or below user configurable 8-bit thresholds.

An internal EEPROM provides nonvolatile configuration of the LTC4284 operation behaviors and parameters. It also records fault information and selected ADC data. Seven bytes of uncommitted memory are reserved for general purpose storage.

An I^2C/SMBus interface accesses the ADC data registers and allows the host to poll the device and determine if a fault has occurred. If the ALERT# line is used as an interrupt, the host can respond to a fault in real time. A reboot command turns off the MOSFETs and automatically restarts after a configurable delay. The SDA line is divided into SDAI (input) and SDAO (output) to facilitate opto-coupling with the system host. Two three-state pins, ADR0 and ADR1, are used to decode eight device addresses.

The communication interface can also be configured through ADR0 and ADR1 for a single-wire broadcast mode, sending ADC data and faults status through SDAO to the host without clocking the SCL line. This single-wire, one-way communication simplifies system design by eliminating two opto-couplers on SCL and SDAI that are required by an I^2C interface. The transmission speed is configurable from 32kHz to 2MHz with four settings.

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The LTC4284 is ideally suited for high power, high availability distributed power systems, allowing a board to be safely inserted or removed from a live negative voltage backplane. The device features two GATE drivers that can be configured into parallel mode, high stress staged start mode, low stress staged start mode and single driver mode, each to optimize SOA and $R_{DS(ON)}$ of MOSFETs for different application requirements. In the following sections, the parallel mode is first chosen to demonstrate the common functions and basic hot-swap applications. The unique features and applications of each operation mode are then described separately.

Figure 1 shows a basic 1.2kW application circuit with the dual-gate drivers configured in parallel mode. Figure 2 shows a more complete application circuit in a dual-feed system with board insertion detection and opto-coupling.

Input Power Supply

The LTC4284 features a floating topology that allows a wide operating voltage range and is robust to faults. For a –48V system, supply to the LTC4284 is derived from the –48V RTN through an external shunt resistor R_{IN} to the V_{IN} and V_Z pins (Figure 1). An internal shunt regulator clamps V_{IN} to 11.5V relative to V_{EE} and provides power to the GATE drivers. V_Z acts as the shunt path of the regulator. A bypass capacitor of at least 0.1µF is recommended between V_{IN}/V_Z and V_{EE}. If EEPROM fault log is enabled (see Fault Log), the minimum bypass capacitance at V_{IN} for the fault log operation to complete upon an undervoltage or power loss condition is

$$C_{IN} \geq 15\left[\frac{\mu F}{mA}\right] \bullet (I_{IN(MAX)} + I_{EXTERNAL}$$

An internal 5V linear regulator that derives from the 11.5V supply powers data converters, logic control circuits, I^2C interface and EEPROM. The 5V output is available at the $INTV_{CC}$ pin for driving external circuits. A bypass capacitor of 1µF is recommended between $INTV_{CC}$ and V_{EE}. To only test data converters or program EEPROM, the main –48V supply is not needed. Instead, a 5V supply may be applied between $INTV_{CC}$ and V_{EE}, with V_{IN} and V_Z connected to $INTV_{CC}$.

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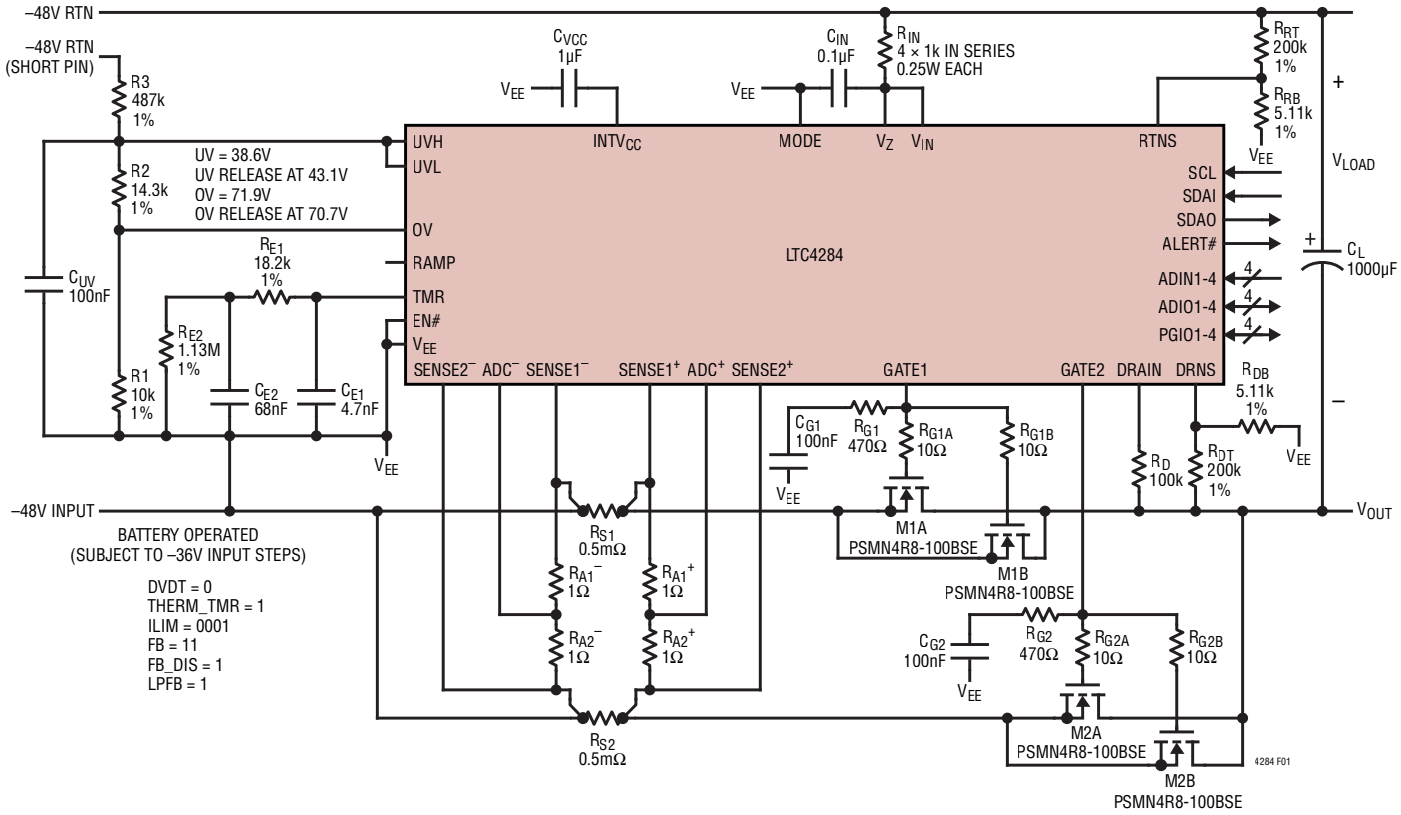

Figure 1. –48V/1200W Hot Swap Controller with SOA Timer and Current Limited Inrush Control in Parallel Mode: GATE1 and GATE2 Simultaneously Turn On and Turn Off to Share Load Current and SOA

R_{IN} should be chosen to accommodate the maximum supply current requirement of the LTC4284 ($I_{IN(MAX)}$ = 4mA) plus the supply current required by any external devices driven by V_{IN} and $INTV_{CC}$ at the minimum supply voltage, $V_{S(MIN)}$ and the maximum V_{IN} voltage, $V_{IN(MAX)}$:

$$R_{IN} \leq \frac{V_{S(MIN)} - V_{IN(MAX)}}{I_{IN(MAX)} + I_{EXTERNAL}}$$

The maximum power dissipation in the resistor is

$$P_{MAX} = \frac{\left(V_{S(MAX)} - V_{IN(MIN)}\right)^2}{R_{IN}}$$

If the power dissipation of R_{IN} is too high for a single resistor, use multiple resistors in series, which provides additional clearance spacing for high voltage surges. Another option uses an external NPN transistor (Q_{IN}) as illustrated in Figure 2b. Each of V_{IN} and V_Z should be bypassed with a capacitor of at least 0.1µF. In this case R_Z is chosen according to

$$R_Z \leq \frac{V_{S(MIN)} - V_{IN(MAX)} - V_{BE}}{\frac{I_{IN(MAX)} + I_{EXTERNAL}}{\beta} + 20\mu A}$$

where V_{BE} and β are the base-emitter voltage and DC current gain of the NPN transistor, respectively and 20µA represents the minimum V_Z operating current. The maximum power dissipation of Q_{IN} is

$$P_{QIN,MAX} = (V_{S(MAX)} - V_{IN(MIN)}) \bullet I_{IN(MAX)}$$

R_{IN} or R_Z may be split into multiple segments in order to achieve the desired standoff voltage or dissipation. Whereas 1206 size resistors are commonly rated for 200V working and 400V peak, pad spacing and circuit board design rules may limit the working rating to as little as 100V.

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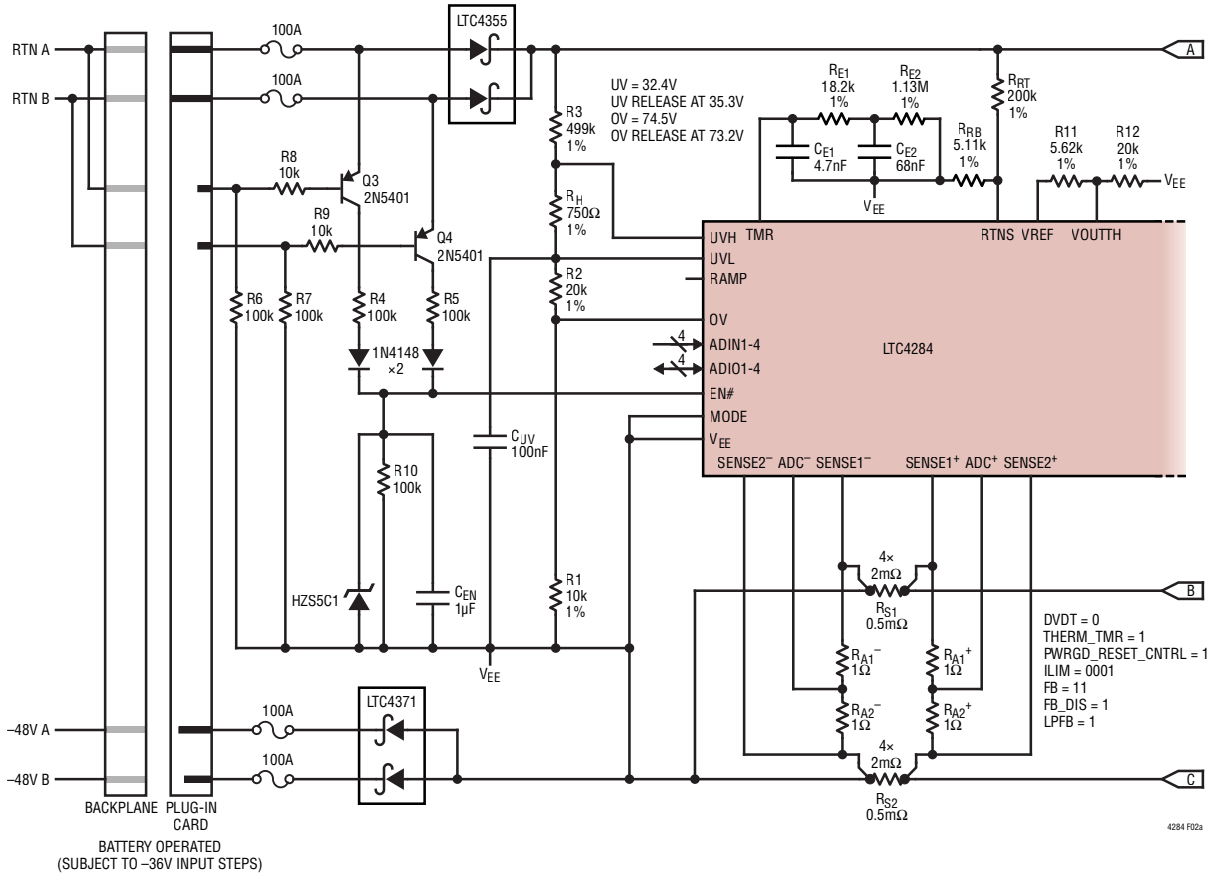

Figure 2a. –48V/1200W Dual-Feed Hot Swap Controller with LTC4284 in Parallel Mode (Part One)

For applications at very high voltages (>300V), a high voltage MOSFET can be used. Figure 3 shows an application circuit with a depletion mode N-channel MOSFET that can withstand up to 1000V drain-to-source voltage. In this case R_Z is chosen according to

$$R_Z \leq \frac{V_{S(MIN)} - V_{IN(MAX)} - V_{GS}}{20\mu A}$$

where V_{GS} is the gate-to-source voltage of the MOSFET (positive for an enhancement mode and negative for a depletion mode transistor) . When using an enhancement mode transistor, V_Z voltage must be kept lower than its absolute maximum of 16V:

$$V_{Z(MAX)} = V_{IN(MAX)} + V_{GS} < 16V$$

In Figures 2b and 3, the voltage drop and power dissipation in the NPN or the MOSFET may be augmented by the use of one or more resistors in series with the collector or drain. If an external 12V supply is available on the application board, it may be used to drive the V_{IN} pin directly as shown in Figure 4.

Turn-On Sequence

The following conditions must be satisfied before the turn-on sequence is started. First the voltage at V_{IN} must exceed the undervoltage lockout level of 8.1V. Next the internal supply $INTV_{CC}$ must cross its 4V undervoltage lockout level. This generates a 1.3ms power-on-reset delay. After the delay times out, the voltages at UVH, UVL and OV must satisfy UVH > 2.048V, UVL > 1.833V and OV < 1.406V to indicate that the input power is within the acceptable range, and EN# must be pulled low. All the above conditions must be satisfied throughout the duration of the startup debounce delay of 128ms. If any of the above conditions is violated during the delay, the delay is reset and restarted. After the delay expires, if the ON bit in CONTROL_1 register 0x0A is high, the LTC4284 turns on the MOSFETs. Otherwise, the MOSFET will be turned

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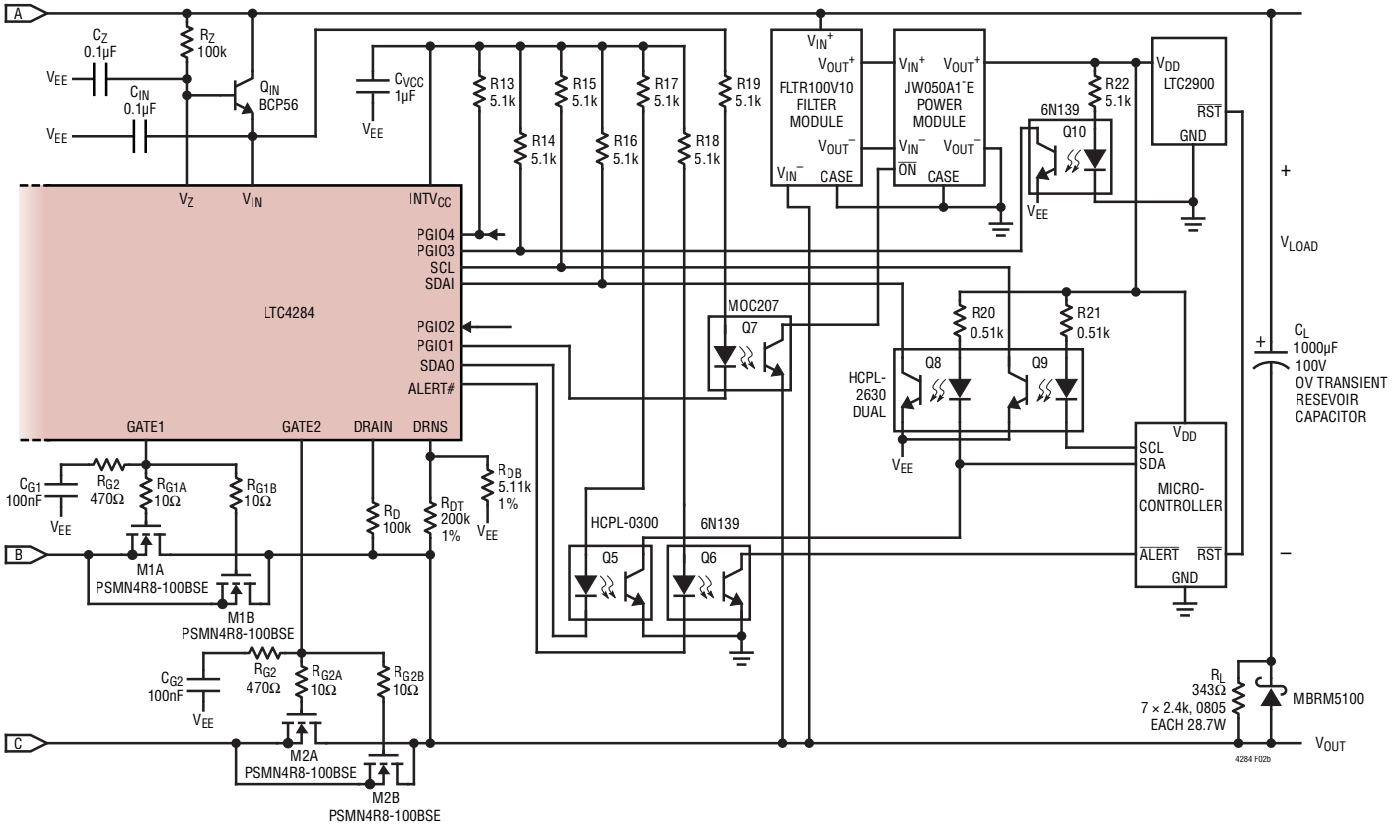

Figure 2b. –48V/1200W Dual-Feed Hot Swap Controller with LTC4284 in Parallel Mode (Part Two)

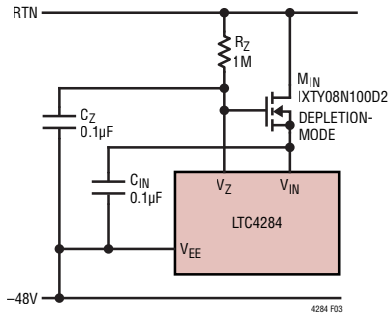

Figure 3. The LTC4284 Can Operate to >300V Using a Depletion Mode N-Channel MOSFET

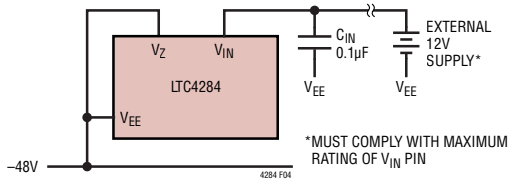

Figure 4. Using an External 12V Supply

on (without additional delay) when the ON bit is set to 1 through the I²C interface. When all turn-on conditions are satisfied, the FET_ON_STATUS bit in SYSTEM_STATUS register 0x00 is set to 1, indicating the MOSFETs are commanded on.

The turn-on sequence continues by charging up the GATEs with 50µA current sources. When the GATE voltage reaches the MOSFET threshold voltage, the MOSFET begins to turn on and the inrush current charges the load capacitor C_L to ramp the MOSFET drain towards V_{EE} in a controlled manner (see Inrush Control). When the MOSFET drain is ramped down to V_{EE} or the output is ramped up to the supply voltage, the GATEs are pulled up to V_{IN} and the MOSFETs are fully enhanced. The GATE1_HIGH and GATE2_HIGH bits in SYSTEM_STATUS register 0x00 are set when GATE1 and GATE2 are above V_{IN} – 1.8V. Figure 5 illustrates the startup sequence of the LTC4284 in parallel mode.

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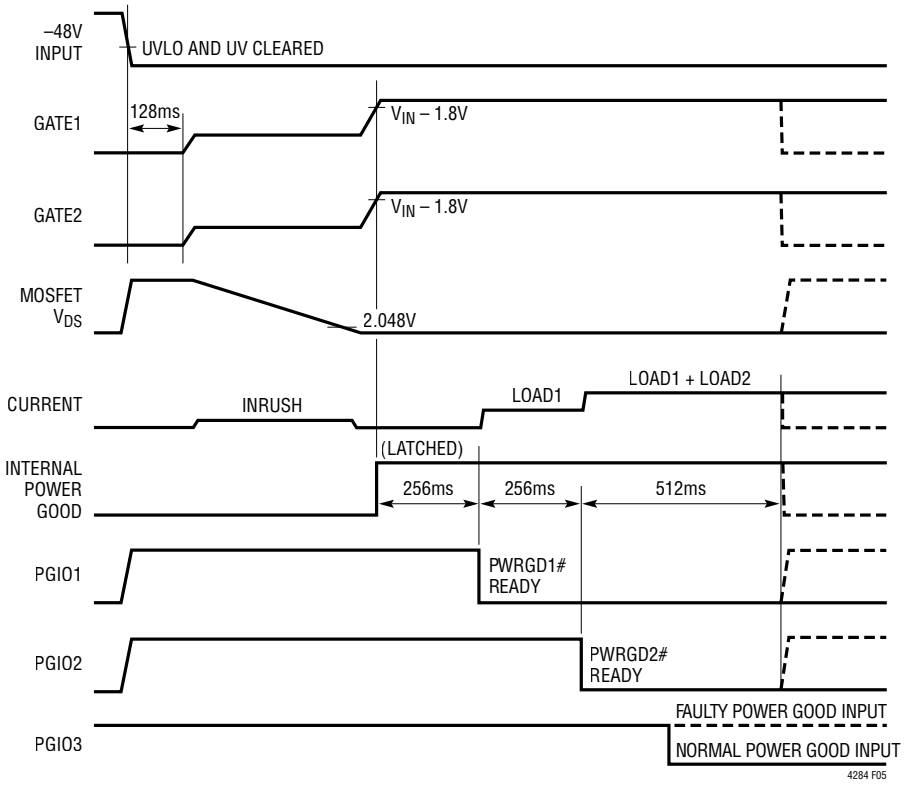

Figure 5. LTC4284 Turn-On Sequence in Parallel Mode

During the power-on-reset delay of 1.3ms, the fault registers are cleared and the control registers are loaded with the data held in the corresponding EEPROM registers. The power-on-reset can be detected using the PORB bit in register 0x0E, which will be cleared when $INTV_{CC}$ dips below 3.8V. Set this bit to 1 in normal operating conditions and keep monitoring this bit. A 0 from subsequent reading indicates a power-on-reset has occurred.

Inrush Control

Inrush current control can be configured in two ways. First, if the DVDT bit in CONTROL_1 register 0x0A is set to 1, the inrush current is controlled in dV/dt mode by an external capacitor connected between RAMP and V_{EE} (the RAMP capacitor, C_R), as shown in Figure 6. In dV/dt mode, the inrush current is limited by controlling a constant output voltage ramp rate (dV/dt). During startup, when the GATE voltage reaches the MOSFET threshold voltage, RAMP outputs a fixed 2.5µA current to charge C_R while the inrush current charges load capacitor C_L.

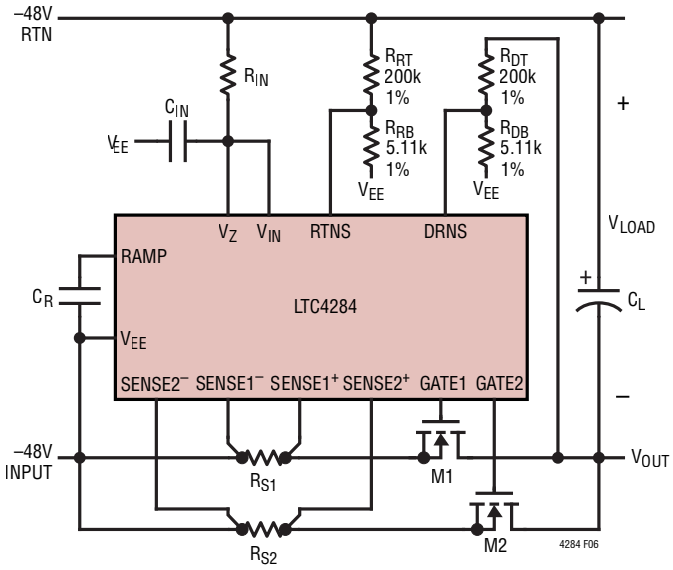

Figure 6. dV/dt Inrush Control Using RAMP Capacitor

During dV/dt control the LTC4284 regulates the RAMP to the attenuated load voltage between RTNS and DRNS with an offset:

$$V_{RAMP} = V_{RTNS} – V_{DRNS} + 0.18V$$

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and regulates the inrush current to a fixed value that is a function of the attenuation ratio, r and the ratio between load capacitance and RAMP capacitance:

$$I_{INRUSH} = 2.5\mu A \bullet r \bullet \frac{C_L}{C_R}$$

The attenuation ratio r is set by the external resistive dividers at RTNS (R_{RT} and R_{RB}) and DRNS (R_{DT} and R_{DB}) in Figure 6:

$$r = \frac{R_{RT}+R_{RB}}{R_{RB}} = \frac{R_{DT}+R_{DB}}{R_{DB}}$$

RTNS and DRNS represent the attenuated input voltage and MOSFET drain voltage, respectively. The differential voltage between RTNS and DRNS therefore represents the attenuated load voltage. The operation range of V_{RTNS}, V_{DRNS} and $V_{RTNS} – V_{DRNS}$ is from 0V to 2.8V.

The dV/dt control is only active during initial startup. After the turn-on sequence is completed and power good signals are activated, the dV/dt inrush control mode is disabled and RAMP is discharged with a 4mA current. RAMP will also be discharged under any GATE turn-off conditions. In the dV/dt mode the inrush current must be set lower than the folded back current limit level to avoid triggering the current limit (see below).

The second inrush control mechanism is active current limiting. This is enabled by clearing the DVDT bit in CONTROL_1 register 0x0A. In this mode the inrush current is regulated to the folded back current limit:

$$I_{INRUSH} = I_{LIM} \bullet \alpha_{STARTUP}$$

where I_{LIM} is the current limit and $\alpha_{STARTUP}$ is the startup foldback factor. I_{LIM} is determined by the current limit sense voltage V_{ILIM} and the sense resistance R_S.

$$I_{LIM} = \frac{V_{ILIM}}{R_S}$$

V_{ILIM} is configurable from 15mV to 30mV in 1mV steps. $\alpha_{STARTUP}$ is configurable to 10%, 20%, 50% and 100% (no foldback) of current limit. During startup the current limit foldback profile is flat and does not change with output voltage. See Current Limit Adjustment and Current Limit Foldback for details. In this mode the RAMP capacitor C_R at the RAMP pin no longer takes effect. If C_R is omitted, RAMP must be left open.

In parallel mode or single driver mode, GATE1 and GATE2 are turned on simultaneously to charge the load capacitor. In staged start modes, GATE1 is turned on first to charge the load capacitor and GATE2 is turned on after the load capacitor is fully charged. See High Stress Staged Start Mode (Mode 3) and Low Stress Staged Start (Mode 4) for details.

Power Good Monitors and PGI Fault

After the MOSFETs are turned on, the following conditions must be met before the power good signals are activated. First, the DRAIN voltage must fall below 2.048V to indicate the MOSFET drain is low. Second, RTNS – DRNS must be higher than the external threshold voltage at VOUTTH to indicate the output voltage is high. Last, GATE voltages must satisfy the GATE high ($>V_{IN}$ – 1.8V) condition. For parallel mode, one GATE must be high and the other GATE must be either high or in current limit. When all three conditions are met, an internal power good signal is latched, the PG_STATUS bit in SYSTEM_STATUS register 0x00 is set, and a series of three delay cycles are started as illustrated in Figure 5. When the first delay of 256ms expires, the first power good signal PGIO1 turns on the first load. When the second delay of 256ms expires, the second power good signal PGIO2 can be used to turn on a second load.

Following the two 256ms delays, a third delay of 512ms is started for monitoring PGIO3 as a power good input (PGI) watchdog. Before this delay expires, PGIO3 must be pulled low or high (polarity configurable by register 0x10) by an external supply monitor to indicate the load is working properly. Otherwise, the MOSFETs are turned off and a PGI fault is logged in FAULT register 0x04. The MOSFETs are allowed to auto-retry after a delay of 128ms following the PGI fault if the PGI_RETRY bit in CONTROL_2 register 0x0B is set to 1. Both power good signals and the power good input can be configured into inverted or non-inverted polarity using PGIO_CONFIG_1 register 0x10 (see Table 12). To disable the PGI watchdog, connect PGIO3 to V_{EE} or $INTV_{CC}$ depending on the configured polarity, or configure PGIO3 as general purpose input or output using register 0x10.

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Power good signals are reset in two configurable ways. If the PWRGD_RESET_CNTRL bit in CONTROL_1 register 0x0A is set to 1, power good signals are reset by an output low condition as indicated by RTNS – DRNS < VOUTTH. In Figure 2a VOUTTH is biased at 0.8V, so power good signals will be reset when RTNS – DRNS drops below 0.8V, which corresponds to V_{OUT} < 32V. If the PWRGD_RESET_CNTRL bit is cleared, power good signals are reset by any GATE turn-off conditions except overvoltage fault. When the power good signals are reset, the power good delays and the PGI delay are also reset.

Turn-Off Sequence

In any of the following conditions, the MOSFETs are turned off by pulling down the GATE pins with 9mA current sources and the FET_ON_STATUS bit in SYSTEM_STATUS register 0x00 is cleared.

1. V_{IN} is lower than 7.6V (V_{IN} undervoltage lockout).
2. $INTV_{CC}$ is lower than 3.8V ($INTV_{CC}$ undervoltage lockout).
3. EN# is high.
4. ON bit in CONTROL_1 register 0x0A is cleared.
5. OV is higher than 1.406V (overvoltage fault).
6. UVL is lower than 1.833V and UVH is lower than 2.048V (undervoltage fault).
7. TMR reaches its 2.048V threshold (overcurrent fault).
8. DRAIN rises above 2.048V or GATE dips below V_{IN} – 1.8V and this condition lasts longer than a preconfigured delay (FET bad fault).
9. PGIO3, when configured as PGI#/PGI input, is high/low when the PGI check delay of 512ms expires (PGI fault).
10. PGIO4 pin, when configured as EXT_FAULT#/EXT_FAULT, is low/high (external fault).
11. The RBT_EN bit in REBOOT register 0xA2 is set.

For condition 8, if the FET_BAD_TURN_OFF bit in CONTROL_1 register 0x0A is cleared, the MOSFETs remain on following a FET bad fault. For condition 10, if the EXT_FAULT_TURN_OFF bit in CONFIG_3 register 0x0F is cleared, the MOSFETs remain on following an external fault. For condition 11, the LTC4284 will automatically reboot after a programmable delay. See Reboot on I^2C Command.

For each independent GATE turn-off fault, the LTC4284 can be configured to latch off the MOSFETs or go into an auto-retry sequence after the fault occurs. In parallel mode or single driver modes, GATE1 and GATE2 are turned off simultaneously. In high stress or low stress staged start modes, GATE2 turn-off depends on GATE1 turn-off and other conditions. Refer to the sectors covering high stress staged start mode and low stress staged start mode for details.

Overcurrent Protection

The LTC4284 features two levels of protection from short-circuit and overcurrent conditions. Load current is monitored by SENSE1,2$^+$ and SENSE1,2$^-$ pins and sense resistors. There are two distinct thresholds for the sense voltages: V_{ILIM} and $V_{ILIM(FAST)}$. V_{ILIM} is configurable from 15mV to 30mV in 1mV steps and $V_{ILIM(FAST)}$ is always twice V_{ILIM}. See Current Limit Adjustment for details.

If the sense voltage of a channel reaches V_{ILIM}, the corresponding GATE is pulled down by 25mA current until the associated active current limit loop is engaged. In the event of a catastrophic short-circuit or a sudden input step, where the sense voltage of a channel reaches $V_{ILIM(FAST)}$, the corresponding GATE is immediately pulled down by a 1.2A current to limit peak current through the MOSFET. When the sense voltage drops to V_{ILIM}, the active current limit loop is engaged.

SOA Timer

During active current limit, the power dissipation in the MOSFET is large. If this power dissipation persists, the MOSFET can reach temperatures that cause damage. MOSFET manufacturers specify the safe limits on operating voltage, current and time as a curve referred to as the Safe Operating Area (SOA). Commonly, a circuit breaker timer sets a maximum time for the MOSFET to operate in a current limit mode. When this timer expires, the MOSFET

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is turned off to protect it from overheating. Traditional circuit breakers often employ a fixed current charging an external capacitor. The minimum timer timeout must be set to allow the worst-case operating condition, such as completely charging a large bypass capacitor at output during startup or riding through a large input step. Then upon fault conditions such as an output short-circuit at full supply voltage, the MOSFET must withstand the large power throughout the entire timer duration. Therefore, the MOSFET must be selected to withstand the worst-case SOA condition that occurs during any possible normal operating condition or fault condition. This not only substantially increases the cost of the MOSFET, but also complicates the design procedure and MOSFET selection.

The LTC4284 features a circuit breaker timer that better fits the SOA of the MOSFET. When active current limit is engaged, the OC_STATUS bit in FAULT_STATUS register 0x03 is set, and the TMR pin is activated and charged up by a current proportional to the power dissipation in the MOSFET that is driven by GATE1. The enabling condition of the TMR charging current depends on the operation mode (see OC_STATUS bit column in Table 1). A proper electric model (RC network) is selected to represent the thermal behavior of the MOSFET. When this RC network is connected between TMR and V_{EE}, the TMR voltage is proportional to the rise in the MOSFET junction temperature. The LTC4284 compares the TMR voltage to a fixed threshold voltage of 2.048V, which represents the maximum allowable junction temperature rise in the MOSFET. When the TMR voltage crosses this threshold, the LTC4284 turns off the MOSFET. Therefore, to provide an appropriate protection of a MOSFET, one simply selects the MOSFET that meets the SOA requirement for allowable operating conditions such as startup and input step. The MOSFET is automatically turned off before it is subject to any condition that would exceed its SOA rating.

Case 1. If active current limit is engaged in normal operation (power good signals are asserted), the TMR pull-up current of the LTC4284 is proportional to the attenuated drain voltage of the MOSFET at DRNS (top line in Figure 7). This is proportional to the power dissipation since the current through the MOSFET is fixed during

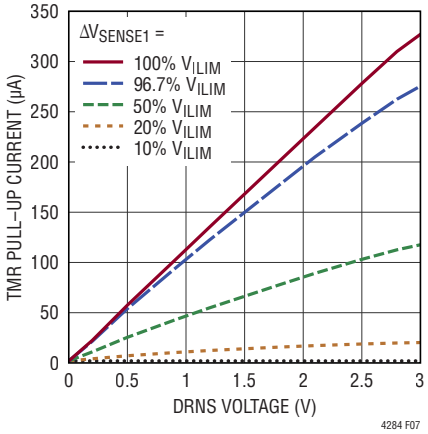

Figure 7. TMR Pull-Up Current vs ΔV_{SENSE1} and DRNS Voltage

current limit (provided that foldback is disabled in normal operation by setting the FB_DIS bit in CONFIG_1 register 0x0D). The TMR pull-up current in this condition is:

$$I_{TMR(UP)} = 111.1\left[\frac{\mu A}{V}\right] \bullet V_{DRNS} + 2\mu A$$

where 111.1μA/V is the transconductance. The TMR pull-up current reaches 202μA at V_{DRNS} = 1.8V, which is tested and specified. The offset of 2μA is introduced to guarantee a minimum pull-up current that prevents TMR from hanging in a resistive short-circuit condition.

The above equation also applies to startup in dV/dt mode (DVDT bit in CONTROL_1 register 0x0A = 1), when the current limit is triggered under a fault condition such as a short-circuit. The accelerated timeout combined with startup foldback (see Current Limit Foldback) protects the startup MOSFET from overstress.

Case 2. During startup in dV/dt mode when current limit is not engaged, TMR pull-up current is disabled:

$I_{TMR(UP)} = 0$

In this case a 2μA pull down current holds TMR low if the THERM_TMR bit in control register 0x0A is set. This avoids undesired timeout before the load capacitor is fully charged by the inrush current, which is set to such a low level that the power dissipation in the startup MOSFET is insignificant.

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Case 3. If current limit is engaged during startup in current limit mode (DVDT bit in CONTROL_1 register 0x0A = 0), the TMR pull-up current is reduced by the foldback ratio:

$$I_{TMR(UP)} = \alpha_{STARTUP} \bullet 111.1\left[\frac{\mu A}{V}\right] \bullet V_{DRNS} + 2\mu A$$

where $\alpha_{STARTUP}$ is the startup foldback ratio that is controlled by the FB bits in CONFIG_1 register 0x0D (see Current Limit Foldback). The reduction keeps the transconductance unchanged compared to that in normal operation with foldback disabled.

Case 4. If current limit is not engaged, either in normal operation or during startup in current limit mode, the TMR pull-up current is gated by the DRAIN voltage. If DRAIN is lower than its threshold, $V_{D,FET(TH)}$, the TMR pull-up current is disabled. $V_{D,FET(TH)}$ is programmable from 72mV to 203mV in geometric scale using the VDTH bits in CONFIG_2 register 0x0E. This is a typical case in normal operating conditions when MOSFETs are fully enhanced. If DRAIN is higher than $V_{D,FET(TH)}$, an internal multiplier charges up TMR with a current approximately proportional to power dissipation in the channel 1 MOSFET:

If $\Delta V_{SENSE1} \geq 0.1V_{ILIM}$,

$$I_{TMR(UP)} = 111.1\left[\frac{\mu A}{V}\right] \bullet V_{DRNS} \bullet \left(\frac{\Delta V_{SENSE1}}{V_{ILIM}} - 0.1\right) + 2\mu A$$

If $\Delta V_{SENSE1} < 0.1V_{ILIM}$,

$$I_{TMR(UP)} = 2\mu A$$

Figure 7 shows the TMR pull-up currents vs V_{DRNS} at four different $V_{SENSE1}^+ - V_{SENSE1}^-$ levels below current limit.

If using an RC network representing the MOSFET thermal model between TMR and V_{EE}, the THERM_TMR bit in CONTROL_1 register 0x0A must be set to 1 to disable the internal 2µA pull-down current. The total resistance in the RC network provides the discharge path to TMR.

The RC network connected to TMR should be configured to represent the electric model of the thermal behavior associated with the MOSFET (M1) driven by GATE1. M1 should be selected so that its SOA is equal to or worse than that of the MOSFET (M2) driven by GATE2. Since GATE2 turns off when GATE1 turns off due to TMR timeout, M2 is automatically protected when M1 is turned off under overload conditions.

The configuration of the RC network for a particular MOSFET starts with selection of a desired number of resistive and capacitive elements and their values in thermal domain based on the thermal impedance plot provided by the MOSFET manufacturer. Three resistors and three capacitors are usually enough to fit the plot fairly well from 10µs to 100ms, which covers the timing range of typical operating and fault conditions. Two resistors and two capacitors may provide an acceptable accuracy for some MOSFETs or conditions. If better fitting accuracy or wider fitting range is desired, more elements may be used. After the thermal RC network is configured, the thermal quantities are then converted to electric quantities according to

$$R_E = k \bullet R_\theta$$

$$C_E = \frac{C_\theta}{k}$$

where R_E and C_E are electric resistance and capacitance, respectively and R_θ and C_θ are thermal resistance and capacitance, respectively. The conversion constant k is given by

$$k = \frac{V_{DS,MAX} \bullet I_{D,MAX}}{I_{TMR(UP),MAX}} \bullet \frac{V_{TMR(TH)}}{\Delta T_{MAX}}$$

where $V_{DS,MAX}$ and $I_{D,MAX}$ are the maximum drain-to-source voltage and maximum drain current of the MOSFET, respectively, $I_{TMR(UP),MAX}$ is the TMR pull-up current corresponding to the maximum power dissipation $P_{MAX} = V_{DS,MAX} \bullet I_{D,MAX}$, $V_{TMR(TH)}$ is TMR threshold voltage (2.048V), and ΔT_{MAX} is the maximum allowable temperature rise of the MOSFET. For example, if $V_{DS,MAX}$ = 72V, $I_{D,MAX}$ = 32A, $I_{TMR(UP),MAX}$ = 202µA (at V_{DRNS} = 1.8V, in current limit) and ΔT_{MAX} = 65°C (maximum junction temperature of MOSFET = 150°C and ambient temperature = 85°C), $k = 3.6 \bullet 10^5$ [V^2/°C]. An RC network consisting of two resistors and capacitors that represent the electric model for the thermal behavior of PSMN4R8-100BSE is show in Figure 2a.

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The LTC4284 also allows a single capacitor connected between TMR and V_{EE} (see Figure 13 and Figure 15). In this case, the THERM_TMR bit in the CONTROL_1 register must be cleared to enable the internal 2µA pull-down current. Once enabled, the 2µA pull-down current keeps TMR low in normal conditions when the pull-up current is disabled. When the pull-up current is enabled under fault conditions, the 2µA pull-down is switched off. A minimum capacitance must be selected to keep the MOSFETs on during worst-case operating conditions, and the MOSFETs must be selected to withstand the worst-case SOA condition during normal operating or fault conditions. Regardless of the value of the THERM_TMR bit, when EN# is higher than its 1.28V threshold, TMR is discharged by a 5mA current. When TMR is below 0.1V, the TMR_LOW bit in SYSTEM_STATUS register 0x00 is set to 1.

Overcurrent Fault and Auto-Retry

Under an overcurrent condition, when the active current limit loops are engaged and TMR is being charged up, the overcurrent present bit, OC_STATUS, in FAULT_STATUS register 0x03 is set. When the TMR voltage reaches its 2.048V threshold, the overcurrent fault bit, OC_FAULT, in the FAULT register 0x04 is set and the GATE pins are pulled down to turn off the MOSFETs.

After the MOSFETs are turned off, the OC_STATUS bit is cleared. The MOSFETs are allowed to turn on again after a cooling delay if the OC_RETRY bits in CONTROL_2 register 0x0B have not been cleared. The auto-retry cooling delay is configurable from 512ms to 65.5s in binary scale using the COOLING_DL bits in CONFIG_2 register 0x0E (See Table 11). During the cooling delay the DELAY_STATUS bit in REBOOT register 0xA2 is set to 1 to indicate the delay timer is running. It will be cleared when the delay expires. The number of retries following an overcurrent fault can be configured to 1, 7 or infinity using the OC_RETRY bits (see Table 10). If a finite retry number is selected, a retry counter reset timer of 16.4s is started upon the retry following an overcurrent fault. If the next overcurrent fault occurs before the timer times out, the retry counter increments and the timer is restarted. Otherwise the retry counter is restarted. When the programmed number of retries is reached, the MOSFETs will be latched off if the next overcurrent fault occurs before the counter reset timer times out. During startup when power good conditions are not met, the counter reset timer is disabled. The retry counter and the counter reset timer for the overcurrent fault are independent of those for the FET bad fault.

If the OC_RETRY bits in the CONTROL_2 register 0x0B have been cleared, the MOSFETs will remain off until the OC_FAULT bit is reset (see Resetting Faults). When the OC_FAULT bit is reset, the MOSFETs are allowed to turn on after the auto-retry delay expires.

Current Limit Adjustment

The current limit voltage, V_{ILIM}, is programmable between 15mV and 30mV in 1mV steps through the I^2C interface using the ILIM bits in CONFIG_1 register 0x0D. The default values are stored in EE_CONFIG_1 register 0xAD in the onboard EEPROM. The fast GATE pull-down sense voltage, $V_{ILIM(FAST)}$, is set to twice of V_{ILIM} through the whole configuration range. The fine scales are useful in adjusting the sense voltage to achieve a given current limit using the limited selection of standard sense resistor values available around 1mΩ. The adjustability allows the LTC4284 to reduce available current for light loads or increase it in anticipation of a surge. This feature also enables the use of board-trace as sense resistors by trimming the sense voltage to match measured copper resistance during final test. The measured copper resistance may be written to the undedicated scratch pad area of the EEPROM (0xE9-0xEF) so that it is available to scale ADC current measurements.

Current Limit Foldback

The LTC4284 current limit can be configured to fold back to four levels: 10%, 20%, 50% and 100% (no foldback) of full current limit using the FB bits in the CONFIG_1 register 0x0D. During the startup inrush control the foldback profile is flat (Figure 8a), resulting in a constant current limit. This is to protect the MOSFETs more effectively upon a resistive output short during startup. With a traditional resistive foldback profile, if the output short resistance is the same as the slope of the foldback profile, the foldback has no effect and MOSFETs with larger SOAs must be selected to withstand the full stress, substantially increasing the MOSFET cost.

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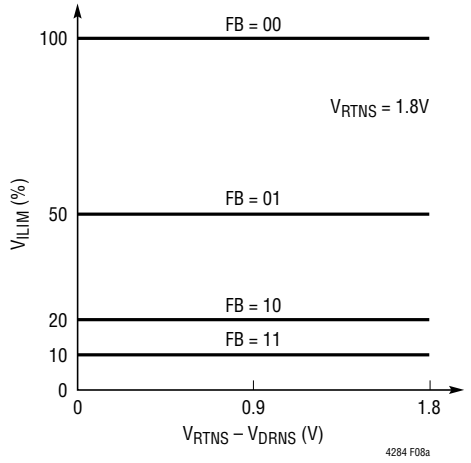

Figure 8a. Current Limit Foldback During Startup

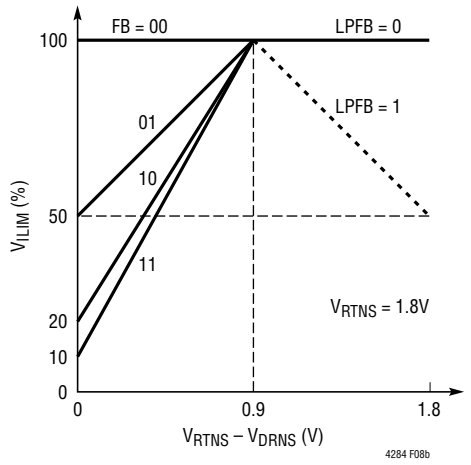

Figure 8b. Current Limit Foldback in Normal Operation

After the internal power good signal is latched (see Power Good Monitors and PGI Fault), the LTC4284 goes into normal operation and the foldback is determined by the attenuated output voltage for the load, RTNS – DRNS (Figure 8b). If the output voltage or RTNS – DRNS drops to 0V in an event such as a catastrophic output short, the current limit sense voltage is folded back to the ratio configured by the FB bits. As shown in Figure 8b, the foldback ratio increases linearly with RTNS – DRNS and reaches 100% when RTNS – DRNS reaches 0.9V, which corresponds to the minimum supply voltage of an application. Above 0.9V the current limit sense voltage stays constant unless the load power foldback (LPFB) bit in the CONFIG_1 register 0x0D is set. If the LPFB bit is set, the current limit sense voltage decreases linearly to 50% when RTNS – DRNS reaches 1.8V (corresponding to the maximum supply voltage). This profile approximately tracks the load power when the output voltage increases with a constant power load.

The LTC4284 foldback profile can differentiate an output short fault from an allowed input step. Upon an output short, RTNS – DRNS drops and current limit is folded back to protect the MOSFETs from overstress. In the event of an input step, RTNS – DRNS increases while the load is charged up. The current limit either stays constant or approximates constant load power (based on the LPFB bit) to approach the optimum output ramp and minimize the temperature rise of the MOSFETs (see Input Step and Optimum Output Ramp). This is superior to a foldback profile capacitance based upon V_{DS} or power dissipation of the MOSFET. In that case, the output short and input step conditions cannot be differentiated, often resulting in unwanted turn-off upon an input step.

Foldback in normal operation can be independently disabled by setting the FB_DIS bit in the CONFIG_1 register 0x0D. With this configuration foldback is only effective during startup, and it should only be used when an RC network representing the thermal model of the MOSFET is connected to TMR. If a single capacitor is used, it is recommended to enable foldback in normal operation by clearing the FB_DIS bit for more conservative protection of the MOSFET. Note that the load power foldback controlled by the LPFB bit is not affected by the FB_DIS bit.

FET Bad Fault and Auto-Retry

In a hot swap application several possible faults can prevent the MOSFETs from turning on fully. A damaged MOSFET may have leakage from gate to drain or have degraded $R_{DS(ON)}$. Debris on the board may also produce leakage or a short from the GATE pins to V_{EE} or the MOSFET drain. In these conditions the LTC4284 may not be able to pull the GATE pins high enough to fully enhance the MOSFETs, or the MOSFETs may not reach the intended $R_{DS(ON)}$ when the GATE pins are fully enhanced. This can put the MOSFETs in a condition where the power in the MOSFETs is higher than its continuous power capability, even though the current is below the current limit. The

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LTC4284 monitors the integrity of the MOSFETs in two ways, and acts on both of them in the same manner.

First, the LTC4284 monitors the MOSFET drain voltage at the DRAIN pin. A comparator detects a DRAIN high condition whenever DRAIN is above a reference voltage, $V_{D,FET(TH)}$ that can be configured to 72mV, 102mV, 143mV or 203mV (geometric scale) using the VDTH bits in the CONFIG_2 register 0x0E.

Second, the LTC4284 monitors the GATE voltages. If the MOSFETs are turned on, but the GATE1 and/or GATE2 voltages are lower than V_{IN} – 1.8V, a GATE low condition is detected. The logic that determines a GATE low condition depends on the operation mode (see Table 1). For the parallel mode, in turn-on state, a GATE low condition is detected in either of the following two conditions: (1) both GATE1 and GATE2 are low; (2) One GATE is low but not in current limit.

When either a DRAIN high or a GATE low condition is present when the MOSFETs are commanded on, the FET_BAD_STATUS bit in FAULT_STATUS register 0x03 is set and an internal FET bad fault timer is started. The FTBD_DL bits in CONFIG_2 register 0x0E configures the timer duration to 256ms, 512ms, 1.02s and 2.05s. If the DRAIN voltage falls below $V_{D,FET(TH)}$ and the GATE low conditions are cleared before the timer times out, the FET_BAD_STATUS bit is cleared and the timer is reset. If the timer does time out, the FET_BAD_FAULT bit in FAULT register 0x04 is set and the MOSFETs are turned off if the FET_BAD_TURN_OFF bit in CONTROL_1 register 0x0A has been set. The DRAIN high condition also activates TMR pull-up current when not in current limit (see SOA Timer).

Note that during startup while the load is being charged, the FET_BAD_STATUS bit is set and the FET bad fault timer is running. To avoid undesired turn-off, the timer duration must be configured long enough for the load to be fully charged.

After the MOSFETs are turned off following a FET bad fault, the FET_BAD_STATUS bit is cleared. The MOSFETs are allowed to turn on again after a cooling delay if the FET_BAD_RETRY bits in CONTROL_2 register 0x0B have not been cleared. The cooling delay is the same as that for an overcurrent fault and is configurable from 512ms to 65.5s in binary scale using the COOLING_DL bits in CONFIG_2 register 0x0E (see Table 11). During the cooling delay the DELAY_STATUS bit in REBOOT register 0xA2 is set. It will be cleared when the delay expires. The FET_BAD_RETRY bits configures the number of retries following a FET bad fault to 1, 7 or infinity (see Table 10). If a finite retry number is selected, a retry counter reset timer of 16.4s is started upon the retry following a FET bad fault. If the next FET bad fault occurs before the timer expires, the retry counter increments and the timer is reset. Otherwise the retry counter is reset. The retry counter and the counter reset timer for the FET bad fault are independent of those for the overcurrent fault.

If the FET_BAD_RETRY bits in CONTROL_2 register 0x0B have been cleared, the MOSFETs will remain off until the FET_BAD_FAULT bit is reset (see Resetting Faults) or the FET_BAD_TURN_OFF bit is cleared through I^2C. In either of those two cases, the MOSFETs are allowed to turn on after the auto-retry delay expires.

Input Step and Optimum Output Ramp

In events such as battery hot swapping or supply surge, the input voltage may experience a sudden step. The magnitude of the input step, ΔV, can be as large as tens of volts. As long as the input voltage does not exceed the overvoltage limit, the input step is not a fault condition and the system should stay on and operate through it. In the presence of the load capacitor, the output does not follow the input immediately, but rather ramps up from the initial supply voltage to the new supply voltage while charging the load capacitor. The V_{DS} of the MOSFET initially jumps to ΔV and then ramps down. Additionally, during the output ramp the MOSFET not only carries the load current, I_L but also the capacitance charging current, I_{CL}, so the total power dissipation in the MOSFET can be very large. If a large input step is possible, it is usually the worst-case operating condition for the SOA of the MOSFET, and proper MOSFETs must be selected to withstand the stress.

In such a condition, the minimum temperature rise of the MOSFET is achieved when I_{CL} matches I_L, or the total current is twice the load current. In other words, the current

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limit should be set to twice the load current during the output ramp:

$$I_{LIM(OPT)} = 2 \bullet I_L$$

This is in contrast to the concept of foldback that is used to protect the MOSFET in a short-circuit condition. The foldback profile of the LTC4284 automatically takes care of both input step and output short-circuit conditions by relating the foldback ratio to the output voltage for the load instead of V_{DS} of the MOSFET. See Figure 8b and Current Limit Foldback for details. Additionally, if the load follows a constant power relationship, the LPFB bit in CONFIG_1 register 0x0D can be set to enable load power foldback so that the current limit approximately tracks twice the load current during the output ramp. The waveforms in Figure 9 show how the LTC4284, operating in the parallel mode, responds to a –36V to –72V input step

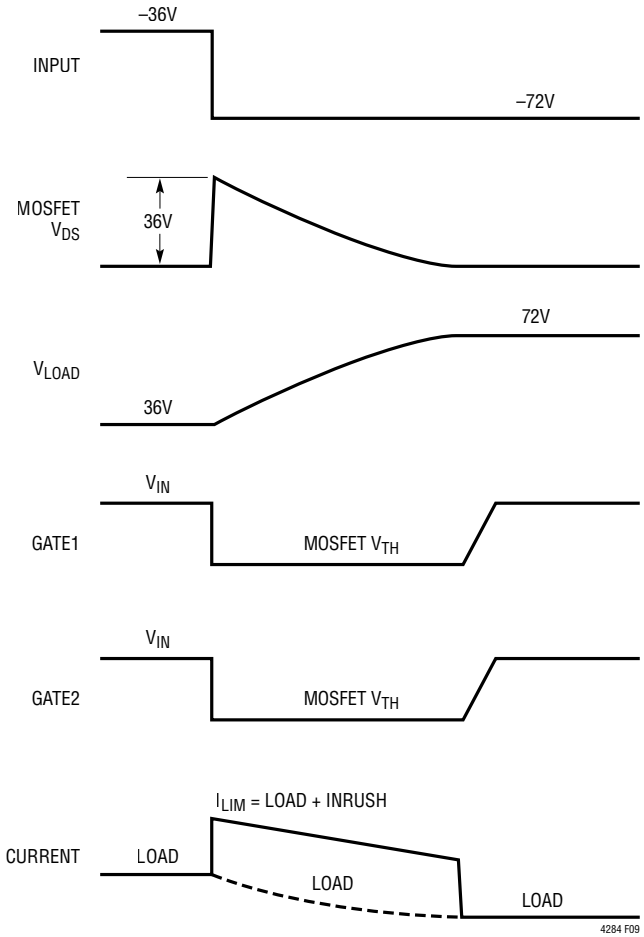

Figure 9. LTC4284 Responds to –36V to –72V Input Step with a Constant Power Load (in Parallel Mode, LPFB = 1)

to achieve the optimum output ramp rate. Note that the power good signals on PGIO1 and PGIO2 are not interrupted during an input step.

Dual-Gate Operation Modes

The LTC4284 features dual-gate drivers that are configured by the MODE pin into four distinct operation modes: single driver, parallel, high stress staged start, and low stress staged start. As shown in Table 1, each mode features specific SOA or $R_{DS(ON)}$ benefit, GATEs on/off behavior, power good signaling and fault detection logic. Leave MODE open (or bias it between 1V and $INTV_{CC}$ – 0.85V) to select the single driver mode (Mode 1). Pull MODE lower than 0.4V (e.g., connect to V_{EE}) to select the parallel mode (Mode 2). Force MODE higher than $INTV_{CC}$ + 2.5V (e.g., connect to V_{IN}) to select the high stress staged start mode (Mode 3). Bias MODE between $INTV_{CC}$ – 0.25V and $INTV_{CC}$ + 0.5V (e.g., connect to $INTV_{CC}$) to select the low stress staged start mode (Mode 4). Each mode has a dedicated status bit in SYSTEM_STATUS register 0x00 (Table 4) and ADC_STATUS register 0x01 (Table 5) to indicate the mode is selected.

Parallel Mode (Mode 2)

The parallel mode works well for systems with large input steps or supply surges. The MOSFETs must be selected to withstand this worst-case operating condition for the SOA. See Input Step and Optimum Output Ramp for details.

High current applications often demand several power MOSFETs in parallel to reach a target $R_{DS(ON)}$ under 1mΩ that is unavailable in a single MOSFET. In such cases several parallel sense resistors are also used to get small values that are not available as a single resistor. Further, dividing the load current amongst multiple devices alleviates the PCB current crowding problem with the use of a single MOSFET.

Parallel MOSFETs share current well when they are fully enhanced, however when the MOSFETs are limiting current the offset mismatch between gate thresholds will cause the MOSFET with the lowest threshold to carry more current than the others. As this MOSFET gets hot it carries even more current since threshold voltage has a negative temperature coefficient. Eventually all the load current may

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Table 1. Configuration of the LTC4284 Dual-Gate Operation Modes

MODE	MODE PIN	FEATURE	TURN ON SEQUENCE	POWER GOOD LATCH*		OC_STATUS BIT†	GATE1 TURN OFF	GATE2 TURN OFF†	FET BAD STATUS/ FAULT
				SET	RESET				
1. Single Driver	Open	GATE Pull-up and Pull-down Doubled	GATE1 and GATE2 Turn On at the Same Time	DRAIN < 2.048V AND V_{OUT} High AND (Both GATE1 AND GATE2 High)	Configurable: (1) V_{OUT} Low (2) GATE1 Off (Except OV)	ACL1 On OR ACL2 On	CBTMR Reaches 2.048V OR Upon Other GATE-Off Faults	GATE1 Off	FET_ON High AND [DRAIN > $V_{D,FET(TH)}$ OR (GATE1 OR GATE2 Low)]
2. Parallel	Tied to V_{EE}	SOA Doubled, $R_{DS(ON)}$ Halved		DRAIN < $V_{D,PG(TH)}$ AND V_{OUT} High AND [One GATE High AND (the Other GATE High OR in ACL)]		Start-Up: ACL1 On OR ACL2 On; Running: Both ACL1 AND ACL2 On			FET_ON High AND [DRAIN > $V_{D,FET(TH)}$ OR (Both GATE1 AND GATE2 Low) OR (One Gate Low AND Not in ACL)]
3. High Stress Staged Start	Tied to V_{IN}	GATE1 Drives High SOA MOSFET, GATE2 Drives Low $R_{DS(ON)}$ MOSFET	GATE1 Turns On First. GATE2 Turns On after GATE1 High and DRAIN Low	DRAIN < $V_{D,PG(TH)}$ AND V_{OUT} High AND (Both GATE1 AND GATE2 High)		ACL1 On		GATE1 Off OR DRAIN > $V_{D,PG(TH)}$ OR GATE1 Low OR ACL1 On	FET_ON High AND [DRAIN > $V_{D,FET(TH)}$ OR (GATE1 OR GATE2 Low)]
4. Low Stress Staged Start	Tied to $INTV_{CC}$	GATE1 Drives Low SOA MOSFET, GATE2 Drives Low $R_{DS(ON)}$ MOSFET		DRAIN < $V_{D,PG(TH)}$ AND V_{OUT} High AND [GATE1 High AND (GATE2 High OR in ACL)]		Start-Up: ACL1 On; Running: Both ACL1 AND ACL2 On		GATE1 Off	FET_ON High AND [DRAIN > $V_{D,FET(TH)}$ OR (Both GATE1 AND GATE2 Low) OR (One Gate Low AND Not in ACL)]

* V_{OUT} High is equivalent to $V_{RTNS} - V_{DRNS}$ > VOUTTH.

† ACL1: Active current limit circuit associated with GATE1; ACL2: Active current limit circuit associated with GATE2.

be carried by a single MOSFET. For this reason, although the overall $R_{DS(ON)}$ can be effectively lowered when a group of MOSFETs are operated in parallel by a single gate driver, they only provide the SOA of a single MOSFET.

The LTC4284 resolves this problem by offering two gate drivers, each with an independent current limit circuit and associated current sense pins. When connecting MODE to V_{EE}, these two gate drivers operate in the parallel mode, in which GATE1 and GATE2 are turned on or off simultaneously. In this mode the LTC4284 allows a group of parallel MOSFETs to be divided into two channels. During current limiting in an overcurrent event such as output short or input step, the independent gate control of the two channels divides the current evenly between them, resulting in twice the SOA performance of the hot swap controller with a single current limit circuit. This allows the use of smaller and less expensive MOSFETs, can start up a load twice as big, or increases SOA margins. Figure 1 and Figure 2 show 1.2kW application examples operating in the parallel mode. Two MOSFETs in each channel are used so that the power dissipation in each MOSFET when fully enhanced is 1W or less.

In the parallel mode, one GATE may be fully enhanced and the other may be in current limit. This is considered a normal operating condition because the V_{DS} of both MOSFETs is small. Hence in this condition if V_{DRAIN} < $V_{D,PG(TH)}$ and $V_{RTNS} - V_{DRNS}$ > VOUTTH, the power good signals will be asserted. Furthermore, this condition does not set the FET_BAD_STATUS bit in FAULT_STATUS register 0x03. The FET_BAD_STATUS bit will be set and the FET bad fault timer will be started if both GATE1 and GATE2 are low or one GATE is low but not in current limit. See FET Bad Fault and Auto-Retry for details.

During startup, either GATE1 or GATE2 in current limit activates TMR pull-up current. In normal operation (internal power good signal latched), the TMR pull-up current will not be activated unless both GATE1 and GATE2 are in current limit. If an RC network is connected to TMR,

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the RC network should represent the thermal behavior of a single MOSFET, since the TMR pull-up current is only related to power dissipation in the channel 1 MOSFET. When TMR reaches 2.048V (representing the maximum allowable temperature rise in the MOSFET), both GATE1 and GATE2 are turned off and an overcurrent fault is logged in FAULT register 0x04.

If the dV/dt inrush control is enabled by setting the DVDT bit in CONTROL_1 register 0x0A, the inrush current during startup may not be evenly distributed between the two channels due to MOSFET threshold mismatch. Therefore, a proper RAMP capacitor must be selected so that the inrush current is lower than the startup current limit of each channel, not the sum of the two channels.

High Stress Staged Start Mode (Mode 3)

The two GATE drivers of the LTC4284 can also be configured to operate in high stress staged start mode by connecting MODE to V_{IN}. In this mode GATE1 drives a high SOA MOSFET (M1) for startup and to withstand overstresses and GATE2 drives less expensive bypass MOSFETs (M2A and M2B) with low $R_{DS(ON)}$ (their SOAs are usually low, too) to carry the load, as shown in Figure 10.

Similar to the parallel mode, the high stress staged start mode also works well for systems where large input steps or supply surges are inevitable. M1 must be selected with large enough SOA to withstand these conditions, in which M1 not only carries the full load current, but also needs to deliver the capacitive current to charge up the load. See Input Step and Optimum Output Ramp for details.

At power-up, GATE1 is turned on first to charge the load and GATE2 is held off. The startup inrush control can be configured into either current limit mode or dV/dt mode using the DVDT bit in CONTROL_1 register 0x0A. If dV/dt mode is selected, the inrush current must be limited substantially lower than the startup current limit. As illustrated in Figure 11, when GATE1 is fully enhanced ($V_{GATE1} > V_{GATE(TH)}$) and the load capacitor is fully charged ($V_{DRAIN} < 2.048$), GATE2 is turned on.

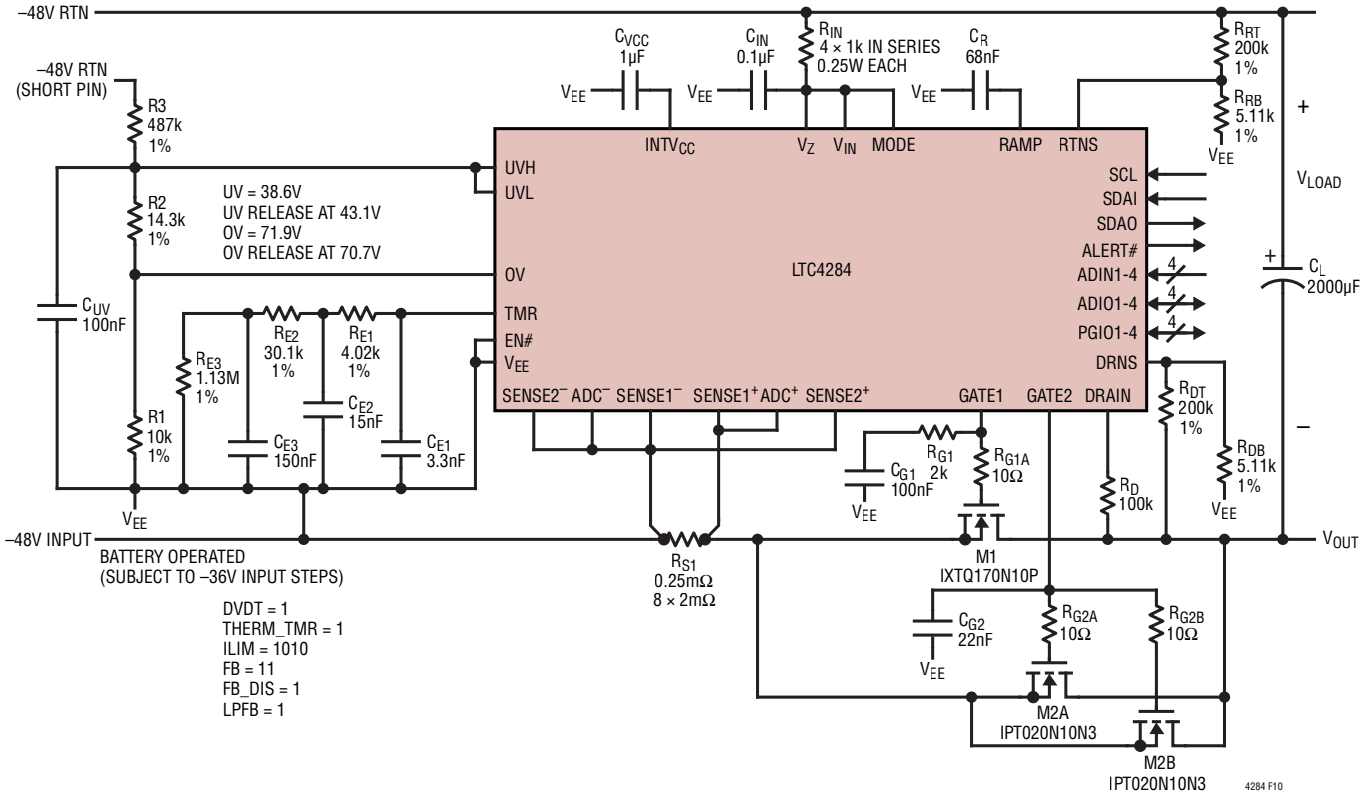

Figure 10. –48V/1800W Hot Swap Controller with SOA Timer and dV/dt Inrush Control in High Stress Staged Start Mode: GATE1 Drives High SOA MOSFET and GATE2 Drives Low $R_{DS(ON)}$ MOSFETs

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After GATE2 is also fully enhanced ($V_{GATE2} > V_{GATE(TH)}$), the internal power good signal is latched provided that $V_{DRAIN} < 2.048$ and $V_{RTNS} – V_{DRNS} >$ VOUTTH. After the power good delays expire, two sequential power good signals are asserted at PGIO1 and PGIO2 (with bits [3:0] in PGIO_CONFIG_1 register 0x10 cleared) and can be used to turn on the loads (see Figure 5). The majority of the load current is delivered by M2A and M2B, which have much lower $R_{DS(ON)}$ than M1.

In this mode the current sense resistor is connected between SENSE1$^+$ and SENSE1$^–$, while SENSE2$^+$ and SENSE2$^–$ are shorted to SENSE1$^–$ to disable the current limit circuit of GATE2. When GATE1 is in current limit in overcurrent events such as an output short or an input step as shown in Figure 12, the LTC4284 immediately switches off GATE2 to protect M2A and M2B from overstress, leaving the current limit of GATE1 to regulate the load current through M1. In this condition the TMR pull-up current is turned on. When the TMR voltage reaches 2.048V, GATE1 is turned off and an overcurrent fault is logged.

The high stress staged start mode decouples SOA from $R_{DS(ON)}$. The MOSFET driven by GATE1 (M1) is selected so that its SOA is large enough to withstand stresses in all operating conditions. The $R_{DS(ON)}$ of M1 is not a major concern, but needs to satisfy $V_{DRAIN} < 2.048$V when GATE2 is off, otherwise GATE2 will not be turned on. The MOSFETs driven by GATE2 (M2A and M2B) are selected so that when fully enhanced, the $R_{DS(ON)}$ is low enough to make the I^2R power dissipation in M2A or M2B below or close to 1W. The SOA of M2A and M2B does not need to be large because GATE2 is switched off in any of the following fault conditions: GATE1 off, GATE1 in current limit, GATE1 low ($V_{GATE1} < V_{GATE(TH)}$), or DRAIN high ($V_{DRAIN} >$ 2.048V). In this way the selection of MOSFET(s) for each channel is easier and the overall cost of MOSFETs may be lower than the parallel mode.

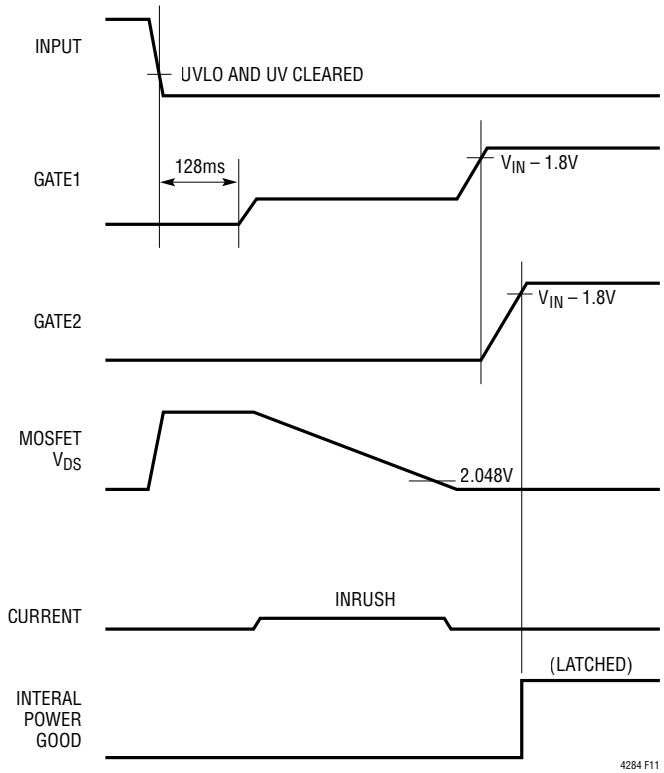

Figure 11. Turn-On Sequence of High Stress Staged Start Mode

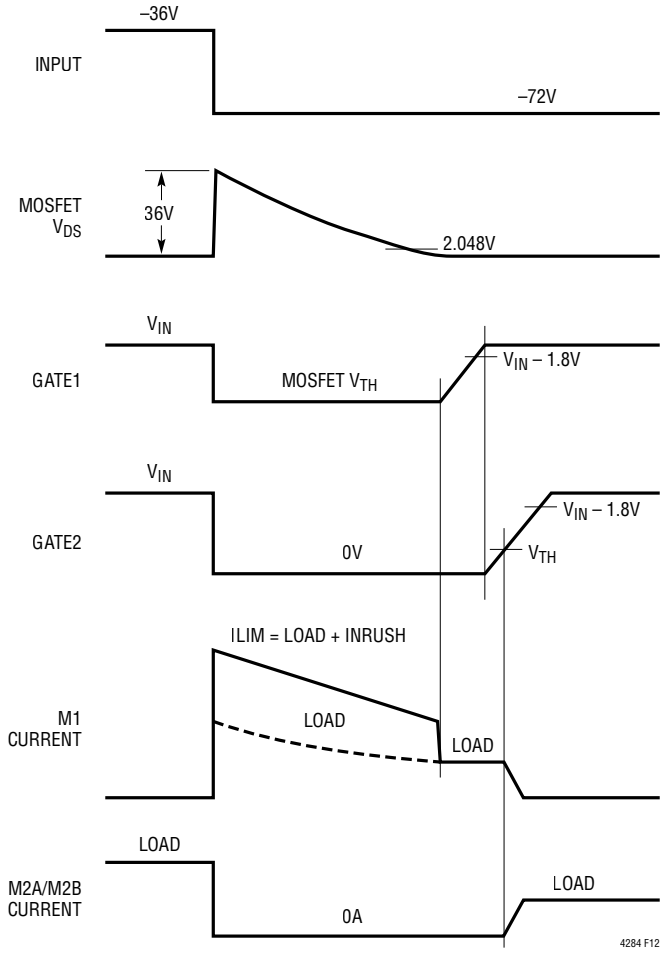

Figure 12. –36V to –72V Input Step Response in High Stress Staged Start Mode (Constant Power Load, LPFB = 1)

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In the high stress staged start mode, either GATE1 low or GATE2 low sets the FET_BAD_STATUS bit in FAULT_STATUS register 0x03 and starts the FET bad fault timer. When the timer expires the FET_BAD_FAULT bit in FAULT register 0x04 is set and both GATE1 and GATE2 are turned off if the FET_BAD_TURN_OFF bit in CONTROL_1 register 0x0A has been set.

Low Stress Staged Start (Mode 4)

The low stress staged start mode is well suited for applications with tightly regulated supply voltages. Since in such a system an input step is no longer a valid operating condition, the worst-case operating condition for the MOSFET SOA is charging up the load during startup. By suppressing the startup inrush current to a very low level, the SOA demand for the startup MOSFET is greatly alleviated. Additionally, the bypass path only needs inexpensive, switching regulator class MOSFETs. Therefore, this architecture minimizes the cost of MOSFETs to achieve a given load current and $R_{DS(ON)}$. However, with the brief timer delay for current limit, it has limited capability to ride through an input step or a sustained load surge in current limit, and due to the low startup current cannot start up a resistive load such as a heating element or incandescent lamp.

Figure 13 shows an application circuit for a 2.5kW system operating in the low stress staged start mode. This mode is enabled by connecting MODE to $INTV_{CC}$. In this mode GATE1 drives a compact, inexpensive MOSFET (M1) with small SOA as a trickle charging device for startup. GATE2 drives parallel low $R_{DS(ON)}$, low SOA MOSFETs (M2A and M2B) with a high current limit configured using parallel small sense resistors to deliver the full load current. The turn-on sequence is exactly the same as in the high stress staged start mode as illustrated in Figure 11: GATE1 turns on first to charge the load and GATE2 turns on after GATE1 is fully enhanced.

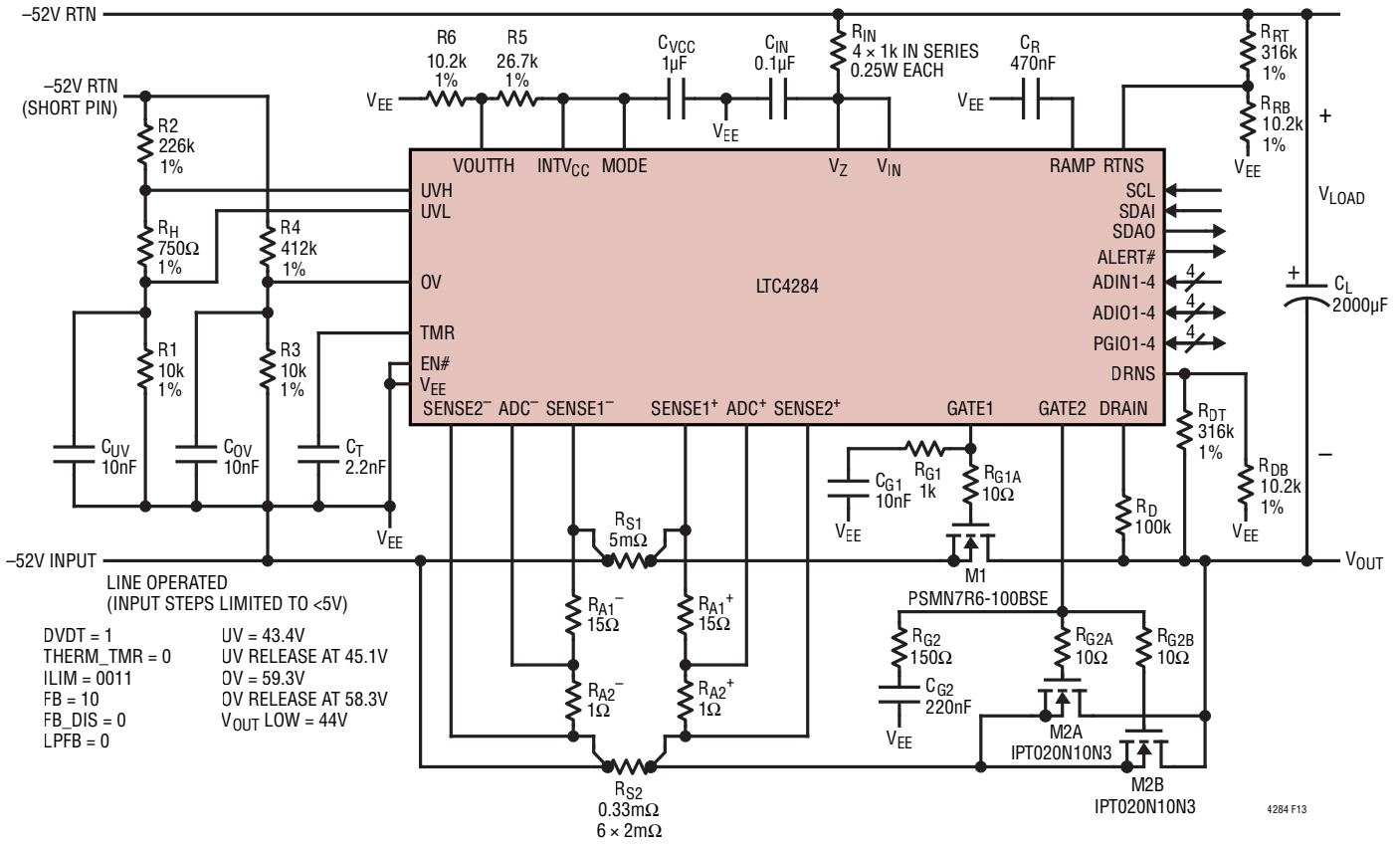

Figure 13. –52V/2500W Hot Swap Controller in Low Stress Staged Start Mode with dV/dt Inrush Control: GATE1 Drives Trickle Startup MOSFET and GATE2 Drives Low $R_{DS(ON)}$ MOSFETs, for Systems with Tightly Regulated Supply Voltages

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GATE2 turns off only if GATE1 turns off, which is different from the high stress staged start mode where GATE2 turns off if GATE1 is in current limit. If an overcurrent event occurs, both GATE1 and GATE2 stay in current limit to share the stress (see Figure 14). Hence the current sense pins for both current limit circuits on GATE1 and GATE2 must be connected to their corresponding sense resistors.

In Figure 13 M1 is configured to deliver a very low inrush current (0.34A) using a RAMP capacitor in the dV/dt startup mode. The current limit is set to 0.72A by the startup foldback ratio and a large sense resistor R_{S1}. When the load is fully charged ($V_{DRAIN} < 2.048$) and the startup MOSFET is fully enhanced ($V_{GATE1} > V_{GATE(TH)}$), GATE2 is turned on. When M2A and M2B are fully enhanced ($V_{GATE2} > V_{GATE(TH)}$), the power good signals are asserted.

The condition to set the FET_BAD_STATUS bit in FAULT_STATUS register 0x03 and starts the FET bad fault timer in this mode is the same as in the parallel mode (see Table 1). Since the FET bad fault timer is running during the trickle startup while the load is slowly charged, the timer duration must be programmed long enough using the FTBD_DL bits in CONFIG_2 register 0x0E to avoid turning off M1 too early.

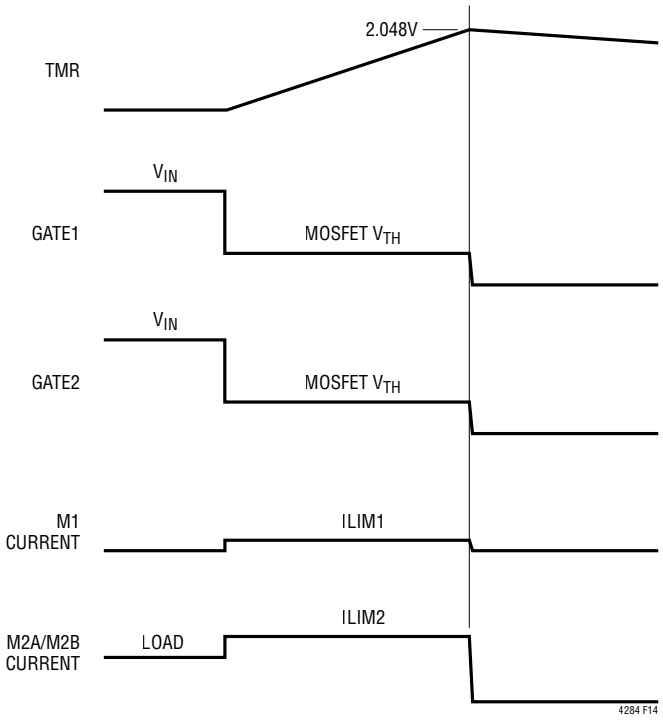

Figure 14. Output-Short Protection in Low Stress Staged Start Mode

During startup in dV/dt mode the TMR pull-up current is disabled. It will not be enabled unless M1 goes into current limit under a fault condition (e.g., start into short-circuit). In normal operation after power good asserted, the TMR pull-up current is enabled when both M1 and M2A/M2B are in current limit. A single, small TMR capacitor as shown in Figure 13 can be used to configure a brief circuit breaker delay, which should be within the worst SOA of M1 and M2A/M2B.

The startup inrush control can also be configured to current limit by clearing the DVDT bit in CONTROL_1 register 0x0A. In this case the TMR pull-up current is enabled during startup and is adjusted according to the foldback ratio. An RC network that represents the electric model for the thermal behavior of M1 should be connected to TMR. Note that after startup when M2A and M2B are turned on, the TMR pull-up current still relates to the power dissipation in M1. M1 should be selected so that its SOA is worse than that of M2A or M2B. In this way M2A and M2B are automatically protected when M1 turns off upon TMR timeout in an overcurrent condition.

Single Driver Mode (Mode 1)

The LTC4284 can also be configured into the single driver mode by floating the MODE pin. There are two possible architectures in this mode. Figure 15 shows the first architecture. GATE1 drives a single MOSFET or parallel MOSFETS so that the LTC4284 behaves the same as a single hot swap controller. GATE2 is left open and its current limit circuit is disabled by shorting the SENSE2$^+$/SENSE2$^-$ pins to V_{EE}.

Figure 16 shows the second architecture, in which GATE1 and GATE2 are combined to drive a single channel of MOSFET(s). SENSE1$^+$ and SENSE2$^+$ are connected together to the positive side of a single current sense resistor and SENSE1$^-$ and SENSE2$^-$ are connected together to the negative side of the resistor. In this way the current limit circuits for both GATE1 and GATE2 are enabled so that the GATE pull-up and pull-down currents are doubled, achieving a faster turn-off in response to fault conditions. The single driver mode can be used in low to medium power applications where a second gate driver is not needed.

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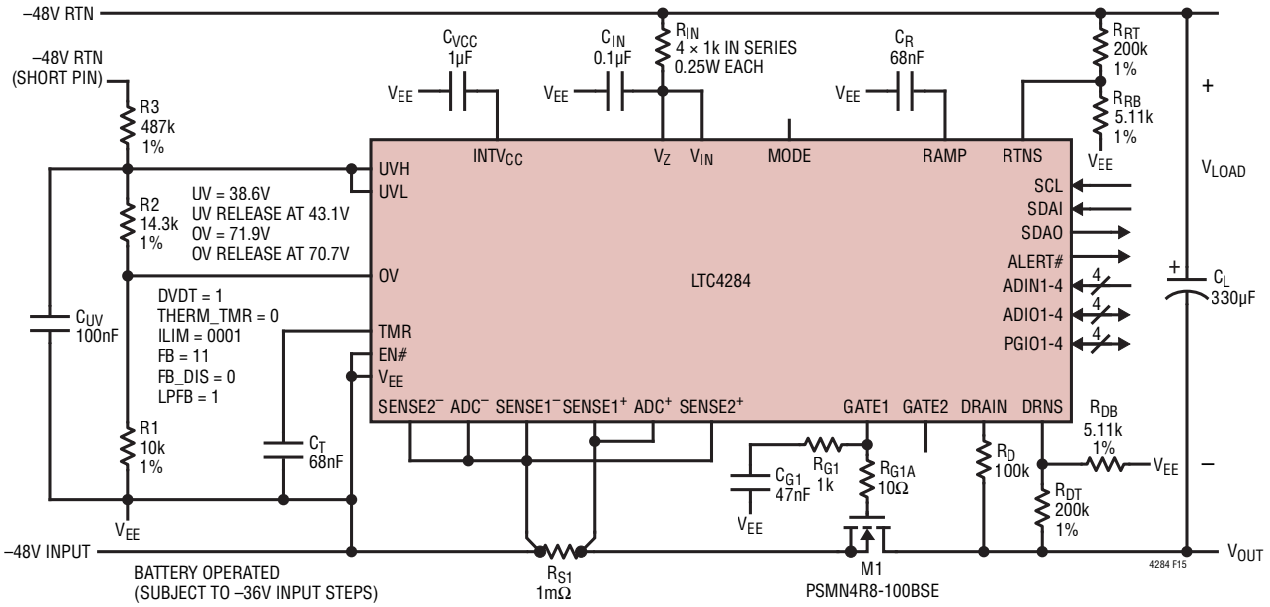

Figure 15. –48V/300W Hot Swap Controller in Single Driver Mode: GATE1 Drives MOSFET and GATE2 Is Open, with dV/dt Inrush Control

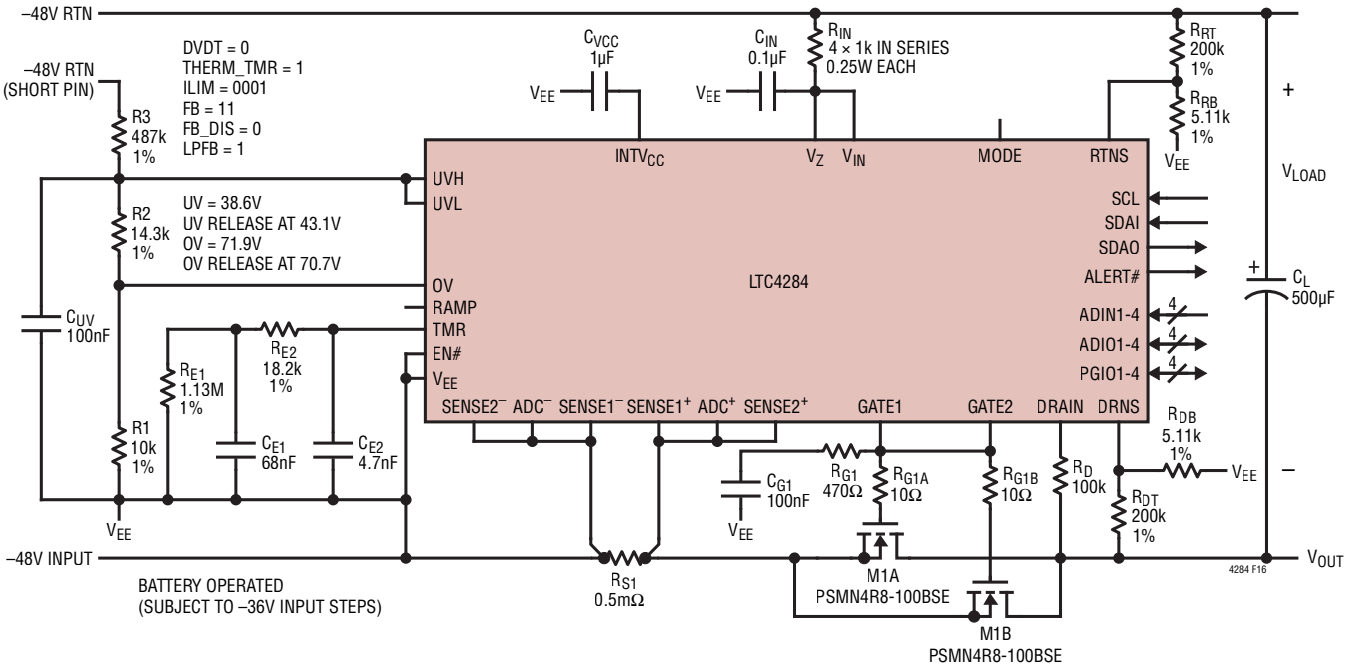

Figure 16. –48V/600W Hot Swap Controller in Single Driver Mode: Both GATE1 and GATE2 Drive MOSFETs, with Current Limit Inrush Control and SOA Timer

Overvoltage Fault and Auto-Retry

The OV pin can be used to monitor a supply overvoltage condition using an external resistive divider. An overvoltage fault occurs when OV rises above its 1.406V threshold. This condition turns off the MOSFETs immediately and sets the OV_STATUS bit in FAULT_STATUS register 0x03 and the OV_FAULT bit in FAULT register 0x04. Note that the power good signals are not affected by the overvoltage fault. If OV subsequently falls back below the threshold

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minus hysteresis of 24mV, the OV_STATUS bit is cleared and the MOSFETs will be allowed to turn on again (without delay) unless overvoltage auto-retry has been disabled by clearing the OV_RETRY bit in CONTROL_2 register 0x0B.

Undervoltage Fault and Auto-Retry

The LTC4284 features two undervoltage pins, UVH and UVL, for precise undervoltage monitoring and adjustable hysteresis. UVH has an accurate rising threshold:

$V_{UVH(TH)}$ = 2.048V, UVH rising

UVL has an accurate falling threshold:

$V_{UVL(TH)}$ = 1.833V, UVL falling

Both pins have a small built-in hysteresis, δV_{UV} (11mV typical). With either a rising or a falling input supply, the undervoltage comparator works in such a way that both UVH and the UVL have to cross their threshold for the comparator output to change state.

The UVH, UVL and OV threshold ratio is designed to match the standard telecom operating range of 43V to 71V and UV hysteresis of 4.5V when UVH and UVL are connected together as in Figure 1, where the UV hysteresis referred to UVL is:

$$\Delta V_{UV(HYST)} = V_{UVH(TH)} - V_{UVL(TH)} = 0.215V$$

Using R1 = 10k, R2 = 14.3k and R3 = 487k as in Figure 1 gives a typical operating range of 43.1V and 70.7V, with an undervoltage shutdown threshold of 38.6V and an overvoltage shutdown threshold of 71.9V.

The UV hysteresis can be adjusted by separating UVH and UVL with a resistor R_H as shown in Figure 17. To increase the UV hysteresis, place the UVL tap above the UVH tap as in Figure 17a. To reduce the UV hysteresis, place the UVL tap under the UVH tap as in Figure 17b. UV hysteresis referred to UVL is given by:

If $V_{UVL} \geq V_{UVH}$,

$$\Delta V_{UVL(HYST)} = \Delta V_{UV(HYST)} + 2.048V \bullet \frac{R_H}{R1+R2}$$

If $V_{UVL} < V_{UVH}$,

$$\Delta V_{UVL(HYST)} = \Delta V_{UV(HYST)} - 2.048V \bullet \frac{R_H}{R1+R2+R_H}$$

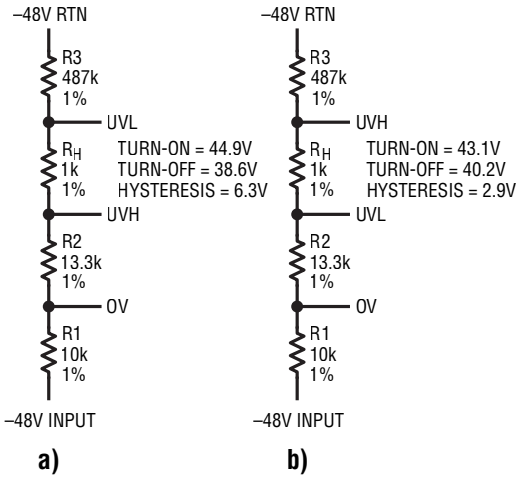

Figure 17. Adjustment of Undervoltage Thresholds for Larger (17a) or Smaller (17b) Hysteresis

In the latter case, the minimum UV hysteresis allowed is the built-in hysteresis of UVH and UVL:

$$\Delta V_{UVL(HYST,MIN)} = \delta V_{UV} = 11mV$$

which occurs when R_H reaches its maximum value:

$$R_{H(MAX)} = 0.11 \bullet (R1 + R2)$$

LTC4284 ensures that the UV comparator is immune to chattering even when R_H is larger than $R_{H(MAX)}$.

An undervoltage fault occurs when UVL falls below 1.833V and UVH falls below 2.048V – δV_{UV}. This condition turns off the MOSFETs and sets the UV_STATUS bit in FAULT_STATUS register 0x03 and the UV_FAULT bit in FAULT register 0x04.

Following the undervoltage fault, the UV_STATUS bit is cleared when the UVH pin rises above 2.048V and UVL rises above 1.833V + δV_{UV}. After a delay of 128ms, the MOSFETs will be allowed to turn on again unless the undervoltage auto-retry has been disabled by clearing the UV_RETRY bit in CONTROL_2 register 0x0B.

When power is applied to the device, if UVL is below the 1.833V threshold and UVH is below 2.048V – δV_{UV} after $INTV_{CC}$ crosses its undervoltage lockout threshold of 4V, an undervoltage fault will be logged in FAULT register 0x04 and can be cleared using the I^2C interface after power-up.

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Because of the compromises of selecting from a table of discrete resistor values (1% resistors in 2% increments, 0.1% resistors in 1% increments), best possible OV and UV accuracy is achieved using separate dividers for each pin, This increases the total number of resistors from three or four to as many as six, but maximizes accuracy, greatly simplifies calculations and facilitates running changes to accommodate multiple standards or customization without any board changes.

To improve noise immunity, put the resistive divider to the UV and OV pins close to the chip and keep traces to RTN and V_{EE} short. A 0.1µF capacitor from UVH or UVL (and OV through resistor R2 as in Figure 17) to V_{EE} helps reject supply noise.

FET Short Fault

A FET short fault will be reported if the data converter measures a current sense voltage between ADC^+ and ADC^- greater than 255µV while the MOSFETs are turned off. This condition sets the FET_SHORT_STATUS bit in FAULT_STATUS register 0x03 and the FET_SHORT_FAULT bit in FAULT register 0x04.

Power Failed Fault

The LTC4284 continuously monitors the output voltage for the load. The differential voltage between RTNS and DRNS represents the attenuated output voltage for the load. An output low status will be reported if RTNS – DRNS is lower than the external reference voltage at VOUTTH. This condition sets the VOUT_LOW status bit in FAULT_STATUS register 0x03. If this condition occurs after the internal power good signal is latched, the POWER_FAILED fault bit in FAULT register 0x04 will also be set. This fault does not turn off the MOSFETs. After RTNS – DRNS rises above VOUTTH, the VOUT_LOW bit is cleared.

External Fault and Auto-Retry

PGIO4 can be configured as EXT_FAULT# or EXT_FAULT using PGIO_CONFIG_1 register 0x10 bits [7:6] to monitor an external fault condition. If the input polarity is configured as EXT_FAULT#, an external fault occurs when PGIO4 falls below its 1.28V threshold. This condition sets the EXT_FAULT_STATUS bit in FAULT_STATUS register 0x03 and the EXT_FAULT bit in FAULT register 0x04. This condition also turns off the MOSFETs if the EXTFLT_TURN_OFF bit in CONFIG_3 register 0x0F has been set. When PGIO4 subsequently rises above 1.28V, the EXT_FAULT_STATUS bit is cleared. After an auto-retry delay, the MOSFETs will be allowed to turn on again unless the external fault auto-retry has been disabled by clearing the EXT_FAULT_RETRY bit in CONTROL_2 register 0x0B. The auto-retry delay for the external fault is configurable from 512ms to 65.5s in binary scale using the COOLING_DL bits in CONFIG_2 register 0x0E. During the delay the DELAY_STATUS bit in REBOOT register 0xA2 is set to 1. It will be cleared when the delay expires.

In Figure 18, PGIO4 is configured as EXT_FAULT and used to monitor MOSFET temperature. When the MOSFET temperature rises above 115°C, the EXT_FAULT bit in FAULT register 0x04 is set and the MOSFET is turned off.

If the EXTFLT_TURN_OFF bit in CONFIG_3 register 0x0F has been cleared, an external fault condition at PGIO4 will not turn off the MOSFETs. Regardless of the value of the EXTFLT_TURN_OFF bit, if the EXT_FAULT_ALERT bit in FAULT_ALERT register 0x15 is set, the high state of the EXT_FAULT bit in FAULT register 0x04 will generate an alert by pulling ALERT# low.

PGIO1-4 and ADIO1-4, when configured as general purpose inputs, can be used to monitor external conditions without turning the MOSFETs off or generating alerts. If any of these pins is pulled above the 1.28V threshold, the associated input status bit in INPUT_STATUS register 0x02 is set.

Cooling Delay

The cooling delay (configurable by the COOLING_DL bits, 0x0E [3:1]) after an overcurrent fault, FET bad or external fault, will not be interrupted by any other fault. If, before expiration of the cooling delay, another overcurrent, FET bad or external fault occurs, the cooling delay will restart and extend the total cooling time. During the cooling delay the DELAY_STATUS bit 0xA2 [1] is set to indicate the delay timer is running. This bit resets when the delay expires. The cooling delay can be terminated by initiating an I^2C reboot command, and is also terminated by UVLO ($INTV_{CC}$ < 3.8V).

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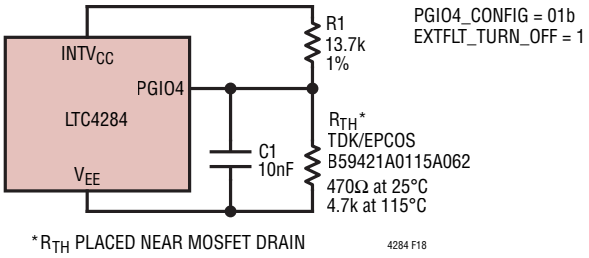

Figure 18. Use PGIO4/EXT_FAULT to Turn Off MOSFET when Drain Temperature Exceeds 115°C

Resetting Faults

Faults are reset with any of the following conditions. First, writing zeros to FAULT register 0x04 will clear the associated fault bits. Second, the entire FAULT register is cleared when the ON bit in CONTROL_1 register 0x0A goes from high to low, or if $INTV_{CC}$ falls below its 3.8V undervoltage lockout. EN# falling from high to low also clears the entire FAULT register. Finally, when UVL is pulled below its 1.024V reset threshold, all fault bits in the FAULT register are cleared. When UVL is brought back above 1.024V but below 1.833V, the UV_FAULT bit is set if UVH is below 2.048V. This can be avoided by holding UVH above 2.048V while toggling UVL to reset faults.

Fault bits with associated fault conditions that are still present (as indicated in FAULT_STATUS register 0x03) cannot be cleared. The FAULT register will not be cleared when auto-retrying. When auto-retry of a specific GATE turn-off fault is disabled using CONTROL_2 register 0x0B, the existence of the associated fault bit keeps the MOSFET off. After the fault bit is cleared and the associated retry delay expires, the MOSFETs are allowed to turn on again. If auto-retry of a fault is enabled, then a high state of the associated fault status bit in 0x03 will hold the MOSFETs off and the FAULT register is ignored. Subsequently, when the condition causing the fault is cleared (and so is the fault status bit in 0x03), the MOSFETs are allowed to turn on again.

Alarms

Besides the fault bits and the EN#_CHANGED bit, the LTC4284 also logs ADC alarms in ADC_ALARM_LOG registers 0x05-0x09 when ADC results are higher than the pre-configured MAX thresholds or lower than the pre-configured MIN thresholds. In addition, when the tick counter or energy meter overflows, the TICK_OVERFLOW bit or METER_OVERFLOW bit is logged into METER_CONTROL register 0x84. Finally, when EEPROM is written through I^2C, the EEPROM_WRITTEN bit is logged into ADC_ALARM_LOG register 0x05. Similar to the fault bits, these alarm bits indicate the history of corresponding conditions and do not reflect the present status of the conditions. Any alarm bit can only be reset by two methods: writing a zero to the alarm bit using I^2C or bringing $INTV_{CC}$ below its undervoltage lockout voltage.

EN# Pin

EN# has a 1.28V logic threshold relative to V_{EE} with a maximum leakage current of 1µA at 3V. It must be pulled low and remain low during the 128ms debounce delay. When the delay expires, the MOSFETs are allowed to turn-on. An internal clamp limits EN# to a minimum of 6V. The pin can be safely connected to higher voltages through a resistor that limits the current up to 5mA. It can be used to monitor board present as shown in Figure 2.

The EN# bit in SYSTEM_STATUS register 0x00 indicates the present state of EN#, and the EN#_CHANGED bit in ADC_ALARM_LOG_1 register 0x05 is set high whenever EN# changes state. The EN#_CHANGED bit can be cleared using the same methods as those for resetting faults (see Resetting Faults) except pulling EN# from high to low. Pulling EN# from high to low sets the EN#_CHANGED bit while clearing the entire FAULT register 0x04.

ON Bit

The ON bit in CONTROL_1 register 0x0A allows one to turn on (ON bit = 1) and turn off (ON bit = 0) the MOSFETs through the I^2C interface. There is no debounce delay associated with this bit, so the MOSFETs are immediately turned on after the bit is flipped from 0 to 1 while all other turn-on conditions are met.

When the ON bit is changed from 1 to 0, the MOSFETs are turned off and all bits in FAULT register 0x04 plus the EN#_CHANGED bit in ADC_ALARM_LOG_1 register 0x05 are cleared.

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Turning the LTC4284 On and Off

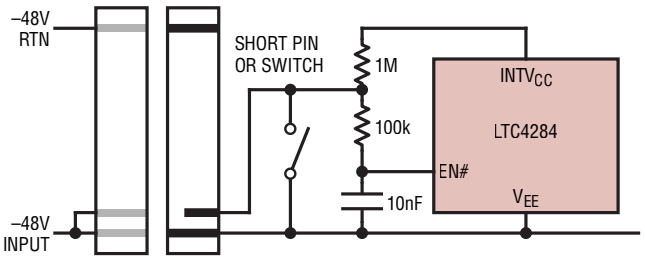
Many methods of on/off control are possible using the EN#, UV/OV, PGIO3 or PGIO4 pins along with the I²C port. EN# works well with logic inputs or floating switch contacts; I²C control is intended for systems where the board operates only under command of a central control processor and UV (UVH, UVL) and OV are useful with signals reference to RTN, as are PGIO3 and PGIO4 when configured as power good input and external fault, respectively.

On/off control is possible with or without I²C intervention. Further, the LTC4284 may reside on either the removable board or on the backplane. Even when operating autonomously, the I²C port can still exercise control over the GATE outputs. UV, OV and other fault conditions seize control as needed to turn off the GATE outputs, regardless of the state of EN# or the I²C port. Figure 19 shows three configurations of on/off control of the LTC4284. Note that the on/off control of GATE2 not only is commanded by the on/off state of GATE1, but also depends on the specific conditions in each operation mode as shown in Table 1.

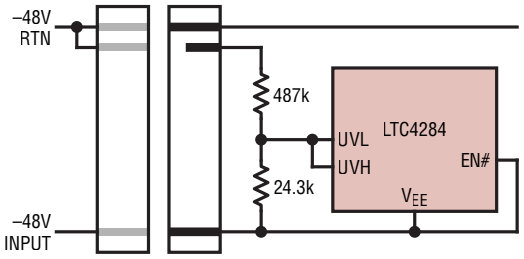
Ejector Switch or Backplane Connection Sense with Insertion Debounce Delay. A high state of EN# turns the GATE outputs off. A low state of EN# turns the GATE outputs on with a debounce delay of 128ms. Figure 19a shows an ejector switch or backplane connection driving EN# as an on/off control with extra insertion debounce delay through the RC constant. This circuit works in both backplane and board resident applications.

Short Pin to RTN. Figure 19b uses the UV divider string to detect board insertion. This method achieves an insertion debounce delay of 128ms and works equally well in both backplane and board resident applications.

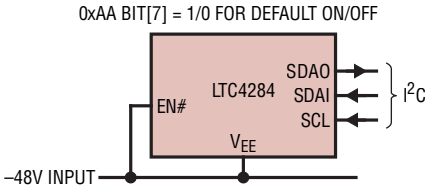
I²C Only Control. The circuit in Figure 19c locks out EN# and controls the GATE outputs with the ON bit in CONTROL_1 register 0x0A. To default on or off at power-up, program the corresponding EEPROM bit (bit[7] in EE_CONTROL_1 register 0xAA) to 1 or 0, respectively. Any of the PGIO1–PGIO4 or ADIO1–ADIO4 pins, when configured as general purpose input, can be used to monitor a connection sense or other control signal. When the ON bit in CONTROL_1 register 0x0A changes from 0 to 1, the LTC4284 turns on the GATE outputs without a delay.



a) Contact Debounce Delay upon Insertion for Use with an Ejector Switch or Backplane Connection Sense



b) Short Pin Connection Sense to RTN



c) I²C Only Control

Figure 19. On/Off Control of the LTC4284

The I²C port can also be used to write a fault bit in FAULT register 0x04 to turn off the GATE outputs if the corresponding fault has been configured to latch off the GATE output using CONTROL_2 register 0x0B. To turn the GATE outputs back on afterwards, clear the fault bit. The GATE outputs will be turned on after an auto-retry delay (except for OV). If a fault has been configured to auto-retry (in either finite or infinite times), setting the corresponding fault bit through I²C will not turn off the GATE outputs.

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Configuring PGIO and ADIO Pins

The LTC4284 has four PGIO pins and four ADIO pins, all of which can be configured as general purpose inputs/outputs using PGIO_CONFIG_1 register 0x10 and ADIO_CONFIG register 0x12. Additionally, PGIO1 and PGIO2 can be configured as two sequential inverted or non-inverted power good signals, PGIO3 can be configured as inverted or non-inverted power good input signal (see Power Good Monitors and PGI Fault), and PGIO4 can be configured as inverted or non-inverted external fault (see External Fault and Auto-Retry). When configured as general purpose outputs, the output data for PGIO1–PGIO4 and ADIO1–ADIO4 are stored in bits[7:4] in PGIO_CONFIG_2 register 0x11 and bits[3:0] in ADC_CONFIG register 0x12, respectively. When selected, ADIO1–ADIO4 are also monitored by the on-board ADC (see Data Converters).

If the PGIO2_ACLB bit in CONTROL_1 register 0x0A is set, PGIO2 is configured as an inverted indicator of active current limit after startup. During startup PGIO2 is held low. After the internal power good signal is latched, if the OC_STATUS bit in FAULT_STATUS register 0x03 is 0, PGIO2 goes high impedance. If the OC_STATUS bit is set to indicate that active current limit is engaged, PGIO2 is pulled low.

Regardless of the configurations, PGIO1–PGIO4 and ADIO1–ADIO4 all have comparators monitoring the voltage on these pins with a threshold of 1.28V. The results are stored in INPUT_STATUS register 0x02.

Design Examples

The design flow starts with specifying the maximum load power and the operating voltage limits (line or battery operated). A line operated system usually has a tightly regulated supply voltage. A battery operated system usually has wide supply range and can experience large input steps when replacing a dropping-out battery with a newly charged one. An operation mode is then selected based on the following guideline.

Single Driver Mode (Mode 1): <800W, line or battery operated.

Parallel Mode (Mode 2): up to 1500W, line or battery operated.

High Stress Staged Start Mode (Mode 3): >1500W, battery operated.

Low Stress Staged Start Mode (Mode 4): >1500W, line operated.

This is a rough guide and the boundaries between different modes may shift up or down depending upon the allowed budget of the MOSFETs.

Example 1: Design Procedure of Parallel Mode with SOA Timer and Current Limit Startup

Consider a battery operated system with maximum load power of 1200W, a supply voltage range of –36V to –72V (–36V to –72V input step is allowed), and a load capacitance of C_L = 1000µF as shown in Figure 2. The parallel mode is chosen based on the above guideline. In the parallel mode, GATE1 and GATE2 drive two parallel channels of MOSFETs to charge the load capacitor simultaneously at startup, share the load current after startup, and turn off simultaneously upon a fault condition such as output overload or short-circuit.

The maximum load current is calculated as

$$I_{L(MAX)} = \frac{P_{L(MAX)}}{V_{S(MIN)}} = \frac{1200W}{36V} = 33.3A$$

Step 1. Configure current limit and select current sense resistors. Since a –36V to –72V input step is a valid operating condition, the current limit should be twice the maximum load current to minimize the temperature rise in the MOSFETs following a large input step:

$$I_{LIM(OPT)} = 2 \cdot I_{L(MAX)} = 66.7A$$

With a constant power load, when the load voltage ramps from 36V to 72V following the input step, the load current is halved. The LPFB (load power foldback) bit in CONFIG_1 register 0x0D is set to 1 so that the current limit will be maintained at approximately twice the load current during the output ramp.

In parallel mode, the two channels share the current equally, so the maximum current each channel carries is

$$I_{CH(MAX)} = \frac{I_{LIM}}{2} = 33.3A$$

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Sense resistors for each channel are selected assuming they will carry the maximum channel current, or 33.3A in this example. Selection is a matter of total cost, sense voltage (configurable from 15mV to 30mV in 1mV steps), allowable dissipation, availability of discrete resistance values, using multiple devices to reduce the sensing errors associated with high current density at the interface between the PCB and resistor, and using multiple devices to ballast current flow across a wide path, between 2 or more connectors, or between 2 or more MOSFETs. These factors are iterated until an acceptable solution is found. First, determine the number of resistors needed to handle the total sense power of each channel. Compute the total sense power starting with the minimum sense voltage or 15mV:

$$P_{S(CH)} = \Delta V_{SENSE(MIN)} \bullet I_{CH(MAX)} = 15mV \bullet 33.3A = 500mW$$

Second, compute the number of resistors needed to handle this power. For example, 1206 resistors are rated for 250mW dissipation. A conservative design is half as much, or 125mW.

$$N_{RS(CH)} = \frac{P_{S(CH)}}{125mW} = \frac{500mW}{125mW} = 4$$

Thus at least four parallel 1206 resistors are needed for each channel. Third, compute the resistance value:

$$R_{S(CH)} = \frac{V_{ILIM(MIN)}}{I_{CH(MAX)}} = \frac{15mV}{33.3A} = 450\mu\Omega$$

Four resistors of 1.8mΩ each would give the correct sense resistance. Fourth, use the closest next-larger available sense resistor value and adjust the sense voltage as needed to restore the current. In this case, a 2mΩ sense resistor value is selected and the sense voltage is adjusted to 16mV. Recompute the numbers:

$$R_{S(CH)} = \frac{2m\Omega}{4} = 500\mu\Omega$$

$$I_{CH(MAX)} = \frac{16mV}{500\mu\Omega} = 32A$$

$$P_{S(CH)} = 16mV \bullet 32A = 512mW$$

The power dissipation of each resistor package is now 512mW/4 = 128mW. The total current limit is now 32A • 2 = 64A, close enough to the optimum value of 66.7A. The above process might be iterated for several combinations of different resistor counts, different package sizes, and even combinations of mixed resistor values.

When a specific design is actually built, there can be small inaccuracies in the current sensing owing to contact and copper trace resistances. An immediate remedy without changing sense resistors is to readjust the sense voltage in 1mV steps. For instance, moving sense voltage from 16mV to 17mV gives a 6.25% increase in current.

Step 2. Select resistive dividers for DRNS (drain sense), RTNS (RTN sense) and VOUTTH (output low threshold). DRNS and RTNS serve multiple purposes. First, they are the inputs to a differential amplifier that measures the attenuated load voltage for dV/dt control at startup (see Inrush Control). In the event of an output overload or short-circuit, the current limit foldback profile in normal operation depends upon the differential input between RTNS and DRNS that represents the output voltage across the load. The current limit starts to fold back when RTNS – DRNS drops below 0.9V and reaches the minimum when RTNS – DRNS drops to zero (see Current Limit Foldback). Additionally, in current limit the DRNS input monitors the MOSFET's V_{DS} and uses this information to scale the TMR pull-up current accordingly. When not in current limit, DRNS monitors V_{DS} and serves as one input to a multiplier which generates the TMR pull-up current. Finally, RTNS and DRNS also serve as inputs to the ADCs so that the input voltage and MOSFET drain voltage can be read remotely. RTNS and DRNS have a maximum useable input voltage of 2.8V, so resistive dividers are required.

To select resistive dividers for RTNS and DRNS, compute the divider ratio r using the maximum supply voltage:

$$r = \frac{V_{S(MAX)}}{1.8V} = \frac{72V}{1.8V} = 40$$

where 1.8V is the operating point of DRNS at which the TMR pull-up current is tested and specified. The resulting

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ADC measurement full scale for input (at RTNS) and MOSFET drain (at DRNS) voltages is

$$V_{FS(MEAS)} = r \bullet 2.048V = 40 \bullet 2.048V = 81.92V$$

which gives a LSB size of 20mV in 12-bit mode. If it was desired to measure gross overvoltage inputs, such as 100V, then a decision would have to be made to sacrifice control dynamic range in favor of ADC measurement range by using a higher divider ratio. An alternative approach is to use ADIN1–ADIN4 inputs for ADC measurements, leaving RTNS and DRNS for control purpose only.

With 72V load voltage corresponding to RTNS – DRNS = 1.8V, in normal operation the current limit starts to fold back when load voltage drops below 36V (or RTNS – DRNS < 0.9V) in overload conditions. This means there is no foldback in normal operating input range between –36V and –72V, allowing the MOSFETs to pass the full load current.

Standard values of 200k and 5.11k give a divider ratio of 40.1. DRNS and RTNS must use identical dividers. While the exact ratio is not important, matching between them is very important. For this reason, 1% resistor tolerance is the minimum requirement; 0.25% or 0.1% is better.

VOUTTH pin sets the threshold of RTNS – DRNS that indicates the low limit of the output voltage to reset power good signals if the PWRGD_RESET_CNTRL bit in CONTROL_1 register 0x0A is set to 1. The low limit is set below the minimum input voltage, so 32V is selected in this example. With a divider ratio of 40 on DRNS and RTNS, the VOUTTH threshold is 32V/40 = 0.8V. This voltage may be realized with a resistive divider between $INTV_{CC}$ (5V) and V_{EE}, or for a better tolerance, between VREF (1.024V) and V_{EE}. For the latter case, a divider of 5.62k and 20k as shown in Figure 2a results in 0.8V at VOUTTH. The source current of VREF is 40µA, well within its specified limit of 200µA.

Step 3. Design the overcurrent timer behavior. The TMR pin can be configured into a SOA timer or a single capacitor circuit breaker timer. The SOA timer requires an RC network representing the MOSFET thermal model to be connected to TMR (see SOA Timer). At least two resistors and two capacitors are needed for minimum accuracy of the thermal behavior. More RC elements are desired for better accuracy. Thus the cost and board area are larger than the single-capacitor timer. The benefit of the SOA timer is that the TMR voltage represents the temperature rise of the MOSFET and its trip threshold represents the maximum allowable peak temperature of the MOSFET. With the SOA timer, selection of MOSFETs is much simpler: they just need to meet the worst-case operation requirements. In fault conditions such as output short, the SOA timer automatically protects the MOSFETs by turning them off once the maximum allowable peak temperature is reached (TMR tripped). With the single capacitor timer, the minimum capacitor must first be selected to keep the MOSFETs on during worst-case operating conditions, then the MOSFETs must be selected to withstand the worst-case SOA conditions during normal operating and fault conditions. The cost of MOSFETs selected based on the single capacitor timer for parallel mode or high stress staged start mode may be substantially higher than that using the SOA timer. It is recommended to use the SOA timer for high power applications using parallel mode or high stress staged start mode, especially for those with large input steps. Therefore, in this example the TMR pin is configured as an SOA timer by setting the THERM_TMR bit in CONTROL_1 register 0x0A to 1, which disables the internal TMR pull-down current.

With the SOA timer protecting the MOSFETs, current limit foldback may be disabled after startup. This can be done by setting the FB_DIS bit in CONTROL_1 register 0x0A to 1. The foldback during startup is not affected by the FB_DIS bit.

Step 4. Select the MOSFETs. With the SOA timer, two operating requirements must be met: (1) the $R_{DS(ON)}$ must be low enough to carry maximum load current; (2) the SOA must be sufficient to stand the worst-case operating condition. The selection for the $R_{DS(ON)}$ requirement is a combination of total MOSFET cost and maximum desired dissipation per package. For the maximum channel current of 32A, two 5mΩ devices result in 1.28W per device. With air flow 1.28W dissipation is acceptable and a third device is unnecessary. The chosen MOSFETs are two PSMN4R8-100BSE devices (each $R_{DS(ON)}$ < 4.8mΩ) for each channel. The components selected so far are shown in Figure 1 and Figure 2a.

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The worst-case MOSFET drain voltage with full load is

$$V_{D(ON),MAX} = \frac{I_{CH(MAX)} \bullet R_{DS(ON),MAX}}{2} = \frac{32A \bullet 4.8m\Omega}{2} = 76.8mV$$

The DRAIN threshold $V_{D,FET(TH)}$ must be set higher than this number with sufficient margin to account for component inaccuracies and temperature coefficient. When the MOSFET drain voltage is higher than this threshold, two things will happen. First, the FET_BAD_STATUS bit in FAULT_STATUS register 0x03 will be set and the FET bad timer will be started. When the timer expires the FET_BAD_FAULT bit in FAULT register 0x04 will be set and the MOSFETs will be turned off if the FET_BAD_TURN_OFF bit in CONTROL_1 register 0x0A has been set. Second, the TMR pull-up current will be enabled even if current limit is not engaged. This current is produced by an internal multiplier monitoring the power dissipation in channel 1. $V_{D,FET(TH)}$ has four discrete settings: 72mV, 102mV, 143mV and 203mV. In this example 143mV is selected by setting the VDTH bits in CONFIG_2 register 0x0E to 10b.

A large input step is usually the worst-case operating condition for SOA. To verify the temperature rise of the MOSFET, it is necessary to run simulations in this condition. With the above selected components and configurations, the temperature rise of the MOSFET when riding through a –36V to –72V input step with full load (1200W and 1000µF) is 46°C (simulated with the LTspice SOAtherm model). At worst-case operating temperature of 85°C, this translates to 131°C in the MOSFET, which has substantial margin from the manufacturer specified maximum temperature of 175°C. With a load capacitance of 2000µF, the temperature rise during the –36V to –72V input step increases to 64°C, still an acceptable figure.

Step 5. Design the startup current and FET bad timer. First the startup mode is selected. As pointed out in Inrush Control, the startup current (or inrush current) can be controlled either by a RAMP capacitor in dV/dt mode or by startup foldback in current limit mode. The current limit mode is selected in this example based on two considerations. First, in the parallel mode, both channels charge the load capacitance during startup. Current limit will equalize the charging currents between the two channels. In the dV/dt mode, the charging current may concentrate on one channel due to MOSFET threshold mismatch. Second, the current limit mode is a better choice to work with the SOA timer that has been selected in Step 3. This is because if the dV/dt mode was selected, the TMR pull-up current would be disabled in normal startup conditions and the SOA timer would not be able to track the temperature rise of the MOSFET during startup.

Choice of the charging current is a trade-off between maximum charging time, maximum inrush current drawn from the backplane, and more importantly, peak power dissipated in the MOSFETs. When charging a capacitor from a voltage source, the charging process dissipates an energy in the pass MOSFET equal to the energy stored in the capacitor. The maximum input voltage results in the maximum energy:

$$E_{MAX} = \frac{C_L \bullet V_{S(MAX)}^2}{2} = \frac{1000\mu F \bullet (72V)^2}{2} = 2.59J$$

This indirectly sets a limit on how quickly the load capacitor can be charged, since the average power dissipation in the MOSFETs is energy/time. In general, the faster the charge rate, the higher the peak temperature. For this reason, it is a good idea to lower the inrush current to no more than necessary to achieve the required startup time. Therefore, the smallest foldback ratio, 10%, is selected by setting the FB bits in CONFIG_1 register 0x0D to 11b, and the startup inrush current is

$$I_{INRUSH} = I_{LIM} \bullet \alpha_{FB} = 64A \bullet 10\% = 6.4A$$

The maximum startup charging time of the load capacitor is then computed:

$$t_{STARTUP(MAX)} = \frac{C_L \bullet V_{S(MAX)}}{I_{INRUSH}} = \frac{1000\mu F \bullet 72V}{6.4A} = 11.25ms$$

This charging time is short enough for most applications. Simulation shows the temperature rise of the MOSFET in this worst-case startup condition is 40°C, lower than that for the –36V to –72V input step calculated in Step 4.

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During startup the FET_BAD_STATUS bit is high and the FET bad timer is running and serves as a watchdog over the controlled startup. The load capacitor must be fully charged before this timer expires, or the GATE outputs will be turned off if the FET_BAD_TURN_OFF bit in CONTROL_1 register 0x0A has been set. There is no concern with this example since the maximum charging time of 11.25ms is much shorter than the minimum FET bad timer delay (256ms).

Step 6. Select the RC network for the SOA timer following the procedure as shown in the SOA Timer section. It was found that two thermal capacitors and two thermal resistors provide fairly good curve fitting for the thermal impedance plot of the chosen MOSFET, PSMN4R8-100BSE in the range between 100µs and 100ms (wide enough for typical operating conditions of this application): $C_{\theta 1}$ = 0.002J/°C, $R_{\theta 1}$ = 0.05°C/W, $C_{\theta 2}$ = 0.03J/°C, $R_{\theta 2}$ = 0.35°C/W. The conversion constant is given by

$$k = \frac{V_{DS,MAX} \bullet I_{D,MAX}}{I_{TMR(UP),MAX}} \bullet \frac{V_{TMR(TH)}}{\Delta T_{MAX}} =$$

$$\frac{72V \bullet 32A}{202\mu A} \bullet \frac{2.048V}{65^{\circ}C} = 3.6 \bullet 10^5 \left[\frac{V^2}{^{\circ}C}\right]$$

where ΔT_{MAX} is the maximum allowable temperature rise and chosen to be 65°C, which corresponds to a maximum MOSFET temperature of 150°C at an operating temperature of 85°C, with 25°C margin from the manufacturer specified maximum temperature of 175°C. The thermal R and C values are then converted to electric R and C values as shown in SOA Timer. After the electrical R and C values are computed, choose the closest next-larger available resistor value and the closest next-smaller available capacitor value. Then the resistance corresponding to the thermal resistance of the board is added to the termination resistance (the largest one). If the computed resistance for the board thermal resistance is over 1MΩ, choose 1MΩ. Assuming a 5°C/W board thermal resistance in this application, it is converted to 5 • 3.6 • 10^5 = 1.8MΩ. So 1MΩ is selected. This avoids accuracy degradation due to board leakage currents. The resulting electrical capacitors and resistors are C_{E1} = 4.7nF, R_{E1} = 18.2k, C_{E2} = 68nF, R_{E2} = 1.13MΩ, as shown in Figure 1 and Figure 2a.

After the SOA timer is configured, rerun simulations to ensure TMR does not reach its 2.048V trip point in all operating conditions including startup and input step. When it trips in fault conditions such as output overload or short-circuit, verify the peak temperature of the MOSFET matches the proposed maximum temperature. Iterations of the above procedure may be needed before the RC network is finalized.

Step 7. Select resistive dividers for UV/OV inputs and ADC averaging resistors

Select resistive dividers so that UV rising threshold is set just below the minimum input voltage and OV falling threshold is set just above the maximum input voltage. A single, 4-resistor divider as shown in Figure 2a gives UV shutdown at 32.4V, UV release at 35.3V, OV shutdown at 74.5V and OV release at 73.2V. This configured range is just wide enough to cover the full input voltage range between 36V to 72V. A 100nF bypass capacitor is selected to filter out noises at UVL/UVH and OV.

Four 1Ω averaging resistors are chosen for the ADC^+ and ADC^- inputs to measure the average current between the two channels. The current ADC has a full scale of 32.768mV. The total sense resistance is 0.25mΩ, giving a full-scale current of 131.1A, with a 32mA LSB size in 12-bit mode.

Example 2: Design Procedure of Low Stress Staged Start Mode with Single Capacitor on TMR Pin and dV/dt Startup

The second example is a line operated –52V system with supply tolerance of 10% (–46.8V to –57.2V) and maximum load power of 2500W as shown in Figure 13. The load capacitance is specified as C_L = 2000µF. The low stress staged start mode is chosen for this example since the power exceeds 1500W and the supply is line regulated, without the concern about a large input step. The low pass staged start mode features a small startup MOSFET, driven by GATE1 (channel 1) and designed to carry a low startup inrush current to charge the load capacitor. After successful startup, low resistance bypass MOSFETs are driven by GATE2 (channel 2) to supply the load current. The current in channel 1 is usually only a small fraction of

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the maximum load current, such as 10% or less. For this reason, its current contribution during normal operation can be ignored for the first phase of the design. Later channel 1 can be accounted for or sized to make up for any shortfall in the high current (channel 2) path, so that full power (2500W) can be supplied at minimum input voltage (46.8V).

The maximum load current is calculated as

$$I_{L(MAX)} = \frac{P_{L(MAX)}}{V_{S(MIN)}} = \frac{2500W}{46.8V} = 53.4A$$

Step 1. Select sufficient bypass MOSFETs to carry the maximum load current. The decision is a combination of total MOSFET cost and maximum desired dissipation per package. For the maximum channel current of 53.4A, two IPT020N10N3 ($R_{DS(ON)} < 2m\Omega$) devices result in 1.415W per package, an acceptable dissipation with air flow. As an option, the IPT015N10N5 ($R_{DS(ON)} < 1.5m\Omega$ could be used, dissipating just 1.06W per package, at a slightly higher cost.

With full load the worst-case drain voltage of the MOSFET is 53.4A • 1mΩ = 53.4mV. Select 102mV as the DRAIN threshold for starting FET bad timer and enabling TMR pull-up current, with sufficient margin to account for inaccuracies. Set the VDTH bits in CONFIG_2 register 0x0E to 01b for this configuration. See detailed design considerations in Example 1, Step 4.

Step 2. Configure current limit and select current sense resistors. Since the input voltage is well regulated, there is no need to set the current limit to twice the load current to minimize temperature rise upon a large input step as in Example 1. The current limit in this example just needs to cover the maximum load current, with enough margin to account for device tolerances. Select sense resistors for channel 2 (bypass channel) first assuming it carries the maximum load current, then add a small current carried by the startup channel for the margin. Compute the sense power of channel 2 starting with the minimum sense voltage or 15mV:

$$P_{S2} = V_{ILIM(MIN)} \bullet I_{L(MAX)} = 15mV \bullet 53.4A = 801mW$$

With 250mW rated 1206 resistors, use 125mW for conservative design and the minimum number of sense resistors to handle the power is

$$N_{RS2} = \frac{P_{S2}}{125mW} = \frac{801mW}{125mW} = 6.4$$

Thus at least 6 parallel 1206 resistors are needed for channel 2. The resistance of channel 2 is

$$R_{S2} = \frac{V_{ILIM(MIN)}}{I_{L(MAX)}} = \frac{15mV}{53.4A} = 281\mu\Omega$$

Six resistors of 1.69mΩ each would give the correct sense resistance. The closest next-larger available sense resistor value is 2mΩ:

$$R_{S2} = \frac{2m\Omega}{6} = 333\mu\Omega$$

Adjust the sense voltage to 18mV to restore the current:

$$I_{LIM2} = \frac{V_{ILIM}}{R_{S2}} = \frac{18mV}{333\mu\Omega} = 54A$$

and recompute the sense power:

$$P_{S2} = 18mV \bullet 54A = 972mW$$

The power dissipation of each resistor package is now 972mW/6 = 162mW, still an acceptable value for 1206 resistors. As a last step, a 5mΩ sense resistor is chosen for a channel 1 current of

$$I_{LIM1} = \frac{V_{ILIM}}{R_{S1}} = \frac{18mV}{5m\Omega} = 3.6A$$

so that the total current limit is

$$I_{LIM} = I_{LIM1} + I_{LIM2} = 54A + 3.6A = 57.6A$$

Taking all tolerances into account, this provides sufficient margin for the maximum load current of 53.4A. Sense voltage may need to be readjusted to account for current sensing inaccuracies such as contact and copper trace resistances, as explained in Example 1, Step 1.

Step 3. Select resistive dividers for DRNS (drain sense), RTNS (RTN sense) and VOUTTH (output low reference).

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See Example 1, Step 2 for detailed design considerations. First compute the divider ratio r for RTNS and DRNS:

$$r = \frac{V_{S(MAX)}}{1.8V} = \frac{57.2V}{1.8V} = 31.78$$

which is rounded to 32. Standard values of 316kΩ and 10.2kΩ give a divider ratio of 31.98. The ADC measurement full-scale for input (at RTNS) and MOSFET drain (at DRNS) voltages is

$$V_{FS(MEAS)} = r \bullet 2.048V = 32 \bullet 2.048V = 65.5V$$

which gives a LSB size of 16mV in 12-bit mode.

With V_{LOAD} = 32 • 1.8V = 57.6V corresponding to RTNS – DRNS = 1.8V, the current limit starts to fold back when V_{LOAD} drops below 28.8V in overload conditions. There is no foldback at normal input between –46.8V and –57.2V, allowing the MOSFETs to pass the full load current.

If 44V is chosen as the output voltage threshold to reset power good signals, with a divider ratio of 32 on DRNS and RTNS, the VOUTTH threshold is 44V/32 = 1.375V. This voltage can be obtained with a resistive divider between $INTV_{CC}$ (5V) and V_{EE}. The divider ratio is 5V/1.375V = 3.64. A divider of 26.7k and 10.2k as shown Figure 13 gives a close enough ratio of 3.62.

Step 4. Design the TMR behavior. See Example 1, Step 3 for general design considerations. Since the inrush current in the low stress staged start mode is at such a low level that the temperature rise of the startup MOSFET is insignificant, there is no need to use an SOA timer for MOSFET protection during startup. After startup there is no concern about a large input step, thus a very short timer delay is needed for MOSFET turn-off upon a fault such as output short-circuit. Therefore, in the low stress staged start mode the TMR function is essentially a filtered circuit breaker and a single timer capacitor on TMR works just fine for this purpose.

Channel 2 dictates the timer capacitor selection since it carries most of the load current. All of the channel 2 current could be concentrated into a single MOSFET. The current limit of channel 2 is 54A in this example, and the MOSFET chosen in Step 1 (IPT020N10N3) can handle 60V and 60A for 100µs. It has been found that 20µs of circuit breaker filtering is sufficient to reject noise encountered in most systems, so the chosen MOSFET is up to the task. The TMR pull-up current is 202µA at maximum overload, with a voltage threshold of 2.048V. Compute the timer capacitance, C_t, for 20µs filter delay:

$$C_t = \frac{I_{TMR(UP),MAX} \bullet t_{FILTER}}{V_{TMR(TH)}} = \frac{202\mu A \bullet 20\mu s}{2.048V} = 2nF$$

Select the closest next-larger available capacitance: C_t = 2.2nF. With single capacitor on TMR, the THERM_TMR bit in CONTROL_1 register 0x0A must be cleared to enable the internal 2µA pull down current. Additionally, the FB_DIS bit in CONTROL_1 register 0x0A should be cleared to keep foldback enabled after startup to protect MOSFETs from damage upon a low impedance short-circuit.

Step 5. Design the startup channel (channel 1) and FET bad timer. At startup in low stress staged start mode, channel 1 charges the load capacitance with a small trickle current. This is a good case to use the dV/dt startup mode (see discussions in Example 1, Step 5). The design procedure involves selecting a RAMP capacitor to set the dV/dt rate for desired charging current, selecting a proper startup current limit and checking the temperature rise of the startup MOSFET under a resistive short condition.

Choice of the charging current is a trade-off between maximum charging time and peak temperature of the startup MOSFET. As discussed in Example 1, Step 5, the charging current should be set to a low level that is just necessary to achieve the required charging time. Suppose an upper limit of 500ms charging time is desired for a 2000µF load capacitor at the maximum input of 57.2V. The necessary charging current is

$$I_{INRUSH(MIN)} = \frac{C_L \bullet V_{S(MAX)}}{t_{STARTUP(MAX)}} = \frac{2000\mu F \bullet 57.2V}{500ms} = 229mA$$

The RAMP capacitor is selected according to

$$C_R = I_{RAMP} \bullet r \bullet \frac{C_L}{I_{INRUSH}} = 2.5\mu A \bullet 32 \bullet \frac{2000\mu F}{229mA} = 699nF$$

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An acceptable value is 470nF, resulting in a nominal inrush of

$$I_{INRUSH} = I_{RAMP} \bullet r \bullet \frac{C_L}{C_R} = 2.5\mu A \bullet 32 \bullet \frac{2000\mu F}{470nF} = 340mA$$

and a maximum startup time of

$$t_{STARTUP(MAX)} = \frac{C_L \bullet V_{S(MAX)}}{I_{INRUSH}} = \frac{2000\mu F \bullet 57.2V}{340mA} = 336ms$$

which is well below the upper limit of 500ms.

The FET bad timer must be set longer than the startup time for the load capacitor to be fully charged, so it is configured to 512ms by setting the FTBD_DL bits in CONFIG_2 register 0x0E to 01b.

The startup current limit should also be configured to a low level to minimize the temperature rise of the startup MOSFET under a resistive short condition, but must be higher than the dV/dt inrush current to avoid current limit being triggered in normal startup conditions. With a foldback ratio of 20%, the startup current limit of channel 1 is

$$I_{LIM1(STARTUP)} = 3.6A \bullet 20\% = 720mA$$

which is more than twice of the inrush current of 340mA, with substantial margin to account for all inaccuracies. Select the 20% foldback ratio by setting the FB bits in CONFIG_1 register 0x0D to 10b. A 10% foldback ratio would result in 360mA current limit, too close to the inrush current.

Since the inrush current is very low, $R_{DS(ON)}$ and SOA of the startup MOSFET are not critical, and a small, low cost device may be used. PSMN7R6-100BSE, with $R_{DS(ON)} < 7.6m\Omega$, is selected as the startup MOSFET. After startup with 3.6A current limit, the worst-case power dissipation in this channel is $(3.6A)^2 \bullet 7.6m\Omega = 98.5mW$, a very low figure that has no concern.

Step 6. Run simulations to verify temperature rises in both the channel 1 and channel 2 MOSFETs under all operating and fault conditions are within the acceptable range. This is a necessary step when using a single capacitor circuit breaker timer as selected in Step 4.

First, check temperature rise in channel 1 MOSFET (M1) during startup. The conditions include normal dV/dt startup to fully charge the 2000µF load capacitor and a fault condition in which M1 charges both the load capacitor and a parallel fault resistor, both at the maximum input voltage. If temperature rise is too high in normal startup condition, the inrush current may be reduced by selecting a larger RAMP capacitor. If the inrush current must be reduced less than the value required to achieve the desired maximum charging time, a larger MOSFET has to be selected for channel 1. For the fault condition, the worst-case is found iteratively by changing the fault resistor value while monitoring the temperature rise. As a starting point, use a resistor of $V_{S(MAX)}/(4 \bullet I_{LIM1(STARTUP)})$ or $57.2/(4 \bullet 0.72) = 20\Omega$ for this example. If the temperature rise is too high, startup current limit may be reduced by selecting a steeper foldback ratio or a larger sense resistor R_{S1}. If the startup current limit must be reduced to less than or close to the dV/dt inrush required for the maximum charging time, a larger MOSFET must be selected. Using the conditions of this example, it is found the worst-case temperature rise in M1 either in normal startup condition or with different fault resistors is lower than 10°C, an insignificant figure. This verifies the selected channel 1 MOSFET, PSMN7R6-100BSE, has more than enough SOA to handle the worst-case dissipation during startup.

Second, check temperature rises in both channel 1 and channel 2 MOSFETs after startup when TMR times out under different overload conditions. The worst-case could be shorting the output to half of the available output voltage so there is no foldback while the V_{DS} of the MOSFETs is still high. If the worst-case temperature rise in any channel is too high, larger MOSFET(s) must be selected for that channel. In this example, the worst-case temperature rise in channel 2 is an acceptable value of about 56°C and that in channel 1 is insignificant (<10°C).

Step 7. Select resistive dividers for UV/OV inputs and ADC averaging resistors

Although it is possible to use a single, four-resistor (or three-resistor if UVH and UVL connected together) divider as shown in Example 1, Step 7, two independent dividers

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with 2 (OV) or 2 to 3 (UV) resistors in each divider make it easier to make non-interactive changes at a later time. The two dividers as shown in Figure 13 gives UV shutdown at 43.4V, UV release at 45.1V, OV shutdown at 59.3V and OV release at 58.3V, which covers the full input voltage range of this example. 10nF capacitors filter out noises on UVL and OV.

For ADC$^+$ and ADC$^-$ inputs, 1Ω is chosen for the averaging resistor on the R_{S2} side (R_{A2}). The averaging resistor on the R_{S1} side is determined by the ratio between R_{S1} and R_{S2}:

$$R_{A1} = R_{A2} \bullet \frac{R_{S1}}{R_{S2}} = 1\Omega \bullet \frac{5m\Omega}{0.33m\Omega} = 15\Omega$$

The current ADC has a full scale of 32.768mV. The total sense resistance is 5mΩ in parallel with six 2mΩ, or 0.312mΩ. With a full scale of 32.768mV on the ADC$^+$ – ADC$^-$ input, this gives a full-scale current of 104.9A and a LSB size of 25.6mA in 12-bit mode.

Layout Considerations

To achieve accurate current sensing, Kelvin connections are required. The minimum trace width for 1oz copper foil is 0.02" per amp to make sure the trace stays at a reasonable temperature. Using 0.03" per amp or wider is recommended. Note that 1oz copper exhibits a sheet resistance of about 530μΩ/square. Use 2oz or heavier copper for high current applications.

The V_{EE} pin of the LTC4284 should be connected to a separate plane from the main –48V input plane. To improve noise immunity, as shown in Figure 20, the V_{EE} connections of all capacitors, resistive dividers, opto-isolators and I^{2}C common must be made directly to the local V_{EE} plane, not the –48V input plane.

The mechanical stress of soldering a part to a board and the heat of an IR reflow or convection soldering oven can cause the ADC full-scale error (FSE) and the current limit voltage (V_{ILIM}) to shift. Refer to Typical Performance Characteristics for ADC FSE and V_{ILIM} shifts of 300 units of LTC4284 after three cycles of the lead-free IR reflow process.

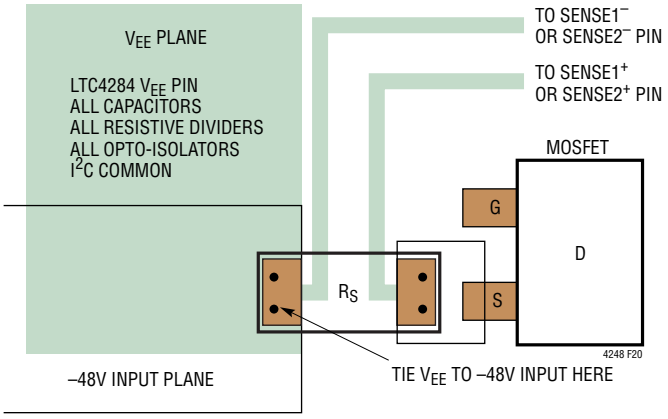

Figure 20. Layout Example of V_{EE} Plane, –48V Input Plane and Sense Resistor Connection

Reboot on I^{2}C Command

The LTC4284 features a reboot command bit, RBT_EN in REBOOT register 0xA2. Setting this bit will cause the LTC4284 to shut down and reboot after a delay. The reboot delay is programmable from 512ms to 65.5s using the three RBT_DL bits in the REBOOT register. A reboot delay allows load capacitance to fully discharge. During the reboot delay the DELAY_STATUS bit in the REBOOT register is set to 1. It will be cleared when the delay expires. The reboot will also copy the contents of the EEPROM to volatile registers in the same way as after initial power-up. On systems where the hot swap controller supplies power to the I^{2}C master, this allows the master to issue a command that power cycles the entire board, including itself. Once set, the RBT_EN bit remains 1 after reboot is completed. Clear it before issuing the next reboot command.

Data Converters

The LTC4284 incorporates a pair of Sigma-Delta A/D converters (ADCs) that are configurable from 8-bit at 1kHz conversion rate to 16-bit at 1Hz conversion rate in five settings using the ADC bits in PGIO_CONFIG_2 register 0x11 (see Table 12). In the default continuous mode, the first ADC (ADC1) continuously monitors the input current through a sense resistor between ADC$^+$ and ADC$^-$. The second ADC (ADC2) is synchronized to ADC1 and

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monitors VPWR for power multiplication plus one of the sixteen auxiliary inputs. These inputs include 10 single-ended signals and 6 differential signals and are selectable using ADC_SELECT registers 0x13-0x14 (see Table 14). If multiple auxiliary inputs are selected, ADC2 will rotate between them in the continuous mode as illustrated in Figure 21. The AUX_ADC_CH bits in ADC_STATUS register 0x01 are refreshed at the end of each conversion to indicate the auxiliary input that completed the latest measurement (see Table 5). If all bits in ADC_SELECT registers 0x13–0x14 are cleared while the ADCs are running in continuous mode, ADC1 and ADC2 continue to measure $ADC^+ – ADC^–$ and VPWR(RTNS/DRNS), respectively. The auxiliary measurements of ADC2 are disabled and the data in 0x41–0x79 from the previous measurement are preserved except 0x4A (ADIN1), which is overwritten by a small number.

The full-scale voltage of any single-ended input is 2.048V. For each differential input, one terminal must be at the same potential of V_{EE}. Normally the negative terminal is at V_{EE} and the full-scale is 32.768mV. If the positive terminal is at V_{EE}, the full scale becomes 33.301mV. When using ADIN1–ADIN4 and ADIO1–ADIO4 as differential inputs, ADIN1, ADIN3, ADIO1 and ADIO3 must be the negative terminals, and ADIN2, ADIN4, ADIO2, ADIO4 must be positive terminals, respectively. Note that for each resolution setting, the resolution of differential auxiliary inputs of ADC2 is one bit less than that of the $ADC^+ – ADC^–$ input of ADC1 or the single-ended inputs.

After each conversion of the two synchronized ADCs, the measured current sense voltage ($ADC^+ – ADC^–$) is multiplied by the measured VPWR(RTNS or DRNS) voltage to calculate input power or MOSFET power, configurable using the VPWR_SELECT bit in CONFIG_3 register 0x0F. All measured results and calculated power are stored to corresponding data registers (see Table 3). They are also compared to the minimum and maximum values that are stored in the minimum and maximum data registers. If the measurement is a new minimum or maximum value, then the corresponding minimum or maximum data registers are updated. Note that all ADC data registers from 0x41 to 0x79 have a length of two bytes or 16 bits, and the data for all resolutions are left justified.

The ADC measurements are compared to the 8-bit minimum and maximum alarm thresholds that are configured using registers 0x1B through 0x40 and will set the corresponding ADC alarm bits in ADC_ALARM_LOG registers 0x05 to 0x09. If the associated ADC alert bit in ADC_ALERT registers 0x16 to 0x1A is set, an ADC alarm bit will generate an alert by pulling ALERT# low and set the ALERT_GENERATED bit in METER_CONTROL register 0x84.

At the end of each ADC measurement, calculated power is added to an accumulator that meters energy. The 6-byte energy meter 0x7A to 0x7F is capable of accumulating 12 days of power at full scale in 12-bit ADC mode, which is several months at a nominal power level. When the meter overflows the METER_OVERFLOW bit in METER_CONTROL register 0x84 is set to 1 and an optional alert is generated if the METER_OVERFLOW_ALERT bit in

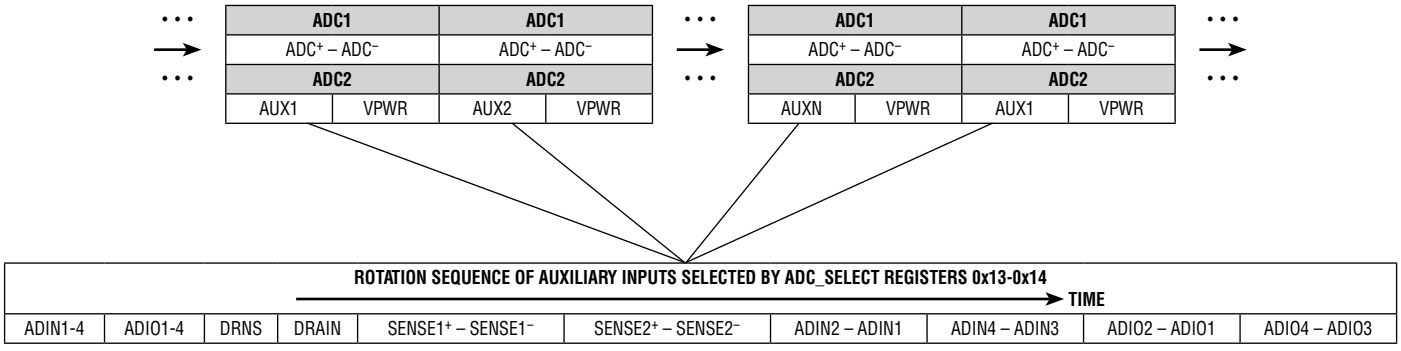

Figure 21. LTC4284 ADC Measurement Pattern in Continuous Mode

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CONFIG_3 register 0x0F is preset to 1. To measure coulombs, the energy meter may be configured to accumulate current rather than power by setting the INTEGRATE_I bit in CONFIG_3 register 0x0F.

The tick counter 0x80 to 0x83 keeps track of how many times power has been added into the energy meter. Dividing the energy by the tick count will yield the average power over the accumulation interval. The 4-byte tick counter will keep count for 9 years in the 12-bit mode before overflowing. When it overflows the TICK_OVERFLOW bit in METER_CONTROL register 0x84 is set to 1 and an optional alert is generated if the TICK_OVERFLOW_ALERT bit in CONFIG_3 register 0x0F is preset to 1. Multiplying the value in the counter by the ADC conversion time yields the time that the energy meter has been accumulating.

Both the energy accumulator and the tick counter are writable, allowing them to be preloaded with a given energy and/or time before overflow so that the LTC4284 will generate an overflow alert after either a specified amount of energy has been delivered or time has passed.

The following formulas are used to convert the values in the ADC data registers into physical units. Since the data are left justified, the same equations apply to all resolutions.

To calculate single-ended voltages measured by ADC2:

$$V = \frac{CODE(word) \bullet 2.048V}{2^{16}}$$

To calculate currents in amperes measured by ADC1 and differential mode ADC2:

$$I = \frac{CODE(word) \bullet 32.768mV}{2^{16} \bullet R_{SENSE}}$$

To calculate power in watts:

$$P = \frac{CODE(word) \bullet 32.768mV \bullet 2.048V}{2^{16} \bullet R_{SENSE}}$$

To calculate energy in joules:

$$E = \frac{CODE(48\,Bits) \bullet 32.768mV \bullet 2.048V \bullet t_{CONV}}{2^{24} \bullet R_{SENSE}}$$

where t_{CONV} is the ADC conversion time depending upon the configured resolution (see Table 12).

To calculate coulombs:

$$Q = \frac{CODE(48\,Bits) \bullet 32.768mV \bullet t_{CONV}}{2^{16} \bullet R_{SENSE}}$$

To calculate average power over the energy accumulation period:

$$P_{AVG} = \frac{E}{t_{CONV} \bullet CODE(COUNTER)}$$

To calculate average current:

$$I_{AVG} = \frac{Q}{t_{CONV} \bullet CODE(COUNTER)}$$

To calculate voltage alarm thresholds:

$$V_{ALARM} = \frac{CODE(byte) \bullet 2.048V}{256}$$

To calculate current Alarm threshold in amperes:

$$I_{ALARM} = \frac{CODE(byte) \bullet 32.768mV}{256 \bullet R_{SENSE}}$$

To calculate power Alarm threshold in watts:

$$P_{ALARM} = \frac{CODE(byte) \bullet 32.768mV \bullet 2.048V}{256 \bullet R_{SENSE}}$$

To synchronize multiple bytes of data from the tick counter and energy meter, use the Read Page protocol (see Data Synchronization and Arbitration). An I^2C read latches the tick counter and energy meter data in buffers while the tick counter and energy meter still increment. Alternatively one can set the METER_HALT bit in METER_CONTROL register 0x84 before reading the data. This will halt the ticker counter and energy meter. Clear the METER_HALT bit afterwards to reactivate incrementing.

The LTC4284 ADCs also feature a snapshot mode that allows a one time measurement of a single data packet: $ADC^+ - ADC^-$, VPWR(RTNS or DRNS), and an auxiliary input selected by the SNAPSHOT_SEL bits in ADC_SNAPSHOT register 0x85. To enable the snapshot mode,

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set the ADC_HALT bit in the ADC_SNAPSHOT register to 1 and write the SNAPSHOT_SEL bits for the desired auxiliary input in one I^2C command. At the falling edge of SCL after bit 0 is received, the ADCs start a single conversion of the selected data packet and the ADC_IDLE bit in ADC_STATUS register 0x01 is cleared to indicate the data is not ready. After completing the conversion, the ADCs are halted, the ADC_IDLE bit is set to indicate the data is ready, and the AUX_ADC_CH bits in the ADC_STATUS register are set to indicate the auxiliary input that is just measured. To make another snapshot measurement, write the ADC_SNAPSHOT register again. To go back to the continuous mode, clear the ADC_HALT bit.

The ADC^+ and ADC^- inputs allow ADC1 to measure the average voltage across the two sense resistors using resistive dividers. In parallel mode (Figure 1) or low stress staged start mode (Figure 13), each channel has its own sense resistor connected between corresponding sense inputs. The averaging resistors should be selected with the same ratio as the sense resistors they connect to, which allows ADC1 to still measure current accurately. In the case as shown in Figure 22, the effective ADC sense resistor is R_S in parallel with $k \bullet R_S$. Scaling the averaging resistors, R_A, by the same scaling factor, k, allows ADC1 to measure the correct sense voltage for this effective sense resistor. The smallest averaging resistor should not exceed 1Ω.

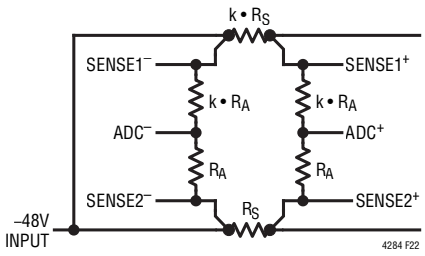

Figure 22. Weighted Averaging Sense Voltages

The 16 auxiliary inputs with the LTC4284 ADCs allow for extensive monitoring of board level signals. Figure 23 shows an example of using ADIO1–ADIO4 as single-ended inputs to monitor individual input voltages of a dual-feed system. The 1.024V VREF is exactly half of the ADC reference voltage and level shifts the ADIO1–ADIO4 inputs within measurable range of the ADC. In Figure 23 one input is –36V (V_{INPUT1}) and the other is –72V (V_{INPUT2}). All node voltages are noted in the circuit. The voltage values in parenthesis are referred to system ground RTN and the others are referred to V_{EE}. With the ADIO1–ADIO4 voltages measured by the ADC and R1/R2 = R3/R4 = R5/R6 = R7/R8, the input voltages are

$$V_{INPUT1} = (V_{ADIO3} - V_{ADIO1})\frac{R1+R2}{R2}$$

$$V_{INPUT2} = (V_{ADIO4} - V_{ADIO2})\frac{R1+R2}{R2}$$

The forward voltage drop of the conducting diode D2 is

$$V_{D2} = V_{REF}\frac{R7}{R8} - V_{ADIO4}\frac{R7+R8}{R8}$$

V_{REF} is ratiometric to the ADC full-scale voltage and can be measured by ADC with one of the ADIN1–ADIN4 pins to calibrate out errors.

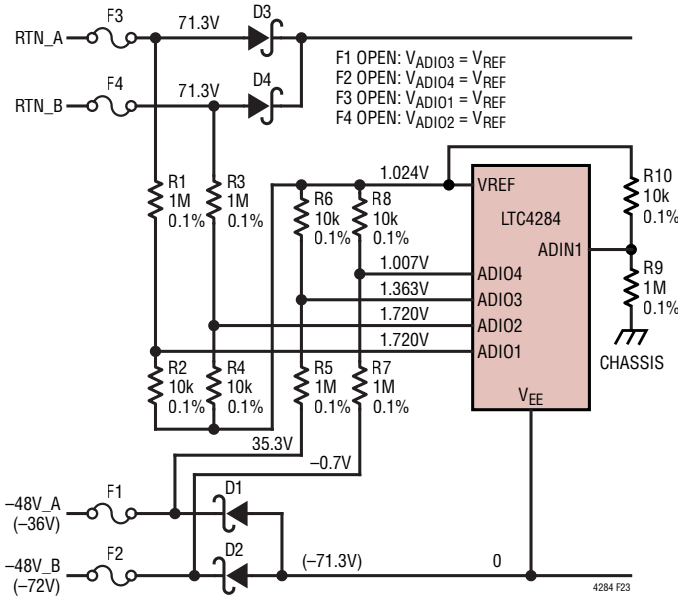

Figure 23. Feed Voltage and Open Fuse Monitoring

The circuit in Figure 23 also monitors fuses on both the RTN and –48V sides. If any one of the four fuses is open, it can be detected by the ADC measurement of the corresponding ADIO input: $V_{ADIO1} = V_{REF}$ indicates fuse F3 is open; $V_{ADIO2} = V_{REF}$ indicates fuse F4 is open; $V_{ADIO3} = V_{REF}$ indicates fuse F1 is open; $V_{ADIO4} = V_{REF}$

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indicates fuse F2 is open. Additionally, chassis ground is monitored with the ADIN1 pin as shown in Figure 23.

Figure 24 shows an example that monitors both individual feed currents and individual channel currents using four differential input pairs. Note that the ADIN2 – ADIN1 and ADIN4 – ADIN3 inputs have a full scale of 33.301mV (positive terminals are at V_{EE}), while the SENSE1$^+$ – SENSE1$^-$ and SENSE2$^+$ – SENSE2$^-$ inputs have a normal full scale of 32.768mV (negative terminals are at V_{EE}).

The output voltage across the load may be calculated from the measured RTNS and DRNS voltages. If a direct measurement of the load voltage is desired, the circuit as shown in Figure 25 may be used.

EEPROM

The LTC4284 has an onboard EEPROM to allow nonvolatile configuration and fault logging. The EEPROM registers are denoted by EE_ in the first column of register Table 3. The EEPROM registers may be read and written like any other register except that the EEPROM takes about 2.2ms to write data.

While the EEPROM is writing, the EEPROM_BUSY bit in the SYSTEM_STATUS register is set. During this time, the I^{2}C interface will NACK attempted writes to EEPROM registers. EEPROM registers will return 0xFF if read while the EEPROM is busy. The FAULT_LOG_CONTROL register is tied together with EEPROM and can't be written while EEPROM is busy. See the Fault Log section for more detail. Other registers may be accessed while EEPROM write is busy. When the EEPROM finishes writing, the EEPROM_BUSY bit will be cleared and the EEPROM_WRITTEN bit in the ADC_ALARM_LOG_1 register will be set.

If the corresponding EEPROM_WRITTEN_ALERT bit in register ADC_ALERT_1 is set, a rising edge on EEPROM_WRITTEN will set ALERT_GENERATED in the METER_CONTROL register. As a result, the ALERT# pin is pulled down. This will alert the host that the LTC4284 EEPROM is ready for more accesses.

When the LTC4284 comes out of UVLO or receives a REBOOT command, the contents of the EEPROM are copied to the corresponding operating registers. This process takes about 1.3ms. During this time, the I^{2}C bus is not available. Any command code received will be NACKed. Registers in the address range 0x0A through 0x40 correspond to EEPROM locations 0xAA through 0xE0. Register 0x90 corresponds to EEPROM location 0xF0. The seven EEPROM bytes in the EE_SCRATCH area are available for any general purpose use. EEPROM is also used to support the fault logging feature. See details in the Fault Log section.

The WP pin prevents I^{2}C writes to the EEPROM when high. Attempts to write to the EEPROM while WP is high will result in a NACK and no action. Fault log writes can take place with WP high, except when the LTC4284 is in single-wire broadcast mode. The EEPROM can be read regardless of the WP pin setting. The current WP pin status is available for reading at the WP_STATUS bit in the REBOOT register.

Factory programmed parts may optionally have the EEPROM locked. In this case the WP pin has no impact. No EEPROM writes are possible. Fault logging is also disabled when the EEPROM is locked. Bit EE_LOCK in the METER_CONTROL register is a 1 when the EEPROM is locked.

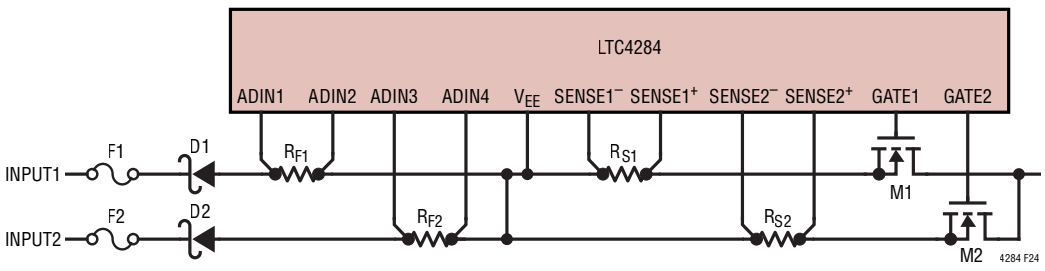

Figure 24. Individual Feed Current and Channel Current Monitoring

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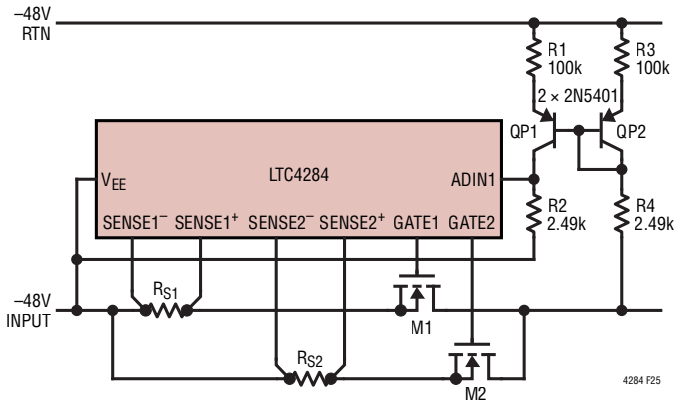

Figure 25. Direct Monitoring of Load Voltage Using a Single ADC Input

Fault Log

The LTC4284's EEPROM supports a fault logging feature. Twelve bytes hold a log for a single fault event (Table 22). In addition, a thirteenth byte provides an EEPROM backup copy for the fault log control register (FAULT_LOG_CONTROL, register 0x90, see Table 21).

Writes to FAULT_LOG_CONTROL always cause a write to the EEPROM backup byte (EE_FAULT_LOG_CONTROL). This causes the EEPROM to go busy, disabling access to all EEPROM registers for about 2.2ms. During this time, FAULT_LOG_CONTROL can be read but not written. If another EEPROM register is written first, FAULT_LOG_CONTROL can't be written until the busy condition clears.

Conditions Leading to a Fault Log Write. A fault condition is defined as any condition in which a bit in the FAULT register (0x04) is set or the EN#_CHANGED bit is set in the ADC_ALARM_LOG_1 register (0x05).

A fault condition will result in a fault log being written if several conditions are met:

1. The fault condition causes GATE1 and GATE2 to be pulled low.
2. V_{IN} is above the UVLO limit.
3. FAULT_LOG_ENABLE in the FAULT_LOG_CONTROL register (0x90) is set.
4. FAULT_LOG_UNLOCK, FAULT_LOG_START and FAULT_LOG_DONE in the FAULT_LOG_CONTROL register are all clear (this ensures any previous fault log has been completely serviced).

The FET_SHORT_FAULT and POWER_FAILED bits don't cause GATE1 and GATE2 to be pulled low, so they don't cause a fault log to be written. Also, the EN#_CHANGED bit doesn't cause a fault log to be written if it is set by the falling edge of EN#.

In addition, fault log writing is disabled if the WP pin is high while the LTC4284 is in single-wire broadcast mode.

Fault Log Writing Sequence. This sequence takes place in the LTC4284 in response to a condition that calls for a fault log write:

1. Freeze a shadow copy of fault bits (register 0x04 and bit [7] of 0x05).
2. Block I^2C access.
3. Set FAULT_LOG_START in the FAULT_LOG_CONTROL register.
4. Write FAULT_LOG_CONTROL to its backup copy in EEPROM.
5. Write the 12 bytes of fault information as detailed in Table 22, fault bits come from the shadow copy.
6. Set FAULT_LOG_DONE in FAULT_LOG_CONTROL.
7. Write FAULT_LOG_CONTROL to its backup copy in EEPROM.
8. Set alert if FAULT_LOG_ALERT is set.
9. Unfreeze the shadow copy of fault bits.
10. Allow I^2C access

The I^2C bus is blocked for about 31ms (14 time t_{WRITE}). During this time, any incoming byte from I^2C will be NACKed. If a fault log write starts in the middle of an I^2C read, bytes of 0xFF will be returned to I^2C in place of expected data.

Resolving Fault Priority. When one fault bit is set, more bits will typically be set soon afterward. With too many bits set, the original cause of the problem is harder to determine. The LTC4284's fault logging logic is designed to capture the first fault indication and disregard subsequent fault bits set until after fault log writing finishes.

The frozen copy of fault bits mentioned in the fault log writing sequence is part of this philosophy. As soon as

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the first fault bit is set which leads to GATE1 and GATE2 low, the frozen copy of fault bits is closed and remains closed until after logging is complete. In the fault log, fault data comes from the frozen copy. During this time, fault information is still accumulated in the main fault registers.

Servicing a Fault Log. After one fault log has been written, further fault log writes will be disabled until the first fault log has been serviced.

The FAULT_LOG_START and FAULT_LOG_DONE bits can't be set or cleared directly by I^2C accesses. To prevent an accidental clearing of fault log information, a multi-byte sequence is required to fully service one fault log so another fault log can be written. The sequence is:

1. Write FAULT_LOG_CONTROL with FAULT_LOG_UNLOCK set
2. Write a second time with FAULT_LOG_UNLOCK set and all other bits clear. This write will clear FAULT_LOG_START and FAULT_LOG_DONE.
3. Write again with FAULT_LOG_UNLOCK, FAULT_LOG_START and FAULT_LOG_DONE all clear. At this time, the FAULT_LOG_ENABLE and FAULT_LOG_ALERT bits may be set as desired.

Additionally, to avoid inadvertently overwriting the logged data through I^2C, bring WP high during servicing.

Incomplete Fault Logs. A fault condition is a likely precursor to an overall loss of power in the LTC4284. For accurate fault logging, the system design must provide sufficient external capacitance as described in Input Power Supply to hold $INTV_{CC}$ up during the time required to write 14 bytes to EEPROM.

The fault log writing sequence described earlier provides a way to detect if the fault log doesn't complete successfully. The first EEPROM write saves FAULT_LOG_CONTROL with the FAULT_LOG_START bit set. Then the final EEPROM write saves FAULT_LOG_CONTROL with both FAULT_LOG_START and FAULT_LOG_DONE bits set.

After a loss of power, the FAULT_LOG_CONTROL register is loaded back from the saved EEPROM copy. If power was lost before a fault log completed, the FAULT_LOG_CONTROL register will have FAULT_LOG_START set, but not FAULT_LOG_END. Also after a loss of power, if the FAULT_LOG_ALERT bit is set and FAULT_LOG_START, FAULT_LOG_DONE or FAULT_LOG_UNLOCK are set, the ALERT# pin will be pulled down to alert the system that an unserviced fault log remains in the chip.

Digital Interface

The LTC4284 communicates with a bus master using a serial 2-wire interface, compatible with both I^2C and SMBus. The 2-wire interface is supplemented by an SMBus-compatible ALERT# output. The LTC4284 is always a bus slave and doesn't use clock stretching.

Many LTC4284 applications require unidirectional isolators such as opto-couplers between the serial interface and the host system. For convenience of opto-coupling with the host, the SDA function is split into SDAI (input) and SDAO (output). For a conventional SDA line, tie SDAI and SDAO together.

When using opto-couplers, connect the SDAI pin to the output of the incoming opto-coupler and connect the SDAO pin to the input of the outgoing opto-coupler (see Figure 2b). If the ALERT# line is used, connect it in the same way as the SDAO pin as shown in Figure 2b.

Bus Compatibility

The basic LTC4284 serial interface is compliant with I^2C and SMBus AC and DC specifications. The timing is compatible with 400Kbit operation for both. This includes the SMBus legacy tHD:DATO timing of 300ns minimum.

In addition, the LTC4284 supports 1Mbit operation which is compatible with I^2C FastMode+ and SMBus 3.0. To use this timing, the FAST_I2C_EN bit in the CONFIG_3 register must be set. This bit may be set to 1 as default by EEPROM, or it can be manually written to 1. If the bit is 0 before writing, the write must be done at 400Kbit or less. With FAST_I2C_EN set, tHD:DATO is reduced to allow higher speed transfers.

The LTC4284 SDAO output is guaranteed to pull down 20mA. This allows the use of a lower value pull-up resistor to reduce the low-to-high delay time.

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START, REPEATED START and STOP Conditions

When the bus is idle, SCL and SDA are high. A bus master signals the start of a transfer with a START condition. START is defined by a falling edge on SDA while SCL is high. The end of the transfer is signaled by a STOP condition. STOP is defined by a rising edge on SDA while SCL is high (see Figure 26).

In between START and STOP, data and handshake bits are transferred with a data value on SDA and a high pulse on SCL. For data or handshake bits, SDA changes only while SCL is low.

A bus master may also signal a REPEATED START condition in the middle of a transfer. Like START, REPEATED START is defined by a falling edge on SDA while SCL is high. REPEATED START is used in read transfers (see Transfer Protocol Types).

ACK/NACK

Data is transferred as a series of 8-bit bytes. Following each data byte is a handshake bit driven by the receiver. SDA low during this bit is interpreted as acknowledge (ACK). SDA high is interpreted as not-acknowledge (NACK).

In all cases, a transfer stops after a NACK bit. If the bus master is sending a data byte, a NACK from the slave indicates an error condition. If all bytes written are ACK'ed, the bus master may also terminate a write by making a STOP condition after the final byte. If the bus master is receiving a data, it returns NACK after the last byte it wants to receive. This is normal, no error condition is implied.

I²C Device Addressing

The bus master addresses a slave by sending a slave address byte after either a START or REPEATED START condition. Bit 0 of the slave address byte is high to select a read transfer and low to select a write. See Transfer Protocol Types for more detail. The LTC4284 ADR1 and ADR0 pins can be configured to select its slave addresses as shown in Table 2.

Single-wire broadcast mode replaces the normal serial-bus interface with a one-wire option which continuously broadcasts important status from the LTC4284. See more details in Single-Wire Broadcast.

Transfer Protocol Types

Figure 26 shows basic elements of the I²C protocol. These are combined to form complete read and write transfers. Figures 27 to 32 show the transfer protocol types supported by the LTC4284.

Table 2. LTC4284 Device Addressing

DESCRIPTION	HEX DEVICE ADDRESS*		BINARY DEVICE ADDRESS								LTC4284 ADDRESS PINS	
	7-Bit	8-Bit	a6	a5	a4	a3	a2	a1	a0	R/W#	ADR1	ADR0
Mass Write	1F	3E	0	0	1	1	1	1	1	0	X	X
Alert Response	0C	19	0	0	0	1	1	0	0	1	X	X
0	10	20	0	0	1	0	0	0	0	X	L	L
1	11	22	0	0	1	0	0	0	1	X	L	NC
2	12	24	0	0	1	0	0	1	0	X	H	NC
3	13	26	0	0	1	0	0	1	1	X	L	H
4	14	28	0	0	1	0	1	0	0	X	NC	L
5	15	2A	0	0	1	0	1	0	1	X	NC	NC
6	16	2C	0	0	1	0	1	1	0	X	H	H
7	17	2E	0	0	1	0	1	1	1	X	NC	H
8	Single-Wire Broadcast Mode										H	L

H = Tie to $INTV_{CC}$; L = Tie to V_{EE}; NC = No connect or open; X = Don't Care
*8-bit hexadecimal address with LSB R/$\overline{W}$ bit = 0
7-bit hexadecimal address with MSB a7 = 0

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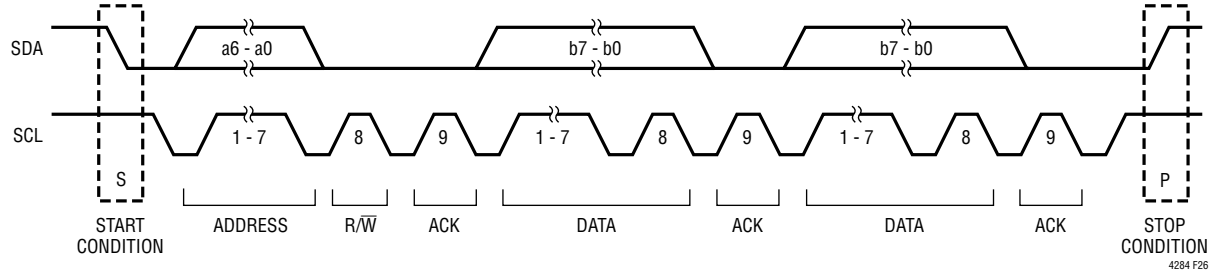

Figure 26. General Data Transfer over I²C

S	ADDRESS	W	A	COMMAND	A	DATA	A	P
	001 a3:a0	0	0	b7:b0	0	b7:b0	0	

4284 F27

FROM MASTER TO SLAVE

FROM SLAVE TO MASTER

A: ACKNOWLEDGE (LOW)
Ā: NOT ACKNOWLEDGE (HIGH)
R: READ BIT (HIGH)
W: WRITE BIT (LOW)
S: START CONDITION
SR: REPEATED START CONDITION
P: STOP CONDITION

Figure 27. Write Byte Protocol

S	ADDRESS	W	A	COMMAND	A	DATA	A	DATA	A	P
	001 a3:a0	0	0	b7:b0	0	b7:b0	0	b7:b0	0	

4284 F28

Figure 28. Write Word Protocol

S	ADDRESS	W	A	COMMAND	A	DATA	• • •	A	DATA	A	P
	001 a3:a0	0	0	b7:b0	0	b7:b0		0	b7:b0	0	

4284 F29

Figure 29. Write Page Protocol

S	ADDRESS	W	A	COMMAND	A	SR	ADDRESS	R	A	DATA	Ā	P
	001 a3:a0	0	0	b7:b0	0		001 a3:a0	1	0	b7:b0	1	

4284 F30

Figure 30. Read Byte Protocol

S	ADDRESS	W	A	COMMAND	A	SR	ADDRESS	R	A	DATA	A	DATA	Ā	P
	001 a3:a0	0	0	b7:b0	0		001 a3:a0	1	0	b7:b0	0	b7:b0	1	

4284 F31

Figure 31. Read Word Protocol

S	ADDRESS	W	A	COMMAND	A	SR	ADDRESS	R	A	DATA	A	• • •	DATA	Ā	P
	001 a3:a0	0	0	b7:b0	0		001 a3:a0	1	0	b7:b0	0		b7:b0	1	

4284 F32

Figure 32. Read Page Protocol

S	ALERT RESPONSE ADDRESS	R	A	DEVICE ADDRESS	Ā	P
	0001100	1	0	001 a3:a0 0	1	

4284 F33

Figure 33. Alert Response Protocol

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Command Codes and Register Addressing

The command byte in each transfer contains the register address for the first byte being accessed. If multiple bytes are accessed in a transfer, each comes from the address following the previous byte. For example, when reading the six-byte ENERGY register, the first byte comes from address 0x7A, the second byte from address 0x7B, up through the final byte from address 0x7F (see Table 3).

It's possible to access two different registers in one transfer. For example, the SYSTEM_STATUS and ADC_STATUS registers can be accessed using a read word transfer with COMMAND equal 0x00. This addressing method is common for I^2C systems, but differs from SMBus. With SMBus, each register occupies a single command code, regardless of register size.

Registers 0x41 to 0x79 are implemented in 16-bit RAM words as shown in Table 3. To save command codes, each occupies only one register address. Consider a four-byte read with command code of 0x41. Data will be returned in this order:

1. Most significant byte of SENSE
2. Least significant byte of SENSE
3. Most significant byte of SENSE_MIN
4. Least significant byte of SENSE_MIN

Write Protocols

For writes, all data bytes come from the bus master and are acknowledged by the slave. Bit 0 of the slave address byte is clear to select write. The COMMAND byte contains the register address for the first byte being written.

A special slave address can be used to implement mass writes. If multiple LTC4284 chips are on the same serial bus, the mass write technique can be used to write all of them at the same time. All LTC4284s respond to a slave address of 0011_111b with the Read/Write# bit clear.

Bit MASS_WRITE_ENABLE in register CONTROL_1 can be set to enable mass writes.

Read Protocols

Reads consist of two parts. First the master sends a slave address byte with bit 0 clear and a COMMAND byte to select the register to be read from. After this, a REPEATED START condition and second slave address byte are sent with bit 0 set (indicating read). The LTC4284 replies with data after the second slave address byte.

Read Page and Write Page Protocols

Read page and write page refer to transfers larger than two bytes. Page accesses are convenient for reading larger registers and for synchronizing data in multiple registers (see Data Synchronization and Arbitration for details). If page accesses are required, the PAGE_READ_WRITE_ENABLE bit in the CONTROL_1 register should be set. If the bit is not set, accesses to more than two bytes of data will be terminated. For an attempted page write, the extra bytes would be NACK'ed. For an attempted page read, the LTC4284 would return 0xFF.

Byte Ordering

The LTC4284 uses big endian ordering for accessing multi-byte registers. That means when a 16-bit word register is accessed, the most significant byte is transferred first, followed by the least significant byte. This is common in I^2C systems. SMBus systems use little endian ordering, with least significant byte transferred first.

ALERT# and Alert Response Protocol

The LTC4284 fully supports the SMBus alert response mechanism. Refer to Figure 33:

1. If ALERT# is low, the LTC4284 will acknowledge the SMBus alert response address (ARA).
2. In the following data byte, the LTC4284 returns its own slave address, with bit 0 clear. Multiple slave devices on the bus may be responding to the same ARA. If a conflict is detected on any bit, the LTC4284 will back off and let the higher priority device continue.
3. If the LTC4284 successfully transfers its entire slave address, it will clear its ALERT_GENERATED bit, and stop pulling ALERT# low.

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There are 52 possible conditions to set ALERT_GENERATED. Each condition (fault or event) has a corresponding alert enable bit. Table 24 has the list of fault/event bits and alert enable bits.

For all cases, ALERT_GENERATED will only be set by a rising edge on the combination of fault/event logically and'ed with alert enable bit. ALERT_GENERATED is set whether a fault/event bit is set first or the corresponding alert enable bit is set first. Once a fault or event bit is set, it won't contribute to ALERT_GENERATED again until the fault or event is cleared.

One event, ADC conversion completed, doesn't have a latched status bit. There is a corresponding ADC_CONV_ALERT bit to enable the ALERT_GENERATED. But when servicing ALERT#, software won't have a way to verify that a completed ADC conversion caused the alert condition. Due to this limitation, the ADC conversion completed alert is not useful unless all other alert sources are masked off.

Typically, software will read the event and fault registers to check status, then write 0's to clear the bits that have been serviced. Event and fault bits can also be set directly by the I^2C bus. A bit set this way leads to ALERT_GENERATED set and ALERT# low in the same way as when the chip sets the bit. ALERT_GENERATED itself can also be set by an I^2C write. These features may be helpful for software test.

Stuck Bus Reset

The LTC4284 has an SMBus-style stuck bus reset. If the serial bus remains stuck for about 30ms, the I^2C controller block will reset itself. When the controller is reset, it stops pulling down SDAO and searches for a new START condition.

In the SMBus definition, the stuck bus timer is cleared by SCL high. Many existing LTC chips including previous hot swap controllers clear the timer when SCL and SDA are both high. This is more thorough because it can detect either SDA or SCL stuck low.

The method presents a problem with the LTC4284. With read page or write page, very long transfers are possible. For each byte of 0x00 transferred, SDA will be low for the whole byte. A long sequence of 0x00 bytes may lead to false stuck bus timeouts. The LTC4284 uses a modified stuck bus mechanism to prevent false timeouts. The timer is cleared If SCL is high and the LTC4284 is not pulling down SDAO.

As with other stuck bus timers, SCL stuck low causes a timeout. In addition, a timeout happens if the LTC4284 continuously pulls down SDAO for 30ms. This could happen if the bus stops with SCL high while the LTC4284 is still pulling down on SDAO.

Data Synchronization and Arbitration

Several RAM locations and registers in the LTC4284 have control shared between ADC logic and the I^2C interface. ADC logic writes data and the I^2C interface reads from them. The RAM locations are at addresses between 0x41 and 0x79. Registers for ENERGY and TICK_COUNTER are at addresses between 0x7A and 0x83. These registers are also written by ADC logic.

ADC writes to ENERGY, TICK_COUNTER and the ADC RAM locations are always done while the I^2C interface is idle. That ensures none of the locations can change in the middle of an I^2C read. For example, when reading a two-byte RAM location, the two bytes read will always be consistent with each other.

The ENERGY and TICK_COUNTER registers are larger, but the same technique can be used. To ensure consistency, read all bytes of each register in a single I^2C operation. For energy calculations, you may also need ENERGY and TICK_COUNTER to be consistent with each other. This can be done by reading both registers together in a single 10-byte I^2C read. The register locations are contiguous to facilitate this approach. Read 10 bytes starting at register location 0x7A.

There are some limits on the length of I^2C transfers. If any one transfer takes longer than an ADC conversion time, some ADC data will be lost. This depends on the bus speed, transfer length and ADC conversion time. See the ADC[2:0] field in Table 12.

As detailed above, the I^2C interface operates in parallel with ADC update logic. In some other cases, I^2C access will be disabled:

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1. After a power-on reset or reboot, I^2C access is disabled while configuration registers are being loaded from EEPROM.
2. While a fault log is being written to EEPROM
3. After a write to the REBOOT register which sets the RBT_EN bit.

In these cases, the I^2C controller ignores all inputs and SDAO is not pulled down. As a result, slave address and other bytes from the bus master will be NACK'ed. This behavior is common in I^2C systems. Be careful with this when operating in an SMBus system. The SMBus specification requires all slave address bytes to be ACK'ed but the 4284 doesn't ACK them in the three cases listed above.

While reading data from the LTC4284, the ACK for each byte comes from the bus master. There's no way for the LTC4284 to indicate a problem during the read. If the I^2C controller is disabled during a read, bytes of 0xFF will be returned by the LTC4284 in place of the expected data.

Single-Wire Broadcast

The LTC4284 can start itself up without any I^2C activity. The chip automatically loads configuration data from EEPROM to working registers after a power up or reboot. In this case, the user may not need a full I^2C interface. For many system applications, a full I^2C interface would require three isolators (see Figure 2b). Use of the single-wire broadcast mode can reduce this to one isolator.

When ADR1 is connected to $INTV_{CC}$ and ADR0 is connected to V_{EE}, single-wire broadcast mode is selected. In this mode, I^2C bus operation is disabled. In its place, status and ADC information are continually transmitted on SDAO. A packet of 20 bytes as shown in Table 2a is transmitted once for each ADC conversion cycle using Manchester encoding.

The packet is in the following format:

Table 2a. Single-Wire Broadcast Data Format

DATA	ADDRESS	SIZE IN BITS
Preamble—0x2A	N/A	8
SENSE	0x41	16
RTNS	0x44	16
POWER	0x47	16
V_{AUX}	Most recent ADC aux reading	16
SYSTEM_STATUS	0x00	8
ADC_STATUS	0x01	8
INPUT_STATUS	0x02	8
FAULT_STATUS	0x03	8
FAULT	0x04	8
ADC_ALARM_LOG	0x05–0x09	40
PEC	N/A	8
Total		160

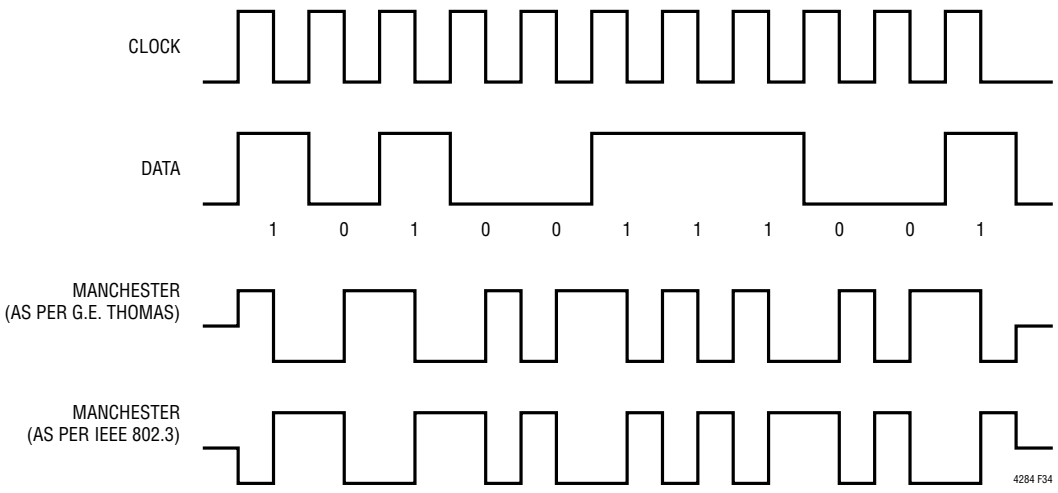

Figure 34. An Example of Manchester Encoding, Showing Both Conventions

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The preamble byte is a fixed pattern to allow hardware or software to detect the packet start and bit rate as shown in Figure 35. V_{AUX} is a selected auxiliary channel measurement. In each ADC conversion cycle, one auxiliary channel may be measured. Bits [7:4] of ADC_STATUS contain the AUX_ADC_CH field to identify which ADC auxiliary input is present in the V_{AUX} field. See the Data Converters section for an explanation of the channel select sequence.

Two different conventions are followed: G.E. Thomas and IEEE 802.3 as shown in Figure 34. For G.E. Thomas convention, each data 1 bit is represented by a falling edge in the middle of the bit cell. For IEEE 802.3 convention, data 1 bits are represented by a rising edge in the middle of the bit cell. G.E. Thomas convention is used for the LTC4284. This is the same as for the LTC4261.

The final byte of the packet is an SMBus-compatible PEC byte. PEC uses an 8-bit CRC with the polynomial X8 + X2 + X + 1. PEC covers all bytes of the packet including the preamble. The PEC accumulator is initialized to 0x00 at the start of the packet.

The data rate of single-wire broadcast can be selected using field BC in the CONFIG_3 register, see Table 11. In broadcast mode, there needs to be enough time to transmit the entire 20-byte packet before another ADC update. That limit means the slowest data rates (128k and 32k) can't be used when the ADC is configured for 8-bit samples. In those two cases, the LTC4284 automatically switches to a minimum 512k data rate for single-wire broadcast.

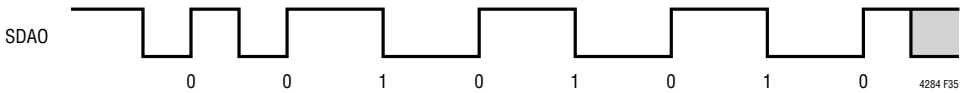

Figure 35. Manchester Encoding for the Preamble Byte of 0x2A

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Table 3. LTC4284 Register Address and Contents

REGISTER NAME	REGISTER ADDRESS*	DESCRIPTION	READ/ WRITE	DATA LENGTH (BYTES)	DEFAULT VALUE
SYSTEM_STATUS	0x00	System status information	R	1	N/A
ADC_STATUS	0x01	ADC conversion status	R	1	N/A
INPUT_STATUS	0x02	PGIO1–PGIO4, ADIO1–ADIO4 general purpose input status	R	1	N/A
FAULT_STATUS	0x03	Fault status information	R	1	N/A
FAULT	0x04	System fault	R/W	1	0x00
ADC_ALARM_LOG	0x05-0x09	ADC measurement alarms	R/W	5	0x0000_0000_00
CONTROL	0x0A-0x0B	Controls the system on/off and auto-retry behaviors	R/W	2	0xDB03
Reserved	0x0C	Read only, always returns 0	R	1	N/A
CONFIG	0x0D-0x0F	Configures current limit, foldback, delays, and other system parameters	R/W	3	0x0CC0_00
PGIO_CONFIG	0x10-0x11	Configures I/O states and outputs of PGIO1–PGIO4	R/W	2	0x0004
ADIO_CONFIG	0x12	Configures I/O states and outputs of ADIO1–ADIO4, controls ADC	R/W	1	0xF0
ADC_SELECT	0x13-0x14	Auxiliary ADC inputs selection	R/W	2	0xFF0F
FAULT_ALERT	0x15	Controls whether ALERT# pulls low after a system fault is logged	R/W	1	0x00
ADC_ALERT	0x16-0x1A	Controls whether ALERT# pulls low after an ADC alarm is logged	R/W	5	0x0000_0000_00
SENSE_MIN_TH	0x1B	ADC alarm threshold for minimum $ADC^+ - ADC^-$	R/W	1	0x00
SENSE_MAX_TH	0x1C	ADC alarm threshold for maximum $ADC^+ - ADC^-$	R/W	1	0xFF
VPWR_MIN_TH	0x1D	ADC alarm threshold for minimum VPWR(RTNS/DRNS) voltage	R/W	1	0x00
VPWR_MAX_TH	0x1E	ADC alarm threshold for maximum VPWR(RTNS/DRNS) voltage	R/W	1	0xFF
POWER_MIN_TH	0x1F	ADC alarm threshold for minimum input power	R/W	1	0x00
POWER_MAX_TH	0x20	ADC alarm threshold for maximum input power	R/W	1	0xFF
ADIN1_MIN_TH	0x21	ADC alarm threshold for minimum ADIN1 voltage	R/W	1	0x00
ADIN1_MAX_TH	0x22	ADC alarm threshold for maximum ADIN1 voltage	R/W	1	0xFF
ADIN2_MIN_TH	0x23	ADC alarm threshold for minimum ADIN2 voltage	R/W	1	0x00
ADIN2_MAX_TH	0x24	ADC alarm threshold for maximum ADIN2 voltage	R/W	1	0xFF
ADIN3_MIN_TH	0x25	ADC alarm threshold for minimum ADIN3 voltage	R/W	1	0x00
ADIN3_MAX_TH	0x26	ADC alarm threshold for maximum ADIN3 voltage	R/W	1	0xFF
ADIN4_MIN_TH	0x27	ADC alarm threshold for minimum ADIN4 voltage	R/W	1	0x00
ADIN4_MAX_TH	0x28	ADC alarm threshold for maximum ADIN4 voltage	R/W	1	0xFF
ADIO1_MIN_TH	0x29	ADC alarm threshold for minimum ADIO1 voltage	R/W	1	0x00
ADIO1_MAX_TH	0x2A	ADC alarm threshold for maximum ADIO1 voltage	R/W	1	0xFF
ADIO2_MIN_TH	0x2B	ADC alarm threshold for minimum ADIO2 voltage	R/W	1	0x00
ADIO2_MAX_TH	0x2C	ADC alarm threshold for maximum ADIO2 voltage	R/W	1	0xFF
ADIO3_MIN_TH	0x2D	ADC alarm threshold for minimum ADIO3 voltage	R/W	1	0x00
ADIO3_MAX_TH	0x2E	ADC alarm threshold for maximum ADIO3 voltage	R/W	1	0xFF
ADIO4_MIN_TH	0x2F	ADC alarm threshold for minimum ADIO4 voltage	R/W	1	0x00
ADIO4_MAX_TH	0x30	ADC alarm threshold for maximum ADIO4 voltage	R/W	1	0xFF
DRNS_MIN_TH	0x31	ADC alarm threshold for minimum DRNS voltage	R/W	1	0x00
DRNS_MAX_TH	0x32	ADC alarm threshold for maximum DRNS voltage	R/W	1	0xFF
DRAIN_MIN_TH	0x33	ADC alarm threshold for minimum DRAIN voltage	R/W	1	0x00

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Table 3. LTC4284 Register Address and Contents (Cont.)

REGISTER NAME	REGISTER ADDRESS*	DESCRIPTION	READ/ WRITE	DATA LENGTH (BYTES)	DEFAULT VALUE
DRAIN_MAX_TH	0x34	ADC alarm threshold for maximum DRAIN voltage	R/W	1	0xFF
SENSE1_MIN_TH	0x35	ADC alarm threshold for minimum $SENSE1^+ – SENSE1^–$	R/W	1	0x00
SENSE1_MAX_TH	0x36	ADC alarm threshold for maximum $SENSE1^+ – SENSE1^–$	R/W	1	0xFF
SENSE2_MIN_TH	0x37	ADC alarm threshold for minimum $SENSE2^+ – SENSE2^–$	R/W	1	0x00
SENSE2_MAX_TH	0x38	ADC alarm threshold for maximum $SENSE2^+ – SENSE2^–$	R/W	1	0xFF
ADIN12_MIN_TH	0x39	ADC alarm threshold for minimum ADIN2 – ADIN1	R/W	1	0x00
ADIN12_MAX_TH	0x3A	ADC alarm threshold for maximum ADIN2 – ADIN1	R/W	1	0xFF
ADIN34_MIN_TH	0x3B	ADC alarm threshold for minimum ADIN4 – ADIN3	R/W	1	0x00
ADIN34_MAX_TH	0x3C	ADC alarm threshold for maximum ADIN4 – ADIN3	R/W	1	0xFF
ADIO12_MIN_TH	0x3D	ADC alarm threshold for minimum ADIO2 – ADIO1	R/W	1	0x00
ADIO12_MAX_TH	0x3E	ADC alarm threshold for maximum ADIO2 – ADIO1	R/W	1	0xFF
ADIO34_MIN_TH	0x3F	ADC alarm threshold for minimum ADIO4 – ADIO3	R/W	1	0x00
ADIO34_MAX_TH	0x40	ADC alarm threshold for maximum ADIO4 – ADIO3	R/W	1	0xFF
SENSE	0x41	Most recent ADC output for $ADC^+ – ADC^–$	R/W	2	0x0000
SENSE_MIN	0x42	Minimum ADC output for $ADC^+ – ADC^–$	R/W	2	0x0000
SENSE_MAX	0x43	Maximum ADC output for $ADC^+ – ADC^–$	R/W	2	0x0000
VPWR	0x44	Most recent ADC output for VPWR(RTNS/DRNS)	R/W	2	0x0000
VPWR_MIN	0x45	Minimum ADC output for VPWR(RTNS/DRNS)	R/W	2	0x0000
VPWR_MAX	0x46	Maximum ADC output for VPWR(RTNS/DRNS)	R/W	2	0x0000
POWER	0x47	Most recent ADC output for power	R/W	2	0x0000
POWER_MIN	0x48	Minimum ADC output for power	R/W	2	0x0000
POWER_MAX	0x49	Maximum ADC output for power	R/W	2	0x0000
ADIN1	0x4A	Most recent ADC output for ADIN1	R/W	2	0x0000
ADIN1_MIN	0x4B	Minimum ADC output for ADIN1	R/W	2	0x0000
ADIN1_MAX	0x4C	Maximum ADC output for ADIN1	R/W	2	0x0000
ADIN2	0x4D	Most recent ADC output for ADIN2	R/W	2	0x0000
ADIN2_MIN	0x4E	Minimum ADC output for ADIN2	R/W	2	0x0000
ADIN2_MAX	0x4F	Maximum ADC output for ADIN2	R/W	2	0x0000
ADIN3	0x50	Most recent ADC output for ADIN3	R/W	2	0x0000
ADIN3_MIN	0x51	Minimum ADC output for ADIN3	R/W	2	0x0000
ADIN3_MAX	0x52	Maximum ADC output for ADIN3	R/W	2	0x0000
ADIN4	0x53	Most recent ADC output for ADIN4	R/W	2	0x0000
ADIN4_MIN	0x54	Minimum ADC output for ADIN4	R/W	2	0x0000
ADIN4_MAX	0x55	Maximum ADC output for ADIN4	R/W	2	0x0000
ADIO1	0x56	Most recent ADC output for ADIO1	R/W	2	0x0000
ADIO1_MIN	0x57	Minimum ADC output for ADIO1	R/W	2	0x0000
ADIO1_MAX	0x58	Maximum ADC output for ADIO1	R/W	2	0x0000
ADIO2	0x59	Most recent ADC output for ADIO2	R/W	2	0x0000
ADIO2_MIN	0x5A	Minimum ADC output for ADIO2	R/W	2	0x0000

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Table 3. LTC4284 Register Address and Contents (Cont.)

REGISTER NAME	REGISTER ADDRESS*	DESCRIPTION	READ/ WRITE	DATA LENGTH (BYTES)	DEFAULT VALUE
ADIO2_MAX	0x5B	Maximum ADC output for ADIO2	R/W	2	0x0000
ADIO3	0x5C	Most recent ADC output for ADIO3	R/W	2	0x0000
ADIO3_MIN	0x5D	Minimum ADC output for ADIO3	R/W	2	0x0000
ADIO3_MAX	0x5E	Maximum ADC output for ADIO3	R/W	2	0x0000
ADIO4	0x5F	Most recent ADC output for ADIO4	R/W	2	0x0000
ADIO4_MIN	0x60	Minimum ADC output for ADIO4	R/W	2	0x0000
ADIO4_MAX	0x61	Maximum ADC output for ADIO4	R/W	2	0x0000
DRNS	0x62	Most recent ADC output for DRNS	R/W	2	0x0000
DRNS_MIN	0x63	Minimum ADC output for DRNS	R/W	2	0x0000
DRNS_MAX	0x64	Maximum ADC output for DRNS	R/W	2	0x0000
DRAIN	0x65	Most recent ADC output for DRAIN	R/W	2	0x0000
DRAIN_MIN	0x66	Minimum ADC output for DRAIN	R/W	2	0x0000
DRAIN_MAX	0x67	Maximum ADC output for DRAIN	R/W	2	0x0000
SENSE1	0x68	Most recent ADC output for $SENSE1^+ - SENSE1^-$	R/W	2	0x0000
SENSE1_MIN	0x69	Minimum ADC output for $SENSE1^+ - SENSE1^-$	R/W	2	0x0000
SENSE1_MAX	0x6A	Maximum ADC output for $SENSE1^+ - SENSE1^-$	R/W	2	0x0000
SENSE2	0x6B	Most recent ADC output for $SENSE2^+ - SENSE2^-$	R/W	2	0x0000
SENSE2_MIN	0x6C	Minimum ADC output for $SENSE2^+ - SENSE2^-$	R/W	2	0x0000
SENSE2_MAX	0x6D	Maximum ADC output for $SENSE2^+ - SENSE2^-$	R/W	2	0x0000
ADIN12	0x6E	Most recent ADC output for ADIN2 – ADIN1	R/W	2	0x0000
ADIN12_MIN	0x6F	Minimum ADC output for ADIN2 – ADIN1	R/W	2	0x0000
ADIN12_MAX	0x70	Maximum ADC output for ADIN2 – ADIN1	R/W	2	0x0000
ADIN34	0x71	Most recent ADC output for ADIN4 – ADIN3	R/W	2	0x0000
ADIN34_MIN	0x72	Minimum ADC output for ADIN4 – ADIN3	R/W	2	0x0000
ADIN34_MAX	0x73	Maximum ADC output for ADIN4 – ADIN3	R/W	2	0x0000
ADIO12	0x74	Most recent ADC output for ADIO2 – ADIO1	R/W	2	0x0000
ADIO12_MIN	0x75	Minimum ADC output for ADIO2 – ADIO1	R/W	2	0x0000
ADIO12_MAX	0x76	Maximum ADC output for ADIO2 – ADIO1	R/W	2	0x0000
ADIO34	0x77	Most recent ADC output for ADIO4 – ADIO3	R/W	2	0x0000
ADIO34_MIN	0x78	Minimum ADC output for ADIO4 – ADIO3	R/W	2	0x0000
ADIO34_MAX	0x79	Maximum ADC output for ADIO4 – ADIO3	R/W	2	0x0000
ENERGY	0x7A-0x7F	Input energy meter	R/W	6	0x0000_0000_0000
TICK_COUNTER	0x80-0x83	Tick counter for energy meter	R/W	4	0x0000_0000
METER_CONTROL	0x84	Controls energy meter and tick counter	R/W	1	0x00
ADC_SNAPSHOT	0x85	Controls ADC snapshot	R/W	1	0x00
Reserved	0x86-0x8F	Read only, always returns 0	R	10	N/A
FAULT_LOG_CONTROL	0x90	Enables logging fault and ADC data into EEPROM	R/W	1	0x00
Reserved	0x91-0xA1	Read only, 0x91–0x9F return 0xFF, 0xA0 and 0xA1 return 0	R	17	N/A
REBOOT	0xA2	Enables reboot and configures reboot delay	R/W	1	0x00

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x. LTC4284 Register Address and Contents (Cont.)

REGISTER NAME	REGISTER ADDRESS*	DESCRIPTION	READ/ WRITE	DATA LENGTH (BYTES)	DEFAULT VALUE
Reserved	0xA3	Read only, always returns 0	R	1	N/A
EE_FAULT	0xA4	Records fault register in EEPROM upon a fault	R/W	1	0x00
EE_ADC_ALARM_LOG	0xA5-0xA9	Records ADC_ALARM_LOG registers in EEPROM upon a fault	R/W	5	0x0000_0000_00
EE_CONTROL	0xAA-0xAB	Stores default of CONTROL registers in EEPROM	R/W	2	0xDB03
Reserved	0xAC	Read only, returns 0xFF if EEPROM busy, otherwise returns 0	R	1	N/A
EE_CONFIG	0xAD-0xAF	Stores default of CONFIG registers in EEPROM	R/W	3	0x0CC0_00
EE_PGIO_CONFIG	0xB0-0xB1	Stores default of PGIO_CONFIG registers in EEPROM	R/W	2	0x0004
EE_ADIO_CONFIG	0xB2	Stores default of ADIO_CONFIG register in EEPROM	R/W	1	0xF0
EE_ADC_SELECT	0xB3-0xB4	Stores default of ADC_SELECT registers in EEPROM	R/W	2	0xFF0F
EE_FAULT_ALERT	0xB5	Stores default of FAULT_ALERT register in EEPROM	R/W	1	0x00
EE_ADC_ALERT	0xB6-0xBA	Stores default of ADC_ALERT registers in EEPROM	R/W	5	0x0000_0000_00
EE_SENSE_MIN_TH	0xBB	Stores default of SENSE_MIN_TH register in EEPROM	R/W	1	0x00
EE_SENSE_MAX_TH	0xBC	Stores default of SENSE_MAX_TH register in EEPROM	R/W	1	0xFF
EE_VPWR_MIN_TH	0xBD	Stores default of VPWR_MIN_TH register in EEPROM	R/W	1	0x00
EE_VPWR_MAX_TH	0xBE	Stores default of VPWR_MAX_TH register in EEPROM	R/W	1	0xFF
EE_POWER_MIN_TH	0xBF	Stores default of POWER_MIN_TH register in EEPROM	R/W	1	0x00
EE_POWER_MAX_TH	0xC0	Stores default of POWER_MAX_TH register in EEPROM	R/W	1	0xFF
EE_ADIN1_MIN_TH	0xC1	Stores default of ADIN1_MIN_TH register in EEPROM	R/W	1	0x00
EE_ADIN1_MAX_TH	0xC2	Stores default of ADIN1_MAX_TH register in EEPROM	R/W	1	0xFF
EE_ADIN2_MIN_TH	0xC3	Stores default of ADIN2_MIN_TH register in EEPROM	R/W	1	0x00
EE_ADIN2_MAX_TH	0xC4	Stores default of ADIN2_MAX_TH register in EEPROM	R/W	1	0xFF
EE_ADIN3_MIN_TH	0xC5	Stores default of ADIN3_MIN_TH register in EEPROM	R/W	1	0x00
EE_ADIN3_MAX_TH	0xC6	Stores default of ADIN3_MAX_TH register in EEPROM	R/W	1	0xFF
EE_ADIN4_MIN_TH	0xC7	Stores default of ADIN4_MIN_TH register in EEPROM	R/W	1	0x00
EE_ADIN4_MAX_TH	0xC8	Stores default of ADIN4_MAX_TH register in EEPROM	R/W	1	0xFF
EE_ADIO1_MIN_TH	0xC9	Stores default of ADIO1_MIN_TH register in EEPROM	R/W	1	0x00
EE_ADIO1_MAX_TH	0xCA	Stores default of ADIO1_MAX_TH register in EEPROM	R/W	1	0xFF
EE_ADIO2_MIN_TH	0xCB	Stores default of ADIO2_MIN_TH register in EEPROM	R/W	1	0x00
EE_ADIO2_MAX_TH	0xCC	Stores default of ADIO2_MAX_TH register in EEPROM	R/W	1	0xFF
EE_ADIO3_MIN_TH	0xCD	Stores default of ADIO3_MIN_TH register in EEPROM	R/W	1	0x00
EE_ADIO3_MAX_TH	0xCE	Stores default of ADIO3_MAX_TH register in EEPROM	R/W	1	0xFF
EE_ADIO4_MIN_TH	0xCF	Stores default of ADIO4_MIN_TH register in EEPROM	R/W	1	0x00
EE_ADIO4_MAX_TH	0xD0	Stores default of ADIO4_MAX_TH register in EEPROM	R/W	1	0xFF
EE_DRNS_MIN_TH	0xD1	Stores default of DRNS_MIN_TH register in EEPROM	R/W	1	0x00
EE_DRNS_MAX_TH	0xD2	Stores default of DRNS_MAX_TH register in EEPROM	R/W	1	0xFF
EE_DRAIN_MIN_TH	0xD3	Stores default of DRAIN_MIN_TH register in EEPROM	R/W	1	0x00
EE_DRAIN_MAX_TH	0xD4	Stores default of DRAIN_MAX_TH register in EEPROM	R/W	1	0xFF
EE_SENSE1_MIN_TH	0xD5	Stores default of SENSE1_MIN_TH register in EEPROM	R/W	1	0x00
EE_SENSE1_MAX_TH	0xD6	Stores default of SENSE1_MAX_TH register in EEPROM	R/W	1	0xFF

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Table 3. LTC4284 Register Address and Contents (Cont.)

REGISTER NAME	REGISTER ADDRESS*	DESCRIPTION	READ/ WRITE	DATA LENGTH (BYTES)	DEFAULT VALUE
EE_SENSE2_MIN_TH	0xD7	Stores default of SENSE2_MIN_TH register in EEPROM	R/W	1	0x00
EE_SENSE2_MAX_TH	0xD8	Stores default of SENSE2_MAX_TH register in EEPROM	R/W	1	0xFF
EE_ADIN12_MIN_TH	0xD9	Stores default of ADIN12_MIN_TH register in EEPROM	R/W	1	0x00
EE_ADIN12_MAX_TH	0xDA	Stores default of ADIN12_MAX_TH register in EEPROM	R/W	1	0xFF
EE_ADIN34_MIN_TH	0xDB	Stores default of ADIN34_MIN_TH register in EEPROM	R/W	1	0x00
EE_ADIN34_MAX_TH	0xDC	Stores default of ADIN34_MAX_TH register in EEPROM	R/W	1	0xFF
EE_ADIO12_MIN_TH	0xDD	Stores default of ADIO12_MIN_TH register in EEPROM	R/W	1	0x00
EE_ADIO12_MAX_TH	0xDE	Stores default of ADIO12_MAX_TH register in EEPROM	R/W	1	0xFF
EE_ADIO34_MIN_TH	0xDF	Stores default of ADIO34_MIN_TH register in EEPROM	R/W	1	0x00
EE_ADIO34_MAX_TH	0xE0	Stores default of ADIO34_MAX_TH register in EEPROM	R/W	1	0xFF
EE_SENSE	0xE1	Records MSB byte of SENSE registers in EEPROM upon a fault	R/W	1	0x00
EE_SENSE_MIN	0xE2	Records MSB byte of SENSE_MIN registers in EEPROM upon a fault	R/W	1	0x00
EE_SENSE_MAX	0xE3	Records MSB byte of SENSE_MAX registers in EEPROM upon a fault	R/W	1	0x00
EE_RTNS	0xE4	Records MSB byte of RTNS registers in EEPROM upon a fault	R/W	1	0x00
EE_RTNS_MIN	0xE5	Records MSB byte of RTNS_MIN registers in EEPROM upon a fault	R/W	1	0x00
EE_RTNS_MAX	0xE6	Records MSB byte of RTNS_MAX registers in EEPROM upon a fault	R/W	1	0x00
POWER_PLAY_ID	0xE7-0xE8	LTpowerPlay ID for LTC4284	R	2	0x1070
EE_SCRATCH	0xE9-0xEF	Spare EEPROM bytes	R/W	7	0x0000_0000_0000
EE_FAULT_LOG_ CONTROL	0xF0	EEPROM backup of FAULT_LOG_CONTROL register	R/W	1	0x00
Reserved	0xF1-0xFF	Read only, always returns 0xFF	R	15	N/A

*For the two-byte ADC data registers from 0x41 to 0x79, the address points to the MSB byte and increments to the LSB byte when using a Write Word or Read Word protocol.

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Table 4. SYSTEM_STATUS Registers (0x00) – Read Only

BIT	NAME	OPERATION
7	FET_ON_STATUS	On/off status of GATE; 1 = GATE commanded on, 0 = GATE commanded off
6	EN#	State of EN# pin; 1 = EN# high, 0 = EN# low
5	GATE2_HIGH	State of GATE2 pin; 1 = GATE2 high, 0 = GATE2 low
4	GATE1_HIGH	State of GATE1 pin; 1 = GATE1 high, 0 = GATE1 low
3	TMR_LOW	Status of TMR pin; 1 = TMR is lower than 0.1V, 0 = TMR is higher than 0.1V
2	EEPROM _BUSY	Status of EEPROM writing; 1 = EEPROM is being written, 0 = EEPROM writing is completed
1	PG_STATUS	Power good status; 1 = power good condition met, 0 = power good condition not met
0	MODE1	Single driver mode (Mode 1) status; 1 = Mode 1 is enabled, 0 = Mode 1 is disabled

Table 5. ADC_STATUS Register (0x01) – Read Only

BIT	NAME	OPERATION
7:4	AUX_ADC_CH	Channel label of the auxiliary input that completed the latest ADC measurement in continuous or snapshot mode

AUX_ADC_CH [7:4]	Auxiliary ADC Input	Register Address
0000	ADIN1	0x4A
0001	ADIN2	0x4D
0010	ADIN3	0x50
0011	ADIN4	0x53
0100	ADIO1	0x56
0101	ADIO2	0x59
0110	ADIO3	0x5C
0111	ADIO4	0x5F
1000	DRNS	0x62
1001	DRAIN	0x65
1010	$SENSE1^+ – SENSE1^-$	0x68
1011	$SENSE2^+ – SENSE2^-$	0x6B
1100	ADIN2 – ADIN1	0x6E
1101	ADIN4 – ADIN3	0x71
1110	ADIO2 – ADIO1	0x74
1111	ADIO4 – ADIO3	0x77

3	ADC_IDLE	Conversion status of ADC; 1 = ADC is idle in snapshot mode, 0 = ADC is in continuous mode or ADC is busy in snapshot mode
2	MODE2	Parallel mode (Mode 2) status; 1 = Mode 2 is enabled, 0 = Mode 2 is disabled
1	MODE3	High stress staged start mode (Mode 3) status; 1 = Mode 3 is enabled, 0 = Mode 3 is disabled
0	MODE4	Low stress staged start mode (Mode 4) status; 1 = Mode 4 is enabled, 0 = Mode 4 is disabled

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Table 6. INPUT_STATUS Register (0x02) – Read Only

BIT	NAME	OPERATION
7	PGIO1_INPUT	State of PGIO1 pin; 1 = PGIO1 high, 0 = PGIO1 low
6	PGIO2_INPUT	State of PGIO2 pin; 1 = PGIO2 high, 0 = PGIO2 low
5	PGIO3_INPUT	State of PGIO3 pin; 1 = PGIO3 high, 0 = PGIO3 low
4	PGIO4_INPUT	State of PGIO4 pin; 1 = PGIO4 high, 0 = PGIO4 low
3	ADIO1_INPUT	State of ADIO1 pin; 1 = ADIO1 high, 0 = ADIO1 low
2	ADIO2_INPUT	State of ADIO2 pin; 1 = ADIO2 high, 0 = ADIO2 low
1	ADIO3_INPUT	State of ADIO3 pin; 1 = ADIO3 high, 0 = ADIO3 low
0	ADIO4_INPUT	State of ADIO4 pin; 1 = ADIO4 high, 0 = ADIO4 low

Table 7. FAULT_STATUS Register (0x03) – Read Only

BIT	NAME	OPERATION
7	EXT_FAULT_STATUS	State of PGIO4 pin when configured to EXT_FAULT#/EXT_FAULT; 1 = PGIO4 low/high, 0 = PGIO4 high/low
6	FET_SHORT_STATUS	FET short status; 1 = FET shorted, 0 = FET not shorted
5	VOUT_LOW	V_{OUT} low status; 1 = $V_{OUT} < V_{OUTTH}$, 0 = $V_{OUT} \geq V_{OUTTH}$
4	PGI_STATUS	State of PGIO3 when configured to PGI#/PGI when PGI check timer expires; 1 = PGIO3 high/low, 0 = PGIO3 low/high
3	FET_BAD_STATUS	FET bad status; 1 = FET bad condition present, 0 = FET bad condition not present
2	OC_STATUS	Active current limit status; 1 = active current limit engaged, 0 = active current limit not engaged
1	UV_STATUS	Input undervoltage status; 1 = UVH and UVL are low, 0 = UVH or UVL high
0	OV_STATUS	Input overvoltage status; 1 = OV high, 0 = OV low

Table 8. FAULT Register (0x04) – Read/Write

BIT	NAME	OPERATION	DEFAULT
7	EXT_FAULT	External fault at PGIO4 pin; 1 = external fault detected, 0 = no external fault	0
6	FET_SHORT_FAULT	FET short fault; 1 = FET short fault occurred, 0 = no FET short fault	0
5	POWER_FAILED	V_{OUT} was low after power good latched; 1 = V_{OUT} low detected, 0 = V_{OUT} has not been low	0
4	PGI_FAULT	PGI fault at PGIO3 pin; 1 = PGI fault occurred, 0 = no PGI fault	0
3	FET_BAD_FAULT	FET bad fault; 1 = FET bad fault occurred, 0 = no FET bad fault	0
2	OC_FAULT	Overcurrent fault; 1 = overcurrent fault occurred, 0 = no overcurrent fault	0
1	UV_FAULT	Undervoltage fault; 1 = undervoltage fault occurred, 0 = no undervoltage fault	0
0	OV_FAULT	Overvoltage fault; 1 = overvoltage fault occurred, 0 = no overvoltage fault	0

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Table 9. ADC_ALARM_LOG Registers (0x05–0x09) – Read/Write

BIT	NAME	OPERATION	DEFAULT
ADC_ALARM_LOG_1 (0x05) – Read/Write			
7	EN#_CHANGED	EN# pin changed state; 1 = EN# changed state, 0 = EN# unchanged	0
6	EEPROM_WRITTEN	EEPROM was written through I^2C; 1 = EEPROM was written, 0 = EEPROM write has not been written	0
5	SENSE_HIGH_ALARM	$ADC^+ – ADC^–$ was above SENSE_MAX_TH; 1 = $ADC^+ – ADC^–$ was high, 0 = $ADC^+ – ADC^–$ has not been high	0
4	SENSE_LOW_ALARM	$ADC^+ – ADC^–$ was below SENSE_MIN_TH; 1 = $ADC^+ – ADC^–$ was low, 0 = $ADC^+ – ADC^–$ has not been low	0
3	VPWR_HIGH_ALARM	VPWR was above VPWR_MAX_TH; 1 = VPWR was high, 0 = VPWR has not been high	0
2	VPWR_LOW_ALARM	VPWR was below VPWR_MIN_TH; 1 = VPWR was low, 0 = VPWR has not been low	0
1	POWER_HIGH_ALARM	POWER was above POWER_MAX_TH; 1 = POWER was high, 0 = POWER has not been high	0
0	POWER_LOW_ALARM	POWER was below POWER_MIN_TH; 1 = POWER was low, 0 = POWER has not been low	0
ADC_ALARM_LOG_2 (0x06) – Read/Write			
7	ADIN1_HIGH_ALARM	ADIN1 was above ADIN1_MAX_TH; 1 = ADIN1 was high, 0 = ADIN1 has not been high	0
6	ADIN1_LOW_ALARM	ADIN1 was below ADIN1_MIN_TH; 1 = ADIN1 was low, 0 = ADIN1 has not been low	0
5	ADIN2_HIGH_ALARM	ADIN2 was above ADIN2_MAX_TH; 1 = ADIN2 was high, 0 = ADIN2 has not been high	0
4	ADIN2_LOW_ALARM	ADIN2 was below ADIN2_MIN_TH; 1 = ADIN2 was low, 0 = ADIN2 has not been low	0
3	ADIN3_HIGH_ALARM	ADIN3 was above ADIN3_MAX_TH; 1 = ADIN3 was high, 0 = ADIN3 has not been high	0
2	ADIN3_LOW_ALARM	ADIN3 was below ADIN3_MIN_TH; 1 = ADIN3 was low, 0 = ADIN3 has not been low	0
1	ADIN4_HIGH_ALARM	ADIN4 was above ADIN4_MAX_TH; 1 = ADIN4 was high, 0 = ADIN4 has not been high	0
0	ADIN4_LOW_ALARM	ADIN4 was below ADIN4_MIN_TH; 1 = ADIN4 was low, 0 = ADIN4 has not been low	0
ADC_ALARM_LOG_3 (0x07) – Read/Write			
7	ADIO1_HIGH_ALARM	ADIO1 was above ADIO1_MAX_TH; 1 = ADIO1 was high, 0 = ADIO1 has not been high	0
6	ADIO1_LOW_ALARM	ADIO1 was below ADIO1_MIN_TH; 1 = ADIO1 was low, 0 = ADIO1 has not been low	0
5	ADIO2_HIGH_ALARM	ADIO2 was above ADIO2_MAX_TH; 1 = ADIO2 was high, 0 = ADIO2 has not been high	0
4	ADIO2_LOW_ALARM	ADIO2 was below ADIO2_MIN_TH; 1 = ADIO2 was low, 0 = ADIO2 has not been low	0
3	ADIO3_HIGH_ALARM	ADIO3 was above ADIO3_MAX_TH; 1 = ADIO3 was high, 0 = ADIO3 has not been high	0
2	ADIO3_LOW_ALARM	ADIO3 was below ADIO3_MIN_TH; 1 = ADIO3 was low, 0 = ADIO3 has not been low	0
1	ADIO4_HIGH_ALARM	ADIO4 was above ADIO4_MAX_TH; 1 = ADIO4 was high, 0 = ADIO4 has not been high	0
0	ADIO4_LOW_ALARM	ADIO4 was below ADIO4_MIN_TH; 1 = ADIO4 was low, 0 = ADIO4 has not been low	0

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BIT	NAME	OPERATION	DEFAULT
ADC_ALARM_LOG_4 (0x08) – Read/Write			
7	DRNS_HIGH_ALARM	DRNS was above DRNS_MAX_TH; 1 = DRNS was high, 0 = DRNS has not been high	0
6	DRNS_LOW_ALARM	DRNS was below DRNS_MIN_TH; 1 = DRNS was low, 0 = DRNS has not been low	0
5	DRAIN_HIGH_ALARM	DRAIN was above DRAIN_MAX_TH; 1 = DRAIN was high, 0 = DRAIN has not been high	0
4	DRAIN_LOW_ALARM	DRAIN was below DRAIN_MIN_TH; 1 = DRAIN was low, 0 = DRAIN has not been low	0
3	SENSE1_HIGH_ALARM	$SENSE1^+ – SENSE1^–$ was above SENSE1_MAX_TH; 1 = $SENSE1^+ – SENSE1^–$ was high, 0 = $SENSE1^+ – SENSE1^–$ has not been high	0
2	SENSE1_LOW_ALARM	$SENSE1^+ – SENSE1^–$ was below SENSE1_MIN_TH; 1 = $SENSE1^+ – SENSE1^–$ was low, 0 = $SENSE1^+ – SENSE1^–$ has not been low	0
1	SENSE2_HIGH_ALARM	$SENSE2^+ – SENSE2^–$ was above SENSE2_MAX_TH; 1 = $SENSE2^+ – SENSE2^–$ was high, 0 = $SENSE2^+ – SENSE2^–$ has not been high	0
0	SENSE2_LOW_ALARM	$SENSE2^+ – SENSE2^–$ was below SENSE2_MIN_TH; 1 = $SENSE2^+ – SENSE2^–$ was low, 0 = $SENSE2^+ – SENSE2^–$ has not been low	0
ADC_ALARM_LOG_5 (0x09) – Read/Write			
7	ADIN12_HIGH_ALARM	ADIN2 – ADIN1 was above ADIN12_MAX_TH; 1 = ADIN2 – ADIN1 was high, 0 = ADIN2 – ADIN1 has not been high	0
6	ADIN12_LOW_ALARM	ADIN2 – ADIN1 was below ADIN12_MIN_TH; 1 = ADIN2 – ADIN1 was low, 0 = ADIN2 – ADIN1 has not been low	0
5	ADIN34_HIGH_ALARM	ADIN4 – ADIN3 was above ADIN34_MAX_TH; 1 = ADIN4 – ADIN3 was high, 0 = ADIN4 – ADIN3 has not been high	0
4	ADIN34_LOW_ALARM	ADIN4 – ADIN3 was below ADIN34_MIN_TH; 1 = ADIN4 – ADIN3 was low, 0 = ADIN4 – ADIN3 has not been low	0
3	ADIO12_HIGH_ALARM	ADIO2 – ADIO1 was above ADIO12_MAX_TH; 1 = ADIO2 – ADIO1 was high, 0 = ADIO2 – ADIO1 has not been high	0
2	ADIO12_LOW_ALARM	ADIO2 – ADIO1 was below ADIO12_MIN_TH; 1 = ADIO2 – ADIO1 was low, 0 = ADIO2 – ADIO1 has not been low	0
1	ADIO34_HIGH_ALARM	ADIO4 – ADIO3 was above ADIO34_MAX_TH; 1 = ADIO4 – ADIO3 was high, 0 = ADIO4 – ADIO3 has not been high	0
0	ADIO34_LOW_ALARM	ADIO4 – ADIO3 was below ADIO34_MIN_TH; 1 = ADIO4 – ADIO3 was low, 0 = ADIO4 – ADIO3 has not been low	0

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Table 10. CONTROL Registers (0x0A-0x0B) – Read/Write

BIT	NAME	OPERATION	DEFAULT
CONTROL_1 (0x0A) – Read/Write			
7	ON	Turns MOSFET on and off; 1 = turn MOSFET on, 0 = turn MOSFET off	1
6	DVDT	Enables dV/dt inrush control during startup; 1 = enabled, 0 = disabled	1
5	THERM_TMR	Turns 2µa TMR pull-down off; 1 = TMR pull-down turned off, 0 = TMR pull-down turned on	0
4	FET_BAD_TURN_OFF	Turns MOSFET off following a FET_BAD_FAULT; 1 = turn MOSFET off, 0 = keep MOSFET on	1
3	PWRGD_RESET_ CNTRL	Configures power good reset; 1 = reset by V_{OUT} low, 0 = reset by MOSFET off	1
2	PGIO2_ACLB	Configures PGIO2; 1 = PGIO2 as inverted output for active current limit engagement after startup; 0 = normal PGIO2 function configured by 0x10 bit[3:2]	0
1	MASS_WRITE_ ENABLE	Enables mass write to all LTC4284S on the I^2C bus; 1 = enabled, 0 = disabled	1
0	PAGE_READ_WRITE_ ENABLE	Enables I^2C page read/write protocols; 1 = enabled, 0 = disabled	1
CONTROL_2 (0x0B) – Read/Write			
7	EXT_FAULT_RETRY	Enables auto-retry following an EXT_FAULT; 1 = unlimited retries, 0 = no retry (latch-off)	0
6	PGI_RETRY	Enables auto-retry following a PGI_FAULT; 1 = unlimited retries, 0 = no retry (latch-off)	0
5:4	FET_BAD_RETRY	Configures auto-retry following a FET_BAD_FAULT and MOSFET turn off **FET_BAD_RETRY [5:4]** / **Number of Retries** 00 / 0 (Latch-Off) 01 / 1 10 / 7 11 / Unlimited	00
3:2	OC_RETRY	Configures auto-retry following an OC_FAULT **OC_RETRY [3:2]** / **Number of Retries** 00 / 0 (Latch-Off) 01 / 1 10 / 7 11 / Unlimited	00
1	UV_RETRY	Enables auto-retry following a UV_FAULT; 1 = unlimited retries, 0 = no retry (latch-off)	1
0	OV_RETRY	Enables auto-retry following an OV_FAULT; 1 = unlimited retries, 0 = no retry (latch-off)	1

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Table 11. CONFIG Registers (0x0D-0x0F) – Read/Write

<table>
<tr><th>BIT</th><th>NAME</th><th>OPERATION</th><th>DEFAULT</th></tr>
<tr><td colspan="4">CONFIG_1 (0x0D) – Read/Write</td></tr>
<tr><td>7:4</td><td>ILIM</td><td>Configures V_{ILIM} and $V_{ILIM(FAST)}$
<table>
<tr><th>ILIM [7:4]</th><th>V_{ILIM} [mV]</th><th>$V_{ILIM(FAST)}$ [mV]</th></tr>
<tr><td>0000</td><td>15</td><td>30</td></tr>
<tr><td>0001</td><td>16</td><td>32</td></tr>
<tr><td>0010</td><td>17</td><td>34</td></tr>
<tr><td>0011</td><td>18</td><td>36</td></tr>
<tr><td>0100</td><td>19</td><td>38</td></tr>
<tr><td>0101</td><td>20</td><td>40</td></tr>
<tr><td>0110</td><td>21</td><td>42</td></tr>
<tr><td>0111</td><td>22</td><td>44</td></tr>
<tr><td>1000</td><td>23</td><td>46</td></tr>
<tr><td>1001</td><td>24</td><td>48</td></tr>
<tr><td>1010</td><td>25</td><td>50</td></tr>
<tr><td>1011</td><td>26</td><td>52</td></tr>
<tr><td>1100</td><td>27</td><td>54</td></tr>
<tr><td>1101</td><td>28</td><td>56</td></tr>
<tr><td>1110</td><td>29</td><td>58</td></tr>
<tr><td>1111</td><td>30</td><td>60</td></tr>
</table></td><td>0000</td></tr>
<tr><td>3:2</td><td>FB</td><td>Configures current limit foldback factor for startup and normal operation
<table>
<tr><th>FB [3:2]</th><th>Foldback Factor, α [% V_{ILIM}]</th></tr>
<tr><td>00</td><td>100 (foldback disabled)</td></tr>
<tr><td>01</td><td>50</td></tr>
<tr><td>10</td><td>20</td></tr>
<tr><td>11</td><td>10</td></tr>
</table></td><td>11</td></tr>
<tr><td>1</td><td>FB_DIS</td><td>Disables foldback after startup; 1 = disabled, 0 = enabled. Foldback during startup is not affected</td><td>0</td></tr>
<tr><td>0</td><td>LPFB</td><td>Enables load power foldback after startup; 1 = enabled, 0 = disabled</td><td>0</td></tr>
<tr><td colspan="4">CONFIG_2 (0x0E) – Read/Write</td></tr>
<tr><td>7:6</td><td>VDTH</td><td>Configures DRAIN voltage threshold for starting FET bad fault filtering timer, $V_{D,FET(TH)}$
<table>
<tr><th>VDTH [7:6]</th><th>$V_{D,FET(TH)}$ [mV]</th></tr>
<tr><td>00</td><td>72</td></tr>
<tr><td>01</td><td>102</td></tr>
<tr><td>10</td><td>143</td></tr>
<tr><td>11</td><td>203</td></tr>
</table></td><td>11</td></tr>
</table>

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BIT	NAME	OPERATION	DEFAULT
5:4	FTBD_DL	Configures FET_Bad fault filtering timer delay, $t_{DL(FETBAD)}$	00
		FTBD_DL [5:4] / **$t_{DL(FETBAD)}$ [s]**: 00 / 0.256; 01 / 0.512; 10 / 1.02; 11 / 2.05	
3:1	COOLING_DL	Configures cooling delay preceding each auto-retry following OC_FAULT, FET_BAD_FAULT or EXT_FAULT, $t_{DL(RTRY)}$	000
		COOLING_DL [3:1] / **$t_{DL(RTRY)}$ [s]**: 000 / 0.512; 001 / 1.02; 010 / 2.05; 011 / 4.10; 100 / 8.19; 101 / 16.4; 110 / 32.8; 111 / 65.5	
0	PORB	Resets to 0 upon power-on reset. Write this bit to 1 to use it as power-on reset indicator: 1 = power-on reset has not occurred, 0 = power-on reset occurred	0

CONFIG_3 (0x0F) – Read/Write

BIT	NAME	OPERATION	DEFAULT
7	EXTFLT_TURN_OFF	Turns MOSFET off following an external fault; 1 = turn MOSFET off, 0 = keep MOSFET on	0
6	VPWR_SELECT	Selects voltage for ADC power multiplication; 1 = selects DRNS (attenuated drain voltage for MOSFET power), 0 = selects RTNS (attenuated input voltage for input power)	0
5	FAST_I2C_EN	Enables fast I^2C mode; 1 = fast I^2C enabled, 0 = fast I^2C disabled	0
4:3	BC	Configures bit rate of single-wire broadcast mode, f_{BC}	00
		BC [4:3] / **f_{BC} [kbit/s]**: 00 / 2048; 01 / 512; 10 / 128 (Not available for 8-bit ADC); 11 / 32 (Not available for 8-bit ADC)	
2	TICK_OVERFLOW_ ALERT	Enables alert when tick counter overflows; 1 = alert enabled, 0 = alert disabled	0
1	METER_OVERFLOW_ ALERT	Enables alert when energy meter overflows; 1 = alert enabled, 0 = alert disabled	0
0	INTEGRATE_I	Enables integration of current; 1 = integrate current, 0 = integrate power	0

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Table 12. PGIO_CONFIG Registers (0x10:0x11) – Read/Write

<table>
<tr><th>BIT</th><th>NAME</th><th>OPERATION</th><th>DEFAULT</th></tr>
<tr><td colspan="4">PGIO_CONFIG_1 (0x10) – Read/Write</td></tr>
<tr><td>7:6</td><td>PGIO4_CONFIG</td><td>Configures behavior of PGIO4 pin
<table><tr><th>PGIO4_CONFIG [7:6]</th><th>PGIO4</th></tr><tr><td>00</td><td>EXT_FAULT#</td></tr><tr><td>01</td><td>EXT_FAULT</td></tr><tr><td>10</td><td>General purpose output</td></tr><tr><td>11</td><td>General purpose input</td></tr></table></td><td>00</td></tr>
<tr><td>5:4</td><td>PGIO3_CONFIG</td><td>Configures behavior of PGIO3 pin
<table><tr><th>PGIO3_CONFIG [5:4]</th><th>PGIO3</th></tr><tr><td>00</td><td>PGI#</td></tr><tr><td>01</td><td>PGI</td></tr><tr><td>10</td><td>General purpose output</td></tr><tr><td>11</td><td>General purpose input</td></tr></table></td><td>00</td></tr>
<tr><td>3:2</td><td>PGIO2_CONFIG</td><td>Configures behavior of PGIO2 pin
<table><tr><th>PGIO2_CONFIG [3:2]</th><th>PGIO2</th></tr><tr><td>00</td><td>Power Good 2#</td></tr><tr><td>01</td><td>Power Good 2</td></tr><tr><td>10</td><td>General purpose output</td></tr><tr><td>11</td><td>General purpose input</td></tr></table></td><td>00</td></tr>
<tr><td>1:0</td><td>PGIO1_CONFIG</td><td>Configures behavior of PGIO1 pin
<table><tr><th>PGIO1_CONFIG [1:0]</th><th>PGIO1</th></tr><tr><td>00</td><td>Power Good 1#</td></tr><tr><td>01</td><td>Power Good 1</td></tr><tr><td>10</td><td>General purpose output</td></tr><tr><td>11</td><td>General purpose input</td></tr></table></td><td>00</td></tr>
<tr><td colspan="4">PGIO_CONFIG_2 (0x11) – Read/Write</td></tr>
<tr><td>7</td><td>PGIO4_OUT</td><td>Output data bit to PGIO4 pin when configured as general purpose output</td><td>0</td></tr>
<tr><td>6</td><td>PGIO3_OUT</td><td>Output data bit to PGIO3 pin when configured as general purpose output</td><td>0</td></tr>
<tr><td>5</td><td>PGIO2_OUT</td><td>Output data bit to PGIO2 pin when configured as general purpose output</td><td>0</td></tr>
<tr><td>4</td><td>PGIO1_OUT</td><td>Output data bit to PGIO1 pin when configured as general purpose output</td><td>0</td></tr>
<tr><td>3</td><td>ADC_CONV_ALERT</td><td>Enables alert when ADC finishes making a conversion; 1 = enable alert, 0 = disable alert</td><td>0</td></tr>
<tr><td>2:0</td><td>ADC</td><td>Configures ADC resolution and conversion rate
<table><tr><th>ADC [2:0]</th><th>ADC Resolution [Bits]</th><th>ADC Conversion Rate f_{CONV} [Hz]</th><th>Sampling Clock Frequency f_S [kHz]</th></tr><tr><td>000</td><td>8</td><td>996</td><td>512</td></tr><tr><td>010</td><td>10</td><td>125</td><td>256</td></tr><tr><td>100</td><td>12</td><td>15.6</td><td>128</td></tr><tr><td>110</td><td>14</td><td>3.91</td><td>128</td></tr><tr><td>xx1</td><td>16</td><td>0.977</td><td>128</td></tr></table></td><td>100</td></tr>
</table>

APPLICATIONS INFORMATION

Table 13. ADIO_CONFIG Register (0x12) – Read/Write

BIT	NAME	OPERATION	DEFAULT
7	ADIO4_CONFIG	Configures behavior of ADIO4 pin; 1 = general purpose input, 0 = general purpose output	1
6	ADIO3_CONFIG	Configures behavior of ADIO3 pin; 1 = general purpose input, 0 = general purpose output	1
5	ADIO2_CONFIG	Configures behavior of ADIO2 pin; 1 = general purpose input, 0 = general purpose output	1
4	ADIO1_CONFIG	Configures behavior of ADIO1 pin; 1 = general purpose input, 0 = general purpose output	1
3	ADIO4_OUT	Output data bit to ADIO4 pin when configured as general purpose output	0
2	ADIO3_OUT	Output data bit to ADIO3 pin when configured as general purpose output	0
1	ADIO2_OUT	Output data bit to ADIO2 pin when configured as general purpose output	0
0	ADIO1_OUT	Output data bit to ADIO1 pin when configured as general purpose output	0

Table 14. ADC_SELECT Registers (0x13-0x14) – Read/Write

BIT	NAME	OPERATION	DEFAULT
ADC_SELECT_1 (0x13) – Read/Write			
7	ADIO4_SELECT	Selects ADIO4 as input for ADC measurement; 1 = selected, 0 = not selected	1
6	ADIO3_SELECT	Selects ADIO3 as input for ADC measurement; 1 = selected, 0 = not selected	1
5	ADIO2_SELECT	Selects ADIO2 as input for ADC measurement; 1 = selected, 0 = not selected	1
4	ADIO1_SELECT	Selects ADIO1 as input for ADC measurement; 1 = selected, 0 = not selected	1
3	ADIN4_SELECT	Selects ADIN4 as input for ADC measurement; 1 = selected, 0 = not selected	1
2	ADIN3_SELECT	Selects ADIN3 as input for ADC measurement; 1 = selected, 0 = not selected	1
1	ADIN2_SELECT	Selects ADIN2 as input for ADC measurement; 1 = selected, 0 = not selected	1
0	ADIN1_SELECT	Selects ADIN1 as input for ADC measurement; 1 = selected, 0 = not selected	1
ADC_SELECT_2 (0x14) – Read/Write			
7	ADIO34_SELECT	Selects ADIO4 – ADIO3 as input for ADC measurement; 1 = selected, 0 = not selected	0
6	ADIO12_SELECT	Selects ADIO2 – ADIO1 as input for ADC measurement; 1 = selected, 0 = not selected	0
5	ADIN34_SELECT	Selects ADIN4 – ADIN3 as input for ADC measurement; 1 = selected, 0 = not selected	0
4	ADIN12_SELECT	Selects ADIN2 – ADIN1 as input for ADC measurement; 1 = selected, 0 = not selected	0
3	SENSE2_SELECT	Selects $SENSE2^+$ – $SENSE2^-$ as input for ADC measurement; 1 = selected, 0 = not selected	1
2	SENSE1_SELECT	Selects $SENSE1^+$ – $SENSE1^-$ as input for ADC measurement; 1 = selected, 0 = not selected	1
1	DRAIN_SELECT	Selects DRAIN as input for ADC measurement; 1 = selected, 0 = not selected	1
0	DRNS_SELECT	Selects DRNS as input for ADC measurement; 1 = selected, 0 = not selected	1

Table 15. FAULT_ALERT Register (0x15) – Read/Write

BIT	NAME	OPERATION	DEFAULT
7	EXT_FAULT_ALERT	Enables alert for external fault; 1 = enable alert, 0 = disable alert	0
6	FET_SHORT_ALERT	Enables alert for FET short fault; 1 = enable alert, 0 = disable alert	0
5	POWER_FAILED_ ALERT	Enables alert for power failed fault; 1 = enable alert, 0 = disable alert	0
4	PGI_ALERT	Enables alert for PGI fault; 1 = enable alert, 0 = disable alert	0
3	FET_BAD_ALERT	Enables alert for FET bad fault; 1 = enable alert, 0 = disable alert	0
2	OC_ALERT	Enables alert for overcurrent fault; 1 = enable alert, 0 = disable alert	0
1	UV_ALERT	Enables alert for undervoltage fault; 1 = enable alert, 0 = disable alert	0
0	OV_ALERT	Enables alert for overvoltage fault; 1 = enable alert, 0 = disable alert	0

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Table 16. ADC_ALERT Registers (0x16-0x1A) – Read/Write

BIT	NAME	OPERATION	DEFAULT
ADC_ALERT_1 (0x16) – Read/Write			
7	EN#_CHANGED_ALERT	Enables alert when EN# pin changed state; 1 = enable alert, 0 = disable alert	0
6	EEPROM_WRITTEN_ALERT	Enables alert when EEPROM is written through I^2C; 1 = enable alert, 0 = disable alert	0
5	SENSE_HIGH_ALERT	Enables alert when $ADC^+ – ADC^–$ was above SENSE_MAX_TH; 1 = enable alert, 0 = disable alert	0
4	SENSE_LOW_ALERT	Enables alert when $ADC^+ – ADC^–$ was below SENSE_MIN_TH; 1 = enable alert, 0 = disable alert	0
3	VPWR_HIGH_ALERT	Enables alert when VPWR was above VPWR_MAX_TH; 1 = enable alert, 0 = disable alert	0
2	VPWR_LOW_ALERT	Enables alert when VPWR was below VPWR_MIN_TH; 1 = enable alert, 0 = disable alert	0
1	POWER_HIGH_ALERT	Enables alert when POWER was above POWER_MAX_TH; 1 = enable alert, 0 = disable alert	0
0	POWER_LOW_ALERT	Enables alert when POWER was below POWER_MIN_TH; 1 = enable alert, 0 = disable alert	0
ADC_ALERT_2 (0x17) – Read/Write			
7	ADIN1_HIGH_ALERT	Enables alert when ADIN1 was above ADIN1_MAX_TH; 1 = enable alert, 0 = disable alert	0
6	ADIN1_LOW_ALERT	Enables alert when ADIN1 was below ADIN1_MIN_TH; 1 = enable alert, 0 = disable alert	0
5	ADIN2_HIGH_ALERT	Enables alert when ADIN2 was above ADIN2_MAX_TH; 1 = enable alert, 0 = disable alert	0
4	ADIN2_LOW_ALERT	Enables alert when ADIN2 was below ADIN2_MIN_TH; 1 = enable alert, 0 = disable alert	0
3	ADIN3_HIGH_ALERT	Enables alert when ADIN3 was above ADIN3_MAX_TH; 1 = enable alert, 0 = disable alert	0
2	ADIN3_LOW_ALERT	Enables alert when ADIN3 was below ADIN3_MIN_TH; 1 = enable alert, 0 = disable alert	0
1	ADIN4_HIGH_ALERT	Enables alert when ADIN4 was above ADIN4_MAX_TH; 1 = enable alert, 0 = disable alert	0
0	ADIN4_LOW_ALERT	Enables alert when ADIN4 was below ADIN4_MIN_TH; 1 = enable alert, 0 = disable alert	0
ADC_ALERT_3 (0x18) – Read/Write			
7	ADIO1_HIGH_ALERT	Enables alert when ADIO1 was above ADIO1_MAX_TH; 1 = enable alert, 0 = disable alert	0
6	ADIO1_LOW_ALERT	Enables alert when ADIO1 was below ADIO1_MIN_TH; 1 = enable alert, 0 = disable alert	0
5	ADIO2_HIGH_ALERT	Enables alert when ADIO2 was above ADIO2_MAX_TH; 1 = enable alert, 0 = disable alert	0
4	ADIO2_LOW_ALERT	Enables alert when ADIO2 was below ADIO2_MIN_TH; 1 = enable alert, 0 = disable alert	0
3	ADIO3_HIGH_ALERT	Enables alert when ADIO3 was above ADIO3_MAX_TH; 1 = enable alert, 0 = disable alert	0
2	ADIO3_LOW_ALERT	Enables alert when ADIO3 was below ADIO3_MIN_TH; 1 = enable alert, 0 = disable alert	0
1	ADIO4_HIGH_ALERT	Enables alert when ADIO4 was above ADIO4_MAX_TH; 1 = enable alert, 0 = disable alert	0
0	ADIO4_LOW_ALERT	Enables alert when ADIO4 was below ADIO4_MIN_TH; 1 = enable alert, 0 = disable alert	0

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BIT	NAME	OPERATION	DEFAULT
ADC_ALERT_4 (0x19) – Read/Write			
7	DRNS_HIGH_ALERT	Enables alert when DRNS was above DRNS_MAX_TH; 1 = enable alert, 0 = disable alert	0
6	DRNS_LOW_ALERT	Enables alert when DRNS was below DRNS_MIN_TH; 1 = enable alert, 0 = disable alert	0
5	DRAIN_HIGH_ALERT	Enables alert when DRAIN was above DRAIN_MAX_TH; 1 = enable alert, 0 = disable alert	0
4	DRAIN_LOW_ALERT	Enables alert when DRAIN was below DRAIN_MIN_TH; 1 = enable alert, 0 = disable alert	0
3	SENSE1_HIGH_ALERT	Enables alert when $SENSE1^+ – SENSE1^-$ was above SENSE1_MAX_TH; 1 = enable alert, 0 = disable alert	0
2	SENSE1_LOW_ALERT	Enables alert when $SENSE1^+ – SENSE1^-$ was below SENSE1_MIN_TH; 1 = enable alert, 0 = disable alert	0
1	SENSE2_HIGH_ALERT	Enables alert when $SENSE2^+ – SENSE2^-$ was above SENSE2_MAX_TH; 1 = enable alert, 0 = disable alert	0
0	SENSE2_LOW_ALERT	Enables alert when $SENSE2^+ – SENSE2^-$ was below SENSE2_MIN_TH; 1 = enable alert, 0 = disable alert	0
ADC_ALERT_5 (0x1A) – Read/Write			
7	ADIN12_HIGH_ALERT	Enables alert when ADIN2 – ADIN1 was above ADIN12_MAX_TH; 1 = enable alert, 0 = disable alert	0
6	ADIN12_LOW_ALERT	Enables alert when ADIN2 – ADIN1 was below ADIN12_MIN_TH; 1 = enable alert, 0 = disable alert	0
5	ADIN34_HIGH_ALERT	Enables alert when ADIN4 – ADIN3 was above ADIN34_MAX_TH; 1 = enable alert, 0 = disable alert	0
4	ADIN34_LOW_ALERT	Enables alert when ADIN4 – ADIN3 was below ADIN34_MIN_TH; 1 = enable alert, 0 = disable alert	0
3	ADIO12_HIGH_ALERT	Enables alert when ADIO2 – ADIO1 was above ADIO12_MAX_TH; 1 = enable alert, 0 = disable alert	0
2	ADIO12_LOW_ALERT	Enables alert when ADIO2 – ADIO1 was below ADIO12_MIN_TH; 1 = enable alert, 0 = disable alert	0
1	ADIO34_HIGH_ALERT	Enables alert when ADIO4 – ADIO3 was above ADIO34_MAX_TH; 1 = enable alert, 0 = disable alert	0
0	ADIO34_LOW_ALERT	Enables alert when ADIO4 – ADIO3 was below ADIO34_MIN_TH; 1 = enable alert, 0 = disable alert	0

Table 17. ENERGY Registers (0x7A-0x7F) – Read/Write

BIT	NAME	OPERATION	DEFAULT
47:0	ENERGY	Data of metered energy	0x0000_0000_0000

Table 18. TICK_COUNTER Registers (0x80-0x83) – Read/Write

BIT	NAME	OPERATION	DEFAULT
31:0	TICK_COUNTER	Counts number of ADC conversion cycles that power measurements have been accumulated in the energy meter	0x0000_0000

Table 19. METER_CONTROL Register (0x84) – Read/Write

BIT	NAME	OPERATION	DEFAULT
7	METER_RESET	Resets energy meter and tick counter until cleared; 1 = reset, 0 = reset cleared	0
6	METER_HALT	Halts energy meter and tick counter from accumulating; 1 = halted, 0 = not halted	0
5	TICK_OVERFLOW	Tick counter has overflowed; 1 = overflowed, 0 = not overflowed	0
4	METER_OVERFLOW	Energy meter accumulator has overflowed; 1 = overflowed, 0 = not overflowed	0
3	ALERT_GENERATED	Latched to 1 when an alert is generated and can only be cleared via I^2C; 1 = alert generated, 0 = alert has not been generated	0
2	EE_LOCK	EEPROM lock status, read only; 1 = EEPROM is factory locked, 0 = EEPROM is not factory locked	0
1:0	Reserved	Read only, always returns 0	00

APPLICATIONS INFORMATION

Table 20. ADC_SNAPSHOT Register (0x85) — Read/Write

BIT	NAME	OPERATION	DEFAULT
7:4	SNAPSHOT_SEL	Selects one of the 16 ADC auxiliary inputs for snapshot measurement	0000
3	ADC_HALT	Enables ADC snapshot mode; 1 = snapshot, 0 = continuous conversion	0
2:0	Reserved	Read only, always returns 0	000

SNAPSHOT_SEL [7:4]	Auxiliary ADC Input
0000	ADIN1
0001	ADIN2
0010	ADIN3
0011	ADIN4
0100	ADIO1
0101	ADIO2
0110	ADIO3
0111	ADIO4
1000	DRNS
1001	DRAIN
1010	$SENSE1^+ – SENSE1^-$
1011	$SENSE2^+ – SENSE2^-$
1100	ADIN2 – ADIN1
1101	ADIN4 – ADIN3
1110	ADIO2 – ADIO1
1111	ADIO4 – ADIO3

Table 21. FAULT_LOG_CONTROL Register (0x90) – Read/Write

BIT	NAME	OPERATION	DEFAULT
7	FAULT_LOG_ENABLE	Enables logging fault registers and ADC data into EEPROM upon a fault; this bit can only be cleared using I^2C; 1 = fault log enabled, 0 = fault log disabled	0
6	FAULT_LOG_UNLOCK	Allows clearing of FAULT_LOG_START and FAULT_LOG_DONE bits to re-enable fault log following a previous fault log; 1 = clearing allowed, 0 = clearing not allowed	0
5	FAULT_LOG_START	Indicates a fault log is started; I^2C can not set this bit but can clear it; 1 = fault log started, 0 = fault log has not been started	0
4	FAULT_LOG_DONE	Indicates a fault log is completed; I^2C can not set this bit but can clear it; 1 = fault log completed, 0 = fault log has not been completed	0
3	FAULT_LOG_ALERT	Enables alert when a fault log is completed; 1 = enable alert, 0 = disable alert	0
2:0	Reserved	Read only, always returns 0	000

APPLICATIONS INFORMATION

Table 22. Registers Recorded to EEPROM During Fault Log

REGISTER NAME	REGISTER ADDRESS	EEPROM ADDRESS	DATA LENGTH (BYTES)	DESCRIPTION
FAULT	0x04	0xA4	1	System fault
ADC_ALARM_LOG	0x05-0x09	0xA5-0xA9	5	ADC measurement alarms
SENSE	0x41	0xE1	1	MSB byte of most recent ADC output for $ADC^+ – ADC^–$
SENSE_MIN	0x42	0xE2	1	MSB byte of minimum ADC output for $ADC^+ – ADC^–$
SENSE_MAX	0x43	0xE3	1	MSB byte of maximum ADC output for $ADC^+ – ADC^–$
VPWR	0x44	0xE4	1	MSB byte of most recent ADC output for VPWR voltage
VPWR_MIN	0x45	0xE5	1	MSB byte of minimum ADC output for VPWR voltage
VPWR_MAX	0x46	0xE6	1	MSB byte of maximum ADC output for VPWR voltage

Table 23. REBOOT Register (0xA2) – Read/Write

BIT	NAME	OPERATION	DEFAULT
7	RBT_EN	Controls auto-reboot; 1 = reboot after delay $t_{DL(RBT)}$, 0 = no reboot. When set to 1, this bit remains 1 after reboot is done. Clear it before issuing the next reboot command	0
6:4	RBT_DL	Configures delay for auto-reboot, $t_{DL(RBT)}$, after the REBOOT bit is set to 1	000
3:2	Reserved	Read only, always returns 0	00
1	DELAY_STATUS	Reboot and cooling delay status; 1 = device is going through a reboot or cooling delay or in latch-off, 0 = reboot or cooling delay has expired or has not been initiated	0
0	WP_STATUS	WP pin status; 1 = WP is high, 0 = WP pin is low	0

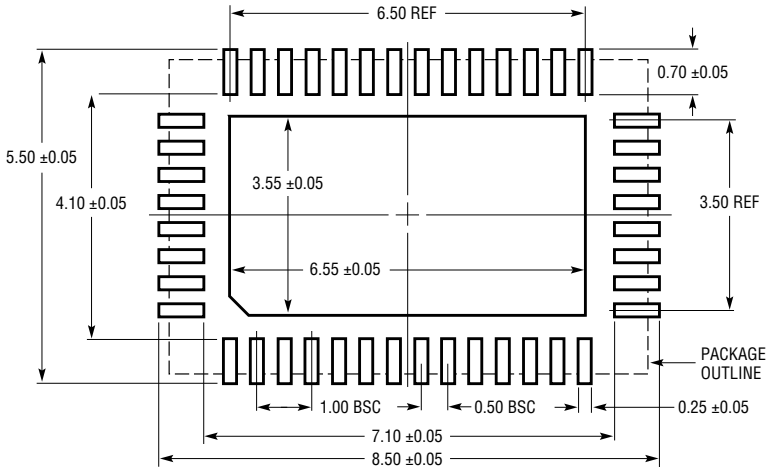
RBT_DL [6:4]	$t_{DL(RBT)}$ [s]
000	0.512
001	1.02
010	2.05
011	4.10
100	8.19
101	16.4
110	32.8
111	65.5

Table 24. Mapping between Faults/Alarms and Alert Masks

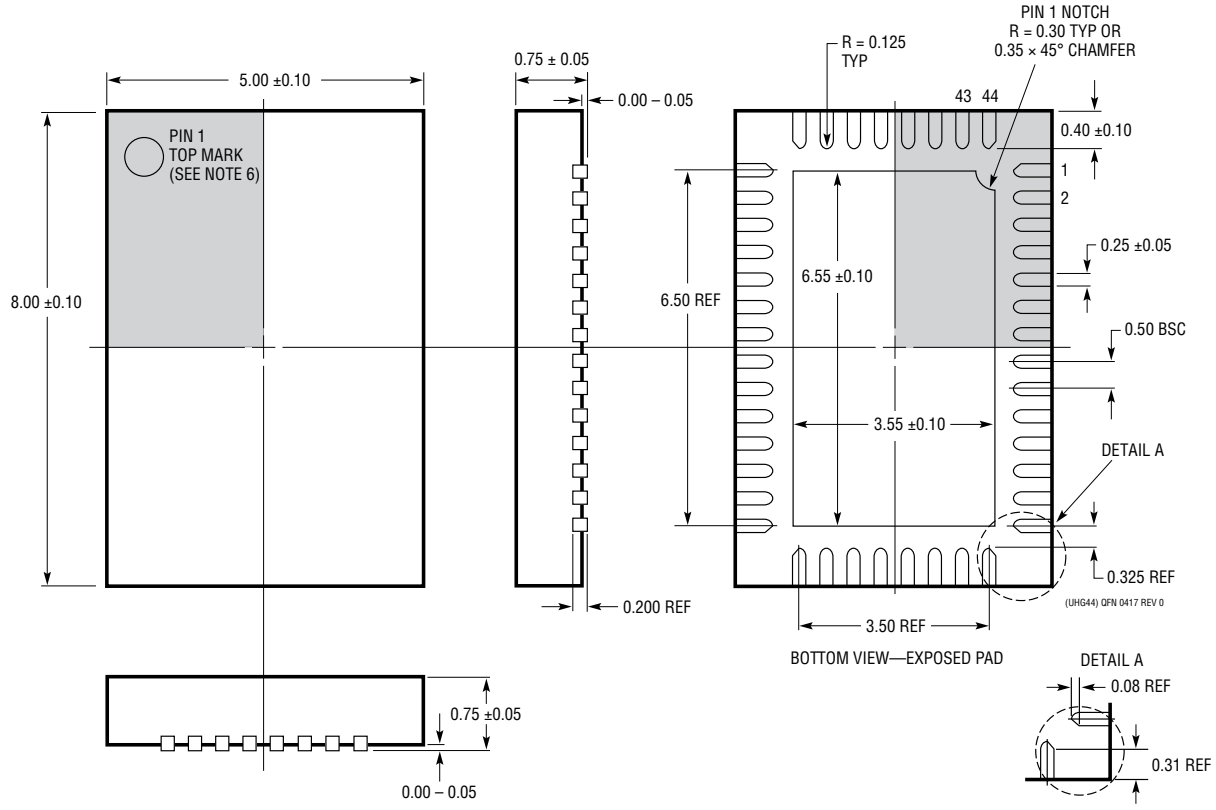
FAULT/ALARM	ALERT MASK
FAULT 0x04 [7:0]	FAULT_ALERT 0x15 [7:0]
ADC_ALARM_LOG_1 0x05 [7:0]	ADC_ALERT_1 0x16 [7:0]
ADC_ALARM_LOG_2 0x06 [7:0]	ADC_ALERT_2 0x17 [7:0]
ADC_ALARM_LOG_3 0x07 [7:0]	ADC_ALERT_3 0x18 [7:0]
ADC_ALARM_LOG_4 0x08 [7:0]	ADC_ALERT_4 0x19 [7:0]
ADC_ALARM_LOG_5 0x09 [7:0]	ADC_ALERT_5 0x1A [7:0]
METER_CONTROL 0x84[4:3]	CONFIG_3 0x0F [2:1]
ADC Conversion Completed	PGIO_CONFIG_2 0x11 [3]
EEPROM Fault Log Completed	FAULT_LOG_CONTROL 0x90 [3]

PACKAGE DESCRIPTION

UHG Package
44-Lead Plastic QFN (5mm × 8mm)
(Reference LTC DWG # 05-08-1581 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	01/20	Added patent number 10263414.	1
		Changed RTN to V_Z resistor value from 1W to 0.25W in figure.	1 ,19, 32, 34, 36
		Changed all register names with RTNS reference to VPWR (i.e. RTNS_MIN changed to VPWR_MIN).	62, 63, 65, 69, 76, 79
		Corrected bit number for METER_CONTROL Reserved register. Added METER_CONTROL EE_LOCK register bit.	77

TYPICAL APPLICATION

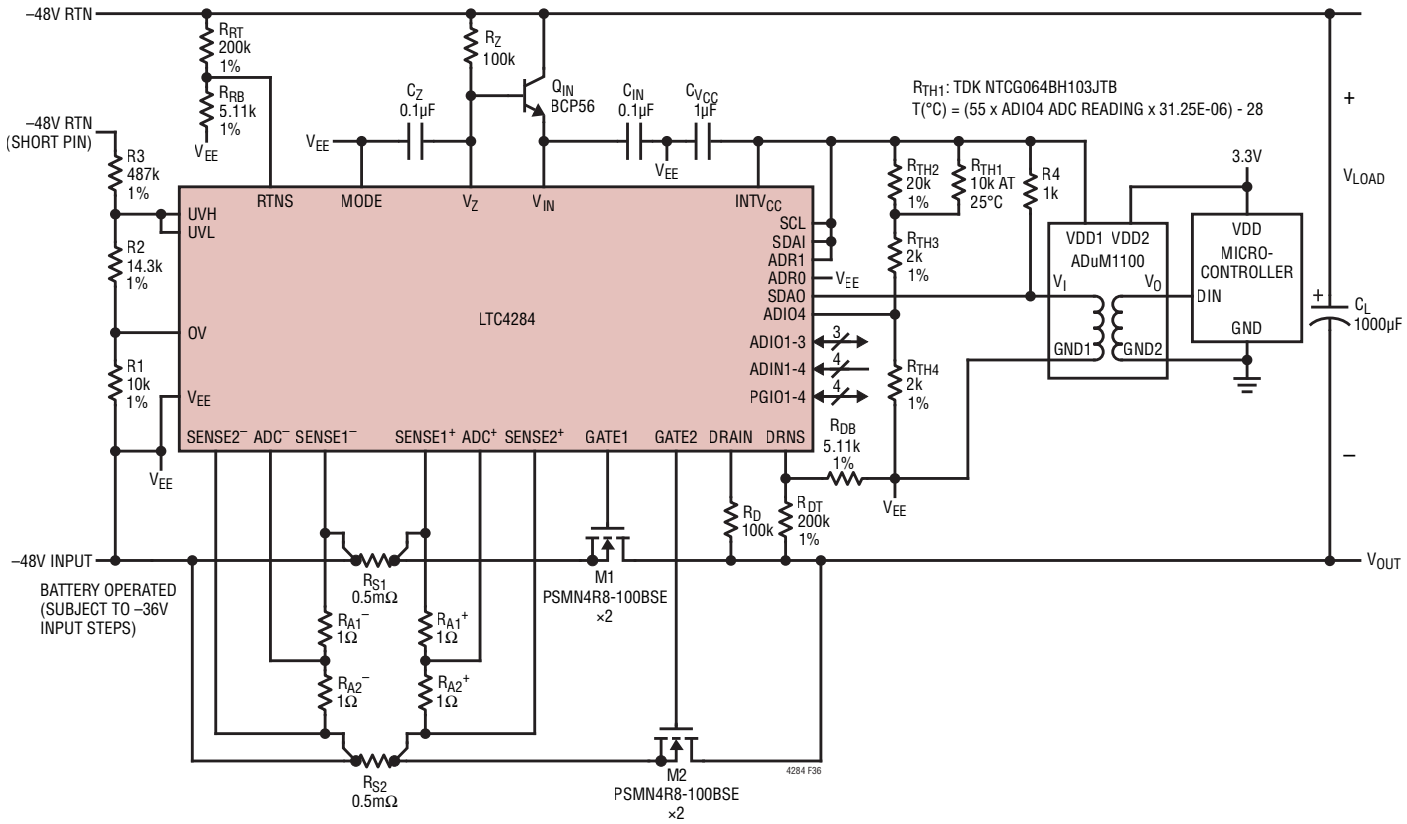


Figure 36. –48V/1200W Hot Swap Controller Monitoring System Status, Faults, Currents, Voltages, Power and Temperature and Transmitting Data at 2MBit/s in Single-Wire Broadcast Mode

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC4283	–48V Hot Swap Controller with Energy Monitor	SOA Timer, 8-Bit to 16-Bit ADC Monitors Current, Voltage, Power and Energy, Internal EEPROM, I²C or Single-Wire Broadcast
LTC4261/LT4261-2	–48V Hot Swap Controller with ADC and I²C	dV/dt Startup Inrush, 10-Bit ADC Monitors Voltages and Current, I²C or Single-Wire Broadcast, Two Sequenced Power Good Outputs, Supplies from –12V
ADM1075	–48V Hot Swap Controller with PMBus	12-Bit ADC Monitors Current, Voltage, Power and Energy
LTC4282/LTC4281	High Current Positive Voltage Hot Swap Controller with I²C Compatible Monitoring	Dual/Single Gate Drive, 12-Bit or 16-Bit ADC Monitors Current, Voltage, Power and Energy, Internal EEPROM, I²C, Supplies from 2.9V to 33V
LT4250L/LT4250H	–48V Hot Swap Controller in SO-8	Active Current Limiting, Supplies from –18V to –80V
LTC4251/LTC4251-1	–48V Hot Swap Controller in SOT-23	Fast Active Current Limiting, supplies from –15V
LTC4252-1/LTC4252-2/ LTC4252A-1/LTC4252A-2	–48V Hot Swap Controller in MS8	Fast Active Current Limiting, Supplies from –15V, ±1% UV/OV (LTC4252A)
LTC4253	–48V Hot Swap Controller with Sequencer	Fast Current Limiting with Three Sequenced Power Good Outputs, Supplies from –15V
LTC4260	Positive High Voltage Hot Swap Controller	With I²C and 8-Bit ADC, Supplies from 8.5V to 80V
LTC4371	Negative Voltage Diode-OR Controller	Controls Two N-Channel MOSFETs, 220ns Turn-Off
LTC4151	High Voltage Current and Voltage Monitor	Operates from 7V to 80V, with I²C and 12-Bit ADC