

# KAF-0261

## 512 (H) x 512 (V) Full Frame CCD Image Sensor

### Description

The KAF-0261 Image Sensor is a high performance, charge coupled device (CCD) designed for a wide range of image sensing applications.

The sensor incorporates true two-phase CCD technology, simplifying the support circuits required to drive the sensor as well as reducing dark current without compromising charge capacity. The sensor also utilizes the TRUESENSE Transparent Gate Electrode to improve sensitivity compared to the use of a standard front side illuminated polysilicon electrode.

Selectable on-chip output amplifiers allow operation to be optimized for different imaging needs: Low Noise (when using the high-sensitivity output) or Maximum Dynamic Range (when using the low-sensitivity output).

The low dark current of the KAF-0261 makes this device suitable for low light imaging applications without sacrificing charge capacity.



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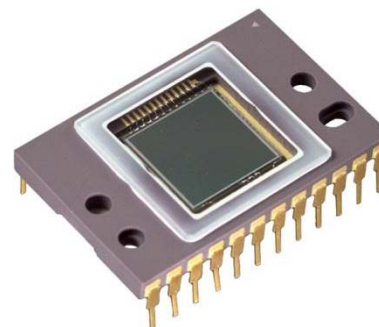


Figure 1. KAF-0261 CCD Image Sensor

Table 1. GENERAL SPECIFICATIONS

Parameter	Typical Value
Architecture	Full Frame CCD
Number of Active Pixels	512 (H) x 512 (V)
Pixel Size	20 $\mu\text{m}$ (H) x 20 $\mu\text{m}$ (V)
Active Image Size	10.2 mm (H) x 10.2 mm (V)
Chip Size	11.3 mm (H) x 11.6 mm (V)
Optical Fill Factor	100%
Output Sensitivity High Sensitivity Output High Dynamic Range Output	10 $\mu\text{V}$ /electron 2.0 $\mu\text{V}$ /electron
Saturation Signal High Sensitivity Output High Dynamic Range	200,000 electrons 500,000 electrons
Readout Noise (1 MHz)	22 electrons rms
Dark Current (25°C, Accumulation Mode)	< 30 pA/cm <sup>3</sup>
Dark Current Doubling Rate	6°C
Dynamic Range (Sat Sig/Dark Noise) High Sensitivity Output	83 dB
High Dynamic Range Output Range	87 dB
Quantum Efficiency (450, 550, 650 nm)	35%, 55%, 58%
Maximum Data Rate High Sensitivity Output High Dynamic Range Output	5 MHz 2 MHz
Transfer Efficiency	> 0.99997
Package	CERDIP Package
Cover Glass	Clear or AR coated, 2 sides

### Features

- True Two Phase Full Frame Architecture
- TRUESENSE Transparent Gate Electrode for High Sensitivity
- 100% Fill Factor
- Low Dark Current
- User-selectable Outputs Allow either Low Noise or High Dynamic Range Operation
- Single Readout Register
- These Devices are Pb-Free and are RoHS Compliant

### Applications

- Scientific Imaging

# KAF-0261

**Table 2. ORDERING INFORMATION**

Catalog Number	Product Name	Description	Marking Code
4H0808	KAF-0261-AAA-CD-BA	Monochrome, No Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Standard Grade	KAF-0261-AAA S/N
4H0809	KAF-0261-AAA-CD-AE	Monochrome, No Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Engineering Sample	
4H0810	KAF-0261-AAA-CP-BA	Monochrome, No Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Standard Grade	
4H0811	KAF-0261-AAA-CP-AE	Monochrome, No Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Engineering Sample	
4H0081	KEK-4H0081-KAF-0261-12-5	Evaluation Board (Complete Kit)	N/A

See Application Note 'Product Naming Convention' for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at [www.truesenseimaging.com](http://www.truesenseimaging.com).

Please address all inquiries and purchase orders to:

Truesense Imaging, Inc.  
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Rochester, New York 14615  
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# KAF-0261

## DEVICE DESCRIPTION

### Architecture

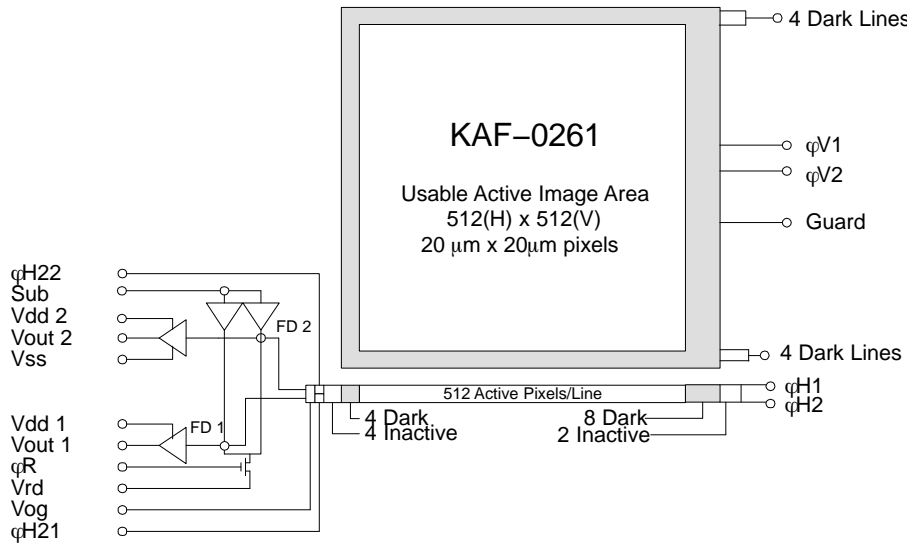


Figure 2. Block Diagram

Shaded areas represent 4 non-imaging pixels at the beginning and 8 non-imaging pixels at the end of each line. There are also 4 non-imaging lines at the top and bottom of each frame.

The KAF-0261 consists of one vertical (parallel) CCD shift register, one horizontal (serial) CCD shift register and a selectable high or low gain output amplifier (See Figure 1). Both registers incorporate two-phase buried channel CCD

technology. The vertical register consists of 20 μm x 20 μm photocopacitor sensing elements (pixels) that also serves as the transport mechanism. The pixels are arranged in a 512 (H) x 512 (V) array; an additional 12 columns (4 at the left and 8 at the right) and 8 rows (4 each at top and bottom) of non-imaging pixels are added as dark reference. There is no storage array, so this device must be synchronized with strobe illumination or shuttered during readout.

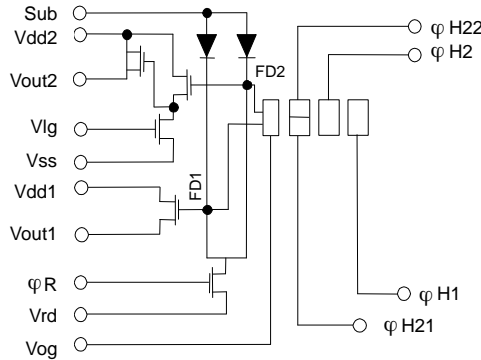


Figure 3. Output Structure

### Output Structure

The final gate of the horizontal register is split into two sections, φH21 and φH22. The split gate structure allows the user to select either of the two output amplifiers. To use the high dynamic range single-stage output (Vout1), φH22 is tied to a negative voltage to block charge transfer, and φH21 is tied to φH2 to transfer charge. To use the high sensitivity two-stage output (Vout2), φH21 is tied to a negative voltage and φH22 is tied to φH2. The charge packets are then dumped onto the appropriate floating diffusion output node

whose potential varies linearly with the quantity of charge in each packet. The amount of potential change is determined by the simple expression  $V_{fd} = Q/C_{fd}$ .

The translation from electrons to voltages is called the output sensitivity or charge-to-voltage conversion. After the output has been sensed off-chip, the reset clock (φR) removes the charge from the floating diffusion via the reset drain (VRD). This, in turn, returns the floating diffusion potential to the reference level determined by the reset drain voltage.

## Image Acquisition

An image is acquired when incident light, in the form of photons, falls on the array of pixels in the vertical CCD register and creates electron-hole pairs (or simply electrons) within the silicon substrate. This charge is collected locally by the formation of potential wells created at each pixel site by induced voltages on the vertical register clock lines ( $\phi V1$ ,  $\phi V2$ ). These same clock lines are used to implement the transport mechanism as well. The amount of charge collected at each pixel is linearly dependent on light level and exposure time and non-linearly dependent on wavelength until the potential well capacity is exceeded. At this point charge will 'bloom' into vertically adjacent pixels.

## Charge Transport

Integrated charge is transported to the output in a two-step process. Rows of charge are first shifted line by line into the horizontal CCD. 'Lines' of charge are then shifted to the output pixel by pixel. The timing diagram illustrated in

Figure 7 illustrates how the integration of charge is performed with  $\phi V1$  and  $\phi V2$  held low. Transfer to the horizontal CCD begins when  $\phi V1$  is brought high, causing charge from the  $\phi V1$  and  $\phi V2$  gates to combine under the  $\phi V1$  gate. The  $\phi V1$  and  $\phi V2$  gates are now reversed in polarity, causing the charge packets to 'spill' forward under the  $\phi V2$  gate of the next pixel. The falling edge of  $\phi V2$  also transfers the first line of charge into the horizontal CCD. A second phase transition places the charge packets under the  $\phi V1$  electrode of the next pixel. The sequence completes when  $\phi V1$  is brought low. Clocking of the vertical register in this way is known as accumulation mode clocking. Next, the horizontal CCD reads out the first line of charge using traditional complementary clocking (using  $\phi H1$  and  $\phi H2$  pins) as shown. The falling edge of  $\phi H2$  forces a charge packet over the output gate (OG) onto one of the output nodes (floating diffusion) which is buffered by the output amplifier. The cycle repeats until all lines are read.

DEVICE DESCRIPTION

Pin Description and Device Orientation

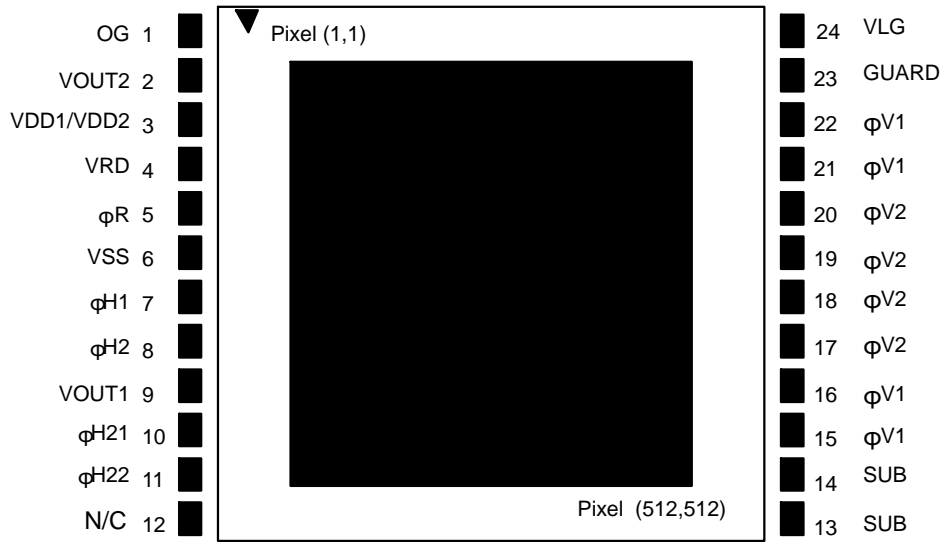


Figure 4. Pinout Diagram

Table 3. PIN DESCRIPTION

Pin	Name	Description
1	OG	Output Gate
2	VOUT2	Video Output from High Sensitivity Two-Stage
3	VDD1 / VDD2	Amplifier Supply for VOUT1 and VOUT2 Amplifiers
4	VRD	Reset Drain
5	$\phi R$	Reset Clock
6	VSS	Output Amplifier Return
7	$\phi H1$	Horizontal (Serial) CCD Clock – Phase 1
8	$\phi H2$	Horizontal (Serial) CCD Clock – Phase 2
9	VOUT1	Video Output from High Dynamic Range Single-Stage Amplifier
10	$\phi H21$	Last Horizontal (Serial) CCD Phase – Split Gate
11	$\phi H22$	Last Horizontal (Serial) CCD Phase – Split Gate

12	N/C	No Connection
13	VSUB	Substrate
14	VSUB	Substrate
15	$\phi V1$	Vertical (Parallel) CCD Clock – Phase 1
16	$\phi V1$	Vertical (Parallel) CCD Clock – Phase 1
17	$\phi V2$	Vertical (Parallel) CCD Clock – Phase 2
18	$\phi V2$	Vertical (Parallel) CCD Clock – Phase 2
19	$\phi V2$	Vertical (Parallel) CCD Clock – Phase 2
20	$\phi V2$	Vertical (Parallel) CCD Clock – Phase 2
21	$\phi V1$	Vertical (Parallel) CCD Clock – Phase 1
22	$\phi V1$	Vertical (Parallel) CCD Clock – Phase 1
23	GUARD	Guard Ring
24	VLG	First Stage Load Transistor Gate for Two-Stage

1. Pins 15, 16, 21, and 22 must be connected together – only one Phase 1–clock driver is required.
2. Pins 17, 18, 19, and 20 must be connected together – only one Phase 2–clock driver is required.

**IMAGING PERFORMANCE**

**Typical Operational Conditions**

All values apply to nominal operating conditions with the recommended timing. Correlated doubling sampling of the

output is assumed and recommended. Many units are expressed in electrons – to convert to voltage, multiply by the amplifier sensitivity.

**Specifications**

**Table 4. ELECTRO-OPTICAL**

Description	Symbol	Min	Typ	Max	Units	Notes	Verification Plan
Optical Fill Factor	FF		100		%		
Photoresponse Non-uniformity	PRNU			5	% rms	Full Array	die <sup>10</sup>
Quantum Efficiency (450, 550, 650 nm)	QE					See QE curve (Figure 7)	design <sup>11</sup>

**Table 5. CCD PARAMETERS COMMON TO BOTH OUTPUTS**

Description	Symbol	Min	Typ	Max	Units	Notes	Verification Plan
Sat. Signal – Vccd register	$N_{e^-sat}$	450	500		ke <sup>-</sup>	2	design <sup>11</sup>
Dark Current	Jd		15.3 400	30 750	pA/cm <sup>2</sup> e <sup>-</sup> /pixel/sec	25°C (mean of all pixels)	die <sup>10</sup>
Dark Current Doubling Temp	DCDR	5	6.3	7.5	°C		design <sup>11</sup>
Dark Signal Non-uniformity	DSNU			750	e <sup>-</sup> /pix/sec	4	die <sup>10</sup>
Charge Transfer Efficiency	CTE		.99997			5	die <sup>10</sup>
Photoresponse Non-linearity	PRNL		1	2	%	9	
Blooming Suppression	Bs		none				

**Table 6. CCD PARAMETERS SPECIFIC TO HIGH GAIN OUTPUT AMPLIFIER**

Description	Symbol	Min	Typ	Max	Units	Notes	Verification Plan
Output Sensitivity	Vout/Ne <sup>-</sup>		10		μV/electron		design <sup>11</sup>
Sat. Signal	$N_{e^-sat}$	180	200	240	ke <sup>-</sup>	1	design <sup>11</sup>
Total Sensor Noise	$n_{e^-total}$		13	20	e <sup>-</sup> rms	7	design <sup>11</sup>
Horizontal CCD Frequency	f <sub>H</sub>		2	5	MHz	6	design <sup>11</sup>
Dynamic Range	DR	79	83		dB	8	design <sup>11</sup>

**Table 7. CCD PARAMETERS SPECIFIC TO LOW GAIN (HIGH DYNAMIC RANGE) OUTPUT AMPLIFIER**

Description	Symbol	Min	Typ	Max	Units	Notes	Verification Plan
Output Sensitivity	Vout/Ne <sup>-</sup>		2		μV/electron		design <sup>11</sup>
Sat. Signal	$N_{e^-sat}$	550K	628K		ke <sup>-</sup>	3	design <sup>11</sup>
Total Sensor Noise	$n_{e^-total}$		22	30	e <sup>-</sup> rms	7	die <sup>10</sup>
Horizontal CCD Frequency	f <sub>H</sub>		0.5	2	MHz	6	design <sup>11</sup>
Dynamic Range	DR	85	87		dB	8	design <sup>11</sup>

- Point where the output saturates when operated with nominal voltages.
- Signal level at the onset of blooming in the vertical (parallel) CCD register.
- Maximum signal level at the output of the high dynamic range output. This signal level will only be achieved when binning pixels containing large signals.
- None of 16 sub arrays (128 x 128) exceed the maximum dark current specification.
- For 2 MHz data rate and T = 30°C to -40°C.
- Using maximum CCD frequency and/or minimum CCD transfer times may compromise performance.
- At T<sub>integration</sub> = 0; data rate = 1 MHz; temperature = -30°C.
- Uses 20LOG (N<sub>e<sup>-</sup>sat</sub> / n<sub>e<sup>-</sup>total</sub>) where N<sub>e<sup>-</sup>sat</sub> refers to the appropriate saturation signal.
- Worst case deviation from straight line fit, between 1% and 90% of Vsat.
- A parameter that is measured on every sensor during production testing.
- A parameter that is quantified during the design verification activity.

TYPICAL PERFORMANCE CURVES (QE)

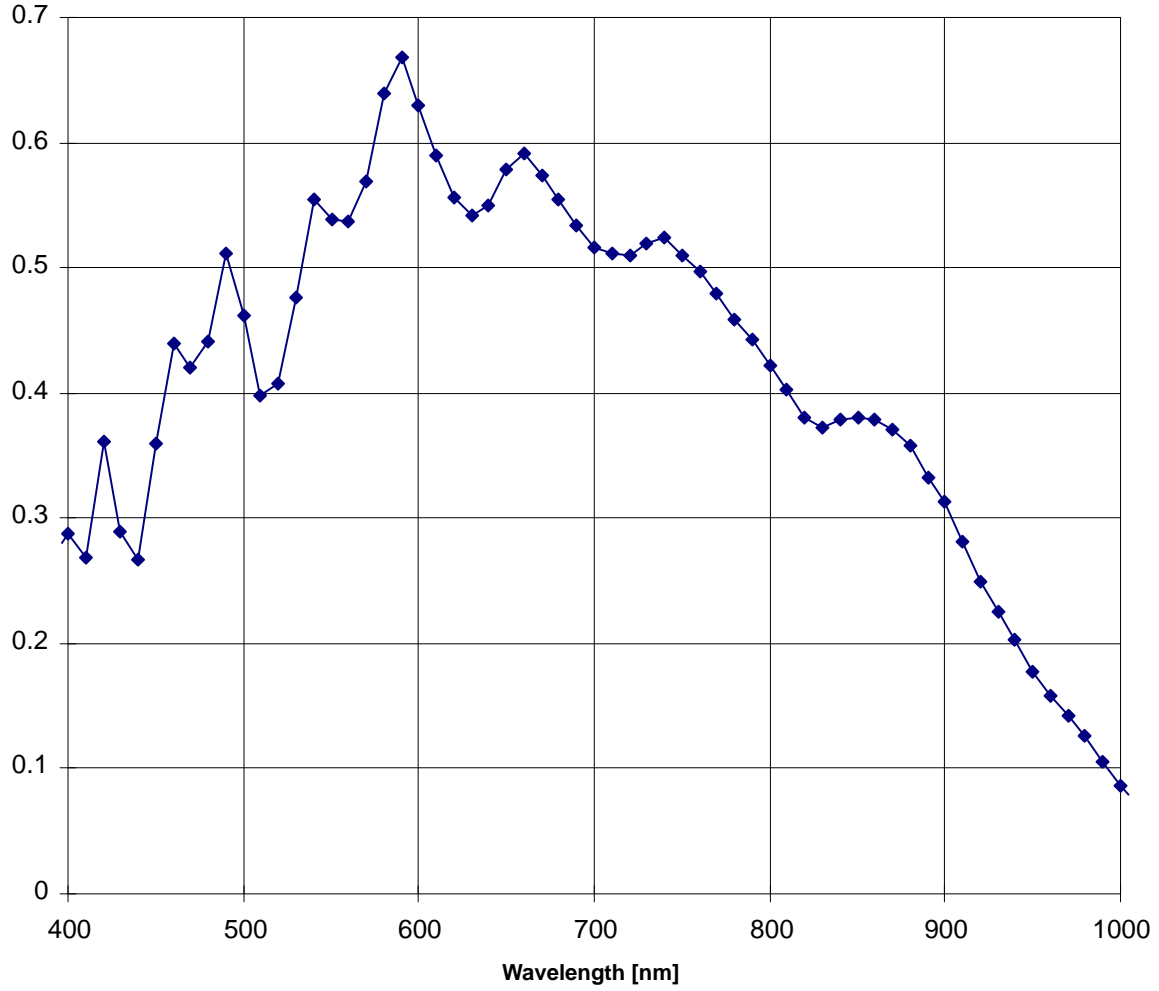


Figure 5. Typical Spectral Response

**DEFECT SPECIFICATIONS**

**Table 8. MAXIMUM DEFECT COUNTS**

Point Defect	Cluster Defect	Column Defect
10	4	0

*Dark Defects*

A pixel which deviates by more than 20% from neighboring pixels when illuminated to 70% of saturation

*Bright Defect*

A pixel whose dark current exceeds 4500 electrons/pixel/second at 25°C

*Cluster Defect*

A grouping of not more than 5 adjacent point defects

*Column Defect*

A grouping of point defects along a single column. (Dark Column)

A column that contains a pixel whose dark current exceeds 150,000 electrons/pixel/second at 25°C. (Bright Column)

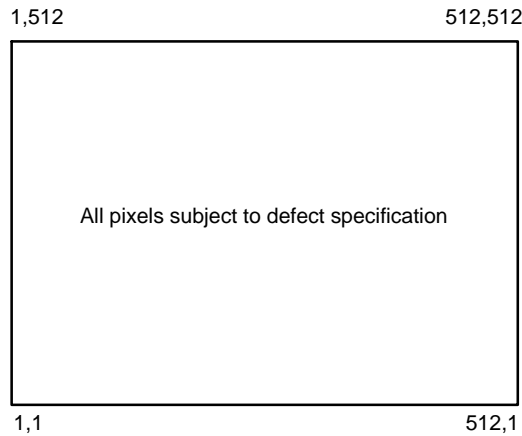
A column that does not exhibit the minimum charge capacity specification. (Low charge capacity)

A column that loses > 500 electrons when the array is illuminated to a signal level of 2000 electrons/pix. (Trap like defects)

*Neighboring Pixels*

The surrounding 128 x 128 pixels of ±64 columns/rows

Defects are separated by no less than 3 pixels in any one direction.



**Figure 6. Active Pixel Region**



## OPERATION

Table 9. ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Minimum	Maximum	Units	Notes
Voltage	All Clocks	-16	+16	V	1
Voltage	OG	0	+8	V	2
Voltage	VRD, VSS, VDD, GUARD	0	+20	V	2
Current	Output Bias Current (IDD)		10	mA	
Capacitance			10	pF	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Voltage between any two clocks or between any clock and Vsub.
2. Voltage with respect to Vsub.

**WARNING:** For maximum performance, built-in gate protection has been added only to the OG pin. These devices require extreme care during handling to prevent electrostatic discharge (ESD) induced damage. Devices are rated as Class 0 (<250 V per JESD22 Human Body Model test), or Class A (<200 V JESD22 Machine Model test).

Table 10. DC BIAS OPERATING CONDITIONS

Description	Symbol	Minimum	Nominal	Maximum	Units	Pin Impedance
Substrate	VSUB	0.0	0.0	0.0	V	Common
Output Amplifier Supply	VDD	15.0	+17.0	17.5	V	5 pF, 2 K $\Omega$ (Note 1)
Output Amplifier Return	VSS	1.4	+2.0	2.1	V	5 pF, 2 K $\Omega$
Reset Drain	VRD	11.5	+12	12.5	V	5 pF, 1 M $\Omega$
Output Gate	OG	4.0	4.5	5.0	V	5 pF, 10 M $\Omega$
Guard Ring	GUARD	9.0	+10.0	15.0	V	350 pF, 10 M $\Omega$
Load Gate	VLG	VSS - 1.0	VSS	VSS + 1.0	V	

1. Vdd = 17 volts for applications where the expected output voltage > 2.0 Volts. For applications where the expected useable output voltage is < 2 Volts Vdd can be reduced to 15 Volts.

## AC Operating Conditions

Table 11. CLOCK LEVELS

Description	Symbol	Level	Minimum	Nominal	Maximum	Units	Pin Impedance
Vertical Clock - Phase 1	$\phi V1$	Low	-10.2	-10.0	-9.0	V	13 nF, 10 M $\Omega$
Vertical Clock - Phase 1	$\phi V1$	High	0.0	0	2.0	V	
Vertical Clock - Phase 2	$\phi V2$	Low	-10.2	-10.0	-9.0	V	16 nF, 10 M $\Omega$
Vertical Clock - Phase 2	$\phi V2$	High	0.0	0	2.0	V	
Horizontal Clock - Phase 1	$\phi H1$	Low	-2.2	-2.0	-1.8	V	160 pF, 10 M $\Omega$
Horizontal Clock - Phase 1	$\phi H1$	High	7.8	+8.0	8.2	V	
Horizontal Clock - Phase 2	$\phi H2$	Low	-2.2	-2.0	-1.8	V	110 pF, 10 M $\Omega$
Horizontal Clock - Phase 2	$\phi H2$	High	7.8	+8.0	8.2	V	
Reset Clock	$\phi R$	Low	2.0	3.0	3.5	V	10 pF, 10 M $\Omega$
Reset Clock	$\phi R$	High		10.0		V	

Table 12. AMPLIFIER SELECTION

Description	Symbol	Level	Using the High Gain Output (Vout2)			Using the High Dynamic Range Output (Vout1)			Units	Pin Impedance
			Min	Nom	Max	Min	Nom	Max		
Horizontal Clock – Phase 1	$\phi H21$	Low	-4	$\phi H2$ low	$\phi H2$ low		$\phi H2$		V	10 pF, 10 M $\Omega$
Horizontal Clock – Phase 1	$\phi H21$	High	-4	$\phi H2$ low	$\phi H2$ low		$\phi H2$		V	
Horizontal Clock – Phase 2	$\phi H22$	Low		$\phi H2$		-4	$\phi H2$ low	$\phi H2$ low	V	10 pF, 10 M $\Omega$
Horizontal Clock – Phase 2	$\phi H22$	High		$\phi H2$		-4	$\phi H2$ low	$\phi H2$ low	V	

- When using Vout1  $\phi H21$  is clocked identically with  $\phi H2$  while  $\phi H22$  is held at a static level. When using Vout2  $\phi H21$  and  $\phi H22$  are exchanged so that  $\phi H22$  is identical to  $\phi H2$  and  $\phi H21$  is held at a static level. The static level should be the same voltage as  $\phi H2$  low.
- The AC and DC operating levels are for room temperature operation. Operation at other temperatures may require adjustments of these voltages. Pins shown with impedances greater than 1 M $\Omega$  are expected resistances. These pins are only verified to 1 M $\Omega$ .
- $\phi V1$ , 2 capacitances are accumulated gate oxide capacitance, and so are an over-estimate of the capacitance.
- This device is suitable for a wide range of applications requiring a variety of different operating conditions. Consult ON Semiconductor in those situations in which operating conditions meet or exceed minimum or maximum levels.

## Timing

Table 13. REQUIREMENTS AND CHARACTERISTICS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
$\phi H1$ , $\phi H2$ Clock Frequency	$f_H$		5	8	MHz	1, 2, 3
V1, V2 Clock Frequency	$f_V$		100	125	kHz	1, 2, 3
Pixel Period (1 Count)	$t_{pix}$	125	200		ns	
$\phi H1$ , $\phi H2$ Set-up Time	$t_{\phi HS}$	500	1000		ns	
$\phi V1$ , $\phi V2$ Clock Pulse Width	$t_{\phi V}$	4	5		$\mu s$	2
Reset Clock Pulse Width	$t_{\phi R}$	10	20		ns	4
Readout Time	$t_{readout}$	40	64		ms	5
Integration Time	$t_{int}$					6
Line Time	$t_{line}$	78	122		$\mu s$	7

- 50% duty cycle values.
- CTE may degrade above the nominal frequency.
- Rise and fall times (10/90% levels) should be limited to 5–10% of clock period. Crossover of register clocks should be between 40–60% of amplitude.
- $\phi R$  should be clocked continuously.
- $t_{readout} = (520 * t_{line})$
- Integration time ( $t_{int}$ ) is user specified. Longer integration times will degrade noise performance due to dark signal fixed pattern and shot noise.
- $t_{line} = (3 * t_{\phi V}) + t_{\phi HS} + 530 * t_{pix} + t_{pix}$

Normal Readout Timing

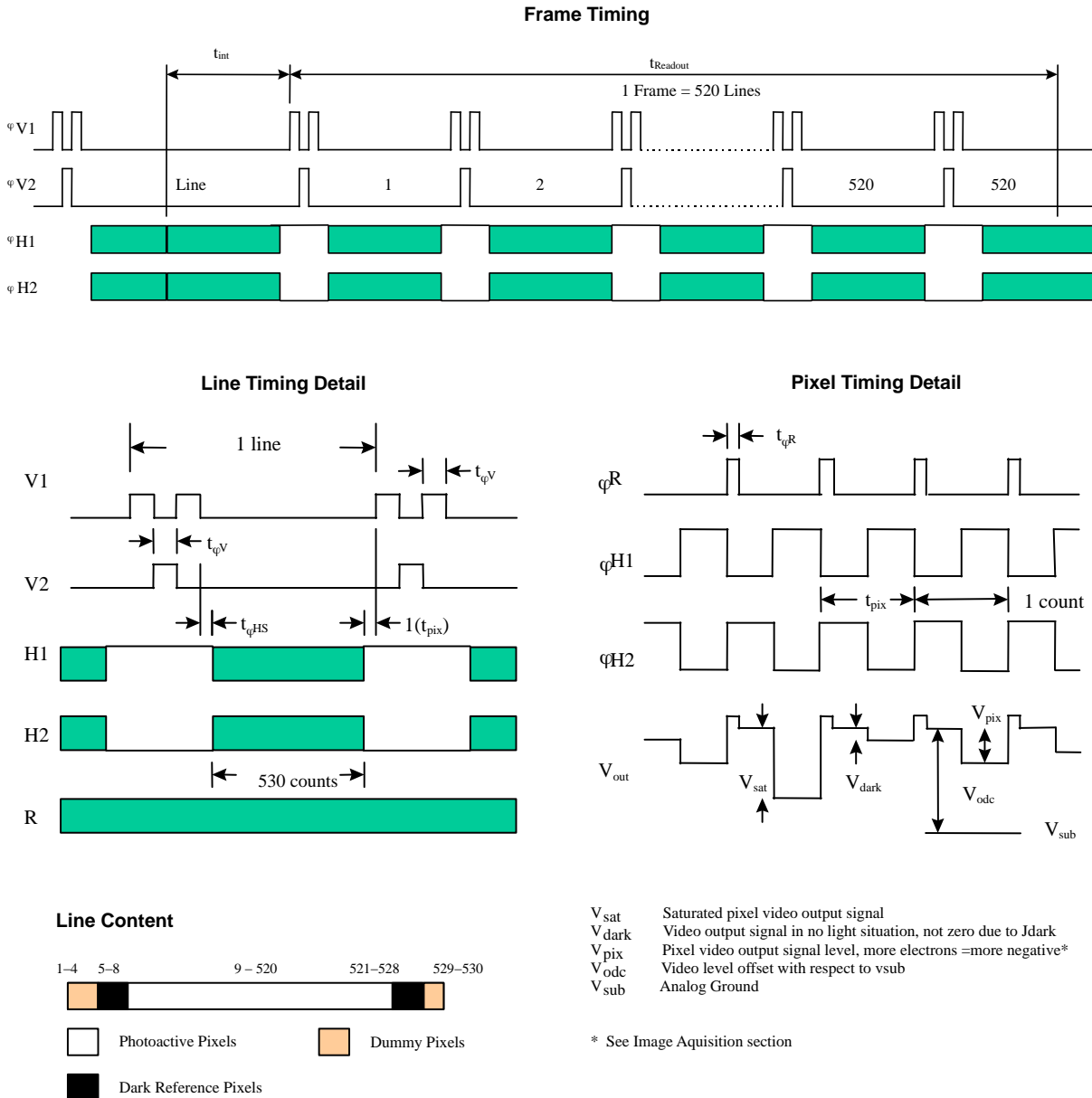


Figure 7. Timing Diagrams

NOTE: This device is suitable for a wide range of applications requiring a variety of different timing frequencies. Therefore, only maximum and minimum values are shown above. Consult ON Semiconductor in those situations, which require special consideration.

**STORAGE AND HANDLING****Table 14. STORAGE CONDITIONS**

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T <sub>ST</sub>	-100	+80	°C	At Device
Operating Temperature	T <sub>OP</sub>	-70	+50	°C	At Device

**ESD**

1. This device contains limited protection against Electrostatic Discharge (ESD). ESD events may cause irreparable damage to a CCD image sensor either immediately or well after the ESD event occurred. Failure to protect the sensor from electrostatic discharge may affect device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250 V per JESD22 Human Body Model test), or Class A (<200 V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note 'Image Sensor Handling Best Practices' for proper handling and grounding procedures. This application note also contains workplace recommendations to minimize electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

**Cover Glass Care and Cleanliness**

1. Avoid storage of the product in the presence of dust or corrosive agents or gases, as deterioration of lead solderability may occur. It is advised that the solderability of the device leads be assessed after an extended period of storage, over one year.
2. Touching the cover glass must be avoided.
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note 'Image Sensor Handling Best Practices'.

**Environmental Exposure**

1. Extremely bright light can potentially harm CCD image sensors. Do not expose to strong sunlight for long periods of time, as the color filters and/or microlenses may become discolored. In addition, long time exposures to a static high contrast scene should be avoided. Localized changes in response may occur from color filter/microlens aging. For Interline devices, refer to Application Note 'Using Interline CCD Image Sensors in High Intensity Visible lighting Conditions'.
2. Exposure to temperatures exceeding maximum specified levels should be avoided for storage and operation, as device performance and reliability may be affected.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity may affect device characteristics and may alter device performance and reliability, and therefore should be avoided.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases, as deterioration of lead solderability may occur. It is advised that the solderability of the device leads be assessed after an extended period of storage, over one year.

**Soldering Recommendations**

1. The soldering iron tip temperature is not to exceed 370°C. Higher temperatures may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating using a grounded 30 W soldering iron. Heat each pin for less than 2 seconds duration.

MECHANICAL INFORMATION

Completed Assembly

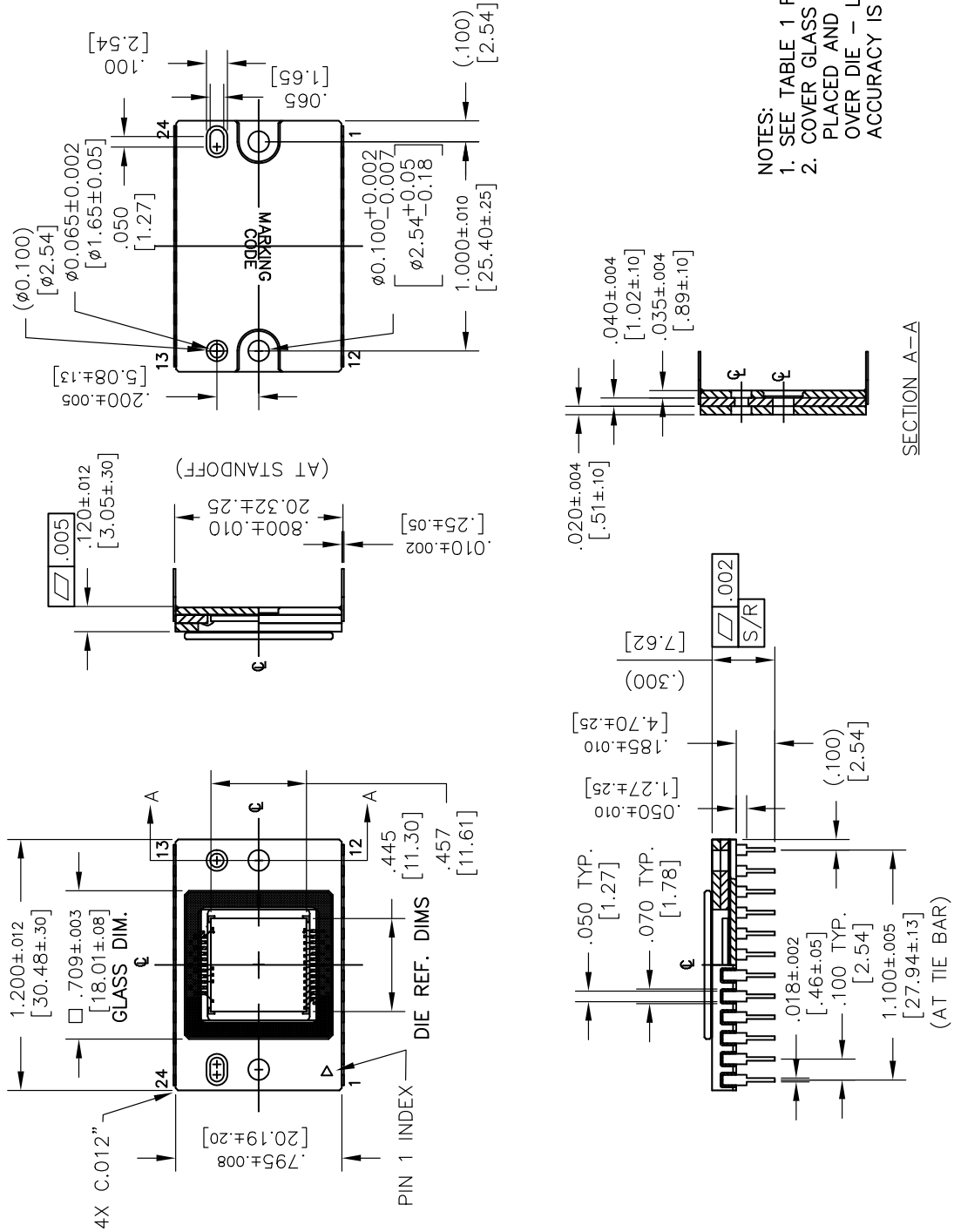


Figure 8. Completed Assembly (1 of 2)

# KAF-0261

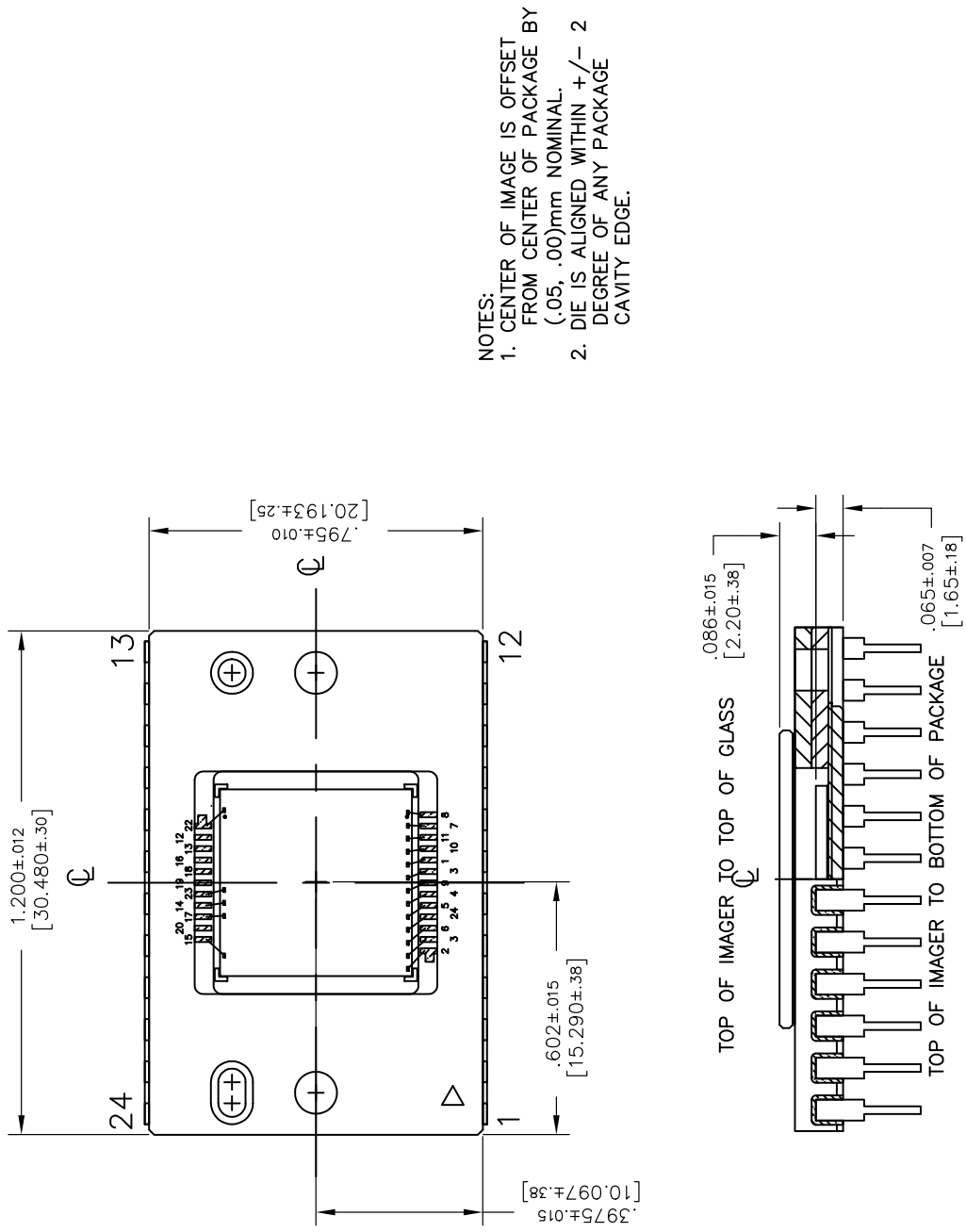


Figure 9. Completed Assembly (2 of 2)

## QUALITY ASSURANCE AND RELIABILITY

### Quality and Reliability

All image sensors conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and visual inspection and electrical testing at key points of the manufacturing process, using industry standard methods. Information concerning the quality assurance and reliability testing procedures and results are available from ON Semiconductor upon request. For further information refer to Application Note 'Quality and Reliability'.

### Replacement

All devices are warranted against failure in accordance with the 'Terms of Sale'. Devices that fail due to mechanical and electrical damage caused by the customer will not be replaced.

### Liability of the Supplier

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer. Product liability is limited to the cost of the defective item, as defined in the 'Terms of Sale'.

### Liability of the Customer

Damage from mishandling (scratches or breakage), electrostatic discharge (ESD), or other electrical misuse of the device beyond the stated operating or storage limits, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

### Test Data Retention


Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

### Mechanical

The device assembly drawing is provided as a reference. ON Semiconductor reserves the right to change any information contained herein without notice. All information furnished by ON Semiconductor is believed to be accurate.

## LIFE SUPPORT APPLICATION POLICY

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