# 12-Bit Monitor and Control System with Multichannel ADC, DACs, Temperature Sensor, and Current Sense

Data Sheet **AD7294**

## FEATURES

- 12-bit SAR ADC with 3 µs conversion time
  - 4 uncommitted analog inputs
    - Differential/single-ended
    - $V_{REF}$, 2 × $V_{REF}$ input ranges
  - 2 high-side current sense inputs
    - 5 V to 59.4 V operating range
    - 0.5% max gain error
    - ±200 mV input range
  - 2 external diode temperature sensor inputs
    - −55°C to +150°C measurement range
    - ±2°C accuracy
    - Series resistance cancellation
  - 1 internal temperature sensor
    - ±2°C accuracy
  - Built-in monitoring features
    - Minimum/maximum recorder for each channel
    - Programmable alert thresholds
    - Programmable hysteresis
  - Four 12-bit monotonic 15 V DACs
    - 5 V span, 0 V to 10 V offset
    - 8 µs settling time
    - 10 mA sink and source capability
    - Power-on resets (POR) to 0 V
  - Internal 2.5 V reference
  - 2-wire fast mode $I^2C$ interface
  - Temperature range: −40°C to +105°C
  - Package type: 64-lead TQFP or 56-lead LFCSP

## APPLICATIONS

- Cellular base stations
  - GSM, EDGE, UMTS, CDMA, TD-SCDMA, W-CDMA, WiMAX
- Point-to-multipoint and other RF transmission systems
- 12 V, 24 V, 48 V automotive applications
- Industrial controls

## GENERAL DESCRIPTION

The AD7294 contains all the functions required for general-purpose monitoring and control of current, voltage, and temperature integrated into a single-chip solution. The device includes low voltage (±200 mV) analog input sense amplifiers for current monitoring across shunt resistors, temperature sense inputs, and four uncommitted analog input channels multiplexed into a SAR analog-to-digital converter (ADC) with a 3 µs conversion time. A high accuracy internal reference is provided to drive both the digital-to-analog converter (DAC) and ADC. Four 12-bit DACs provide the outputs for voltage control. The AD7294 also includes limit registers for alarm functions. The device is designed on Analog Devices, Inc., high voltage DMOS process for high voltage compliance, 59.4 V on the current sense inputs, and up to a 15 V DAC output voltage.

The AD7294 is a highly integrated solution that offers all the functionality necessary for precise control of the power amplifier in cellular base station applications. In these types of applications, the DACs provide 12-bit resolution to control the bias currents of the power transistors. Thermal diode-based temperature sensors are incorporated to compensate for temperature effects. The ADC monitors the high-side current and temperature. All this functionality is provided in a 64-lead TQFP or a 56-lead LFCSP operating over a temperature range of −40°C to +105°C.

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**1/12—Rev. G to Rev. H**

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**5/10—Rev. C to Rev. D**

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**1/08—Revision 0: Initial Version**

# FUNCTIONAL BLOCK DIAGRAM

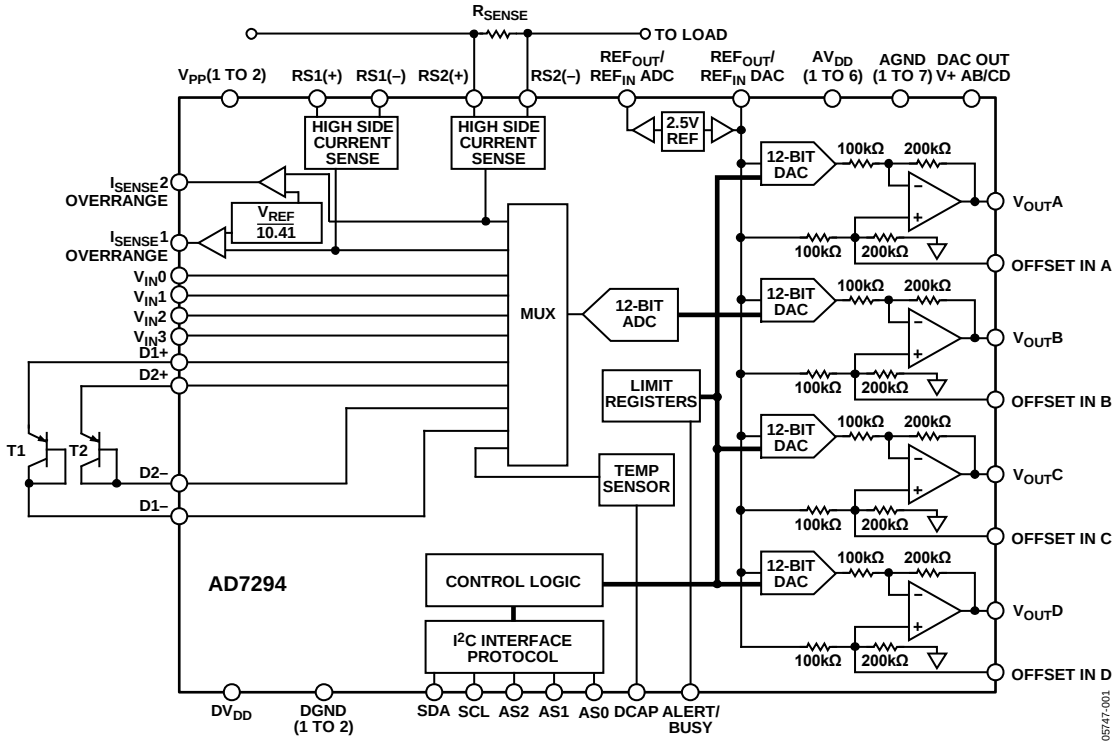


*Figure 1.*

# SPECIFICATIONS

## DAC SPECIFICATIONS

$AV_{DD}$ = $DV_{DD}$ = 4.5 V to 5.5 V, AGND = DGND = 0 V, internal 2.5 V reference; $V_{DRIVE}$ = 2.7 V to 5.5 V; $T_A$ =−40°C to +105°C, unless otherwise noted. DAC OUTV+ AB and DAC OUTV+ CD = 4.5 V to 16.5 V, OFFSET IN x is floating, therefore, the DAC output span = 0 V to 5 V.

**Table 1.**

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| ACCURACY | | | | | |
| Resolution | 12 | | | Bits | |
| Relative Accuracy (INL) | | ±1 | ±3 | LSB | |
| Differential Nonlinearity (DNL) | | ±0.3 | ±1 | LSB | Guaranteed monotonic |
| Zero-Scale Error | | 2.5 | 8 | mV | |
| Full-Scale Error of DAC and Output Amplifier | | | 15.5[1] | mV | DAC OUTV+ = 5.0 V |
| Full-Scale Error of DAC | | 2 | | mV | DAC OUTV+ = 15.0 V |
| Offset Error | | | ±8.575 | mV | Measured in the linear region, $T_A$ = −40°C to +105°C |
| | | | ±2 | mV | Measured in the linear region, $T_A$ = 25°C |
| Offset Error Temperature Coefficient | | ±5 | | ppm/°C | |
| Gain Error | | ±0.025 | ±0.155 | % FSR | |
| Gain Temperature Coefficient | | ±5 | | ppm/°C | |
| DAC OUTPUT CHARACTERISTICS | | | | | |
| Output Voltage Span | 0 | | $2 \times V_{REF}$ | V | 0 V to 5 V for a 2.5 V reference |
| Output Voltage Offset | 0 | | 10 | V | The output voltage span can be positioned in the 0 V to 15 V range; if the OFFSET IN x is left floating, the offset pin = $2/3 \times V_{REF}$ , giving an output of 0 V to $2 \times V_{REF}$ |
| Offset Input Pin Range | 0 | | 5 | | $V_{OUT} = 3\ V_{OFFSET} - 2 \times V_{REF} + V_{DAC}$ |
| DC Input Impedance[2] | | 75 | | kΩ | 100 kΩ to $V_{REF}$, and 200 kΩ to AGND, see Figure 48 |
| Output Voltage Settling Time[2] | | 8 | | µs | 1/4 to 3/4 change within 1/2 LSB, measured from last SCL edge |
| Slew Rate[2] | | 1.1 | | V/µs | |
| Short-Circuit Current[2] | | 40 | | mA | Full-scale current shorted to ground |
| Load Current[2] | | ±10 | | mA | Source and/or sink within 200 mV of supply |
| Capacitive Load Stability[2] | 10 | | | nF | $R_L = \infty$ |
| DC Output Impedance[2] | | 1 | | Ω | |
| REFERENCE | | | | | |
| Reference Output Voltage | 2.49 | 2.5 | 2.51 | V | ±0.4% maximum at 25°C, $AV_{DD}$ = $DV_{DD}$ = 4.5 V to 5.5 V |
| Reference Input Voltage Range | 0 | | $AV_{DD}$ − 2 | V | |
| Input Current | | 100 | 125 | µA | $V_{REF}$ = 2.5 V |
| Input Capacitance[2] | | 20 | | pF | |
| $V_{REF}$ Output Impedance[2] | | 25 | | Ω | |
| Reference Temperature Coefficient | | 10 | 25 | ppm/°C | |

[1] This value indicates that the DAC output amplifiers can output voltages 15.5 mV below the DAC OUTV+ supply. If higher DAC OUTV+ supply voltages are used, the full-scale error of the DAC is typically 2 mV with no load.
[2] Samples are tested during initial release to ensure compliance; they are not subject to production testing.

## ADC SPECIFICATIONS

$AV_{DD}$ = $DV_{DD}$ = 4.5 V to 5.5 V, AGND = DGND = 0 V, $V_{REF}$ = 2.5 V internal or external; $V_{DRIVE}$ = 2.7 V to 5.5 V; $V_{PP}$ = $AV_{DD}$ to 59.4 V; $T_A$ = −40°C to +105°C, unless otherwise noted.

**Table 2.**

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| DC ACCURACY | | | | | |
| Resolution | | 12 | | Bits | |
| Integral Nonlinearity (INL)[1] | | ±0.5 | ±1 | LSB | Differential mode |
| | | ±0.5 | ±1.5 | LSB | Single-ended or pseudo differential mode |
| Differential Nonlinearity (DNL)[1] | | ±0.5 | ±0.99 | LSB | Differential, single-ended, and pseudo differential modes |
| Single-Ended Mode | | | | | |
| Offset Error | | ±1 | ±7 | LSB | |
| Offset Error Match | | ±0.4 | | LSB | |
| Gain Error | | ±0.5 | ±2.5 | LSB | |
| Gain Error Match | | ±0.4 | | LSB | |
| Differential Mode | | | | | |
| Positive Gain Error | | ±1 | | LSB | |
| Positive Gain Error Match | | ±0.5 | | LSB | |
| Zero Code Error | | ±3 | | LSB | |
| Zero Code Error Match | | ±0.5 | | LSB | |
| Negative Gain Error | | ±1 | | LSB | |
| Negative Gain Error Match | | ±0.5 | | LSB | |
| CONVERSION RATE | | | | | |
| Conversion Time[2] | | 3 | | µs | |
| Autocycle Update Rate[2] | | 50 | | µs | |
| Throughput Rate | | | 22.22 | kSPS | $f_{SCL}$ = 400 kHz |
| ANALOG INPUT[3] | | | | | |
| Single-Ended Input Range | 0 | | $V_{REF}$ | V | 0 V to $V_{REF}$ mode |
| | 0 | | $2 \times V_{REF}$ | V | 0 V to $2 \times V_{REF}$ mode |
| Pseudo Differential Input Range: $V_{IN+} - V_{IN-}$[4] | 0 | | $V_{REF}$ | | 0 V to $V_{REF}$ mode |
| | 0 | | $2 \times V_{REF}$ | | 0 V to $2 \times V_{REF}$ mode |
| Fully Differential Input Range: $V_{IN+} - V_{IN-}$ | $-V_{REF}$ | | $+V_{REF}$ | | 0 V to $V_{REF}$ mode |
| | $-2 \times V_{REF}$ | | $+2 \times V_{REF}$ | | 0 V to $2 \times V_{REF}$ mode |
| Input Capacitance[2] | | 30 | | pF | |
| DC Input Leakage Current | | | ±1 | µA | |
| DYNAMIC PERFORMANCE | | | | | |
| Signal-to-Noise Ratio (SNR)[1] | | 73 | | dB | $f_{IN}$ = 10 kHz sine wave; differential mode |
| | | 72 | | dB | $f_{IN}$ = 10 kHz sine wave; single-ended and pseudo differential modes |
| Signal-to-Noise + Distortion (SINAD) Ratio[1] | | 71.5 | | dB | $f_{IN}$ = 10 kHz sine wave; differential mode |
| | | 72.5 | | dB | $f_{IN}$ = 10 kHz sine wave; single-ended and pseudo differential modes |
| Total Harmonic Distortion (THD)[1] | | −81 | | dB | $f_{IN}$ = 10 kHz sine wave; differential mode |
| | | −79 | | dB | $f_{IN}$ = 10 kHz sine wave; single-ended and pseudo differential modes |
| Spurious-Free Dynamic Range (SFDR)[1] | | −81 | | dB | $f_{IN}$ = 10 kHz sine wave; differential mode |
| | | −79 | | | $f_{IN}$ = 10 kHz sine wave; single-ended and pseudo differential modes |
| Channel-to-Channel Isolation[2] | | −90 | | dB | $f_{IN}$ = 10 kHz to 40 kHz |

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| TEMPERATURE SENSOR—INTERNAL | | | | | |
| Operating Range | −40 | | +105 | °C | |
| Accuracy | | | ±2 | °C | Internal temperature sensor, $T_A$ = −30°C to +90°C |
| | | | ±2.5 | °C | Internal temperature sensor, $T_A$ = −40°C to +105°C |
| Resolution | | 0.25 | | °C | LSB size |
| Update Rate | | 5 | | ms | |
| TEMPERATURE SENSOR—EXTERNAL | | | | | External transistor is 2N3906 |
| Operating Range | −55 | | +150 | °C | Limited by external diode |
| Accuracy | | | ±2 | °C | $T_A = T_{DIODE}$ = −40°C to +105°C |
| Resolution | | 0.25 | | °C | LSB size |
| Low Level Output Current Source[2] | | 8 | | µA | |
| Medium Level Output Current Source[2] | | 32 | | µA | |
| High Level Output Current Source[2] | | 128 | | µA | |
| Maximum Series Resistance ($R_S$) for External Diode[2] | | | 100 | Ω | For < ±0.5°C additional error, $C_P$ = 0, see Figure 31 |
| Maximum Parallel Capacitance ($C_P$) for External Diode[2] | | | 1 | nF | $R_S$ = 0, see Figure 30 |
| CURRENT SENSE | | | | | $V_{PP} = AV_{DD}$ to 59.4 V |
| $V_{PP}$ Supply Range | $AV_{DD}$ | | 59.4 | V | |
| Gain | 12.4375 | 12.5 | 12.5625 | | Gain of 12.5 gives a gain error = 0.5% maximum; delivers ±200 mV range with +2.5 V reference |
| RS(+)/RS(−) Input Bias Current | | 25 | 32 | µA | |
| CMRR/PSRR[2] | | 80 | | dB | Inputs shorted to $V_{PP}$ |
| Offset Error | | ±50 | ±340 | µV | |
| Offset Drift | | 1 | | µV/°C | |
| Amplifier Peak-To-Peak Noise[2] | | 400 | | µV | Referred to input |
| $V_{PP}$ Supply Current | | 0.18 | 0.25 | mA | $V_{PP}$ = 59.4 V |
| REFERENCE | | | | | |
| Reference Output Voltage | 2.49 | | 2.51 | V | ±0.2% maximum at 25°C only |
| Reference Input Voltage Range | 0.1 | | 4.1 | V | For four uncommitted ADCs |
| | 1 | | $AV_{DD}$ − 2 | | For current sense |
| DC Leakage Current | | | ±2 | µA | |
| $V_{REF}$ Output Impedance[2] | | 25 | | Ω | |
| Input Capacitance[2] | | 20 | | pF | |
| Reference Temperature Coefficient | | 10 | 25 | ppm/°C | |

[1] See the Terminology section for more details.
[2] Sampled during initial release to ensure compliance, not subject to production testing.
[3] $V_{IN+}$ or $V_{IN-}$ must remain within GND/$V_{DD}$.
[4] $V_{IN-}$ = 0 V for specified performance. For full input range on $V_{IN-}$, see Figure 40.

## GENERAL SPECIFICATIONS

$AV_{DD}$ = $DV_{DD}$ = 4.5 V to 5.5 V, AGND = DGND = 0 V, $V_{REF}$ = 2.5 V internal or external; $V_{DRIVE}$ = 2.7 V to 5.5 V; $V_{PP}$ = $AV_{DD}$ to 59.4 V; DAC OUTV+ AB and DAC OUTV+ CD = 4.5 V to 16.5 V; OFFSET IN x is floating, therefore, DAC output span = 0 V to 5 V; $T_A$ = −40°C to +105°C, unless otherwise noted.

**Table 3.**

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| LOGIC INPUTS | | | | | |
| Input High Voltage, $V_{IH}$ | 0.7 $V_{DRIVE}$ | | | V | SDA, SCL only |
| Input Low Voltage, $V_{IL}$ | | | 0.3 $V_{DRIVE}$ | V | SDA, SCL only |
| Input Leakage Current, $I_{IN}$ | | | ±1 | µA | |
| Input Hysteresis, $V_{HYST}$ | 0.05 $V_{DRIVE}$ | | | V | |
| Input Capacitance, $C_{IN}$ | | 8 | | pF | |
| Glitch Rejection | | 50 | | ns | Input filtering suppresses noise spikes of less than 50 ns |
| $I^2C$ Address Pins Maximum External Capacitance if Floating | | | 30 | pF | Tristate input |
| LOGIC OUTPUTS | | | | | |
| SDA, ALERT | | | | | SDA and ALERT/BUSY are open-drain outputs |
| Output Low Voltage, $V_{OL}$ | | | 0.4 | V | $I_{SINK}$ = 3 mA |
| | | | 0.6 | V | $I_{SINK}$ = 6 mA |
| Floating-State Leakage Current | | | ±1 | µA | |
| Floating-State Output Capacitance | | 8 | | pF | |
| $I_{SENSE}$ OVERRANGE | | | | | $I_{SENSE}$ OVERRANGE is a push-pull output |
| Output High Voltage, $V_{OH}$ | | | $V_{DRIVE}$ − 0.2 | V | $I_{SOURCE}$ = 200 µA for push-pull outputs |
| Output Low Voltage, $V_{OL}$ | | | 0.2 | V | $I_{SINK}$ = 200 µA for push-pull outputs |
| Overrange Setpoint | $V_{FS}$ | $V_{FS}$ × 1.2 | | mV | $V_{FS}$ = ±$V_{REF}$ ADC/12.5 |
| POWER REQUIREMENTS | | | | | |
| $V_{PP}$ | $AV_{DD}$ | | 59.4 | V | |
| $AV_{DD}$ | 4.5 | | 5.5 | V | |
| V(+) | 4.5 | | 16.5 | V | |
| $DV_{DD}$ | 4.5 | | 5.5 | V | Tie $DV_{DD}$ to $AV_{DD}$ |
| $V_{DRIVE}$ | 2.7 | | 5.5 | V | |
| $I_{DD}$ Dynamic | | 5.3 | 6.5 | mA | $AV_{DD}$ + $DV_{DD}$ + $V_{DRIVE}$, DAC outputs unloaded |
| DAC OUTV+ x, $I_{DD}$ | | 0.6 | 1.2 | mA | At midscale output voltage, DAC outputs unloaded |
| Power Dissipation | | 70 | 105 | mW | |
| Power-Down | | | | | |
| $I_{DD}$ | | 0.5 | 1 | µA | For each $AV_{DD}$ and $V_{DRIVE}$ |
| $DI_{DD}$ | | 1 | 16.5 | µA | |
| DAC OUTV+ x, $I_{DD}$ | | 35 | 60 | µA | |
| Power Dissipation | | | 2.5 | mW | |

## TIMING CHARACTERISTICS

### *I²C Serial Interface*

$AV_{DD}$ = $DV_{DD}$ = 4.5 V to 5.5 V, AGND = DGND = 0 V, $V_{REF}$ = 2.5 V internal or external; $V_{DRIVE}$ = 2.7 V to 5.5 V; $V_{PP}$ = $AV_{DD}$ to 59.4 V; DAC OUTV+ AB and DAC OUTV+ CD = 4.5 V to 16.5 V; OFFSET IN x is floating, therefore, DAC output span = 0 V to 5 V; $T_A$ = −40°C to +105°C, unless otherwise noted.

**Table 4.**

| Parameter[1] | Limit at $T_{MIN}$, $T_{MAX}$ | Unit | Description |
|---|---|---|---|
| $f_{SCL}$ | 400 | kHz max | SCL clock frequency |
| $t_1$ | 2.5 | µs min | SCL cycle time |
| $t_2$ | 0.6 | µs min | $t_{HIGH}$, SCL high time |
| $t_3$ | 1.3 | µs min | $t_{LOW}$, SCL low time |
| $t_4$ | 0.6 | µs min | $t_{HD,STA}$, start/repeated start condition hold time |
| $t_5$ | 100 | ns min | $t_{SU,DAT}$, data setup time |
| $t_6$ | 0.9 | µs max | $t_{HD,DAT}$, data hold time |
| | 0 | µs min | $t_{HD,DAT}$, data hold time |
| $t_7$ | 0.6 | µs min | $t_{SU,STA}$, setup time for repeated start |
| $t_8$ | 0.6 | µs min | $t_{SU,STO}$, stop condition setup time |
| $t_9$ | 1.3 | µs min | $t_{BUF}$, bus free time between a stop and a start condition |
| $t_{10}$ | 300 | ns max | $t_R$, rise time of SCL and SDA when receiving |
| | 0 | ns min | $t_R$, rise time of SCL and SDA when receiving (CMOS compatible) |
| $t_{11}$ | 300 | ns max | $t_F$, fall time of SDA when transmitting |
| | 0 | ns min | $t_F$, fall time of SDA when receiving (CMOS compatible) |
| | 300 | ns max | $t_F$, fall time of SCL and SDA when receiving |
| | $20 + 0.1C_b$[2] | ns min | $t_F$, fall time of SCL and SDA when transmitting |
| $C_b$ | 400 | pF max | Capacitive load for each bus line |

[1] See Figure 2.
[2] $C_b$ is the total capacitance in pF of one bus line. $t_R$ and $t_F$ are measured between 0.3 $DV_{DD}$ and 0.7 $DV_{DD}$.

### *Timing and Circuit Diagrams*

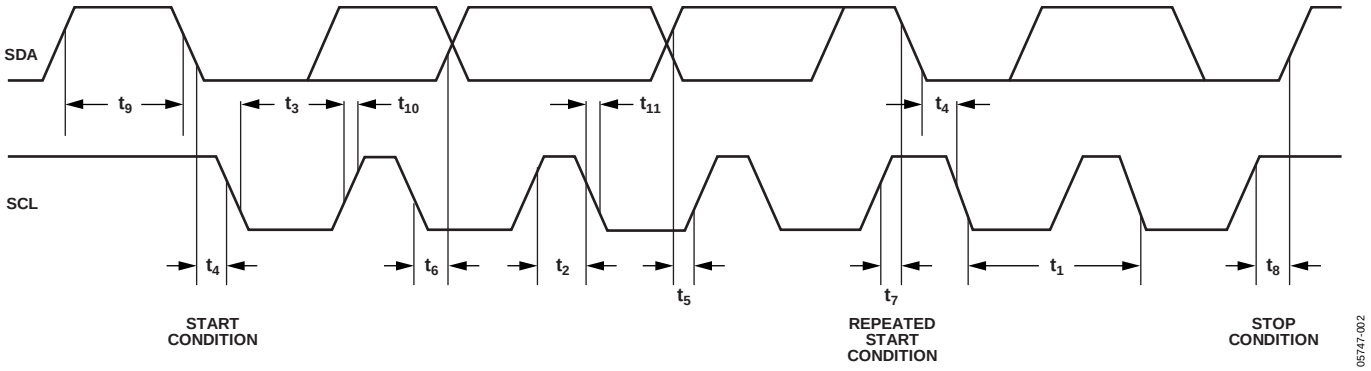


*Figure 2. I²C-Compatible Serial Interface Timing Diagram*

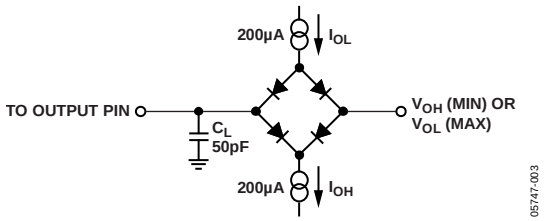


*Figure 3. Load Circuit for Digital Output*

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted.[1]

**Table 5.**

| Parameter | Rating |
|---|---|
| $V_{PP}$x to AGND | −0.3 V to +70 V |
| $AV_{DD}$x to AGND | −0.3 V to +7 V |
| DAC OUTV+ AB to AGND | −0.3 V to +17 V |
| DAC OUTV+ CD to AGND | −0.3 V to +17 V |
| $DV_{DD}$ to DGND | −0.3 V to +7 V |
| $V_{DRIVE}$ to OPGND | −0.3 V to +7 V |
| Digital Inputs to OPGND | −0.3 V to $V_{DRIVE}$ + 0.3 V |
| SDA/SCL to OPGND | −0.3 V to +7 V |
| Digital Outputs to OPGND | −0.3 V to $V_{DRIVE}$ + 0.3 V |
| RS(+)/RS(−) to $V_{PP}$x | $V_{PP}$ − 0.3 V to $V_{PP}$ + 0.3 V |
| $REF_{OUT}/REF_{IN}$ ADC to AGND | −0.3 V to $AV_{DD}$ + 0.3 V |
| $REF_{OUT}/REF_{IN}$ DAC to AGND | −0.3 V to $AV_{DD}$ + 0.3 V |
| OPGND to AGND | −0.3 V to +0.3 V |
| OPGND to DGND | −0.3 V to +0.3 V |
| AGND to DGND | −0.3 V to +0.3 V |
| $V_{OUT}$x to AGND | −0.3 V to DAC OUTV(+) + 0.3 V |
| Analog Inputs to AGND | −0.3 V to $AV_{DD}$ + 0.3 V |
| Operating Temperature Range | |
| B Version | −40°C to +105°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature ($T_J$ Max) | 150°C |
| ESD Human Body Model | 1 kV |
| Reflow Soldering Peak Temperature | 260°C |

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

To conform with IPC 2221 industrial standards, it is advisable to use conformal coating on the high voltage pins.

## THERMAL RESISTANCE

**Table 6. Thermal Resistance**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| 64-Lead TQFP | 54 | 16 | °C/W |
| 56-Lead LFCSP | 21 | 2 | °C/W |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

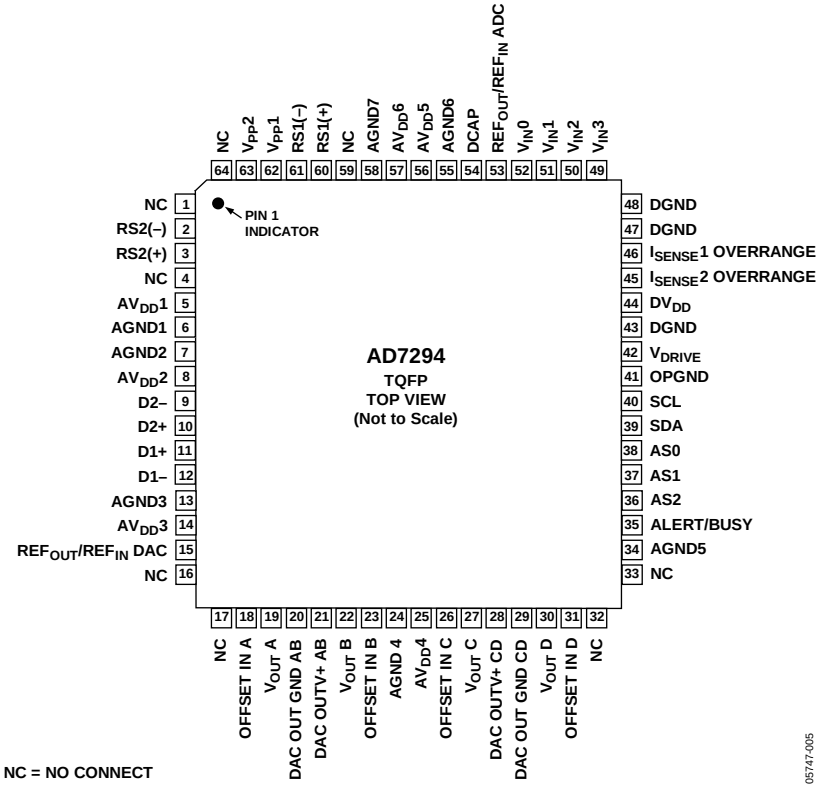


*Figure 4. TQFP Pin Configuration*

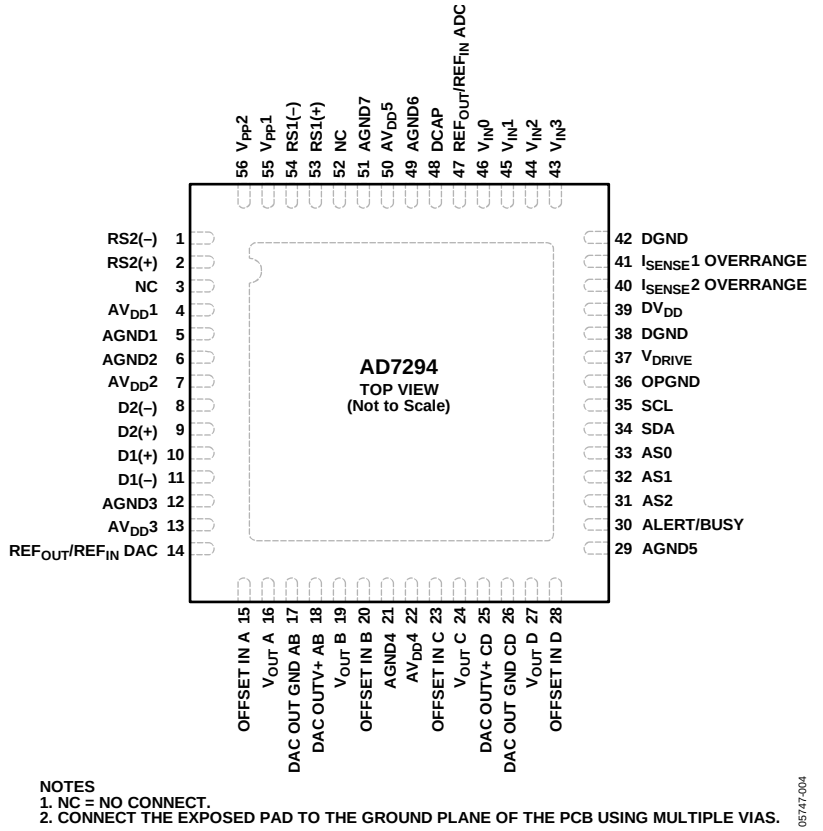


*Figure 5. LFCSP Pin Configuration*

**Table 7. Pin Function Descriptions**

| TQFP Pin No. | LFCSP Pin No. | Mnemonic | Description |
|---|---|---|---|
| 2, 61 | 1, 54 | RS2(−), RS1(−) | Connection for External Shunt Resistor. |
| 3, 60 | 2, 53 | RS2(+), RS1(+) | Connection for External Shunt Resistor. |
| 1, 4, 16, 17, 32, 33, 59, 64 | 3, 52 | NC | No Connection. Do not connect these pins. |
| 5, 8, 14, 25, 56, 57 | 4, 7, 13, 22, 50 | $AV_{DD}1$ to $AV_{DD}6$ for TQFP; $AV_{DD}1$ to $AV_{DD}4$ for LFCSP | Analog Supply Pins. The operating range is 4.5 V to 5.5 V. These pins provide the supply voltage for all the analog circuitry on the AD7294. Connect the $AV_{DD}$ and $DV_{DD}$ pins together to ensure that all supply pins are at the same potential. This supply should be decoupled to AGND with one 10 µF tantalum capacitor and a 0.1 µF ceramic capacitor for each $AV_{DD}$ pin. |
| 6, 7, 13, 24, 34, 55, 58 | 5, 6 12, 21, 29, 49, 51 | AGND1 to AGND7 | Analog Ground. Ground reference point for all analog circuitry on the AD7294. Refer all analog input signals and any external reference signal to this AGND voltage. Connect all seven of these AGND pins to the AGND plane of the system. Note that AGND5 is a DAC ground reference point and should be used as a star ground for circuitry being driven by the DAC outputs. Ideally, the AGND and DGND voltages should be at the same potential and must not be more than 0.3 V apart, even on a transient basis. |
| 9, 12 | 8, 11 | D2(−), D1(−) | Temperature Sensor Analog Input. These pins are connected to the external temperature sensing transistor. See Figure 46 and Figure 47. |
| 10, 11 | 9, 10 | D2(+), D1(+) | Temperature Sensor Analog Input. These pins are connected to the external temperature sensing transistor. See Figure 46 and Figure 47. |
| 15 | 14 | $REF_{OUT}/REF_{IN}$ DAC | DAC Reference Output/Input Pin. The $REF_{OUT}/REF_{IN}$ DAC pin is common to all four DAC channels. On power-up, the default configuration of this pin is external reference ($REF_{IN}$). Enable the internal reference by writing to the power-down register; see Table 27. Decoupling capacitors (220 nF recommended) are connected to this pin to decouple the reference buffer. Provided the output is buffered, the on-chip reference can be taken from this pin and applied externally to the rest of a system. A maximum external reference voltage of $AV_{DD}$ − 2 V can be supplied to the $REF_{OUT}$ portion of the $REF_{OUT}/REF_{IN}$ DAC pin. |
| 18, 23, 26, 31 | 15, 20 23,28 | OFFSET IN A to OFFSET IN D | DAC Analog Offset Input Pins. These pins set the desired output range for each DAC channel. The DACs have an output voltage span of 5 V, which can be shifted from 0 V to 5 V to a maximum output voltage of 10 V to 15 V by supplying an offset voltage to these pins. These pins can be left floating, in which case decouple them to AGND with a 100 nF capacitor. |
| 19, 22, 27, 30 | 16, 19, 24, 27 | $V_{OUT}$ A to $V_{OUT}$ D | Buffered Analog DAC Outputs for Channel A to Channel D. Each DAC analog output is driven from an output amplifier that can be offset using the OFFSET IN x pin. The DAC has a maximum output voltage span of 5 V that can be level shifted to a maximum output voltage level of 15 V. Each output is capable of sourcing and sinking 10 mA and driving a 10 nF load. |
| 20, 29 | 17, 26 | DAC OUT GND AB, DAC OUT GND CD | Analog Ground. Analog ground pins for the DAC output amplifiers on $V_{OUT}$A and $V_{OUT}$B, and $V_{OUT}$C and $V_{OUT}$D, respectively. |
| 21, 28 | 18, 25 | DAC OUTV+ AB, DAC OUTV+ CD | Analog Supply. Analog supply pins for the DAC output amplifiers on $V_{OUT}$A and $V_{OUT}$B, and $V_{OUT}$C and $V_{OUT}$D, respectively. The operating range is 4.5 V to 16.5 V. |
| 35 | 30 | ALERT/BUSY | Digital Output. Selectable as an alert or busy output function in the configuration register. This is an open-drain output. An external pull-up resistor is required.<br>When configured as an alert, this pin acts as an out-of-range indicator and becomes active when the conversion result violates the $DATA_{HIGH}$ or $DATA_{LOW}$ register values. See the Alert Status Registers section.<br>When configured as a busy output, this pin becomes active when a conversion is in progress. |
| 38, 37, 36 | 33, 32, 31 | AS0, AS1, AS2 | Digital Logic Input. Together, the logic state of these inputs selects a unique $I^2C$ address for the AD7294. See Table 34 for details. |
| 39 | 34 | SDA | Digital Input/Output. Serial bus bidirectional data; external pull-up resistor required. |

| TQFP Pin No. | LFCSP Pin No. | Mnemonic | Description |
|---|---|---|---|
| 40 | 35 | SCL | Serial $I^2C$ Bus Clock. The data transfer rate in $I^2C$ mode is compatible with both 100 kHz and 400 kHz operating modes. Open-drain input; external pull-up resistor required. |
| 41 | 36 | OPGND | Dedicated Ground Pin for $I^2C$ Interface. |
| 42 | 37 | $V_{DRIVE}$ | Logic Power Supply. The voltage supplied at this pin determines at what voltage the interface operates. Decouple this pin to DGND. The voltage range on this pin is 2.7 V to 5.5 V and may be different to the voltage level at $AV_{DD}$ and $DV_{DD}$, but should never exceed either by more than 0.3 V. To set the input and output thresholds, connect this pin to the supply to which the $I^2C$ bus is pulled. |
| 43, 47, 48 | 38, 42 | DGND | Digital Ground. This pin is the ground for all digital circuitry. |
| 44 | 39 | $DV_{DD}$ | Logic Power Supply. The operating range is 4.5 V to 5.5 V. These pins provide the supply voltage for all the digital circuitry on the AD7294. Connect the $AV_{DD}$ and $DV_{DD}$ pins together to ensure that all supply pins are at the same potential. Decouple this supply to DGND with a10 µF tantalum capacitor and a 0.1 µF ceramic capacitor. |
| 46, 45 | 41, 40 | $I_{SENSE}1$ OVERRANGE, $I_{SENSE}2$ OVERRANGE | Fault Comparator Outputs. These pins connect to the high-side current sense amplifiers. |
| 49, 50, 51, 52 | 43, 44, 45, 46 | $V_{IN}3$ to $V_{IN}0$ | Uncommitted ADC Analog Inputs. These pins are programmable as four single-ended channels or two true differential analog input channel pairs. See Table 1 and Table 13 for more details. |
| 53 | 47 | $REF_{OUT}/REF_{IN}$ ADC | ADC Reference Input/Output Pin. The $REF_{OUT}/REF_{IN}$ ADC pin provides the reference source for the ADC. Upon power-up, the default configuration of this pin is external reference ($REF_{IN}$). Enable the internal reference by writing to the power-down register; see Table 27. Connect decoupling capacitors (220 nF recommended) to this pin to decouple the reference buffer. Provided the output is buffered, the on-chip reference can be taken from this pin and applied externally to the rest of a system. A maximum external reference voltage of 2.5 V can be supplied to the $REF_{OUT}$ portion of the $REF_{OUT}/REF_{IN}$ ADC pin. |
| 54 | 48 | DCAP | External Decoupling Capacitor Input for Internal Temperature Sensor. Decouple this pin to AGND using a 0.1 µF capacitor. In normal operation, the voltage is typically 3.7 V. |
| 62, 63 | 55, 56 | $V_{PP}1$, $V_{PP}2$ | Current Sensor Supply Pins. Power supply pins for the high-side current sense amplifiers. Operating range is from $AV_{DD}$ to 59.4 V. Decouple this supply to AGND. See the Current Sense Filtering section. |
| N/A[1] | 0 | EPAD | The exposed pad is located on the underside of the package. Connect the exposed pad to the ground plane of the PCB using multiple vias. |

[1] N/A means not applicable.

# TYPICAL PERFORMANCE CHARACTERISTICS

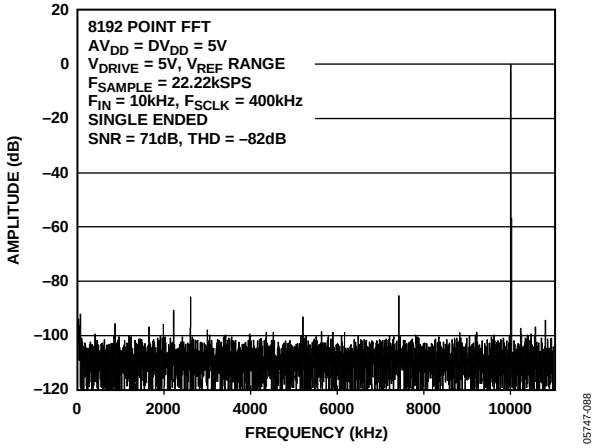


Figure 6. Signal-to-Noise Ratio Single-Ended, $V_{REF}$ Range

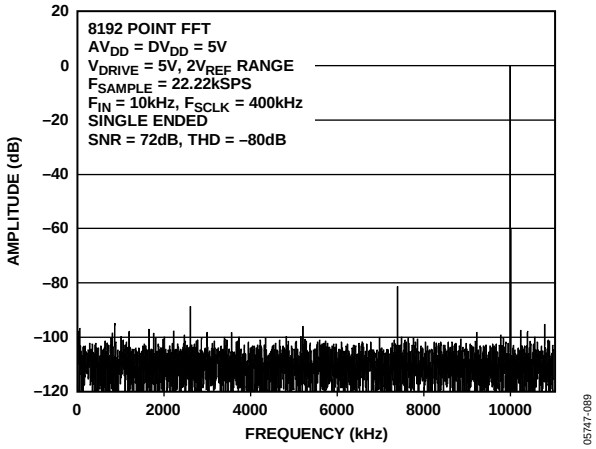


Figure 7. Signal-to-Noise Ratio Single-Ended, 2 × $V_{REF}$ Range

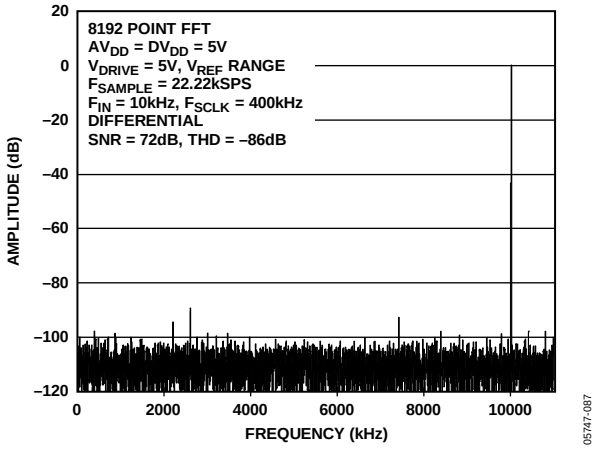


Figure 8. Signal-to-Noise Ratio Differential, $V_{REF}$ Range

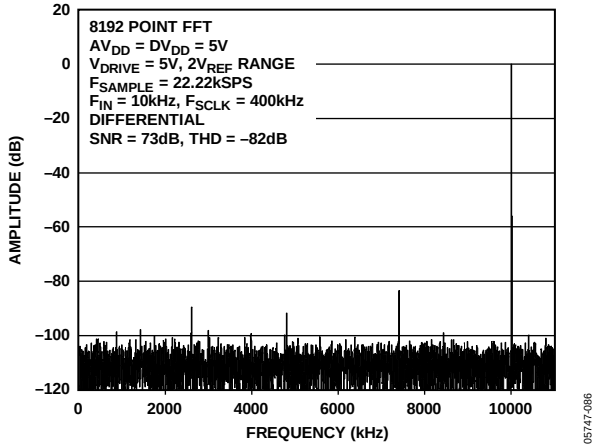


Figure 9. Signal-to-Noise Ratio Differential, 2 × $V_{REF}$ Range

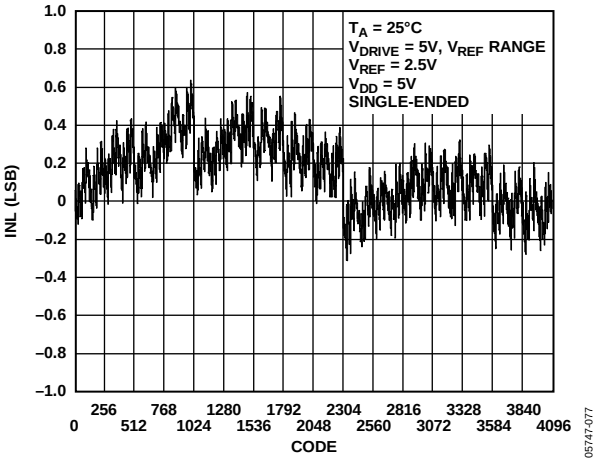


Figure 10. ADC INL Single-Ended, $V_{REF}$ Range

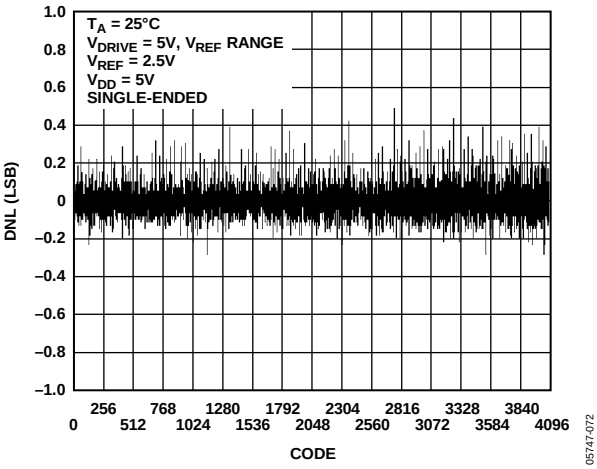


Figure 11. ADC DNL Single-Ended, $V_{REF}$ Range

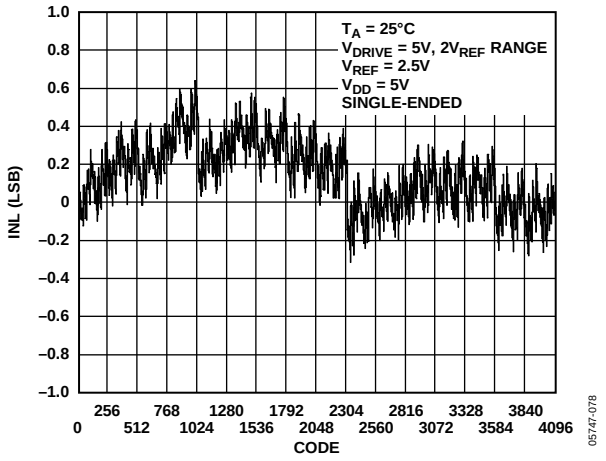


Figure 12. ADC INL Single-Ended, 2 × $V_{REF}$ Range

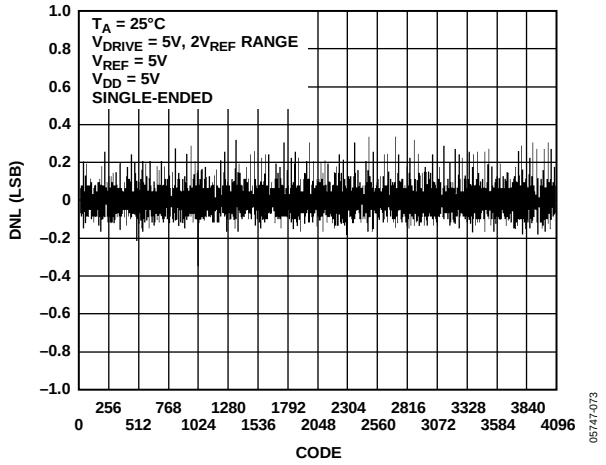


Figure 13. ADC DNL Single-Ended, 2 × $V_{REF}$ Range

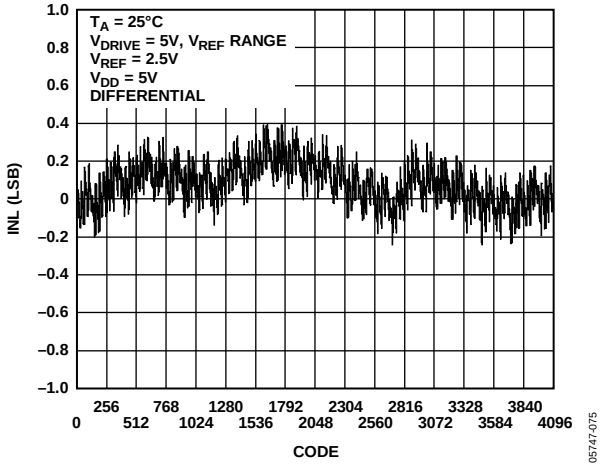


Figure 14. ADC INL Differential, $V_{REF}$ Range

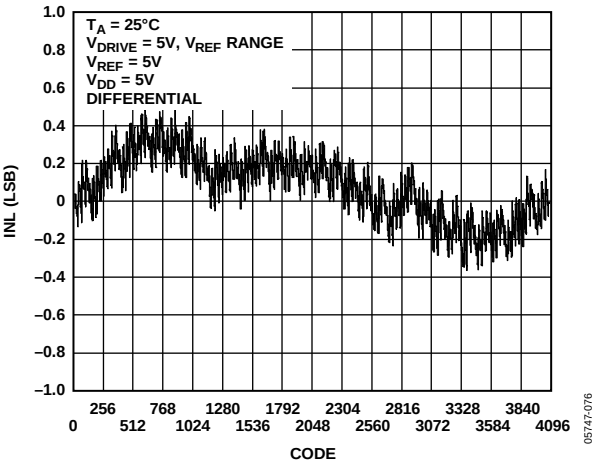


Figure 15. ADC INL Differential, $V_{REF}$ Range

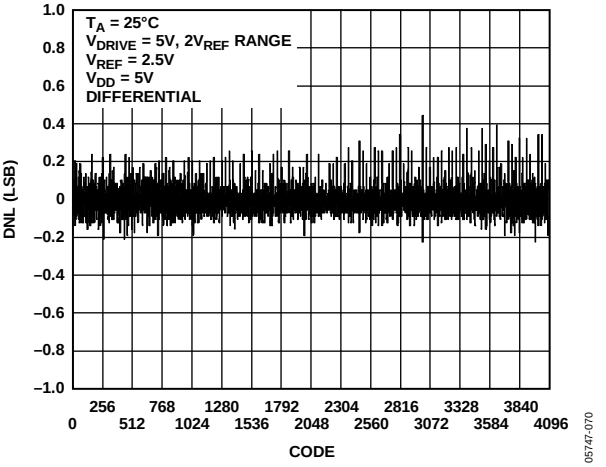


Figure 16. ADC DNL Differential, 2 × $V_{REF}$ Range

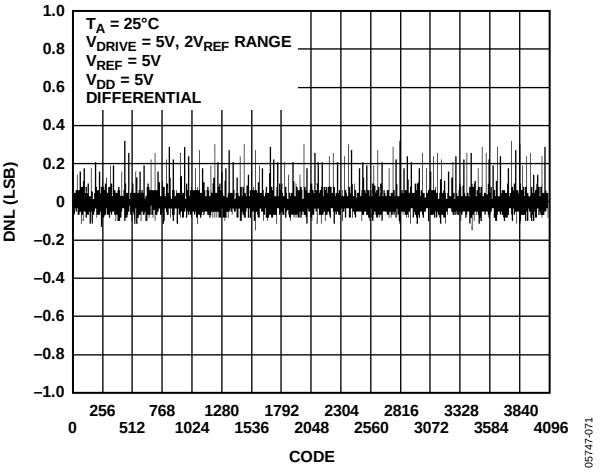


Figure 17. ADC DNL Differential, 2 × $V_{REF}$ Range

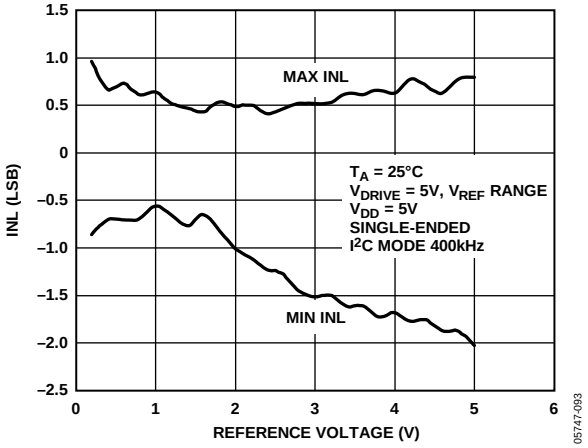


Figure 18. ADC INL vs. Reference Voltage

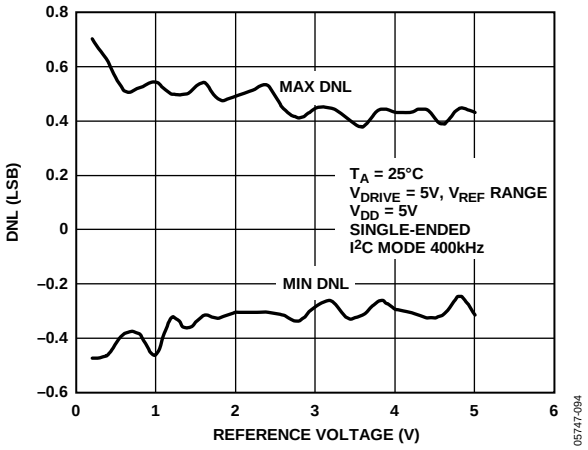


Figure 19. ADC DNL vs. Reference Voltage

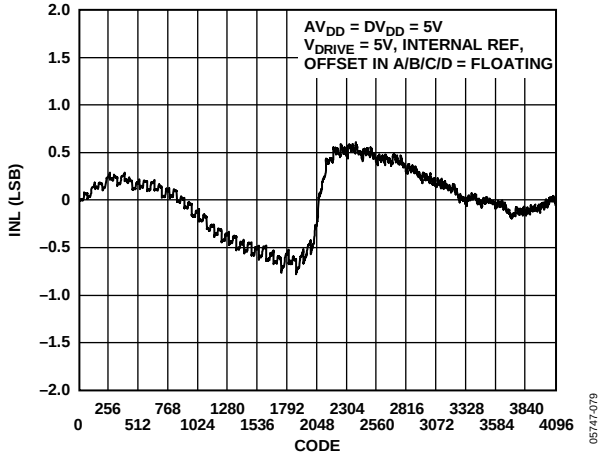


Figure 20. DAC INL

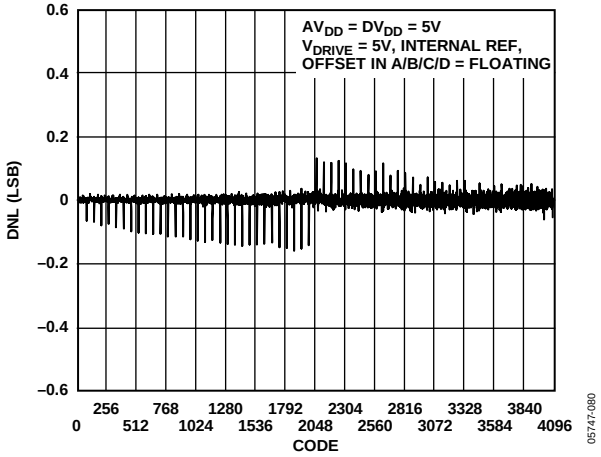


Figure 21. DAC DNL

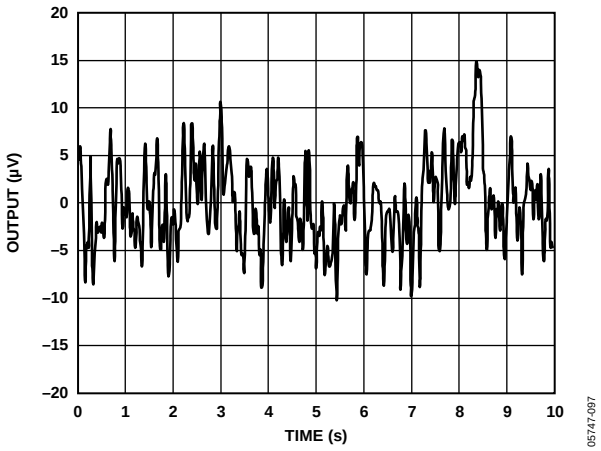


Figure 22. 0.1 Hz to 10 Hz DAC Output Noise (Code 800)

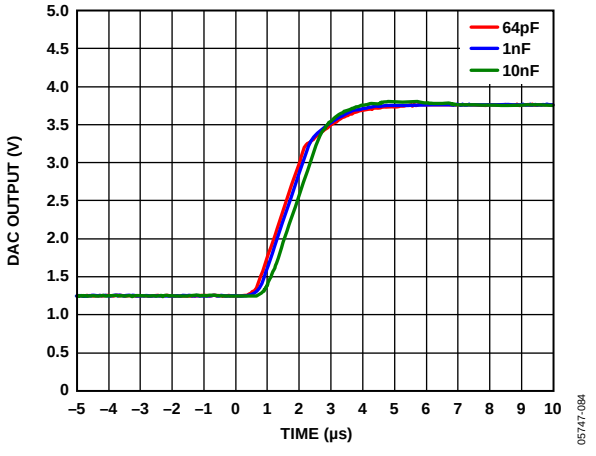


Figure 23. Settling Time for a ¼ to ¾ Output Voltage Step

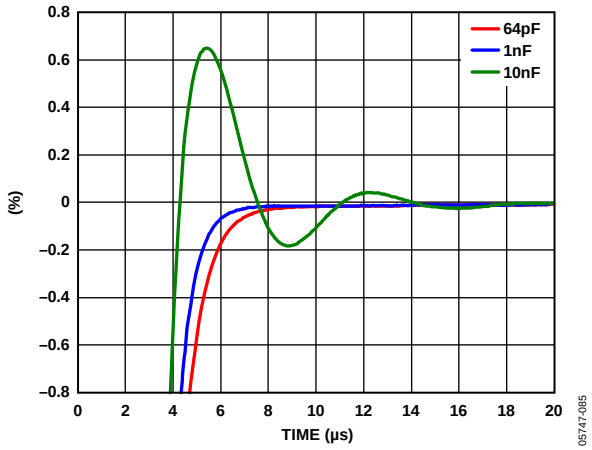


Figure 24. Zoomed in Settling for a ¼ to ¾ Output Voltage Step

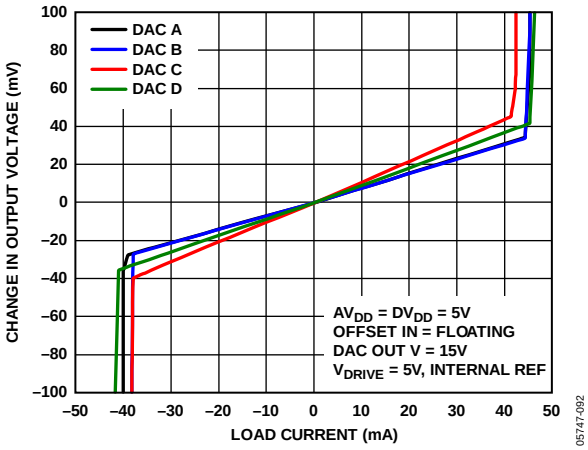


Figure 27. DAC Output Voltage vs. Load Current, Input Code = x800

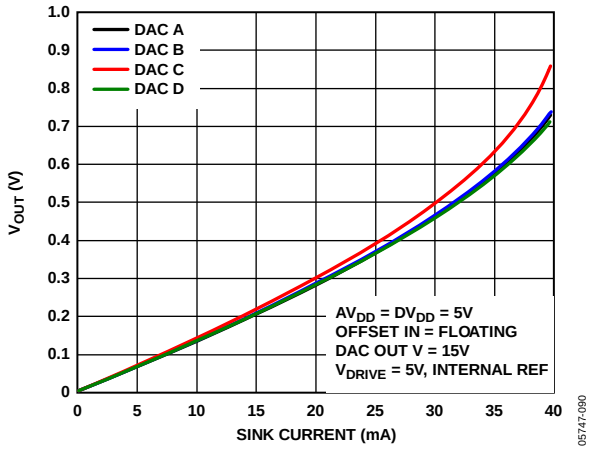


Figure 25. DAC Sinking Current at Input Code = x000, ($V_{OUT}$ = 0 V)

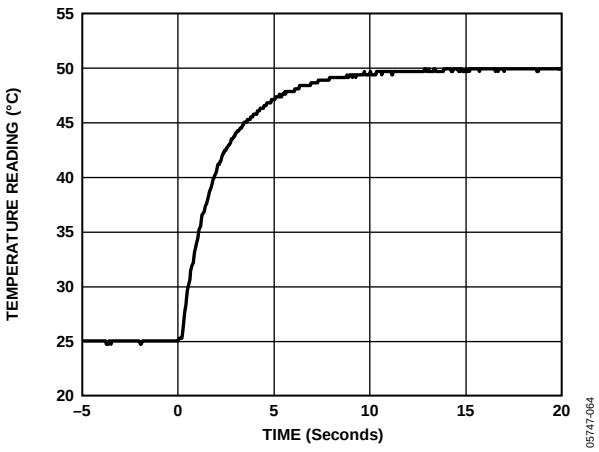


Figure 28. Response of the AD7294 to Thermal Shock Using 2N3906 (2N3906 Placed in a Stirred Oil Bath)

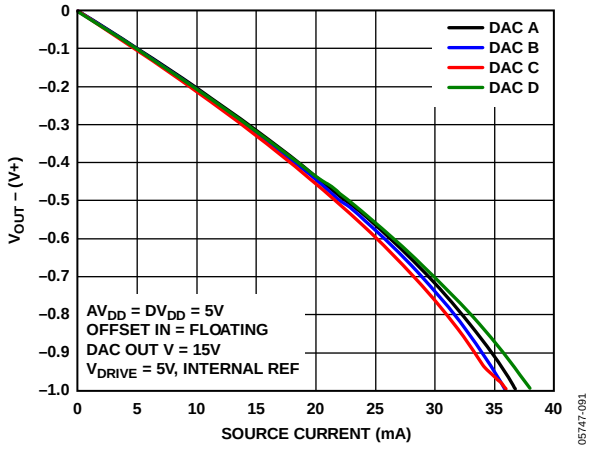


Figure 26. DAC Sourcing Current at Input Code = x000, ($V_{OUT}$ = 0 V)

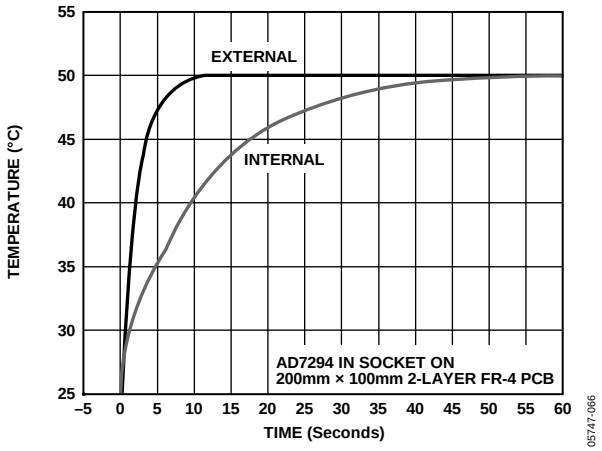


Figure 29. Response to Thermal Shock from Room Temperature into 50°C Stirred Oil (Both the AD7294 and the 2N3906 are Placed in a Stirred Oil Bath)

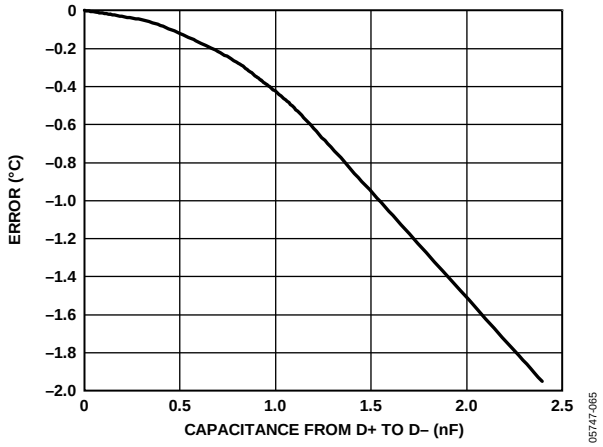


Figure 30. Temperature Error vs. Capacitor Between D+ and D–

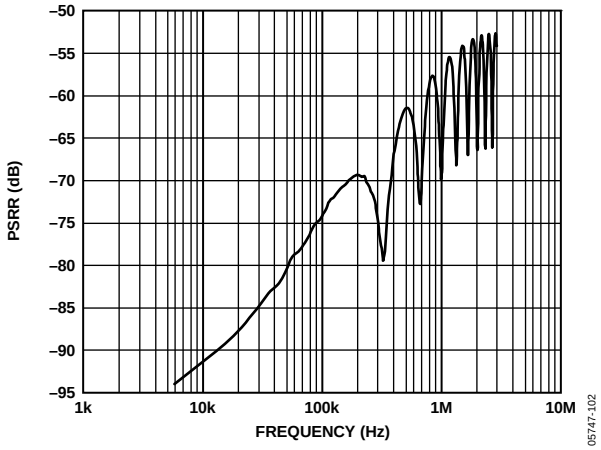


Figure 33. $I_{SENSE}$ Power Supply Rejection Ratio vs. Supply Ripple Frequency Without $V_{PP}$ Supply Decoupling Capacitors for a 500 mV Ripple

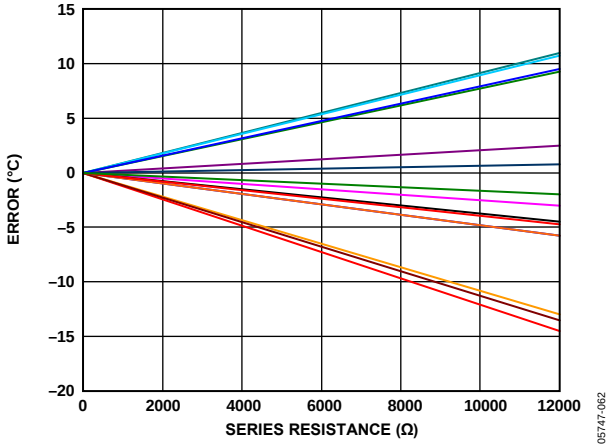


Figure 31. Temperature Error vs. Series Resistance for 15 Typical Devices

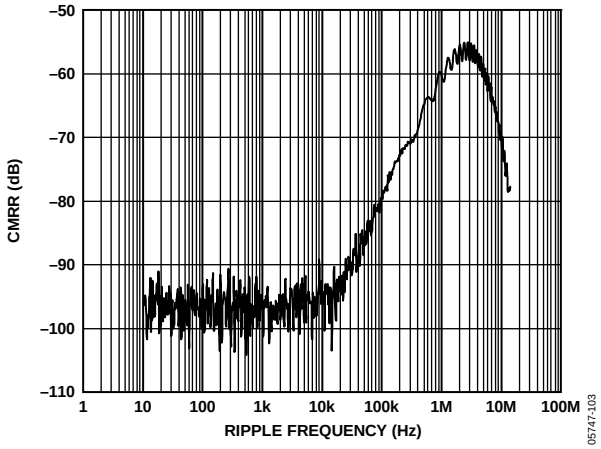


Figure 34. $I_{SENSE}$ Common-Mode Rejection Ratio vs. Ripple Frequency for a 400 mV Peak-To-Peak Ripple

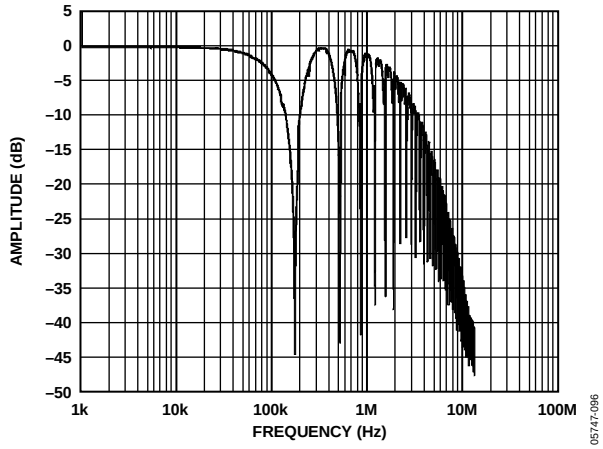


Figure 32. Frequency Response of the High-Side Current Sensor on the AD7294

# TERMINOLOGY

## DAC TERMINOLOGY

**Relative Accuracy**
For the DAC, relative accuracy or integral nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function.

**Differential Nonlinearity**
Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design.

**Zero Code Error**
Zero code error is a measure of the output error when zero code (0x0000) is loaded to the DAC register. Ideally, the output should be 0 V. The zero code error is always positive in the AD7294 because the output of the DAC cannot go below 0 V. Zero code error is expressed in mV.

**Full-Scale Error**
Full-scale error is a measure of the output error when full-scale code (0xFFFF) is loaded to the DAC register. Ideally, the output should be $V_{DD}$ − 1 LSB. Full-scale error is expressed in mV.

**Gain Error**
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from ideal, expressed as a percent of the full-scale range.

**Total Unadjusted Error**
Total unadjusted error (TUE) is a measure of the output error, taking all of the various errors into account.

**Zero Code Error Drift**
Zero code error drift is a measure of the change in zero code error with a change in temperature. It is expressed in µV/°C.

**Gain Error Drift**
Gain error drift is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

## ADC TERMINOLOGY

**Signal-to-Noise and Distortion Ratio (SINAD)**
The measured ratio of signal-to-noise and distortion at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-noise and distortion ratio for an ideal N-bit converter with a sine wave input is given by

$$Signal\text{-}to\text{-}(Noise + Distortion) = (6.02\ N + 1.76)\ \text{dB}$$

Thus, the SINAD is 74 dB for an ideal 12-bit converter.

**Total Harmonic Distortion (THD)**
The ratio of the rms sum of harmonics to the fundamental. For the AD7294, it is defined as

$$THD(\text{dB}) = 20\log\frac{\sqrt{V_2^{\,2} + V_3^{\,2} + V_4^{\,2} + V_5^{\,2} + V_6^{\,2}}}{V_1}$$

where $V_1$ is the rms amplitude of the fundamental and $V_2$, $V_3$, $V_4$, $V_5$, and $V_6$ are the rms amplitudes of the second through sixth harmonics.

**Peak Harmonic or Spurious Noise**
The ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Typically, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

**Integral Nonlinearity**
The maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition.

**Differential Nonlinearity**
The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

**Offset Error**
The deviation of the first code transition (00…000) to (00…001) from the ideal—that is, AGND + 1 LSB.

**Offset Error Match**
The difference in offset error between any two channels.

**Gain Error**
The deviation of the last code transition (111…110) to (111…111) from the ideal (that is, $REF_{IN}$ − 1 LSB) after the offset error has been adjusted out.

**Gain Error Match**
The difference in gain error between any two channels.

# THEORY OF OPERATION

## ADC OVERVIEW

The AD7294 provides the user with a 9-channel multiplexer, an on-chip track-and-hold, and a successive approximation ADC based around a capacitive DAC. The analog input range for the device can be selected as a 0 V to $V_{REF}$ input or a 2 × $V_{REF}$ input, configured with either single-ended or differential analog inputs. The AD7294 has an on-chip 2.5 V reference that can be disabled when an external reference is preferred. If the internal ADC reference is to be used elsewhere in a system, the output must first be buffered.

The various monitored and uncommitted input signals are multiplexed into the ADC. The AD7294 has four uncommitted analog input channels, $V_{IN}0$ to $V_{IN}3$. These four channels allow single-ended, differential, and pseudo differential mode measurements of various system signals.

## ADC TRANSFER FUNCTIONS

The designed code transitions occur at successive integer LSB values (1 LSB, 2 LSB, and so on). In single-ended mode, the LSB size is $V_{REF}/4096$ when the 0 V to $V_{REF}$ range is used and 2 × $V_{REF}/4096$ when the 0 V to 2 × $V_{REF}$ range is used. The ideal transfer characteristic for the ADC when outputting straight binary coding is shown in Figure 35.

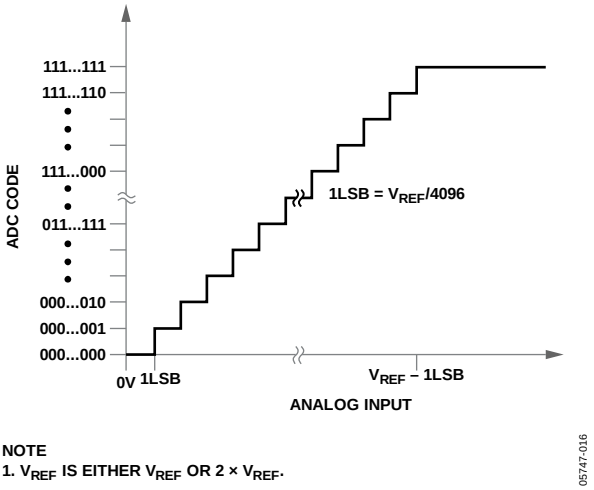


*Figure 35. Single-Ended Transfer Characteristic*

In differential mode, the LSB size is 2 × $V_{REF}/4096$ when the 0 V to $V_{REF}$ range is used, and 4 × $V_{REF}/4096$ when the 0 V to 2 × $V_{REF}$ range is used. The ideal transfer characteristic for the ADC when outputting twos complement coding is shown in Figure 36 (with the 2 × $V_{REF}$ range).

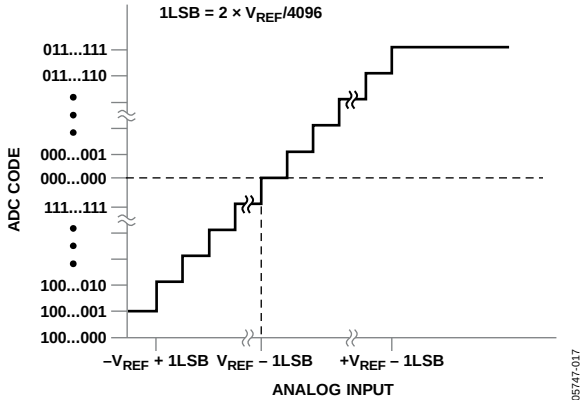


*Figure 36. Differential Transfer Characteristic with $V_{REF} \pm V_{REF}$ Input Range*

For $V_{IN}0$ to $V_{IN}3$ in single-ended mode, the output code is straight binary, where

$V_{IN}$ = 0 V, $D_{OUT}$ = x000, $V_{IN}$ = $V_{REF}$ − 1 LSB, and $D_{OUT}$ = xFFF

In differential mode, the code is twos complement, where
$V_{IN+} - V_{IN-}$ = 0 V, and $D_{OUT}$ = x00
$V_{IN+} - V_{IN-} = V_{REF}$ − 1 LSB, and $D_{OUT}$ = x7FF
$V_{IN+} - V_{IN-} = -V_{REF}$, and $D_{OUT}$ = x800

Channel 5 and Channel 6 (current sensor inputs) are twos complement, where

$V_{IN+} - V_{IN-}$ = 0 mV, and $D_{OUT}$ = x000

$V_{IN+} - V_{IN-} = V_{REF}/12.5$ − 1 LSB, $D_{OUT}$ = x7FF

$V_{IN+} - V_{IN-} = -V_{REF}/12.5$, $D_{OUT}$ = x800

Channel 7 to Channel 9 (temperature sensor inputs) are twos complement with the LSB equal to 0.25°C, where

$T_{IN}$ = 0°C, and $D_{OUT}$ = x000
$T_{IN}$ = +255.75°C, and $D_{OUT}$ = x7FF
$T_{IN}$ = −256°C, and $D_{OUT}$ = x800

## ANALOG INPUTS

The AD7294 has a total of four analog inputs. Depending on the configuration register setup, they can be configured as two single-ended inputs, two pseudo differential channels, or two fully differential channels. See the Register Setting section for further details.

### *Single-Ended Mode*

The AD7294 can have four single-ended analog input channels. In applications where the signal source has high impedance, it is recommended to buffer the analog input before applying it to the ADC. The analog input range can be programmed to be either 0 V to $V_{REF}$ or 0 V to 2 × $V_{REF}$. In 2 × $V_{REF}$ mode, the input is effectively divided by 2 before the conversion takes place. Note that the voltage with respect to GND on the ADC analog input pins cannot exceed $AV_{DD}$.

If the analog input signal to be sampled is bipolar, the internal reference of the ADC can be used to externally bias up this signal so that it is correctly formatted for the ADC. Figure 37 shows a typical connection diagram when operating the ADC in single-ended mode.

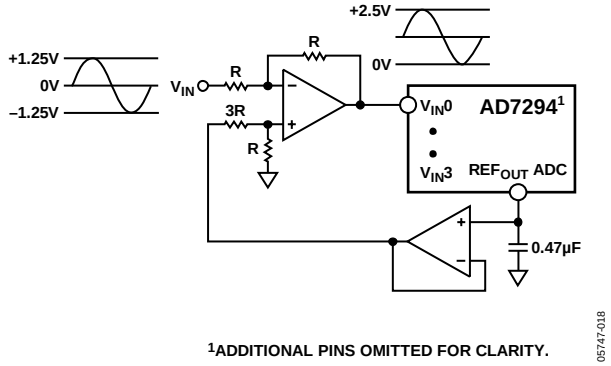


*Figure 37. Single-Ended Mode Connection Diagram*

### Differential Mode

The AD7294 can have two differential analog input pairs. Differential signals have some benefits over single-ended signals, including noise immunity based on the common-mode rejection of the device and improvements in distortion performance. Figure 38 defines the fully differential analog input of the AD7294.

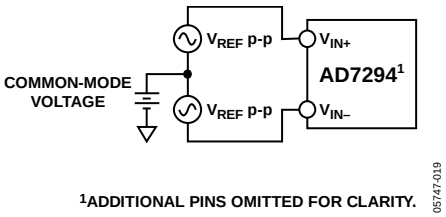


*Figure 38. Differential Input Definition*

The amplitude of the differential signal is the difference between the signals applied to $V_{IN+}$ and $V_{IN-}$ in each differential pair ($V_{IN+} - V_{IN-}$). The resulting converted data is stored in twos complement format in the result register. Simultaneously drive $V_{IN}0$ and $V_{IN}1$ by two signals, each of amplitude $V_{REF}$ (or 2 × $V_{REF}$, depending on the range chosen), that are 180° out of phase. Assuming the 0 V to $V_{REF}$ range is selected, the amplitude of the differential signal is, therefore, $-V_{REF}$ to $+V_{REF}$ peak-to-peak (2 × $V_{REF}$), regardless of the common mode ($V_{CM}$).

The common mode is the average of the two signals

$$(V_{IN+} + V_{IN-})/2$$

The common mode is, therefore, the voltage on which the two inputs are centered.

This results in the span of each input being $V_{CM} \pm V_{REF}/2$. This voltage has to be set up externally, and its range varies with the reference value, $V_{REF}$. As the value of $V_{REF}$ increases, the common-mode range decreases. When driving the inputs with an amplifier, the actual common-mode range is determined by the output voltage swing of the amplifier.

The common mode must be in this range to guarantee the functionality of the AD7294.

When a conversion takes place, the common mode is rejected, resulting in a virtually noise-free signal of amplitude $-V_{REF}$ to $+V_{REF}$, corresponding to the digital output codes of −2048 to +2047 in twos complement format.

If the 2 × $V_{REF}$ range is used, the input signal amplitude extends from $-2 \times V_{REF}$ ($V_{IN+}$ = 0 V, $V_{IN-}$ = $V_{REF}$) to $+2 \times V_{REF}$ ($V_{IN-}$ = 0 V, $V_{IN+}$ = $V_{REF}$).

### Driving Differential Inputs

The differential modes available on $V_{IN}0$ to $V_{IN}3$ in Table 13 require that $V_{IN+}$ and $V_{IN-}$ be driven simultaneously with two equal signals that are 180° out of phase. The common mode on which the analog input is centered must be set up externally. The common-mode range is determined by $V_{REF}$, the power supply, and the particular amplifier used to drive the analog inputs. Differential modes of operation with either an ac or dc input provide the best THD performance over a wide frequency range. Because not all applications have a signal preconditioned for differential operation, there is often a need to perform a single-ended-to-differential conversion.

### Using an Op Amp Pair

An op amp pair can be used to directly couple a differential signal to one of the analog input pairs of the AD7294. The circuit configurations illustrated in Figure 39 show how a dual op amp can be used to convert a single-ended bipolar signal into a differential unipolar input signal.

The voltage applied to Point A sets up the common-mode voltage. As shown in Figure 39, Point A connects to the reference, but any value in the common-mode range can be the input at Point A to set up the common mode. The AD8022 is a suitable dual op amp that can be used in this configuration to provide differential drive to the AD7294.

Care is required when choosing the op amp because the selection depends on the required power supply and system performance objectives. The driver circuits in Figure 39 are optimized for dc coupling applications requiring best distortion performance. The differential op amp driver circuit shown in Figure 39 is configured to convert and level shift a single-ended, ground referenced (bipolar) signal to a differential signal centered at the $V_{REF}$ level of the ADC.

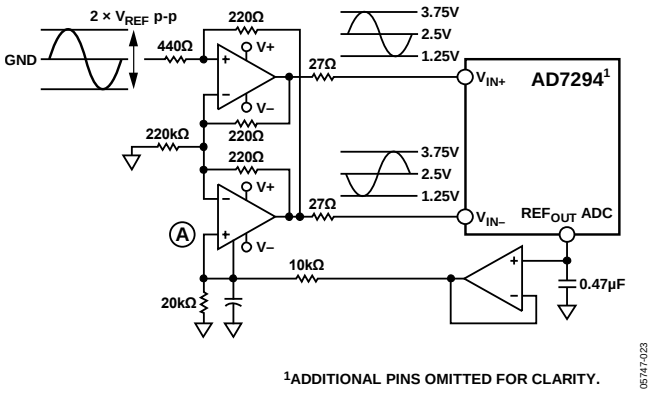


*Figure 39. Dual Op Amp Circuit to Convert a Single-Ended Bipolar Signal into a Differential Unipolar Signal*

### *Pseudo Differential Mode*

The four uncommitted analog input channels can be configured as two pseudo differential pairs. Uncommitted input, $V_{IN}0$ and $V_{IN}1$, are a pseudo differential pair, as are $V_{IN}2$ and $V_{IN}3$. In this mode, $V_{IN+}$ is connected to the signal source, which can have a maximum amplitude of $V_{REF}$ (or 2 × $V_{REF}$, depending on the range chosen) to make use of the full dynamic range of the device. A dc input is applied to $V_{IN-}$. The voltage applied to this input provides an offset from ground or a pseudo ground for the $V_{IN+}$ input. Which channel is $V_{IN+}$ is determined by the ADC channel allocation. The differential mode must be selected to operate in the pseudo differential mode. The resulting converted pseudo differential data is stored in twos complement format in the result register.

The governing equation for the pseudo differential mode, for $V_{IN}0$ is

$$V_{OUT} = 2(V_{IN+} - V_{IN-}) - V_{REF_ADC}$$

where $V_{IN+}$ is the single-ended signal and $V_{IN-}$ is a dc voltage.

The benefit of pseudo differential inputs is that they separate the analog input signal ground from the ADC ground, allowing dc common-mode voltages to be cancelled. The typical voltage range for $V_{IN-}$ while in pseudo differential mode is shown in Figure 40; Figure 41 shows a connection diagram for pseudo differential mode.

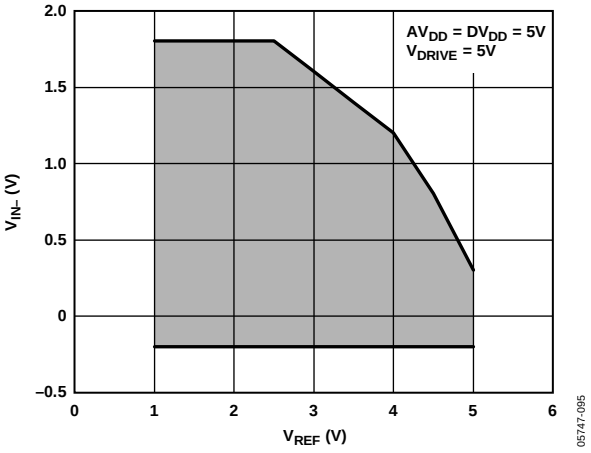


*Figure 40. $V_{IN-}$ Input Range vs. $V_{REF}$ in Pseudo Differential Mode*

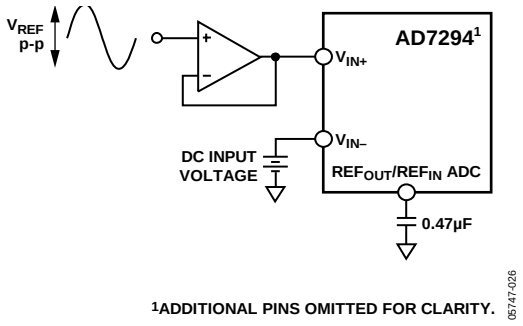


*Figure 41. Pseudo Differential Mode Connection Diagram*

## CURRENT SENSOR

Two bidirectional high-side current sense amplifiers are provided that can accurately amplify differential current shunt voltages in the presence of high common-mode voltages from $AV_{DD}$ up to 59.4 V. Each amplifier can accept a ±200 mV differential input. Both current sense amplifiers have a fixed gain of 12.5 and utilize an internal 2.5 V reference.

An analog comparator is also provided with each amplifier for fault detection. The threshold is defined as

1.2 × *Full-Scale Voltage Range*

When this limit is reached, the output is latched onto a dedicated pin. This output remains high until the latch is cleared by writing to the appropriate register.

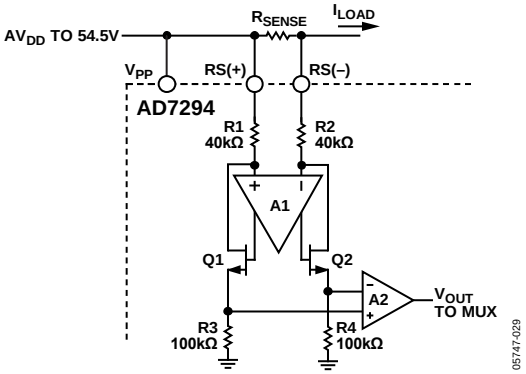


*Figure 42. High-Side Current Sense*

The AD7294 current sense comprises two main blocks: a differential and an instrumentation amplifier. A load current flowing through the external shunt resistor produces a voltage at the input terminals of the AD7294. Resistors R1 and R2 connect the input terminals to the differential amplifier (A1). A1 nulls the voltage appearing across its own input terminals by adjusting the current through R1 and R2 with Transistor Q1 and Transistor Q2. Common-mode feedback maintains the sum of these currents at approximately 50 µA. When the input signal to the AD7294 is zero, the currents in R1 and R2 are equal. When the differential signal is nonzero, the current increases through one of the resistors and decreases in the other. The current difference is proportional to the size and polarity of the input signal.

The differential currents through Q1 and Q2 are converted into a differential voltage by R3 and R4. A2 is configured as an instrumentation amplifier, buffering this voltage and providing additional

gain. Therefore, for an input voltage of ±200 mV at the pins, an output span of ±2.5 V is generated.

The current sensors on the AD7294 are designed to remove any flicker noise and offset present in the sensed signal. This is achieved by implementing a chopping technique that is transparent to the user. The $V_{SENSE}$ signal is first converted by the AD7294, the analog inputs to the amplifiers are then swapped, and the differential voltage is once again converted by the AD7294. The two conversion results enable the digital removal of any offset or noise. Switches on the amplifier inputs enable this chopping technique to be implemented. This process requires 6 µs in total to return a final result.

### Choosing $R_{SENSE}$

The resistor values used in conjunction with the current sense amplifiers on the AD7294 are determined by the specific application requirements in terms of voltage, current, and power. Small resistors minimize power dissipation, have low inductance to prevent any induced voltage spikes, and have good tolerance, which reduce current variations. The final values chosen are a compromise between low power dissipation and good accuracy. Low value resistors have less power dissipated in them, but higher value resistors may be required to utilize the full input range of the ADC, thus achieving maximum SNR performance.

When the sense current is known, the voltage range of the AD7294 current sensor (200 mV) is divided by the maximum sense current to yield a suitable shunt value. If the power dissipation in the shunt resistor is too large, the shunt resistor can be reduced, in which case, less of the ADC input range is used. Using less of the ADC input range results in conversion results, which are more susceptible to noise and offset errors because offset errors are fixed and are thus more significant when smaller input ranges are used.

$R_{SENSE}$ must be able to dissipate the $I^2R$ losses. If the power dissipation rating of the resistor is exceeded, its value may drift or the resistor may be damaged resulting in an open circuit. This can result in a differential voltage across the terminals of the AD7294 in excess of the absolute maximum ratings. Additional protection is afforded to the current sensors on the AD7294 by the recommended current limiting resistors, RF1 and RF2, as illustrated in Figure 43. The AD7294 can handle a maximum continuous current of 30 mA; thus, an RF2 of 1 kΩ provides adequate protection for the AD7294.

If $I_{SENSE}$ has a large high frequency component, take care to choose a resistor with low inductance. Low inductance metal film resistors are best suited for these applications.

### Current Sense Filtering

In some applications, it may be desirable to use external filtering to reduce the input bandwidth of the amplifier (see Figure 43). The −3 dB differential bandwidth of this filter is equal to

$$BW_{DM} = 1/(4\pi RC)$$

Note that the maximum series resistance on the RS(+) and RS(−) inputs (as shown in Figure 42) is limited to a maximum of 1 kΩ due to back-to-back ESD protection diodes from RS(+) and RS(−) to $V_{PP}$. Also, note that if RF1 and RF2 are in series with R1 and R2 (shown in Figure 42), it affects the gain of the amplifier. Any mismatch between RF1 and RF2 can introduce offset error.

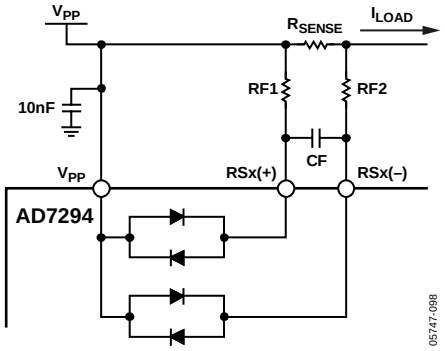


*Figure 43. Current Sense Filtering ($RS_X$ Can Be Either RS1 or RS2)*

For certain RF applications, the optimum value for RF1 and RF2 is 1 kΩ whereas CF1 can range from 1 µF to 10 µF. CF2 is a decoupling capacitor for the $V_{PP}$ supply. Its value is application dependent, but for initial evaluation, values in the range of 1 nF to 100 nF are recommended.

### Kelvin Sense Resistor Connection

When using a low value sense resistor for high current measurement, the problem of parasitic series resistance can arise. The lead resistance can be a substantial fraction of the rated resistance, making the total resistance a function of lead length. Avoid this problem by using a Kelvin sense connection. This type of connection separates the current path through the resistor and the voltage drop across the resistor. Figure 44 shows the correct way to connect the sense resistor between the RS(+) and RS(−) pins of the AD7294.

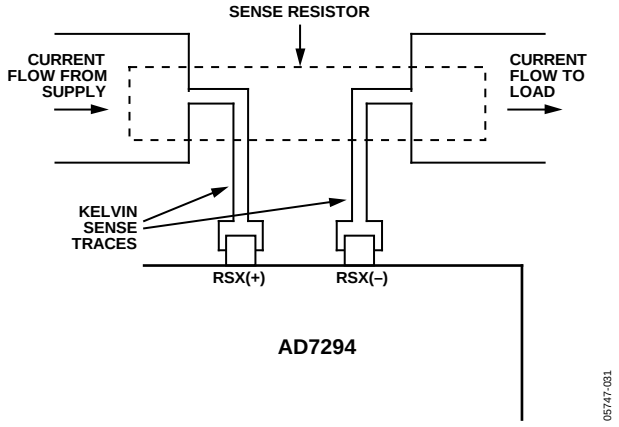


*Figure 44. Kelvin Sense Connections (RSX Can Be Either RS1 or RS2)*

## ANALOG COMPARATOR LOOP

The AD7294 contains two setpoint comparators that are used for independent analog control. This circuitry enables users to quickly detect if the sensed voltage across the shunt has

increased about the preset ($V_{REF}$ × 1.2)/12.5. If this occurs, the $I_{SENSE}$ OVERRANGE pin is set to a high logic level enabling appropriate action to be taken to prevent any damage to the external circuitry.

The setpoint threshold level is fixed internally in the AD7294, and the current sense amplifier saturates above this level. The comparator also triggers if a voltage of less than $AV_{DD}$ is applied to the $R_{SENSE}$ or $V_{PP}$ pin.

## TEMPERATURE SENSOR

The AD7294 contains one local and two remote temperature sensors. The temperature sensors continuously monitor the three temperature inputs and new readings are automatically available every 5 ms.

The on-chip, band gap temperature sensor measures the temperature of the system. Diodes are used in conjunction with the two remote temperature sensors to monitor the temperature of other critical board components.

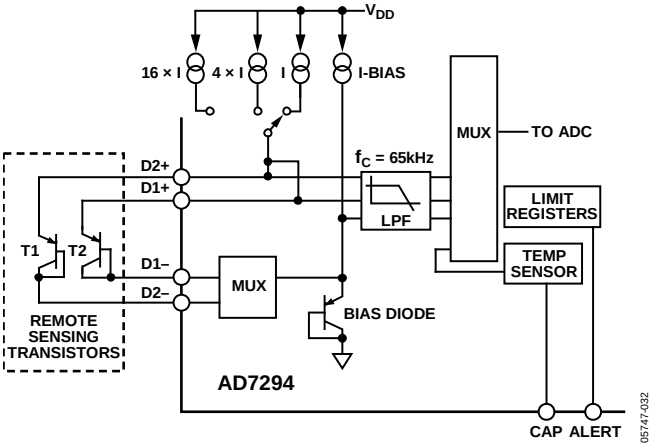


*Figure 45. Internal and Remote Temperature Sensors*

The temperature sensor module on the AD7294 is based on the three current principle (see Figure 45), where three currents are passed through a diode and the forward voltage drop is measured at each diode, allowing the temperature to be calculated free of errors caused by series resistance.

Each input integrates, in turn, over a period of several hundred microseconds. This takes place continuously in the background, leaving the user free to perform conversions on the other channels. When integration is complete, a signal passes to the control logic to initiate a conversion automatically. If the ADC is in command mode, the temperature conversion is performed as soon as the next conversion is completed. In autocycle mode, the conversion is inserted into an appropriate place in the current sequence; see the Register Setting section for further details. If the ADC is idle, the conversion takes place immediately.

Three registers store the result of the last conversion on each temperature channel; these can be read at any time. In addition, in command mode, one or both of the two external channel registers can be read out as part of the output sequence.

### *Remote Sensing Diode*

The AD7294 is designed to work with discrete transistors, 2N3904 and 2N3906. If an alternative transistor is used, the AD7294 operates as specified provided the following conditions are adhered to.

#### Ideality Factor

The ideality factor, $n_f$, of the transistor is a measure of the deviation of the thermal diode from ideal behavior. The AD7294 is trimmed for an $n_f$ value of 1.008. Use the following equation to calculate the error introduced at a Temperature T (°C) when using a transistor whose $n_f$ does not equal 1.008:

$$\Delta T = (n_f - 1.008) \times (273.15\ \text{K} + T)$$

To factor this in, the user can write the ΔT value to the offset register. The AD7294 automatically adds it to, or subtracts it from, the temperature measurement.

#### Base Emitter Voltage

The AD7294 operates as specified provided that the base-emitter voltage is greater than 0.25 V at 8 µA at the highest operating temperature, and less than 0.95 V at 128 µA for the lowest operating temperature.

#### Base Resistance

The base resistance should be less than 100 Ω.

#### $h_{FE}$ Variation

Use a transistor with small variation in $h_{FE}$ (approximately 50 to 150). Small variation in $h_{FE}$ indicates tight control of the $V_{BE}$ characteristics.

For RF applications, the use of high Q capacitors functioning as a filter protects the integrity of the measurement. These capacitors, such as Johanson Technology 10 pF high Q capacitors: Reference Code 500R07S100JV4T, should be connected between the base and the emitter, as close to the external device as possible. However, large capacitances affect the accuracy of the temperature measurement; thus, the recommended maximum capacitor value is 100 pF. In most cases, a capacitor is not required; the selection of any capacitor is dependent on the noise frequency level.

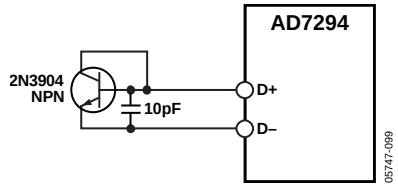


*Figure 46. Measuring Temperature Using an NPN Transistor*

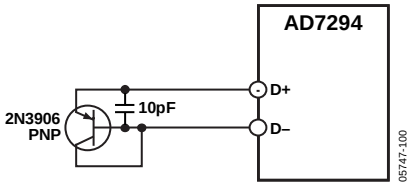


*Figure 47. Measuring Temperature Using a PNP Transistor*

### Series Resistance Cancellation

The AD7294 has been designed to automatically cancel out the effect of parasitic, base, and collector resistance on the temperature reading. This gives a more accurate result, without the need for any user characterization of the parasitic resistance. The AD7294 can compensate for up to 100 Ω in a process that is transparent to the user.

## DAC OPERATION

The AD7294 contains four 12-bit DACs that provide digital control with 12 bits of resolution with a 2.5 V internal reference. The DAC core is a thin film 12-bit string DAC with a 5 V output span and an output buffer that can drive the high voltage output stage. The DAC has a span of 0 V to 5 V with a 2.5 V reference input. The output range of the DAC, which is controlled by the offset input, can be positioned from 0 V to 15 V.

### Resistor String

The resistor string structure is shown in Figure 48. It consists of a string of $2^n$ resistors, each of Value R. The code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. This architecture is inherently monotonic, voltage out, and low glitch. It is also linear because all of the resistors are of equal value.

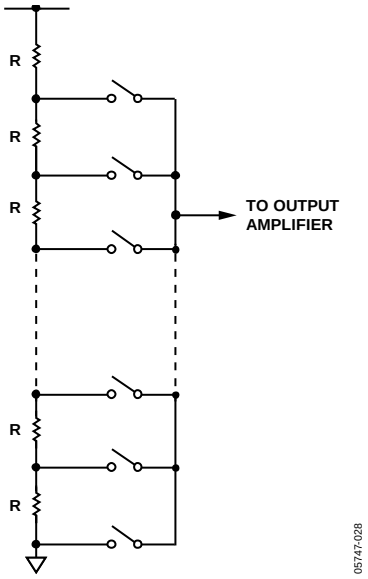


*Figure 48. Resistor String Structure*

### Output Amplifier

Referring to Figure 48, the purpose of A1 is to buffer the DAC output range from 0 V to $V_{REF}$. The second amplifier, A2, is configured such that when an offset is applied to OFFSET IN x, its output voltage is three times the offset voltage minus twice the DAC voltage.

$$V_{OUT} = 3V_{OFFSET} - 2V_{DAC}$$

The DAC word is digitally inverted on-chip such that

$$V_{OUT} = 3V_{OFFSET} + 2(V_{DAC} - V_{REF})$$

$$\text{and } V_{DAC} = \left[V_{REF} \times \left(\frac{D}{2^n}\right)\right]$$

where:

$V_{DAC}$ is the output of the DAC before digital inversion.
$D$ is the decimal equivalent of the binary code that is loaded to the DAC register.
$n$ is the bit resolution of the DAC.

An example of the offset function is given in Table 8.

**Table 8. Offset Voltage Function Example**

| Offset Voltage | $V_{OUT}$ with 0x000 | $V_{OUT}$ with 0xFFF |
|---|---|---|
| 1.67 V | 0 V | 5 V – 1 LSB |
| 3.33 V | 5 V | 10 V – 1 LSB |
| 5.00 V | 10 V | 15 V – 1 LSB |

The user has the option of leaving the offset pin open, in which case the voltage on the noninverting input of Op Amp A2 is set by the resistor divider, giving

$$V_{OUT} = 2V_{DAC}$$

This generates the 5 V output span from a 2.5 V reference. Digitally inverting the DAC allows the circuit to operate as a generic DAC when no offset is applied. If the offset pin is not being driven, it is best practice to place a 100 nF capacitor between the pin and ground to improve both the settling time and the noise performance of the DAC.

Note that a significant amount of power can be dissipated in the DAC outputs. A thermal shutdown circuit sets the DAC outputs to high impedance if a die temperature of >150°C is measured by the internal temperature sensor. This also sets the overtemperature alert bit in Alert Register C, see the Alerts and Limits Theory section. Note that this feature is disabled when the temperature sensor powers down.

## ADC AND DAC REFERENCE

The AD7294 has two independent internal high performance 2.5 V references, one for the ADCs and the other for the four on-chip DACs. If the application requires an external reference, it can be applied to the $REF_{OUT}/REF_{IN}$ DAC pin and/or to the $REF_{OUT}/REF_{IN}$ ADC pin. The internal reference should be buffered before being used by external circuitry. Decouple both the $REF_{OUT}/REF_{IN}$ DAC pin and the $REF_{OUT}/REF_{IN}$ ADC pin to AGND using a 220 nF capacitor. On power-up, the AD7294 is configured for use with an external reference. To enable the internal references, write a zero to both the D4 and D5 bits in the power-down register (see the Register Setting section for more details). Both the ADC and DAC references require a minimum of 60 µs to power up and settle to a 12-bit performance when a 220 nF decoupling capacitor is used.

The AD7294 can also operate with an external reference. Suitable reference sources for the AD7294 include the AD780, AD1582, ADR431, REF193, and ADR391. In addition, choosing a reference with an output trim adjustment, such as the ADR441, allows a system designer to trim system errors by setting a reference voltage to a voltage other than the nominal.

Long-term drift is a measure of how much the reference drifts over time. A reference with a low long-term drift specification ensures that the overall solution remains stable during its entire lifetime. If an external reference is used, select a low temperature coefficient specification to reduce the temperature dependence of the system output voltage on ambient conditions.

## $V_{DRIVE}$ FEATURE

The AD7294 also has a $V_{DRIVE}$ feature to control the voltage at which the $I^2C$ interface operates. The $V_{DRIVE}$ pin is connected to the supply to which the $I^2C$ bus is pulled. This pin sets the input and output threshold levels for the digital logic pins and the $I_{SENSE}$ OVERRANGE pins. The $V_{DRIVE}$ feature allows the AD7294 to easily interface to both 3 V and 5 V processors. For example, if the AD7294 is operated with a $V_{DD}$ of 5 V, the $V_{DRIVE}$ pin can be powered from a 3 V supply, allowing a large dynamic range with low voltage digital processors. Thus, the AD7294 can be used with the $2 \times V_{REF}$ input range with a $V_{DD}$ of 5 V, yet remains capable of interfacing to 3 V digital devices. Decouple this pin to DGND with a 100 nF and a 1 µF capacitor.

# REGISTER SETTING

The AD7294 contains internal registers (see Figure 49) that store conversion results, high and low conversion limits, and information to configure and control the device.

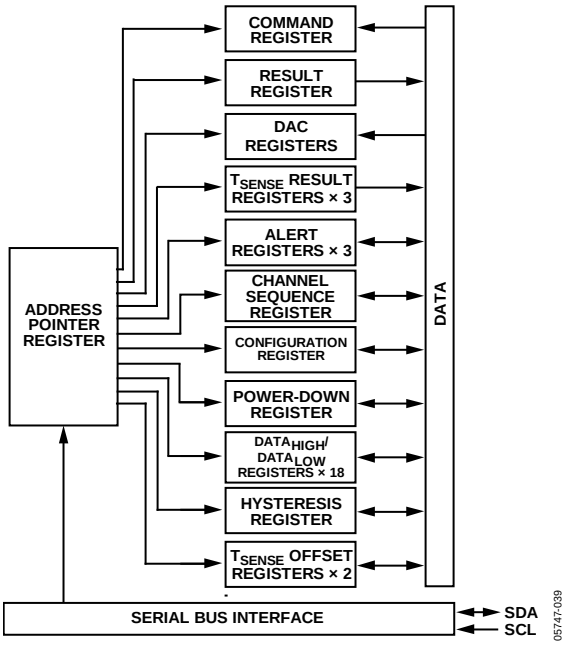


*Figure 49. AD7294 Register Structure*

Each data register has an address to which the address pointer register points when communicating with it. The command register is the only register that is a write-only register; the rest are read/write registers.

## ADDRESS POINTER REGISTER

The address pointer register is an 8-bit register, in which the 6 LSBs are used as pointer bits to store an address that points to one of the AD7294 data registers, see Table 9.

**Table 9. AD7294 Register Address**

| Address in Hex | Registers (R is Read/W is Write) |
|---|---|
| 00 | Command Register (W) |
| 01 | Result Register (R)/$DAC_A$ Value (W) |
| 02 | $T_{SENSE}1$ Result (R)/$DAC_B$ Value (W) |
| 03 | $T_{SENSE}2$ Result (R)/$DAC_C$ Value (W) |
| 04 | $T_{SENSE}INT$ Result (R)/$DAC_D$ Value (W) |
| 05 | Alert Register A (R/W) |
| 06 | Alert Register B (R/W) |
| 07 | Alert Register C (R/W) |
| 08 | Channel Sequence Register (R/W) |
| 09 | Configuration Register (R/W) |
| 0A | Power-Down Register (R/W) |
| 0B | $DATA_{LOW}$ Register $V_{IN}0$ (R/W) |
| 0C | $DATA_{HIGH}$ Register $V_{IN}0$ (R/W) |
| 0D | Hysteresis Register $V_{IN}0$ (R/W) |
| 0E | $DATA_{LOW}$ Register $V_{IN}1$ (R/W) |
| 0F | $DATA_{HIGH}$ Register $V_{IN}1$ (R/W) |
| 10 | Hysteresis Register $V_{IN}1$ (R/W) |
| 11 | $DATA_{LOW}$ Register, $V_{IN}2$ (R/W) |
| 12 | $DATA_{HIGH}$ Register $V_{IN}2$ (R/W) |
| 13 | Hysteresis Register $V_{IN}2$ (R/W) |
| 14 | $DATA_{LOW}$ Register $V_{IN}3$ (R/W) |
| 15 | $DATA_{HIGH}$ Register $V_{IN}3$ (R/W) |
| 16 | Hysteresis Register $V_{IN}3$ (R/W) |
| 17 | $DATA_{LOW}$ Register $I_{SENSE}1$ (R/W) |
| 18 | $DATA_{HIGH}$ Register $I_{SENSE}1$ (R/W) |
| 19 | Hysteresis Register $I_{SENSE}1$ (R/W) |
| 1A | $DATA_{LOW}$ Register $I_{SENSE}2$ (R/W) |
| 1B | $DATA_{HIGH}$ Register $I_{SENSE}2$ (R/W) |
| 1C | Hysteresis Register $I_{SENSE}2$ (R/W) |
| 1D | $DATA_{LOW}$ Register $T_{SENSE}1$ (R/W) |
| 1E | $DATA_{HIGH}$ Register $T_{SENSE}1$ (R/W) |
| 1F | Hysteresis Register $T_{SENSE}1$ (R/W) |
| 20 | $DATA_{LOW}$ Register $T_{SENSE}2$ (R/W) |
| 21 | $DATA_{HIGH}$ Register $T_{SENSE}2$ (R/W) |
| 22 | Hysteresis Register $T_{SENSE}2$ (R/W) |
| 23 | $DATA_{LOW}$ Register $T_{SENSE}INT$ (R/W) |
| 24 | $DATA_{HIGH}$ Register $T_{SENSE}INT$ (R/W) |
| 25 | Hysteresis Register $T_{SENSE}INT$ (R/W) |
| 26 | $T_{SENSE}1$ Offset Register (R/W) |
| 27 | $T_{SENSE}2$ Offset Register (R/W) |
| 40 | Factory Test Mode |
| 41 | Factory Test Mode |

## COMMAND REGISTER (0x00)

Writing in the command register puts the device into command mode. When in command mode, the device cycles through the selected channels from LSB (D0) to MSB (D7) on each subsequent read (see Table 10). A channel is selected for conversion if a one is written to the desired bit in the command register. On power-up, all bits in the command register are set to zero. If the external $T_{SENSE}$ channels are selected in the command register byte, it is not actually requesting a conversion. The result of the last automatic conversion is output as part of the sequence (see the Modes of Operation section).

If a command mode conversion is required while the autocycle mode is active, it is necessary to disable the autocycle mode before proceeding to the command mode (see the Autocycle Mode section for more details).

## RESULT REGISTER (0x01)

The result register is a 16-bit read-only register. The conversion results for the four uncommitted ADC inputs and the two $I_{SENSE}$ channels are stored in the result register for reading.

Bit D14 to Bit D12 are the channel allocation bits, each of which identifies the ADC channel that corresponds to the subsequent result (see the ADC Channel Allocation section for more details). Bit D11 to Bit D0 contain the most recent ADC result. D15 is reserved as an alert_flag bit. Table 11 lists the contents of the first byte that is read from the AD7294 results register; Table 12 lists the contents of the second byte read.

**Table 10. Command Register**[1]

| | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| **Bits** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| **Channel** | Read out last result from $T_{SENSE}2$ | Read out last result from $T_{SENSE}1$ | $I_{SENSE}2$ | $I_{SENSE}1$ | $V_{IN}3$ (S.E.) or $V_{IN}3 - V_{IN}2$ (DIFF) | $V_{IN}2$ (S.E.) or $V_{IN}2 - V_{IN}3$ (DIFF) | $V_{IN}1$ (S.E.) or $V_{IN}1 - V_{IN}0$ (DIFF) | $V_{IN}0$ (S.E.) or $V_{IN}0 - V_{IN}1$ (DIFF) |

[1] S.E. indicates single-ended and DIFF indicates differential.

**Table 11. Result Register (First Read)**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** |
| Alert_Flag | $CH_{ID2}$ | $CH_{ID1}$ | $CH_{ID0}$ | B11 | B10 | B9 | B8 |

**Table 12. Result Register (Second Read)**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |

### *ADC Channel Allocation*

The three channel address bits indicate which channel the result in the result register represents. Table 13 details the channel ID bits (S.E. indicates single-ended and DIFF indicates differential).

**Table 13. ADC Channel Allocation**

| | Channel ID | | |
|---|---|---|---|
| **Function** | **$CH_{ID2}$** | **$CH_{ID1}$** | **$CH_{ID0}$** |
| $V_{IN}0$ (S.E.) or $V_{IN}0 - V_{IN}1$ (DIFF) | 0 | 0 | 0 |
| $V_{IN}1$ (S.E.) or $V_{IN}1 - V_{IN}0$ (DIFF) | 0 | 0 | 1 |
| $V_{IN}2$ (S.E.) or $V_{IN}2 - V_{IN}3$ (DIFF) | 0 | 1 | 0 |
| $V_{IN}3$ (S.E.) or $V_{IN}3 - V_{IN}2$ (DIFF) | 0 | 1 | 1 |
| $I_{SENSE}1$ | 1 | 0 | 0 |
| $I_{SENSE}2$ | 1 | 0 | 1 |
| $T_{SENSE}1$ | 1 | 1 | 0 |
| $T_{SENSE}2$ | 1 | 1 | 1 |

## TSENSE1, TSENSE2 RESULT REGISTERS (0X02 AND 0X03)

Register $T_{SENSE}1$ and Register $T_{SENSE}2$ are 16-bit read only registers. The MSB, D15 is the alert_flag bit whereas Bit D14 to Bit D12 contain the three ADC channel allocation bits. D11 is reserved for flagging diode open circuits. The temperature reading from the ADC is stored in an 11-bit twos complement format, D10 to D0 (see Table 14 and Table 15). Conversions take place approximately every 5 ms.

**Table 14. $T_{SENSE}$ Register (First Read)**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** |
| Alert_Flag | $CH_{ID2}$ | $CH_{ID1}$ | $CH_{ID0}$ | B11 | B10 | B9 | B8 |

**Table 15. Register (Second Read)**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |

## TSENSEINT RESULT REGISTER (0X04)

The $T_{SENSE}$INT register is a 16-bit read-only register used to store the ADC data generated from the internal temperature sensor. Similar to the $T_{SENSE}1$ and $T_{SENSE}2$ result registers, this register stores the temperature readings from the ADC in an 11-bit twos complement format, D10 to D0, and uses the MSB as a general alert flag. Bits[D14:D11] are not used and are set to zero. Conversions take place approximately every 5 ms. The temperature data format in Table 16 also applies to the internal temperature sensor data.

### *Temperature Value Format*

The temperature reading from the ADC is stored in an 11-bit twos complement format, D10 to D0, to accommodate both positive and negative temperature measurements. The temperature data format is provided in Table 16.

**Table 16. $T_{SENSE}$ Data Format**

| **Input** | **D10 (MSB)** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0 (LSB)** |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Value (°C)** | −256 | +128 | +64 | +32 | +16 | +8 | +4 | +2 | +1 | +0.5 | +0.25 |

## $DAC_A$, $DAC_B$, $DAC_C$, $DAC_D$, REGISTERS (0x01 TO 0x04)

Writing to these register addresses sets the $DAC_A$, $DAC_B$, $DAC_C$, and $DAC_D$ output voltage codes, respectively. Bits[D11:D0] in the write result register are the data bits sent to $DAC_A$. Bit D15 to Bit D12 are ignored.

**Table 17. DAC Register (First Write)[1]**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** |
| X | X | X | X | B11 | B10 | B9 | B8 |

[1] X is don't care.

**Table 18. DAC Register (Second Write)**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |

## ALERT STATUS REGISTER A (0x05), REGISTER B (0x06), AND REGISTER C (0x07)

The alert status registers (A, B, and C) are 8-bit read/write registers that provide information on an alert event. If a conversion results in activating the ALERT/BUSY pin or the alert_flag bit in the result register or $T_{SENSE}$ registers, the alert status register can be read to gain further information. To clear the full content of any one of the alert registers, write a code of FF (all ones) to the relevant registers. Alternatively, the user can write to the respective alert bit in the selected alert register to clear the alert associated with that bit. The entire contents of all the alert status registers can be cleared by writing a 1 to Bit D1 and Bit D2 in the configuration register, as shown in Table 24. However, this operation then enables the ALERT/BUSY pin for subsequent conversions. See the Alerts and Limits Theory section for more details.

## CHANNEL SEQUENCE REGISTER (0x08)

The channel sequence register is an 8-bit read/write register that allows the user to sequence the ADC conversions to be performed in autocycle mode. Table 22 shows the content of the channel sequence register. See the Modes of Operation section for more information.

**Table 19. Alert Status Register A**

| Alert Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| **Function** | $V_{IN}3$ high alert | $V_{IN}3$ low alert | $V_{IN}2$ high alert | $V_{IN}2$ low alert | $V_{IN}1$ high alert | $V_{IN}1$ low alert | $V_{IN}0$ high alert | $V_{IN}0$ low alert |

**Table 20. Alert Status Register B**

| Alert Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| **Function** | Reserved | Reserved | $I_{SENSE}2$ overrange | $I_{SENSE}1$ overrange | $I_{SENSE}2$ high alert | $I_{SENSE}2$ low alert | $I_{SENSE}1$ high alert | $I_{SENSE}1$ low alert |

**Table 21. Alert Status Register C**

| Alert Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| **Function** | Open-diode flag | Overtemp alert | $T_{SENSE}$INT high alert | $T_{SENSE}$INT low alert | $T_{SENSE}2$ high alert | $T_{SENSE}2$ low alert | $T_{SENSE}1$ high alert | $T_{SENSE}1$ low alert |

**Table 22. Channel Sequence Register**

| Channel Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| **Function** | Reserved | Reserved | $I_{SENSE}2$ | $I_{SENSE}1$ | $V_{IN}3$ | $V_{IN}2$ | $V_{IN}1$ | $V_{IN}0$ |

## CONFIGURATION REGISTER (0x09)

The configuration register is a 16-bit read/write register that sets the operating modes of the AD7294. The bit functions of the configuration register are outlined in Table 23 and Table 24. On power-up, the configuration register is reset to 0x0000.

### *Sample Delay and Bit Trial Delay*

It is recommended that no I²C bus activity occur when a conversion is taking place; however, this may not be possible, for example, when operating in autocycle mode. Bit D14 and Bit D13 in the configuration register are used to delay critical sample intervals and bit trials from occurring while there is activity on the I²C bus. On power-up, Bit D14 (noise-delayed sampling), Bit D13 (noise-delayed bit trials), and Bit D3 (I²C filters) are enabled (set to 0). This configuration is appropriate for low frequency applications because the bit trials are prevented from occurring when there is activity on the I²C bus, thus ensuring good dc linearity performance. For high frequency input signals, it may be desirable to have a known sampling point, thus the noise-delayed sampling can be disabled by writing a 1 to Bit D14 in the configuration register. This ensures that the sampling instance is fixed relative to SDA, resulting in improved SNR performance. If noise-delay samplings extend longer than 1 µs, the current conversion terminates. This termination can occur if there are edges on SDA that are outside the I²C specification. When noise-delayed sampling is enabled, the rise and fall times must meet the I²C-specified standard. When D13 is enabled, the conversion time may vary.

The default configuration for Bit D3 (enabled) is recommended for normal operation because it ensures that the I²C requirements for $t_{Of}$ (minimum) and $t_{SP}$ are met. The I²C filters reject glitches shorter than 50 ns. If this function is disabled, the conversion results are more susceptible to noise from the I²C bus.

**Table 23. Configuration Register Bit Function Description D15 to D8**

| Channel Bit | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|---|
| **Function** | Reserved | Noise-delayed sampling. Use to delay critical sample intervals from occurring when there is activity on the I²C bus. | Noise-delayed bit trials. Use to delay critical bit trials from occurring when there is activity on the I²C bus. | Autocycle mode | Pseudo differential mode for $V_{IN}3/V_{IN}4$ | Pseudo differential mode for $V_{IN}1/V_{IN}2$ | Differential mode for $V_{IN}3/V_{IN}4$ | Differential mode for $V_{IN}1/V_{IN}2$ |
| **Setting** | | Enabled = 0<br>Disabled = 1 | Enabled = 0<br>Disabled = 1 | Enabled = 1<br>Disabled = 0 | Enabled = 1<br>Disabled = 0 | Enabled = 1<br>Disabled = 0 | Enabled = 1<br>Disabled = 0 | Enabled = 1<br>Disabled = 0 |

**Table 24. Configuration Register Bit Function Description D7 to D0**

| Channel Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| **Function** | $2V_{REF}$ range for $V_{IN}4$ | $2V_{REF}$ range for $V_{IN}3$ | $2V_{REF}$ range for $V_{IN}2$ | $2V_{REF}$ range for $V_{IN}1$ | I²C filters | ALERT pin | BUSY pin (D2 = 0), clear alerts (D2 = 1) | Select ALERT pin polarity (active high/ active low) |
| **Setting** | Enabled = 1<br>Disabled = 0 | Enabled = 1<br>Disabled = 0 | Enabled = 1<br>Disabled = 0 | Enabled = 1<br>Disabled = 0 | Enabled = 0<br>Disabled = 1 | Enabled<br>D2 = 1<br>D1 = 0<br>Disabled<br>D2 = 0 | Enabled<br>D1 = 1 + D0 = 0<br>Disabled D1 = 0 | Active high = 1<br>Active low = 0 |

**Table 25. Alert/Busy Function Description**

| D2 | D1 | ALERT/BUSY Pin Functions |
|---|---|---|
| 0 | 0 | Pin does not provide any interrupt signal. |
| 0 | 1 | Configures pin as a busy output. |
| 1 | 0 | Configures pin as an alert output. |
| 1 | 1 | Resets the ALERT/BUSY output pin, the alert_flag bit in the conversion result register, and the entire alert status register (if any is active). 1,1 is written to Bits[D2:D1] in the configuration register to reset the ALERT/BUSY pin, the alert_flag bit, and the alert status register. Following this write, the contents of the configuration register read 1, 0 for Bit D2 and Bit D1, respectively, if read back. |

**Table 26. ADC Input Mode Example**

| D11 | D10 | D9 | D8 | Description |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | All channels single-ended |
| 0 | 0 | 0 | 1 | Differential mode on $V_{IN}1/V_{IN}2$ |
| 0 | 1 | 0 | 1 | Pseudo differential mode on $V_{IN}1/V_{IN}2$ |

## POWER-DOWN REGISTER (0x0A)

The power-down register is an 8-bit read/write register that powers down various sections on the AD7294 device. On power-up, the default value for the power-down register is 0x30. The content of the power-down register is provided in Table 27.

**Table 27. Power-Down Register Description**

| Bit | Function |
|---|---|
| D7 | Power down the full chip |
| D6 | Reserved |
| D5 | Power down the ADC reference buffer (to allow external reference, 1 at power-up) |
| D4 | Power down the DAC reference buffer (to allow external reference, 1 at power-up) |
| D3 | Power down the temperature sensor |
| D2 | Power down $I_{SENSE}1$ |
| D1 | Power down $I_{SENSE}2$ |
| D0 | DAC outputs set to high impedance (set automatically if die temperature >150°C) |

In normal operation, the two MSBs of the I²C slave address are set to 11 by an internal ROM. However, in full power-down mode (power down by setting Bit D7 = 1), this ROM is switched off and the slave address MSBs become 00. Therefore, to exit the full-power-down state, it is necessary to write to the AD7294 using this modified slave address.

After writing 0 to power down Bit D7, the slave address MSBs return to their original 11 value.

## $DATA_{HIGH}/DATA_{LOW}$ REGISTERS: 0x0B, 0x0C ($V_{IN}0$); 0x0E, 0x0F ($V_{IN}1$); 0x11, 0x12 ($V_{IN}2$); 0x14, 0x15 ($V_{IN}3$)

The $DATA_{HIGH}$ and $DATA_{LOW}$ registers for a channel are 16-bit, read/write registers (see Table 29 and Table 30). General alert is flagged by the MSB, D15. D14 to D12 are not used in the register and are set to 0s. The remaining 12 bits set the high and low limits for the relevant channel. For single-ended mode, the default values for $V_{IN}0$ to $V_{IN}3$, are 000 and FFF in binary format. For differential mode on $V_{IN}0$ to $V_{IN}3$, the default values for $DATA_{HIGH}$ and $DATA_{LOW}$ are 7FF and 800, twos complement format. Note that if the device is configured in either single-ended or differential mode and the mode is changed, the user must reprogram the limits in the $DATA_{HIGH}$ and $DATA_{LOW}$ registers.

Channel 7 to Channel 9 ($T_{SENSE}1$, $T_{SENSE}2$, and $T_{SENSE}INT$) default to 3FF and 400 for the $DATA_{HIGH}$ and $DATA_{LOW}$ limits because they are in twos complement 11-bit format.

**Table 28. Default Values for $DATA_{HIGH}$ and $DATA_{LOW}$ Registers**

| ADC Channel | Single-Ended | | Differential | |
|---|---|---|---|---|
| | $DATA_{LOW}$ | $DATA_{HIGH}$ | $DATA_{LOW}$ | $DATA_{HIGH}$ |
| $V_{IN}0$ | 000 | FFF | 800 | 7FF |
| $V_{IN}1$ | 000 | FFF | 800 | 7FF |
| $V_{IN}2$ | 000 | FFF | 800 | 7FF |
| $V_{IN}3$ | 000 | FFF | 800 | 7FF |
| $I_{SENSE}1$ | N/A | N/A | 800 | 7FF |
| $I_{SENSE}2$ | N/A | N/A | 800 | 7FF |
| $T_{SENSE}1$ | N/A | N/A | 400 | 3FF |
| $T_{SENSE}2$ | N/A | N/A | 400 | 3FF |
| $T_{SENSE}INT$ | N/A | N/A | 400 | 3FF |

**Table 29. AD7294 $DATA_{HIGH/LOW}$ Register (First Read/Write)**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| Alert_Flag | 0 | 0 | 0 | B11 | B10 | B9 | B8 |

**Table 30. AD7294 $DATA_{HIGH/LOW}$ Register (Second Read/Write)**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |

## HYSTERESIS REGISTERS: 0X0D (VIN0), 0X10 (VIN1), 0X13 (VIN2), 0X16 (VIN3)

Each hysteresis register is a 16-bit read/write register wherein only the 12 LSBs of the register are used; the MSB signals the alert event. If FFF is written to the hysteresis register, the hysteresis register enters the minimum/maximum mode, see the Alerts and Limits Theory section for further details.

**Table 31. Hysteresis Register (First Read/Write)**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| Alert_Flag | 0 | 0 | 0 | B11 | B10 | B9 | B8 |

**Table 32. Hysteresis Register (Second Read/Write)**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |

## $T_{SENSE}$ OFFSET REGISTERS (0x26 AND 0x27)

The AD7294 has temperature offset, 8-bit twos complement registers for both Remote Channel $T_{SENSE}1$ and Remote Channel $T_{SENSE}2$. It allows the user to add or subtract an offset to the temperature.

The offset registers for $T_{SENSE}1$ and $T_{SENSE}2$ are 8-bit read/write registers that store data in a twos complement format. This data is subtracted from the temperature readings taken by $T_{SENSE}1$ and $T_{SENSE}2$ temperature sensors. The offset is implemented before the values are stored in the $T_{SENSE}$ result register.

The offset registers can be used to compensate for transistors with different ideality factors because the $T_{SENSE}$ results are based on the 2N3906 transistor ideality factor. Different transistors with different ideality factors result in different offsets within the region of interest, which can be compensated for by using this register.

**Table 33. $T_{SENSE}$ Offset Data Format**

| Input | MSB D7 | D6 | D5 | D4 | D3 | D2 | D1 | LSB D0 |
|---|---|---|---|---|---|---|---|---|
| **Value (°C)** | −32 | +16 | +8 | +4 | +2 | +1 | +0.5 | +0.25 |

# I²C INTERFACE

## GENERAL I²C TIMING

Figure 50 shows the timing diagram for general read and write operations using an I²C-compliant interface.

The I²C bus uses open-drain drivers; therefore, when no device is driving the bus, both SCL and SDA are high. This is known as idle state. When the bus is idle, the master initiates a data transfer by establishing a start condition, defined as a high-to-low transition on the serial data line (SDA) while the serial clock line (SCL) remains high. This indicates that a data stream follows. The master device is responsible for generating the clock.

Data is sent over the serial bus in groups of nine bits—eight bits of data from the transmitter followed by an acknowledge bit (ACK) from the receiver. Data transitions on the SDA line must occur during the low period of the clock signal and remain stable during the high period. The receiver should pull the SDA line low during the acknowledge bit to signal that the preceding byte has been received correctly. If this is not the case, cancel the transaction.

The first byte that the master sends must consist of a 7-bit slave address, followed by a data direction bit. Each device on the bus has a unique slave address; therefore, the first byte sets up communication with a single slave device for the duration of the transaction.

The transaction can be used either to write to a slave device (data direction bit = 0) or to read data from it (data direction bit = 1). In the case of a read transaction, it is often necessary first to write to the slave device (in a separate write transaction) to tell it from which register to read. Reading and writing cannot be combined in one transaction.

When the transaction is complete, the master can keep control of the bus, initiating a new transaction by generating another start bit (high-to-low transition on SDA while SCL is high). This is known as a repeated start (Sr). Alternatively, the bus can be relinquished by releasing the SCL line followed by the SDA line. This low-to-high transition on SDA while SCL is high is known as a stop bit (P), and it leaves the I²C bus in its idle state (no current is consumed by the bus).

The example in Figure 50 shows a simple write transaction with an AD7294 as the slave device. In this example, the AD7294 register pointer is being set up ready for a future read transaction.

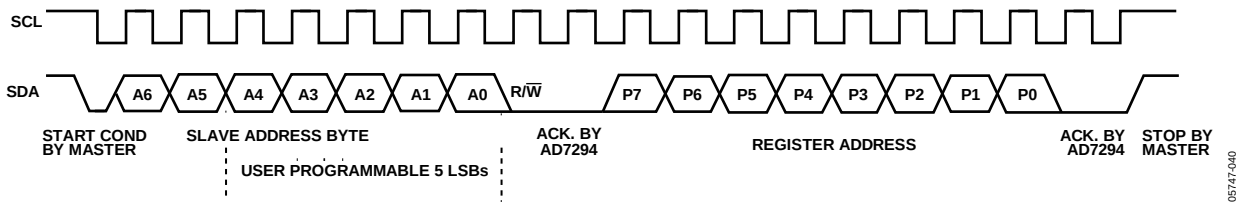


*Figure 50. General I²C Timing*

## SERIAL BUS ADDRESS BYTE

The first byte the user writes to the device is the slave address byte. Similar to all I²C-compatible devices, the AD7294 has a 7-bit serial address. The 5 LSBs are user-programmable by the 3 three-state input pins, as shown in Table 34.

In Table 34, H means tie the pin to $V_{DRIVE}$, L means tie the pin to DGND, and NC refers to a pin left floating. Note that in this final case, the stray capacitance on the pin must be less than 30 pF to allow correct detection of the floating state; therefore, any PCB trace must be kept as short as possible.

**Table 34. Slave Address Control Using Three-State Input Pins**

| AS2 | AS1 | AS0 | Slave Address (A6 to A0) |
|---|---|---|---|
| L | L | L | 0x61 |
| L | L | H | 0x62 |
| L | L | NC | 0x63 |
| L | H | L | 0x64 |
| L | H | H | 0x65 |
| L | H | NC | 0x66 |
| L | NC | L | 0x67 |
| L | NC | H | 0x68 |
| L | NC | NC | 0x69 |
| H | L | L | 0x6A |
| H | L | H | 0x6B |
| H | L | NC | 0x6C |
| H | H | L | 0x6D |
| H | H | H | 0x6E |
| H | H | NC | 0x6F |
| H | NC | L | 0x70 |
| H | NC | H | 0x71 |
| H | NC | NC | 0x72 |
| NC | L | L | 0x73 |
| NC | L | H | 0x74 |
| NC | L | NC | 0x75 |
| NC | H | L | 0x76 |
| NC | H | H | 0x77 |
| NC | H | NC | 0x78 |
| NC | NC | L | 0x79 |
| NC | NC | H | 0x7A |
| NC | NC | NC | 0x7B |

## INTERFACE PROTOCOL

The AD7294 uses the following I²C protocols.

### *Writing a Single Byte of Data to an 8-Bit Register*

The alert registers (0x05, 0x06, 0x07), power-down register (0x0A), channel sequence register (0x08), temperature offset registers (0x26, 0x27), and the command register (0x00) are 8-bit registers; therefore, only one byte of data can be written to each. In this operation, the master device sends a byte of data to the slave device (see Figure 51). To write data to the register, the command sequence is as follows:

1. The master device asserts a start condition.
2. The master sends the 7-bit slave address followed by a zero for the direction bit, indicating a write operation.
3. The addressed slave device asserts an acknowledge on SDA.
4. The master sends a register address.
5. The slave asserts an acknowledge on SDA.
6. The master sends a data byte.
7. The slave asserts an acknowledge on SDA.
8. The master asserts a stop condition to end the transaction.

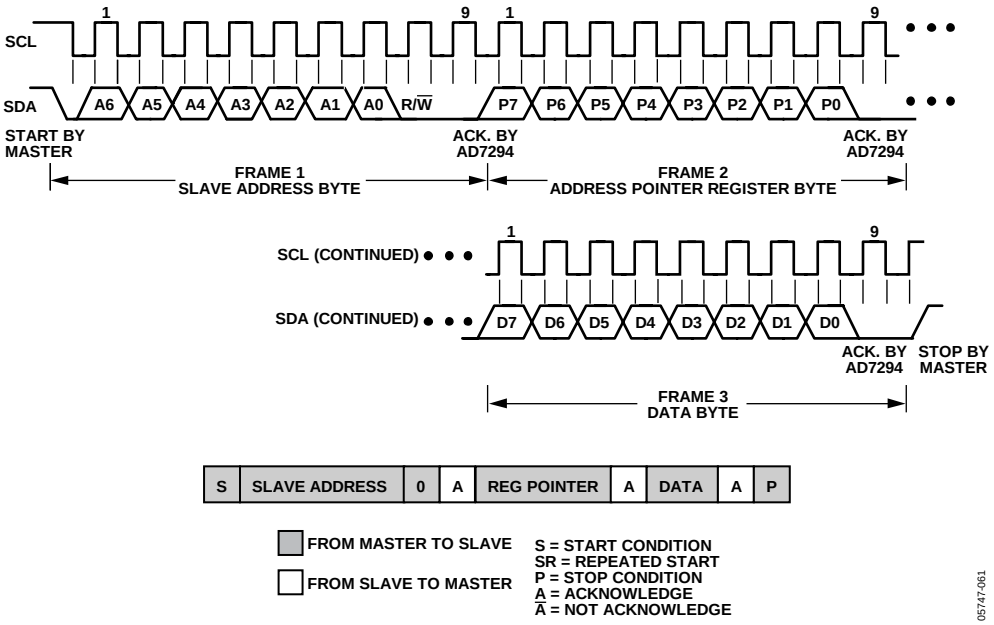


*Figure 51. Single Byte Write Sequence*

### Writing Two Bytes of Data to a 16-Bit Register

The limit and hysteresis registers (0x0B to 0x25), the result registers (0x01 to 0x04), and the configuration register (0x09) are 16-bit registers; therefore, two bytes of data are required to write a value to any one of these registers. Writing two bytes of data to one of these registers consists of the following sequence:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master sends a register address. The slave asserts an acknowledge on SDA.
5. The master sends the first data byte (most significant).
6. The slave asserts an acknowledge on SDA.
7. The master sends the second data byte (least significant).
8. The slave asserts an acknowledge on SDA.
9. The master asserts a stop condition on SDA to end the transaction.

### Writing to Multiple Registers

Writing to multiple address registers consists of the following:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device (AD7294) asserts an acknowledge on SDA.
4. The master sends a register address, for example the Alert Status Register A register address. The slave asserts an acknowledge on SDA.
5. The master sends the data byte.
6. The slave asserts an acknowledge on SDA.
7. The master sends a second register address, for example the configuration register. The slave asserts an acknowledge on SDA.
8. The master sends the first data byte.
9. The slave asserts an acknowledge on SDA.
10. The master sends the second data byte.
11. The slave asserts an acknowledge on SDA.
12. The master asserts a stop condition on SDA to end the transaction.

The previous examples detail writing to two registers only (the Alert Status Register A and the configuration register). However, the AD7294 can read from multiple registers in one write operation as shown in Figure 53.

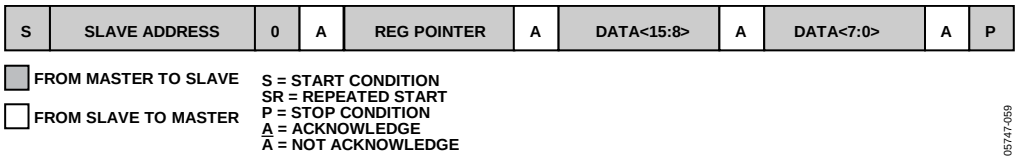


*Figure 52. Writing Two Bytes of Data to a 16-Bit Register*

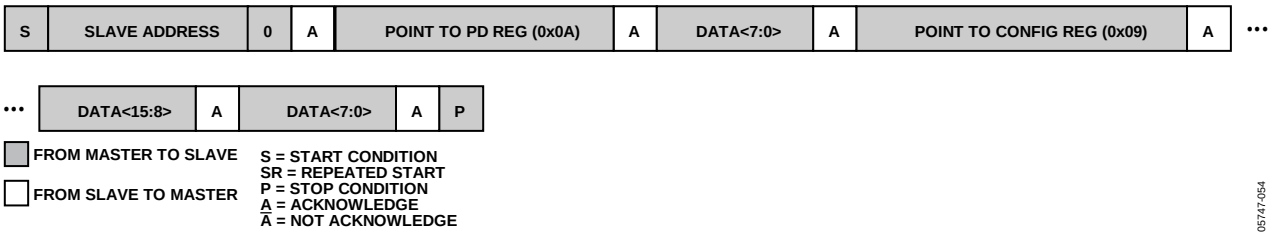


*Figure 53. Writing to Multiple Registers*

### Reading Data from an 8-Bit Register

Reading the contents from any of the 8-bit registers is a single byte read operation, as shown in Figure 55. In this protocol, the first part of the transaction writes to the register pointer. When the register address has been set up, any number of reads can be performed from that particular register without having to write to the address pointer register again. When the required number of reads is completed, the master should not acknowledge the final byte. This tells the slave to stop transmitting, allowing a stop condition to be asserted by the master. Further reads from this register can be performed in a future transaction without having to rewrite to the register pointer.

If a read from a different address is required, the relevant register address has to be written to the address pointer register, and again, any number of reads from this register can then be performed. In the next example, the master device receives two bytes from a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the read bit (high).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master receives a data byte.
5. The master asserts an acknowledge on SDA.
6. The master receives another 8-bit data byte.
7. The master asserts a no acknowledge (NACK) on SDA to inform the slave that the data transfer is complete.
8. The master asserts a stop condition on SDA, and the transaction ends.

### Reading Two Bytes of Data from a 16-Bit Register

In this example, the master device reads three lots of two-byte data from a slave device, but as many lots consisting of two-bytes can be read as required. This protocol assumes that the particular register address has been set up by a single byte write operation to the address pointer register (see the previous read example).

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the read bit (high).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master receives a data byte.
5. The master asserts an acknowledge on SDA.
6. The master receives a second data byte.
7. The master asserts an acknowledge on SDA.
8. The master receives a data byte.
9. The master asserts an acknowledge on SDA.
10. The master receives a second data byte.
11. The master asserts an acknowledge on SDA.
12. The master receives a data byte.
13. The master asserts an acknowledge on SDA.
14. The master receives a second data byte.
15. The master asserts a no acknowledge on SDA to notify the slave that the data transfer is complete.
16. The master asserts a stop condition on SDA to end the transaction.

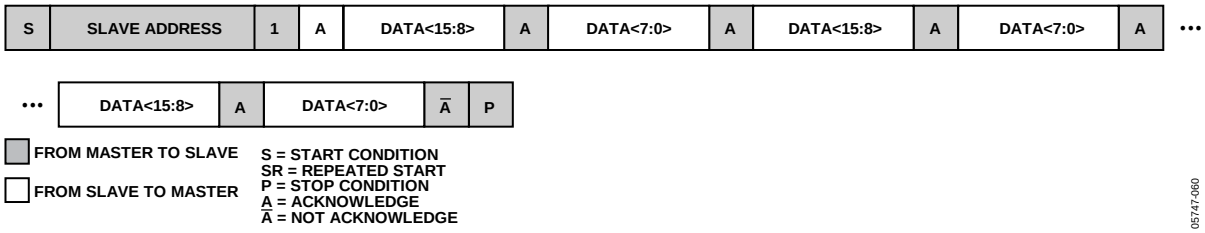


*Figure 54. Reading Three Lots of Two Bytes of Data from the Conversion Result Register*

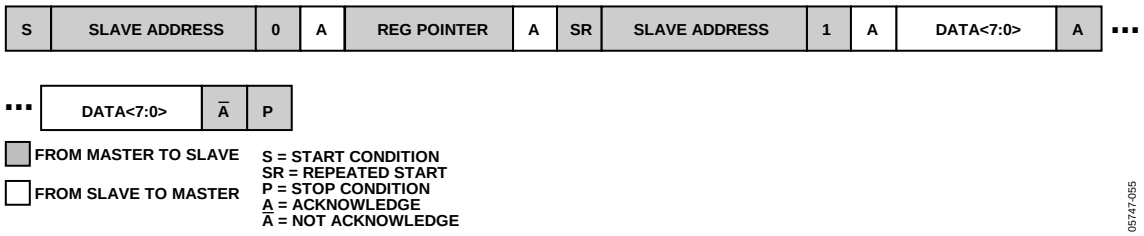


*Figure 55. Reading Two Single Bytes of Data from a Selected Register*

# MODES OF OPERATION

There are two different methods of initiating a conversion on the AD7294: command mode and autocycle mode.

## COMMAND MODE

In command mode, the AD7294 ADC converts on-demand on either a single channel or a sequence of channels. To enter this mode, the required combination of channels is written into the command register (0x00). The first conversion takes place at the end of this write operation, in time for the result to be read out in the next read operation. While this result is being read out, the next conversion in the sequence takes place, and so on.

To exit the command mode, the master should not acknowledge the final byte of data. This stops the AD7294 transmitting, allowing the master to assert a stop condition on the bus. It is therefore important that, after writing to the command register, a repeated start (Sr) signal be used rather than a stop (P) followed by a start (S) when switching to read mode; otherwise, the command mode exits after the first conversion.

After writing to the command register, the register pointer is returned to its previous value. If a new pointer value is required (typically the ADC Result Register 0x01), it can be written immediately following the command byte. This extra write operation does not affect the conversion sequence because the second conversion triggers only at the start of the first read operation.

The maximum throughput that can be achieved using this mode with a 400 kHz I²C clock is (400 kHz/18) = 22.2 kSPS.

Figure 56 shows the command mode converting on a sequence of channels including $V_{IN}0$, $V_{IN}1$, and $I_{SENSE}1$.

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device (AD7294) asserts an acknowledge on SDA.
4. The master sends the Command Register Address 0x00. The slave asserts an acknowledge on SDA.
5. The master sends the Data Byte 0x13, which selects the $V_{IN}0$, $V_{IN}1$, and $I_{SENSE}1$ channels.
6. The slave asserts an acknowledge on SDA.
7. The master sends the result register address (0x01). The slave asserts an acknowledge on SDA.
8. The master sends the 7-bit slave address followed by the write bit (high).
9. The slave (AD7294) asserts an acknowledge on SDA.
10. The master receives a data byte, which contains the alert_flag bit, the channel ID bits, and the four MSBs of the converted result for Channel $V_{IN}0$. The master then asserts an acknowledge on SDA.
11. The master receives the second data byte, which contains the eight LSBs of the converted result for Channel $V_{IN}0$. The master then asserts on acknowledge on SDA.
12. Point 10 and Point 11 repeat for Channel $V_{IN}1$ and Channel $I_{SENSE}1$.
13. Once the master has received the results from all the selected channels, the slave again converts and outputs the result for the first channel in the selected sequence. Point 10 to Point 12 are repeated.
14. The master asserts a no acknowledge on SDA and a stop condition on SDA to end the conversion and exit command mode.

The AD7294 automatically exits command mode if no read occurs in a 5 ms period. To change the conversion sequence, rewrite a new sequence to the command mode.

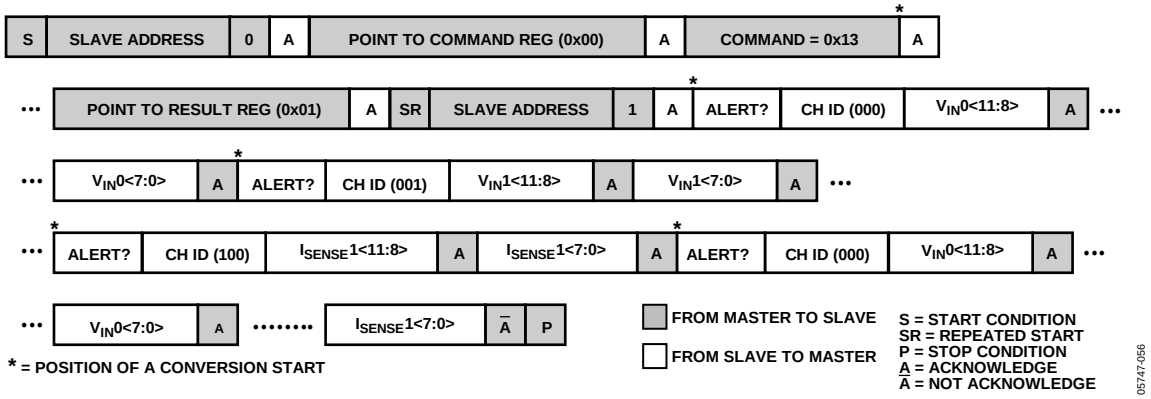


*Figure 56. Command Mode Operation*

## AUTOCYCLE MODE

The AD7294 can be configured to convert continuously on a programmable sequence of channels making it the ideal mode of operation for system monitoring. These conversions take place in the background approximately every 50 µs, and are transparent to the master. Typically, this mode is used to automatically monitor a selection of channels with either the limit registers programmed to signal an out-of-range condition via the alert function or the minimum/maximum recorders tracking the variation over time of a particular channel. Reads and writes can be performed at any time (the ADC Result Register 0x01 contains the most recent conversion result).

On power up, this mode is disabled. To enable this mode, write to Bit D12 in the configuration register (0x09) and select the desired channels for conversion in the channel sequence register (0x08).

If a command mode conversion is required while the autocycle mode is active, it is necessary to disable the autocycle mode before proceeding to the command mode. This is achieved either by clearing Bit D12 of the configuration register or by writing 0x00 to the channel sequence register. When the command mode conversion is complete, the user must exit command mode by issuing a stop condition before reenabling autocycle mode.

When switching out of autocycle mode to command mode, the temperature sensor must be given sufficient time to settle and complete a new temperature integration cycle. Therefore, temperature sensor conversions performed within the first 500 ms after switching from autocycle mode to command mode may result in false temperature high and low alarms being triggered. It is recommended to disable temperature sensor alarms for the first 500 ms after mode switching by writing 0x400 to the $DATA_{LOW}$ $T_{SENSE}x$ register and 0x3FF to the $DATA_{HIGH}$ register $T_{SENSE}x$. The temperature sensor alerts should be reconfigured to the desired alarm level once the 500 ms has elapsed. Alternatively, temperature alerts triggered during the first 500 ms after mode switching should be ignored.

# ALERTS AND LIMITS THEORY

## ALERT_FLAG BIT

The alert_flag bit indicates whether the conversion result being read or any other channel result has violated the limit registers associated with it. If an alert occurs and the alert_flag bit is set, the master can read the alert status register to obtain more information on where the alert occurred.

## ALERT STATUS REGISTERS

The alert status registers are 8-bit read/write registers that provide information on an alert event. If a conversion results in activation of the ALERT/BUSY pin or the alert_flag bit in the result register or $T_{SENSE}$ registers, the alert status register can be read to get more information (see Figure 57 for the alert register structure).

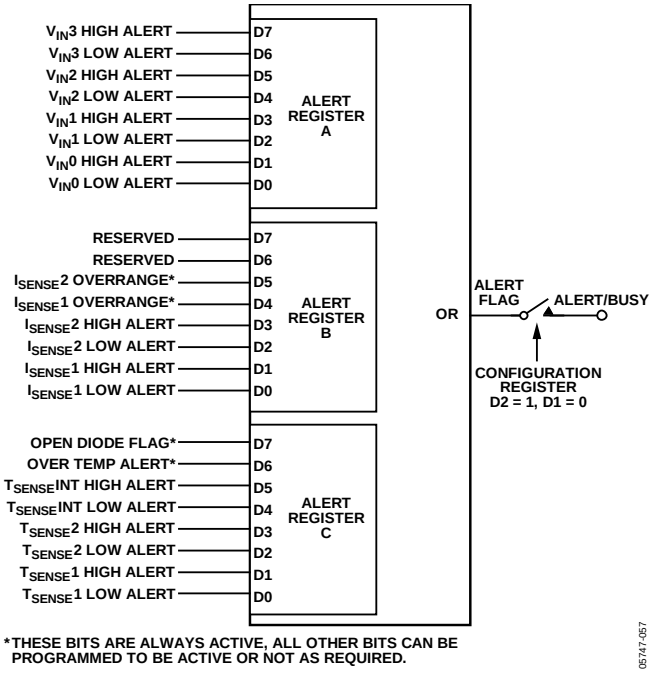


*Figure 57. Alert Register Structure*

Register A (see Table 19) consists of four channels with two status bits per channel, one corresponding to each of the $DATA_{HIGH}$ and $DATA_{LOW}$ limits. It stores the alert event data for $V_{IN}3$ to $V_{IN}0$, which are the standard voltage inputs. When the content of this register is read, any bit with a status of 1 indicates a violation of its associated limit; that is, it identifies the channel and whether the violation occurred on the upper or lower limit. If a second alert event occurs on another channel before the content of the alert register has been read, the bit corresponding to the second alert event is also set.

Register B (see Table 20) consists of three channels also with two status bits per channel, representing the specified $DATA_{HIGH}$ and $DATA_{LOW}$ limits. Bits[D3:D0] correspond to the high and low limit alerts for the current sense inputs. Bit D4 and Bit D5 represent the $I_{SENSE}1$ OVERRANGE and $I_{SENSE}2$ OVERRANGE of $V_{REF}/10.41$. During power-up, it is possible for the fault outputs to be triggered, depending on which supply comes up first. Clearing these bits as part of the initialization routine is recommended on power-up by writing a 1 to both D4 and D5.

Internal circuitry in the AD7294 can alert if either the D1± or the D2± input pins for the external temperature sensor are open circuit. The most significant bit of Register C (see Table 21) alerts the user when an open diode flag occurs on the external temperature sensors. If the internal temperature sensor detects an AD7294 die temperature greater than 150°C, the overtemperature alert bit, Bit D6 in Register C, is set and the DAC outputs are set to a high impedance sate. The remaining six bits in Register 6 store alert event data for $T_{SENSE}1$, $T_{SENSE}2$, and $T_{SENSE}INT$ with two status bits per channel, one corresponding to each of the $DATA_{HIGH}$ and $DATA_{LOW}$ limits.

To clear the full content of any one of the alert registers, write a code of FF (all ones) to the relevant registers. Alternatively, the user can write to the respective alert bit in the selected alert register to clear the alert associated with that bit. The entire contents of all the alert status registers can be cleared by writing a 1 to Bit D1 and Bit D2 in the configuration register, as shown in Table 24. However, this operation then enables the ALERT/BUSY pin for subsequent conversions.

## $DATA_{HIGH}$ AND $DATA_{LOW}$ MONITORING FEATURES

The AD7294 signals an alert (in either hardware via the ALERT/BUSY pin, software via the alert_flag bit, or both, depending on the configuration) if the result moves outside the upper or lower limit set by the user.

The $DATA_{HIGH}$ register stores the upper limit that activates the ALERT/BUSY output pin and/or the alert_flag bit in the conversion result register. If the conversion result is greater than the value in the $DATA_{HIGH}$ register, an alert occurs. The $DATA_{LOW}$ register stores the lower limit that activates the ALERT/BUSY output pin and/or the alert_flag bit in the conversion result register. If the conversion result is less than the value in the $DATA_{LOW}$ register, an alert occurs.

An alert associated with either the $DATA_{HIGH}$ or $DATA_{LOW}$ register is cleared automatically once the monitored signal is back in range; that is, the conversion result is between the limits. The content of the alert register is updated after each conversion. A conversion is performed every 50 µs in autocycle mode, so the content of the alert register may change every 50 µs. If the ALERT pin signals an alert event and the content of the alert register is not read before the next conversion is complete, the content of the register may be changed if the signal being monitored returns between the prespecified limits. In these circumstances, the ALERT pin no longer signals the occurrence of an alert event.

The hysteresis register can be used to avoid flicker on the ALERT/BUSY pin. If the hysteresis function is enabled, the conversion result must return to a value of at least N LSB below the $DATA_{HIGH}$ register value, or N LSB above the $DATA_{LOW}$ register value for the ALERT/BUSY output pin and alert_flag bit to be reset. The value of N is taken from the 12-bit hysteresis register associated with that channel. By setting the hysteresis register to a code close to the maximum output code for the ADC, that is, 0x77D, $DATA_{HIGH}$ or $DATA_{LOW}$ alerts do not clear automatically by the AD7294.

Bit D11 of the $T_{SENSE}$ $DATA_{HIGH}$ or $DATA_{LOW}$ limit registers is the diode open-circuit flag. If this bit is set to 0, it indicates the presence of an open circuit between the Dx+ and Dx− pins. An alert triggered on either $I_{SENSE}$ OVERRANGE pin remains until it is cleared by the user writing to the alert register. The contents of the $DATA_{HIGH}$ and $DATA_{LOW}$ registers are reset to their default values on power-up (see Table 28).

## HYSTERESIS

The hysteresis value determines the reset point for the ALERT/BUSY pin and/or alert_flag bit if a violation of the limits occurs. The hysteresis register stores the hysteresis value, N, when using the limit registers. Each pair of limit registers has a dedicated hysteresis register. For example, if a hysteresis value of 8 LSBs is required on the upper and lower limits of $V_{IN}0$, the 16-bit word 0000 0000 0000 1000 should be written to the hysteresis register of $V_{IN}0$ (see Table 9). On power-up, the hysteresis registers contain a value of 8 LSBs for nontemperature result registers and 8°C, or 32 LSBs, for the $T_{SENSE}$ registers. If a different hysteresis value is required, that value must be written to the hysteresis register for the channel in question.

The advantage of having hysteresis registers associated with each of the limit registers is that it prevents chatter on the alert bits associated with each ADC channel. Figure 58 shows the limit checking operation.

### *Using the Limit Registers to Store Minimum/Maximum Conversion Results*

If FFF is written to the hysteresis register for a particular channel, the $DATA_{HIGH}$ and $DATA_{LOW}$ registers for that channel no longer act as limit registers as previously described, but act as storage registers for the maximum and minimum conversion results. This function is useful when an alert signal is not required in an application, but it is still required to monitor the minimum and maximum conversion values over time. Note that on power-up, the contents of the $DATA_{HIGH}$ register for each channel are set to maximum code, whereas the contents of the $DATA_{LOW}$ registers are set to minimum code by default.

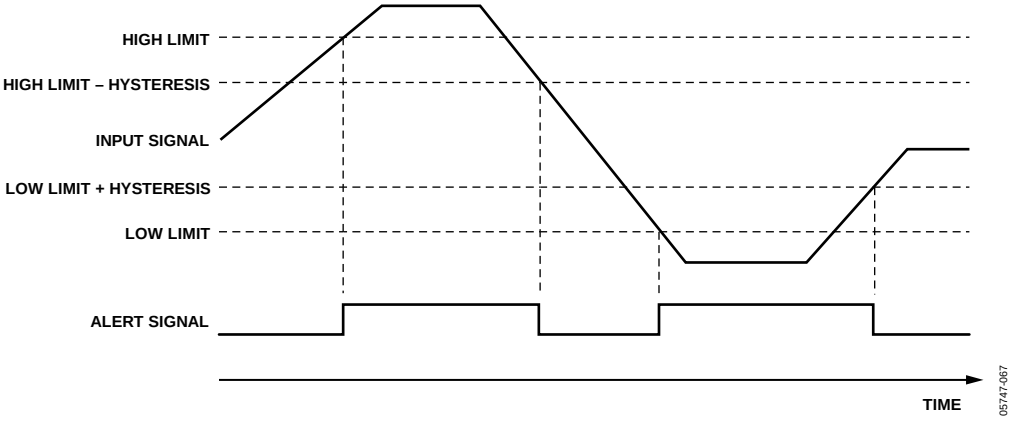


*Figure 58. Limit Checking*

# APPLICATIONS INFORMATION

The AD7294 contains all the functions required for general-purpose monitoring and control of current, voltage, and temperature. With its 59.4 V maximum common-mode range, the device is useful in industrial and automotive applications where current sensing in the presence of a high common-mode voltage is required. For example, the device is ideally suited for monitoring and controlling a power amplifier in a cellular base station.

## BASE STATION POWER AMPLIFIER MONITOR AND CONTROL

The AD7294 is used in a power amplifier signal chain to achieve the optimal bias condition for the LDMOS transistor. The main factors influencing the bias conditions are temperature, supply voltage, gate voltage drift, and general processing parameters. The overall performance of a power amplifier configuration is determined by the inherent tradeoffs required in efficiency, gain, and linearity. The high level of integration offered by the AD7294 allows the use of a single chip to dynamically control the drain bias current to maintain a constant value over temperature and time, thus significantly improving the overall performance of the power amplifier. The AD7294 incorporates the functionality of eight discrete components bringing considerable board area savings over alternative solutions.

The circuit in Figure 59 is a typical system connection diagram for the AD7294. The device monitors and controls the overall performance of two final stage amplifiers. The gain control and phase adjustment of the driver stage are incorporated in the application and are carried out by the two available uncommitted outputs of the AD7294. Both high-side current senses measure the amount of current on the respective final stage amplifiers. The comparator outputs, $I_{SENSE}1$ OVERRANGE and $I_{SENSE}2$ OVERRANGE pins, are the controlling signals for switches on the RF inputs of the LDMOS power FETs. If the high-side current sense reads a value above a specified limit compared with the setpoint, the RF IN signal is switched off by the comparator.

By measuring the transmitted power (Tx) and the received power (Rx), the device can dynamically change the drivers and PA signal to optimize performance. This application requires a logarithmic detector/controller, such as Analog Devices AD8317 or AD8362.

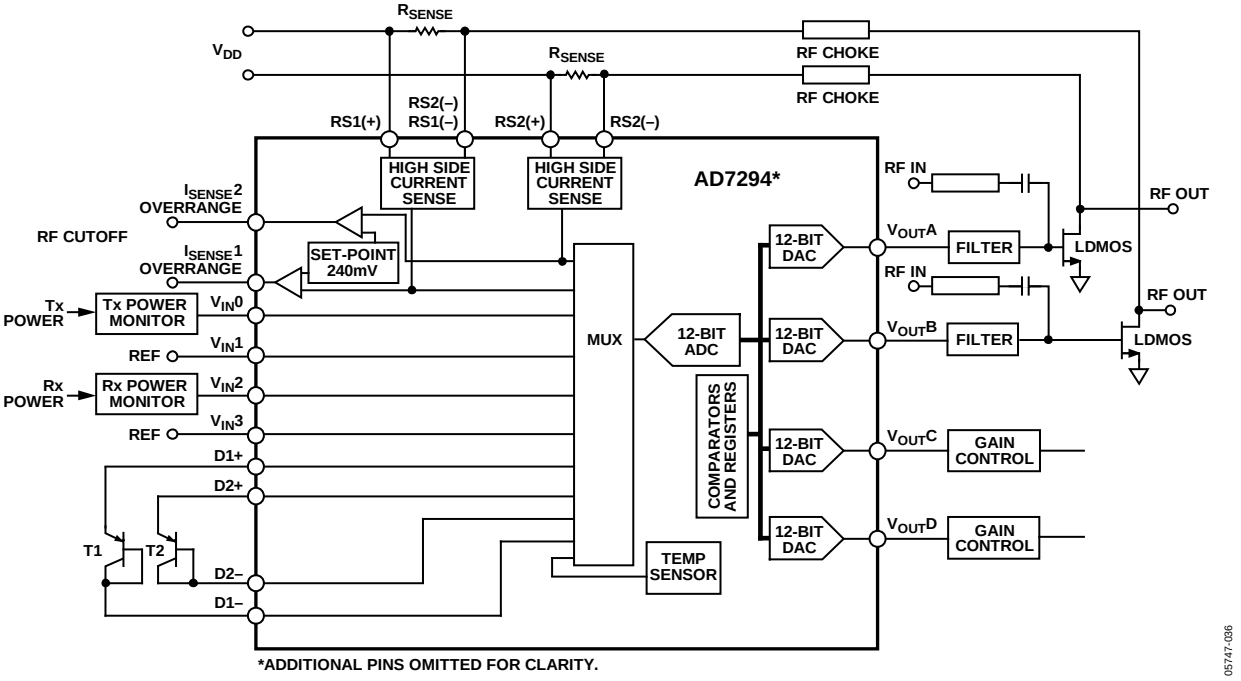


*Figure 59. Typical HPA Monitor and Control Application*

## GAIN CONTROL OF POWER AMPLIFIER

In gain control mode, a setpoint voltage, proportional in dB to the desired output power, is applied to a power detector such as the AD8362. A sample of the output power from the power amplifier (PA), through a directional coupler and attenuator (or by other means), is fed to the input of the AD8362. The VOUT is connected to the gain control terminal of the PA, see Figure 60. Based on the defined relationship between VOUT and the RF input signal, the AD8362 adjusts the voltage on VOUT (VOUT is now an error amplifier output) until the level at the RF input corresponds to the applied VSET. The AD7294 completes a feedback loop that tracks the output of the AD8362 and adjusts the VSET input of the AD8362 accordingly.

VOUT of the AD8362 is applied to the gain control terminal of the power amplifier. For this output power control loop to be stable, a ground referenced capacitor must be connected to the CLPF pin. This capacitor integrates the error signal (which is actually a current) that is present when the loop is not balanced. In a system where a variable gain amplifier (VGA) or variable voltage attenuator (VVA) feeds the power amp, only one AD8362 is required. In such a case, the gain on one of the devices (VVA, PA) is fixed and $V_{OUT}$ feeds the control input of the other.

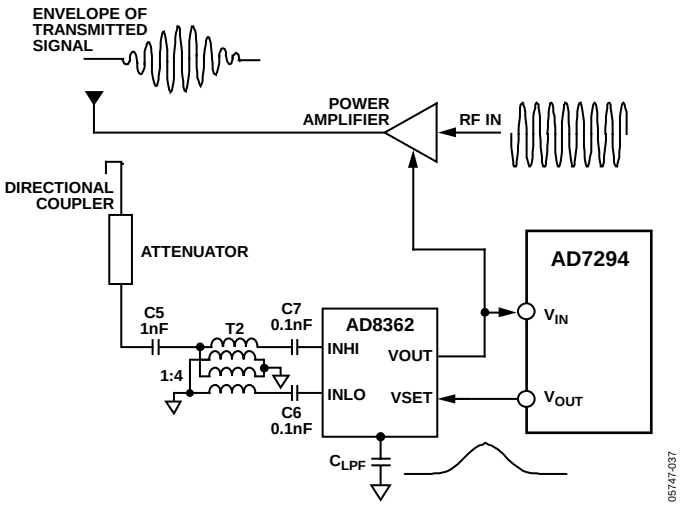


*Figure 60. Setpoint Controller Operation*

# LAYOUT AND CONFIGURATION

## POWER SUPPLY BYPASSING AND GROUNDING

For optimum performance, carefully consider the power supply and ground return layout on any PCB where the AD7294 is used. The PCB containing the AD7294 should have separate analog and digital sections, each having its own area of the board. The AD7294 should be located in the analog section on any PCB.

Decouple the power supply to the AD7294 to ground with 10 µF and 0.1 µF capacitors. Place the capacitors as physically close as possible to the device, with the 0.1 µF capacitor ideally right up against the device. It is important that the 0.1 µF capacitor have low effective series resistance (ESR) and low effective series inductance (ESL); common ceramic types of capacitors are suitable. The 0.1 µF capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching. The 10 µF capacitors are the tantalum bead type.

The power supply line should have as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Shield clocks and other components with fast switching digital signals from other parts of the board by a digital ground. Avoid crossover of digital and analog signals, if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects on the board. The best board layout technique is the microstrip technique where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side; however, this is not always possible with a 2-layer board.

### *Layout Considerations for External Temperature Sensors*

Power amplifier boards can be electrically noisy environments. Take care to protect the analog inputs from noise, particularly when measuring the very small voltages from a remote diode sensor.

Take the following precautions:

- Place the remote sensing diode as close as possible to the AD7294. If the worst noise sources are avoided, this distance can be 4 inches to 8 inches.
- Route the D+ and D− tracks close together, in parallel, with grounded guard tracks on each side. Provide a ground plane under the tracks, if possible.
- Use wide tracks to minimize inductance and reduce noise pickup. A 10 mil track minimum width and spacing is recommended, as shown in Figure 61.

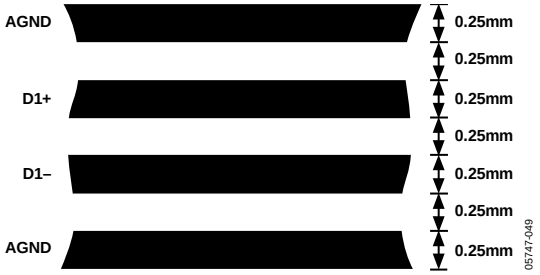


*Figure 61. Arrangement of Signal Tracks*

- Try to minimize the number of copper/solder joints because they can cause thermocouple effects. Where copper/solder joints are used, make sure that they are in both the Dx+ and Dx− path and are at the same temperature.
- Place a 10 pF capacitor between the base and emitter of the discrete diode, as close as possible to the diode.
- If the distance to the remote sensor is more than 20 cm, the use of twisted-pair cable is recommended.

Because the measurement technique uses switched current sources, excessive cable and/or filter capacitance can affect the measurement. When using long cables, the filter capacitor can be reduced or removed.

# OUTLINE DIMENSIONS

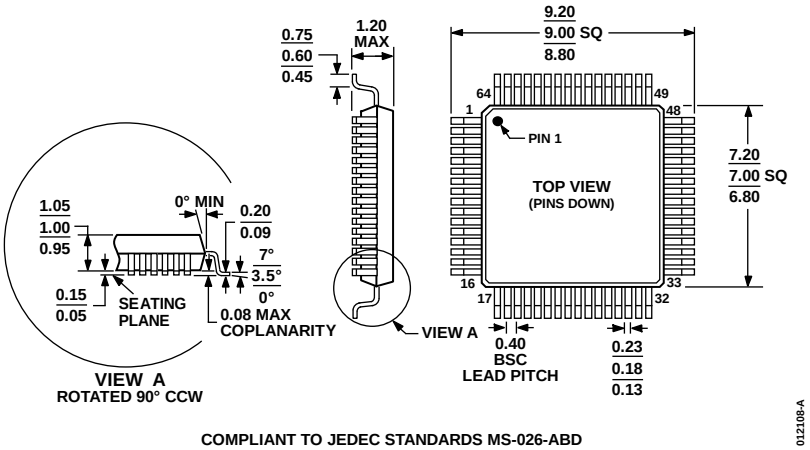


*Figure 62. 64-Lead Thin Plastic Quad Flat Package [TQFP]*
*(SU-64-1)*
*Dimensions shown in millimeters*

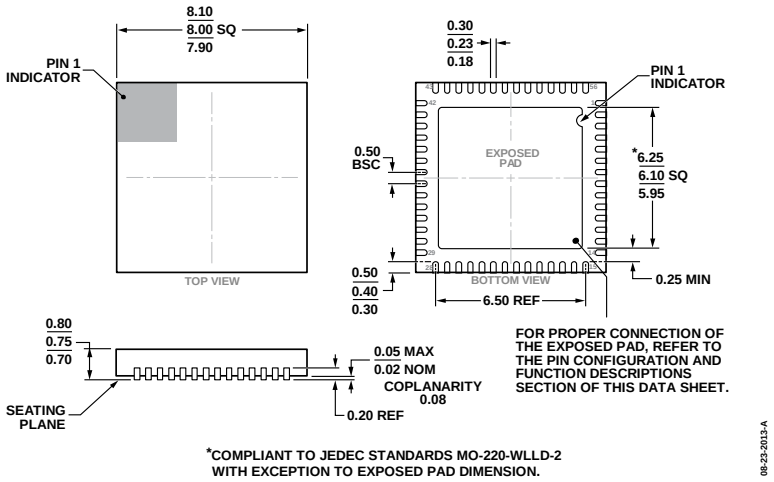


*Figure 63. 56-Lead Lead Frame Chip Scale Package [LFCSP]*
*8 mm × 8 mm body and 0.75mm Package Height*
*(CP-56-11)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| AD7294BSUZ | −40°C to +105°C | 64-Lead Thin Plastic Quad Flat Package [TQFP] | SU-64-1 |
| AD7294BSUZRL | −40°C to +105°C | 64-Lead Thin Plastic Quad Flat Package [TQFP] | SU-64-1 |
| AD7294BCPZ | −40°C to +105°C | 56-Lead Lead Frame Chip Scale Package [LFCSP] | CP-56-11 |
| AD7294BCPZRL | −40°C to +105°C | 56-Lead Lead Frame Chip Scale Package [LFCSP] | CP-56-11 |
| EVAL-AD7294EBZ | | Evaluation Board | |

[1] Z = RoHS Compliant Part.

## NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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