XC6129 Series

ETR0222-002

Voltage Detector with Delay Time Adjustable

■GENERAL DESCRIPTION

XC6129 series is an ultra small highly accurate voltage detector with external capacitor type delay function.
The device includes a highly accurate reference voltage source, manufactured using CMOS process and laser trimming technology, it maintains low power consumption and high accuracy. The device includes the built-in delay circuit. A release delay time or detect delay time can be set freely by connecting an external delay capacitor to Cd pin.
There are two kinds of the output configuration for the XC6129 such as CMOS or N-channel open drain. The series has a function to prevent an indefinite operation. Therefore, when the input pin voltage is under minimum operating voltage, the function controls an output pin voltage in the indefinite operation less than 0.4V (MAX.). Also, the series allows a choice of an output logic when detection; therefore, it is suitable for various electric devices using Microcontrollers.

Ultra small package USPN-4 and SSOT-24 (standard) are ideally suited for small design of portable devices and high densely mounting applications.

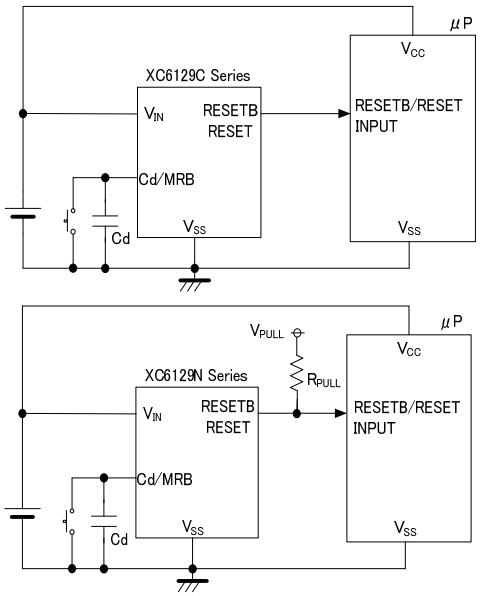
■APPLICATIONS

- Microprocessor
- Logic circuit reset circuitry
- Battery check
- Charge voltage monitors
- Memory battery back-up switch circuits
- System power on reset
- Power failure detection circuits
- Delay circuit

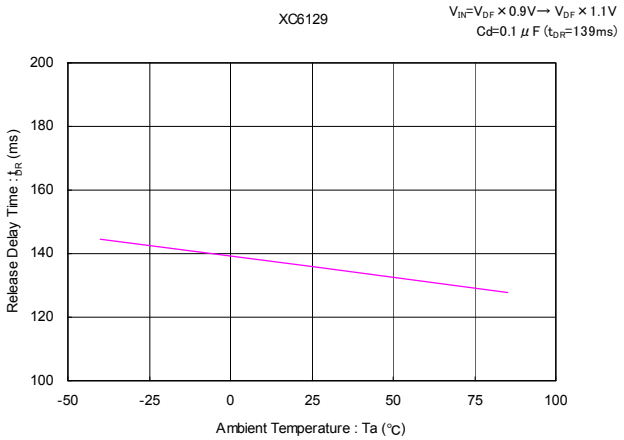
■FEATURES

High Accuracy	:	±0.8% (Ta=25℃)
Temperature Characteristic	:	±50ppm/℃ (TYP.)
Hysteresis Width	:	V_{DF}x5% (TYP.) or Less than V_{DF}x1%
Low Power Consumption	:	0.42μA TYP. (at Detect, V_{DF}=2.7V)
		0.58μA TYP. (at Release, V_{DF}=2.7V)
Detect Voltage Options	:	1.5V～5.5V (0.1V increments)
Operating Voltage Range	:	1.3V～6.0V
Output Configuration	:	CMOS or N-channel Open Drain
Output Logic	:	Active High or Active Low
Release Delay Time	:	13.9ms (Cd=0.01μF, R_P=2MΩ)
Detect Delay Time	:	17.9ms (Cd=0.01μF, Rn=2MΩ)
Manual Reset Input	:	When Cd pin is “L” level, detect state
Operating Ambient Temperature	:	-40℃ ～ +85℃
Packages	:	USPN-4, SSOT-24
Environmentally Friendly	:	EU RoHS Compliant, Pb Free

■TYPICAL APPLICATION CIRCUITS

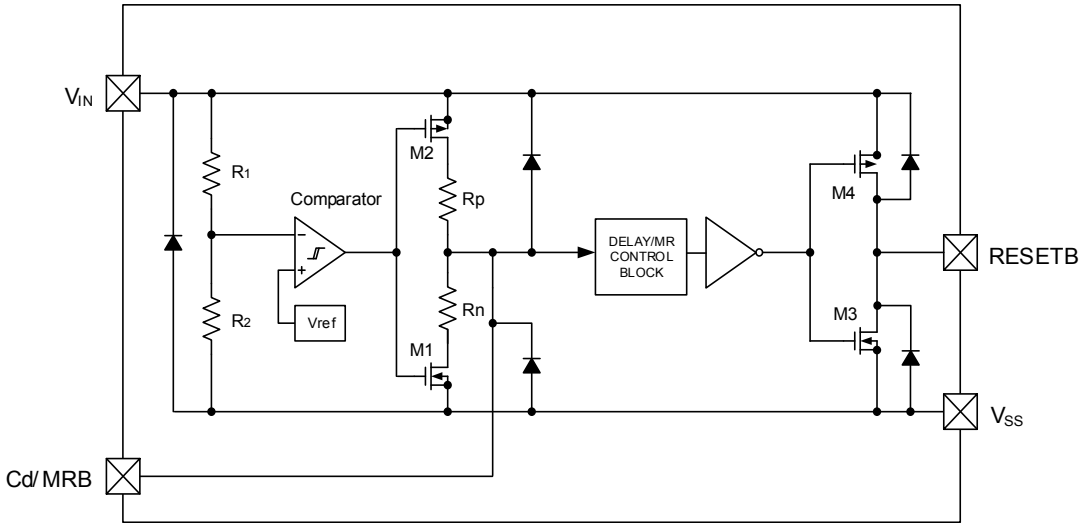


■ TYPICAL PERFORMANCE CHARACTERISTICS

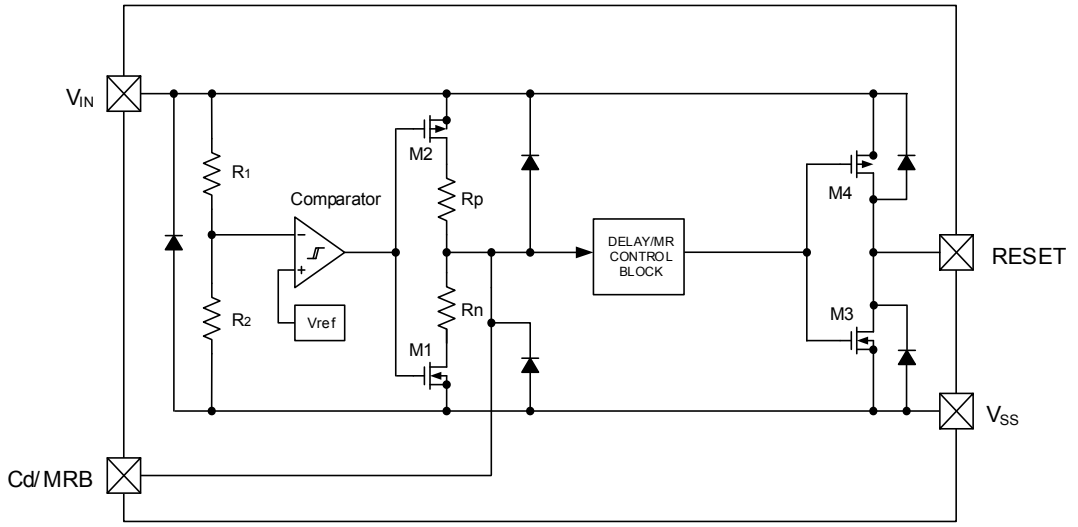


■BLOCK DIAGRAMS

1) XC6129C Series (Type A/B/C/D/E/F)



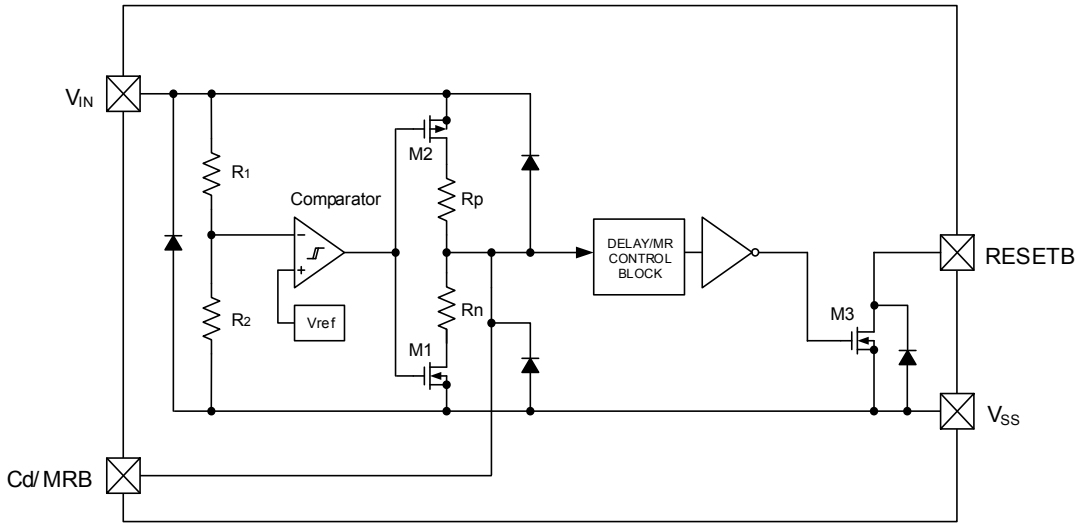
2) XC6129C Series (Type G/J/L)



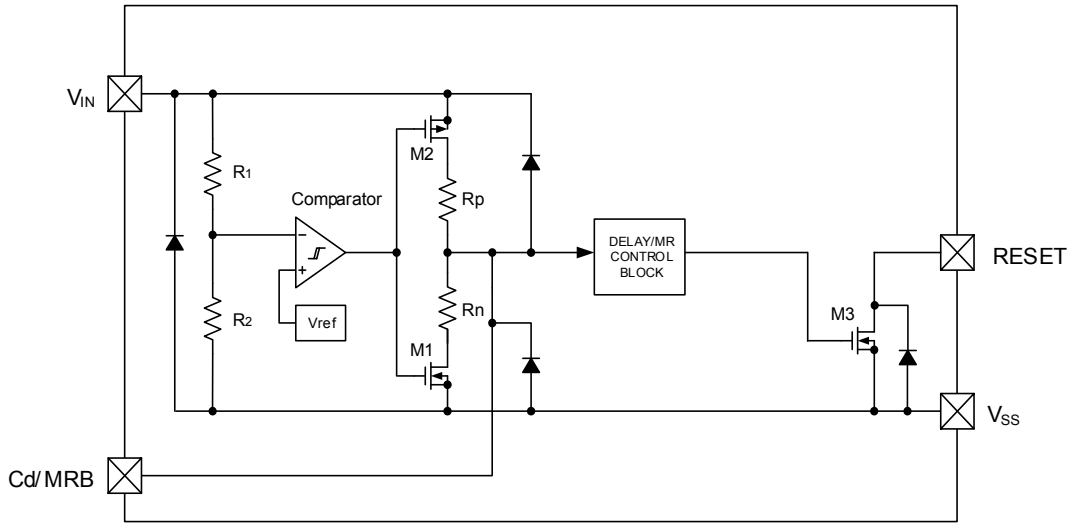
* Diodes inside the circuits are ESD protection diodes and parasitic diodes.

■BLOCK DIAGRAMS

3) XC6129N Series (Type A/C/E)



4) XC6129N Series (Type G/J/L)



* Diodes inside the circuits are ESD protection diodes and parasitic diodes.

■PRODUCT CLASSIFICATION

●Ordering Information

XC6129①②③④⑤⑥−⑦(*1)

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Output Configuration	C	CMOS output
		N	Nch open drain output
②③	Detect Voltage	15~55	e.g. 1.8V → ②=1, ③=8
④	Type	A	Refer to Selection Guide
		B	
		C	
		D	
		E	
		F	
		G	
		J	
		L	
⑤⑥−⑦ (*1)	Packages (Order Unit)	NR-G	SSOT-24 (3,000/Reel)
		7R-G	USPN-4 (5,000/Reel)

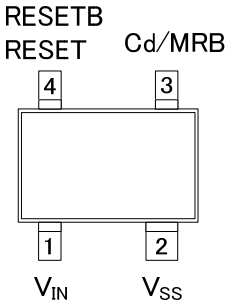
(*1) The “-G” suffix denotes Halogen and Antimony free as well as being fully EU RoHS compliant.

●Selection Guide

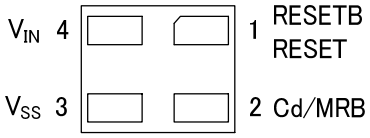
TYPE	RESETB/RESET OUTPUT	HYSTERESIS WIDTH	RELEASE DELAY	DETECT DELAY	Undefined Operation Protect
A	Reset Active Low	5% (TYP.)	Yes	No	No
B					Yes (*2)
C			No	Yes	No
D					Yes (*2)
E			Yes	Yes	No
F					Yes (*2)
G	Reset Active High		Yes	No	No
J			No	Yes	
L			Yes	Yes	

(*2) Only supported with CMOS output.

■PIN CONFIGURATION



SSOT-24
(TOP VIEW)



USPN-4
(BOTTOM VIEW)

■PIN ASSIGNMENT

PIN NUMBER		PIN NAME	FUNCTIONS
SSOT-24	USPN-4		
1	4	V_{IN}	Power Input
2	3	V_{SS}	Ground
3	2	Cd/MRB	Adjustable Pin for DelayTime /Manual Reset
4	1	RESETB	Reset Output (Active Low) (*1)
		RESET	Reset Output (Active High) (*2)

(*1) Type A～F (Refer to the ④ in Ordering Information table)
(*2) Type G～M (Refer to the ④ in Ordering Information table)

■FUNCTION CHART

PIN NAME	SIGNAL	STATUS
Cd/MRB	L	Forced Reset
	H	Release
	OPEN	Normal Operation

Refer to the table below.

1) Output Logic: Active Low

●Function Chart

V_{IN}	$V_{Cd//MRB}$	Transition of V_{RESETB} Condition
$V_{IN} \geqq V_{DF}+V_{HYS}$	$V_{Cd/MRB} \leqq V_{MRL}$	Reset (Low Level) (*1)
	$V_{Cd/MRB} \geqq V_{MRH}$	Release (High Level) (*2)
$V_{IN} \leqq V_{DF}$	$V_{Cd/MRB} \leqq V_{MRL}$	Reset (Low Level) (*1)
	$V_{Cd/MRB} \geqq V_{MRH}$	Undefined (*3)

2) Output Logic: Active High

●Function Chart

V_{IN}	$V_{Cd/MRB}$	Transition of V_{RESET} Condition
$V_{IN} \geqq V_{DF}+V_{HYS}$	$V_{Cd/MRB} \leqq V_{MRL}$	Reset (High Level) (*2)
	$V_{Cd/MRB} \geqq V_{MRH}$	Release (Low Level) (*1)
$V_{IN} \leqq V_{DF}$	$V_{Cd/MRB} \leqq V_{MRL}$	Reset (High Level) (*2)
	$V_{Cd/MRB} \geqq V_{MRH}$	Undefined (*3)

(* 1) CMOS output: V_{IN} × 0.1 or less, N-ch open drain output, pull-up voltage × 0.1 or less.

(* 2) CMOS output: V_{IN} × 0.9 or higher, N-ch open drain output, pull-up voltage × 0.9 or higher.

(* 3) Refer to the OPERATING DESCRIPTION <Manual reset function> below.

■ABSOLUTE MAXIMUM RATINGS

Ta=25℃

PARAMETER		SYMBOL	RATINGS	UNITS
Input Voltage		V_{IN}	-0.3～+6.5	V
Output Current	XC6129C (*1)	I_{RBOUT}	±50	mA
	XC6129N (*2)	I_{ROUT}	50	
Output Voltage	XC6129C (*1)	V_{RESETB}	V_{SS}-0.3～V_{IN}+0.3 or +6.5 (*3)	V
	XC6129N (*2)	V_{RESET}	V_{SS}-0.3～+6.5	
Cd/MRB Pin Voltage		$V_{Cd/MRB}$	V_{SS}-0.3～V_{IN}+0.3	V
Cd/MRB Pin Current		$I_{Cd/MRB}$	±5	mA
Power Dissipation	SSOT-24	Pd	150	mW
	USPN-4		100	
Operating Ambient Temperature		Topr	-40～+85	℃
Storage Temperature		Tstg	-55～+125	℃

* All voltages are described based on the V_{SS}.

(*1) CMOS Output

(*2) N-ch Open Drain Output

(*3) The maximum value should be either V_{IN}+0.3 or +6.5 in the lowest.

■ELECTRICAL CHARACTERISTICS

●XC6129xxxA~XC6129xxxF Series (Output Logic: Active Low)

Ta=25℃

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Detect Voltage	V_{DF}	$V_{DF(T)}$ (*1)=1.5V～5.5V	$V_{DF(T)}$×0.992	$V_{DF(T)}$	$V_{DF(T)}$×1.008	V	①
			E-1 (*2)				
Temperature Characteristics	$\Delta V_{DF}/(\Delta Topr \cdot V_{DF})$	-40℃≦Topr≦85℃	-	±50	-	ppm/℃	①
Hysteresis Width	V_{HYS}	-	V_{DF}×0.03	V_{DF}×0.05	V_{DF}×0.07	V	①
Supply Current 1	I_{SS1}	V_{IN}= V_{DF}×0.9V (Detect)	E-2 (*2)			μA	②
Supply Current 2	I_{SS2}	V_{IN}=V_{DF}×1.1V (Release) (Type:A,C,E)	E-3 (*2)				
		V_{IN}=V_{DF}×1.1V (Release) (Type:B,D,F)	E-31 (*2)				
Operating Voltage	V_{IN}	-	1.3	-	6.0	V	−
Output Current	I_{RBOUT1}	V_{IN}=1.3V, V_{RESETB}=0.5V (N-ch)	1.7	3.0	-	mA	③
		V_{IN}=2.0V(*3), V_{RESETB}=0.5V (N-ch)	5.2	6.7	-		
		V_{IN}=3.0V(*4), V_{RESETB}=0.5V (N-ch)	8.6	10.2	-		
		V_{IN}=4.0V(*5), V_{RESETB}=0.5V (N-ch)	10.6	12.3	-		
		V_{IN}=5.0V(*6), V_{RESETB}=0.5V (N-ch)	11.7	13.5	-		
	I_{RBOUT2} (*7)	V_{IN}=2.0V(*8), V_{RESETB}=V_{IN}-0.5V (P-ch)	-	-1.9	-0.9		
		V_{IN}=3.0V(*9), V_{RESETB}=V_{IN}-0.5V (P-ch)	-	-3.1	-2.1		
		V_{IN}=4.0V(*10), V_{RESETB}=V_{IN}-0.5V (P-ch)	-	-4.0	-3.0		
		V_{IN}=5.0V(*11), V_{RESETB}=V_{IN}-0.5V (P-ch)	-	-4.7	-3.7		
		V_{IN}=6.0V, V_{RESETB}=V_{IN}-0.5V (P-ch)	-	-5.2	-4.2		
Leakage Current: CMOS Output (P-ch)	I_{LEAK}	V_{IN}=V_{DF}×0.9V, V_{RESETB}=0V	-	-0.01	-	μA	③
Leakage Current: N-ch Open Drain Output		V_{IN}=6.0V, V_{RESETB}=6.0V	-	0.01	0.1		
Delay Resistance (*12)	Rp	V_{IN}=6.0V, $V_{Cd/MRB}$ =0V (Type: A, B, E, F)	1.8	2.0	2.15	MΩ	④
	Rn	V_{IN}=$V_{Cd/MRB}$=V_{DF}×0.9V (Type: C, D, E, F)					
Undefined Operation (*13)	V_{UNS}	V_{IN}<1.3V	-	-	0.4	V	⑧
Release Delay Time	t_{DR0}	V_{IN}=V_{DF}×0.9V→V_{DF}×1.1V (*14) Cd: OPEN	-	0.05	-	ms	⑤
Detect Delay Time	t_{DF0}	V_{IN}=V_{DF}×1.1V→V_{DF}×0.9V (*15) Cd: OPEN	-	0.13	-	ms	⑤
Cd Threshold Voltage	V_{TCD}	V_{IN}=V_{DF}×1.1V～6.0V (Release)	V_{IN}×0.44	V_{IN}×0.50	V_{IN}×0.56	V	⑥
		V_{IN}=V_{DF}×0.9V (Detect)					
MRB Low Level Voltage	V_{MRL}	V_{IN}=V_{DF}×1.1V～6.0V	0	-	V_{IN}×0.17	V	⑥
MRB High Level Voltage	V_{MRH}	V_{IN}=V_{DF}×1.1V～6.0V	V_{IN}×0.56	-	V_{IN}	V	⑥
Minimum MRB Pulse Width	t_{MRB}	V_{IN}=V_{DF}×1.1V $V_{Cd/MRB}$ =V_{IN}→0V→V_{IN}	5.0	-	-	μs	⑦

(*1) $V_{DF(T)}$: Nominal detect voltage
(*2) For the detail value, please refer to “Voltage Table”.
(*3) For $V_{DF(T)}$＞2.0V only
(*4) For $V_{DF(T)}$＞3.0V only
(*5) For $V_{DF(T)}$＞4.0V only
(*6) For $V_{DF(T)}$＞5.0V only
(*7) For XC6129C (CMOS output) only
(*8) For $V_{DF(T)}$≦1.8V only
(*9) For $V_{DF(T)}$≦2.7V only。
(*10) For $V_{DF(T)}$≦3.7V only
(*11) For $V_{DF(T)}$≦4.6V only
(*12) Resistance is calculated from voltage applied to Cd/MRB pin and current.
(*13) Types B/D/F of XC6129C series only.
(*14) Time from V_{IN}=V_{DF} + V_{HYS} until V_{RESETB}=V_{DF} × 1.1 × 0.9 when V_{IN} rises. (CMOS output)
Time from V_{IN}=V_{DF} + V_{HYS} until V_{RESETB}=Pull-up voltage × 0.9 when V_{IN} rises. (N-ch open drain output)
(*15) Time from V_{IN}=V_{DF} until V_{RESETB}=V_{DF} × 0.9 × 0.1 when V_{IN} drops. (CMOS output)
Time from V_{IN}=V_{DF} until V_{RESETB}=Pull-up voltage × 0.1 when V_{IN} drops. (N-ch open drain output)

■ELECTRICAL CHARACTERISTICS (Continued)

●XC6129xxxG~XC6129xxxL Series (Output Logic: Active High)

Ta=25℃

PARAMETER		SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Detect Voltage		V_{DF}	$V_{DF(T)}$ (*1)=1.5V～5.5V	$V_{DF(T)}$×0.992	$V_{DF(T)}$	$V_{DF(T)}$×1.008	V	①
				E-1 (*2)				
Temperature Characteristics		ΔV_{DF}/ (ΔTopr･V_{DF})	-40℃≦Topr≦85℃	-	±50	-	ppm/℃	①
Hysteresis Width		V_{HYS}	-	V_{DF}×0.03	V_{DF}×0.05	V_{DF}×0.07	V	①
Supply Current 1		I_{SS1}	V_{IN}=V_{DF}×0.9V (Detect)	E-2 (*2)			μA	②
Supply Current 2		I_{SS2}	V_{IN}= V_{DF}×1.1V (Release)	E-3 (*2)				
Operating Voltage		V_{IN}	-	1.3	-	6.0	V	–
Output Current		I_{ROUT1}	V_{IN}=2.0V(*3), V_{RESET}=0.5V (N-ch)	5.2	6.7	-	mA	③
			V_{IN}=3.0V(*4), V_{RESET}=0.5V (N-ch)	8.6	10.2	-		
			V_{IN}=4.0V(*5), V_{RESET}=0.5V (N-ch)	10.6	12.3	-		
			V_{IN}=5.0V(*6), V_{RESET}=0.5V (N-ch)	11.7	13.5	-		
			V_{IN}=6.0V, V_{RESET}=0.5V (N-ch)	12.4	14.3	-		
		I_{ROUT2} (*7)	V_{IN}=1.3V, V_{RESET}=V_{IN}-0.5V (P-ch)	-	-0.9	-0.1		
			V_{IN}=2.0V(*8), V_{RESET}=V_{IN}-0.5V (P-ch)	-	-1.9	-0.9		
			V_{IN}=3.0V(*9), V_{RESET}=V_{IN}-0.5V (P-ch)	-	-3.1	-2.1		
			V_{IN}=4.0V(*10), V_{RESET}=V_{IN}-0.5V (P-ch)	-	-4.0	-3.0		
			V_{IN}=5.0V(*11), V_{RESET}=V_{IN}-0.5V (P-ch)	-	-4.7	-3.7		
Leakage Current	CMOS Output (P-ch)	I_{LEAK}	V_{IN}=6.0V, V_{RESET}=0V	-	-0.01	-	μA	③
	N-ch Open Drain Output		V_{IN}=V_{DF}×0.9V, V_{RESET}=6.0V	-	0.01	0.1		
Delay Resistance (*12)		Rp	V_{IN}=6.0V, $V_{Cd/MRB}$=0V (Type: G, L)	1.8	2.0	2.15	MΩ	④
		Rn	V_{IN}= $V_{Cd/MRB}$=V_{DF}×0.9V (Type: J,L)					
Release Delay Time		t_{DR0}	V_{IN}=V_{DF}×0.9V→V_{DF}×1.1V (*13) Cd: OPEN	-	0.05	-	ms	⑤
Detect Delay Time		t_{DF0}	V_{IN}=V_{DF}×1.1V→V_{DF}×0.9V (*14) Cd: OPEN	-	0.13	-	ms	⑤
Cd Threshold Voltage		V_{TCD}	V_{IN}=V_{DF}×1.1V～6.0V (Release)	V_{IN}×0.44	V_{IN}×0.50	V_{IN}×0.56	V	⑥
			V_{IN}=V_{DF}×0.9V (Detect)					
MRB Low Level Voltage		V_{MRL}	V_{IN}=V_{DF}×1.1V～6.0V	0	-	V_{IN}×0.17	V	⑥
MRB High Level Voltage		V_{MRH}	V_{IN}=V_{DF}×1.1V～6.0V	V_{IN}×0.56	-	V_{IN}	V	⑥
Minimum MRB Pulse Width		t_{MRB}	V_{IN}=V_{DF}×1.1V $V_{Cd/MRB}$=V_{IN}→0V→V_{IN}	5.0	-	-	μs	⑦

(*1) $V_{DF(T)}$: Nominal detect voltage
(*2) For the detail value, please refer to “Voltage Table”.
(*3) For $V_{DF(T)}$≦1.8V only
(*4) For $V_{DF(T)}$≦2.7V only
(*5) For $V_{DF(T)}$≦3.7V only
(*6) For $V_{DF(T)}$≦4.6V only
(*7) For XC6129C (CMOS output) only
(*8) For $V_{DF(T)}$＞2.0V only
(*9) For $V_{DF(T)}$＞3.0V only。
(*10) For $V_{DF(T)}$＞4.0V only
(*11) For $V_{DF(T)}$＞5.0V only
(*12) Resistance is calculated from voltage applied to Cd/MRB pin and current.
(*13) Time from V_{IN}=V_{DF} + V_{HYS} until V_{RESETB}=V_{DF} × 1.1 × 0.1 when V_{IN} rises. (CMOS output)
Time from V_{IN}=V_{DF} + V_{HYS} until V_{RESETB}=Pull-up voltage × 0.1 when V_{IN} rises. (N-ch open drain output)
(*14) Time from V_{IN}=V_{DF} until V_{RESETB}=V_{DF} × 0.9 × 0.9 when V_{IN} drops. (CMOS output)
Time from V_{IN}=V_{DF} until V_{RESETB}=Pull-up voltage × 0.9 when V_{IN} drops. (N-ch open drain output)

■ELECTRICAL CHARACTERISTICS (Continued)

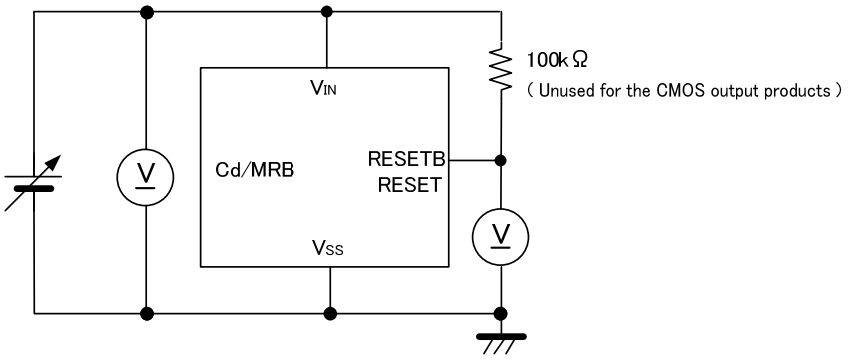
●Voltage Table

Ta=25℃

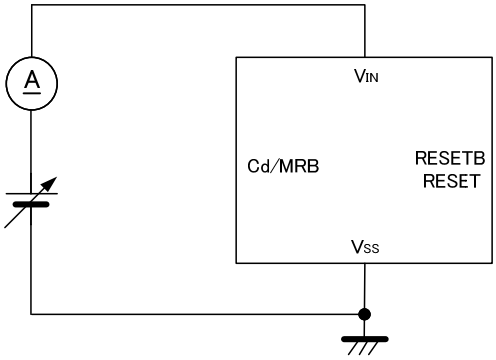
NOMINAL DETECT VOLTAGE	E-1		E-2			E-3			E-31		
	DETECT VOLTAGE (V)		Supply Current1 (μA)			Supply Current2 (μA)					
$V_{DF(T)}$ (V)	V_{DF}		I_{SS1}			I_{SS2}					
	MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
1.5	1.4880	1.5120	-	0.38	1.11	-	0.47	1.39	-	0.63	1.67
1.6	1.5872	1.6128									
1.7	1.6864	1.7136									
1.8	1.7856	1.8144									
1.9	1.8848	1.9152									
2.0	1.9840	2.0160									
2.1	2.0832	2.1168	-	0.42	1.16	-	0.58	1.60	-	0.74	1.88
2.2	2.1824	2.2176									
2.3	2.2816	2.3184									
2.4	2.3808	2.4192									
2.5	2.4800	2.5200									
2.6	2.5792	2.6208									
2.7	2.6784	2.7216									
2.8	2.7776	2.8224									
2.9	2.8768	2.9232									
3.0	2.9760	3.0240									
3.1	3.0752	3.1248									
3.2	3.1744	3.2256									
3.3	3.2736	3.3264									
3.4	3.3728	3.4272									
3.5	3.4720	3.5280	-	0.47	1.31	-	0.71	1.90	-	0.87	2.18
3.6	3.5712	3.6288									
3.7	3.6704	3.7296									
3.8	3.7696	3.8304									
3.9	3.8688	3.9312									
4.0	3.9680	4.0320									
4.1	4.0672	4.1328									
4.2	4.1664	4.2336									
4.3	4.2656	4.3344									
4.4	4.3648	4.4352									
4.5	4.4640	4.5360									
4.6	4.5632	4.6368									
4.7	4.6624	4.7376									
4.8	4.7616	4.8384	-	0.52	1.41	-	0.83	2.17	-	0.99	2.45
4.9	4.8608	4.9392									
5.0	4.9600	5.0400									
5.1	5.0592	5.1408									
5.2	5.1584	5.2416									
5.3	5.2576	5.3424									
5.4	5.3568	5.4432									
5.5	5.4560	5.5440									

■TEST CIRCUITS

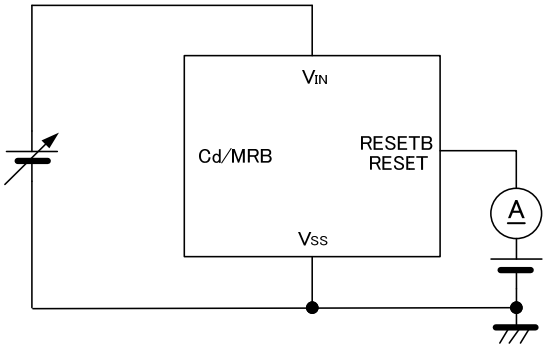
CIRCUIT①



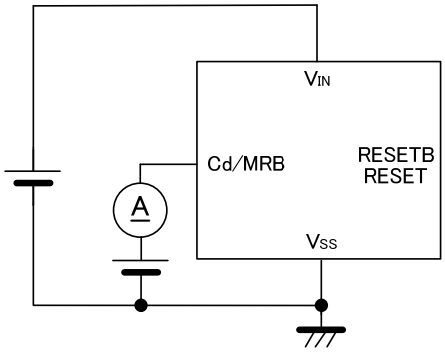
CIRCUIT②



CIRCUIT③

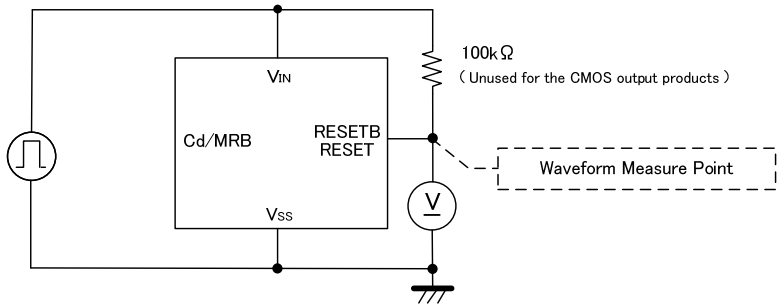


CIRCUIT④

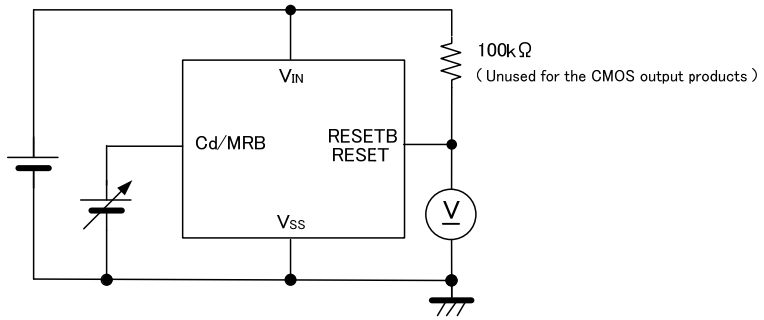


■TEST CIRCUITS (Continued)

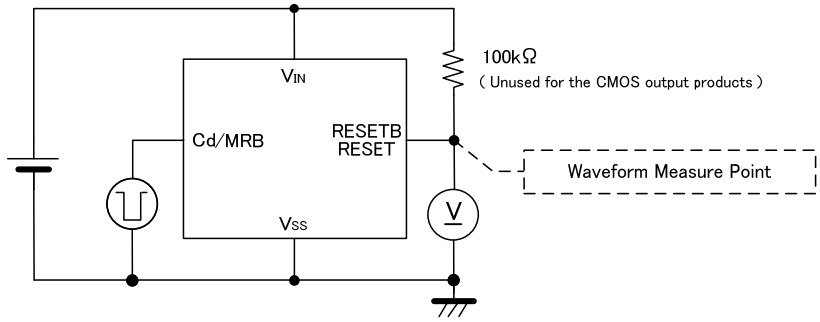
CIRCUIT⑤



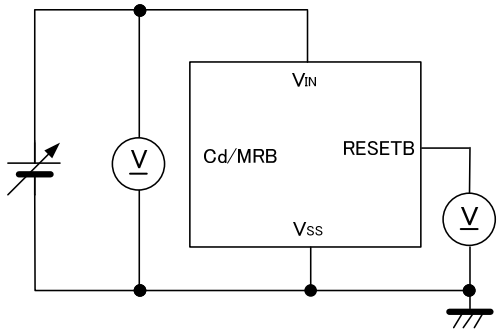
CIRCUIT⑥



CIRCUIT⑦

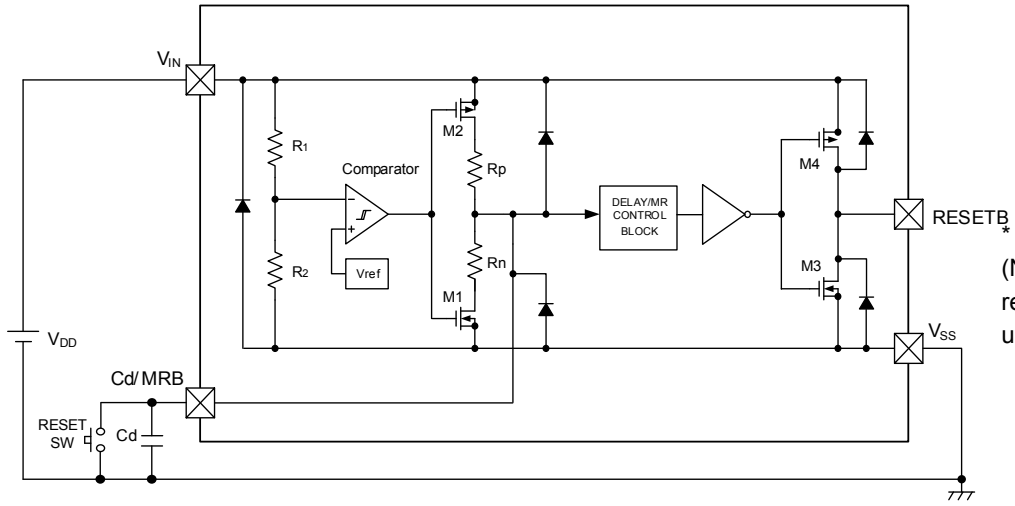


CIRCUIT⑧



■OPERATIONAL DESCRIPTION

Fig. 1 shows a typical circuit Fig. 2 shows the timing chart of Fig. 1.



* The XC6129N series (N-ch open drain output) requires a resistor to pull up the output.

Fig. 1: Typical circuit (Active Low product)

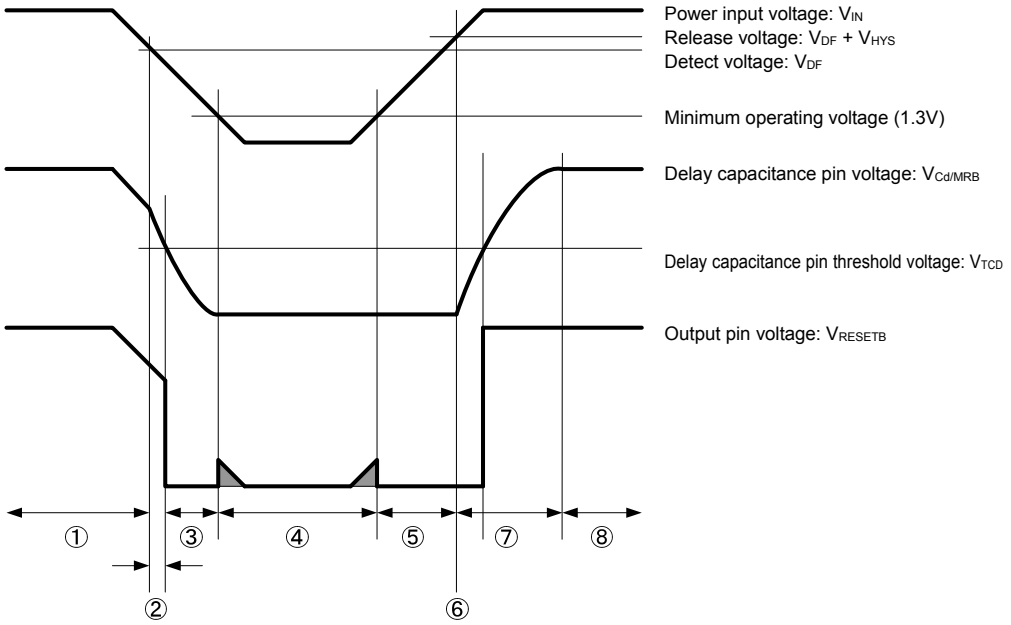


Fig. 2: Timing chart of Fig. 1

(1) In the initial state, a voltage sufficiently high in relation to the release voltage is applied to the V_{IN} power input pin, and the Cd/MRB delay capacitance pin is charged to the power input pin voltage.

The power input pin voltage starts to drop, and during the interval until it reaches the detect voltage ($V_{IN}>V_{DF}$), the output pin voltage V_{RESETB} is at High level.

(2) The power input pin voltage continues to drop, and when it reaches the detect voltage ($V_{IN}=V_{DF}$), the Nch transistor for delay capacitance discharge turns ON and discharge of the delay capacitance starts.

When the delay capacitance pin drops below the delay capacitance pin threshold voltage, V_{RESETB} changes to Low level.

The time from $V_{IN}=V_{DF}$ until V_{RESETB} changes to Low level is the detect delay t_{DF} (the detect time when the delay capacitance pin is open is t_{DF0}).

■OPERATIONAL DESCRIPTION (Continued)

(3) The power input pin voltage drops further, and during the interval when it is below the detect voltage V_{DF} and higher than 1.3V, the delay capacitance pin is discharged to ground level and the output pin voltage V_{RESETB} maintains Low level.

(4) During the interval in which the power input pin voltage drops below 1.3V and then rises back to 1.3V or higher, the output pin voltage V_{RESETB} may not be able to maintain Low level. Operation during this interval is called “unstable operation”, and the voltage that appears in V_{RESETB} is called the “unstable operation voltage V_{UNS}”.

(5) The power input pin voltage rises, and during the interval that it is higher than 1.3V until it reaches the release voltage ($1.3V \leq V_{IN} < V_{DF}+V_{HYS}$), the output pin voltage V_{RESETB} maintains Low level.

(6) The power input pin voltage continues to rise, and when it reaches the release voltage ($V_{DF}+V_{HYS}$), the Nch transistor for delay capacitance discharge turns OFF and charging of the delay capacitance pin through delay resistor Rp starts.

(7) During the interval that the power input pin voltage continues to maintain a voltage higher than the release voltage, the delay capacitance pin is charged up to the power input pin voltage.
When the delay capacitance pin voltage reaches V_{TCD}, the output pin voltage V_{RESETB} changes to High level.
The time from $V_{IN}=V_{DF}+V_{HYS}$ until V_{RESETB} changes to High level is the release delay time t_{DR} (the release time when the delay capacitance pin is open is t_{DR0}).

(8) During the time that the power input pin voltage is higher than the detect voltage ($V_{IN}>V_{DF}$), the output pin voltage V_{RESETB} maintains High level.

The above operational explanation is for detection using Active Low products.
For Active High products, reverse the logic of V_{RESETB}.

■OPERATIONAL DESCRIPTION (Continued)

<Release delay time / detect delay time>

The release delay time and detect delay time are determined by the delay resistance (Rp and Rn) and the delay capacitance (Cd). The delay resistance is set to 2MΩ (TYP.) internally in the circuit, and thus the delay time can be changed using the delay capacitance.

You can select a product type that has or does not have the release delay time function and the detect delay time function. (Refer to the Selection Guide.)

The release delay t_{DR} is calculated using equation (1).

$t_{DR}=Rp\times Cd\times\{-\ln(1-V_{TCD}/V_{IN})\}+t_{DR0}$ …(1) * ln is the natural logarithm.

Rn : Delay resistance 2.0MΩ (TYP.)

V_{TCD} : Delay capacitance pin threshold voltage $V_{IN}/2$ (TYP.)

When t_{DR0} can be neglected, this can be calculated in a simple manner using equation (2).

$t_{DR}=Rp\times Cd\times[-\ln\{1-(V_{IN}/2)/V_{IN}\}]=Rp\times Cd\times 0.693$ …(2)

Example: When the delay capacitance Cd is 0.68μF, the release delay time t_{DR} is $2.0\times10^{6}\times0.68\times10^{-6}\times0.693=942$(ms).

The detect delay t_{DF} is calculated using equation (3).

$t_{DF}=Rn\times Cd\times\{-\ln(V_{TCD}/V_{IN1})\}+t_{DF0}$ …(3) * ln is the natural logarithm.

Rn: Delay resistance 2.0MΩ (TYP.)

V_{TCD}: Delay capacitance pin threshold voltage $V_{IN2}/2$ (TYP.) *V_{IN2} is the power input pin voltage at detection.

V_{IN1}: Power input pin voltage at release

When $V_{IN}=V_{DF}\times1.1V\rightarrow V_{DF}\times0.9V$ and t_{DF0} can be neglected, this can be calculated in a simple manner using equation (4).

$t_{DF}=Rn\times Cd\times\{-\ln(V_{IN2}/2)/V_{IN1}\}=Rn\times Cd\times[-\ln\{(V_{DF}\times0.9\times0.5)/(V_{DF}\times1.1)\}]=Rn\times Cd\times0.894$ …(4)

For details of the detect delay time of equation (4), refer to Fig. 3.

Example: When the delay capacitance Cd is 0.68μF at $V_{IN}=V_{DF}\times1.1V\rightarrow V_{DF}\times0.9V$, the detect delay time t_{DF} is $2.0\times10^{6}\times0.68\times10^{-6}\times0.894=1216$(ms).

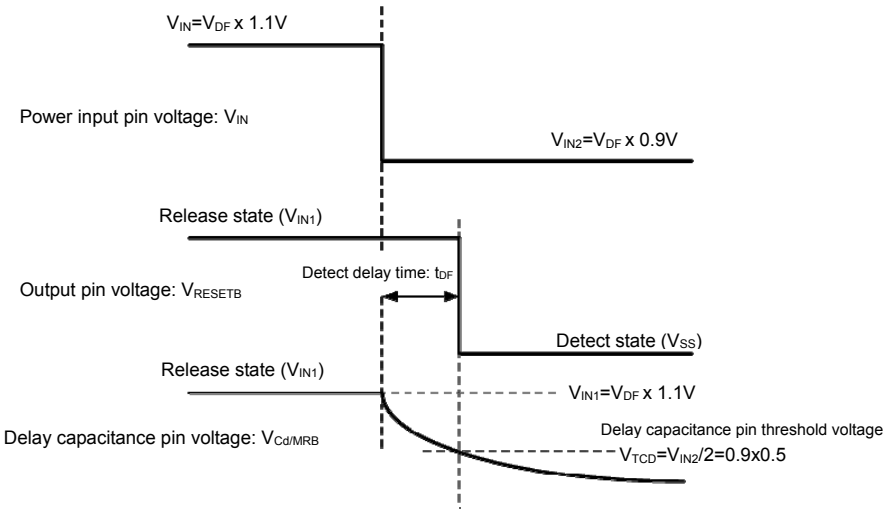


Fig. 3: Detect delay time of equation (4) (timing chart)

Delay time table

Delay capacitance Cd (μF)	Release delay time t_{DR} (ms) (*1)		Detect delay time t_{DF} (ms) (*1)	
	TYP.	MIN.toMAX. (*2)	TYP.	MIN.toMAX. (*2)
0.01	13.9	10.4 to 17.7	17.9	12.7 to 22.0
0.022	30.5	22.9 to 38.9	39.3	28.0 to 48.4
0.047	65.1	48.9 to 83.0	84.0	59.8 to 103.3
0.1	139	104 to 177	179	127 to 220
0.22	305	229 to 389	393	280 to 484
0.47	651	489 to 830	840	598 to 1033
1	1386	1042 to 1766	1788	1274 to 2198

The release delay time values are the values calculated from equation (2).

The detect delay time values are the values calculated from equation (4).

(*1) Note that the delay time will vary depending on the actual capacitance value of the delay capacitance Cd.

(*2) The values are calculated with consideration given to deviations in the delay resistance and delay capacitance pin threshold voltage.

■OPERATIONAL DESCRIPTION (Continued)

<Manual reset function>

The reset output pin signal can be forced into the detect state by inputting a voltage into the delay capacitance pin when in the release state.

When the delay capacitance pin voltage input reaches an H→L level signal, the reset output pin outputs an H→L level signal. (RESETB : Active Low type)

When the delay capacitance pin voltage input reaches an H→L level signal, the reset output pin outputs an L→H level signal. (RESET : Active High type)

* During manual reset, there is no delay time even when a delay capacitance is connected.
* When the delay capacitance pin voltage input reaches an L→H level signal in the detection state, the reset output pin outputs an L→H level signal.
(RESETB : Active Low type)
* When the delay capacitance pin voltage input reaches an L→H level signal in the detection state, the reset output pin outputs an H→L level signal.
(RESET : Active High type)

Under the detect condition, the condition will be kept even if the RESET switch turns on and off.

In the case that either H level or L level is fed to the Cd/MRB pin without the RESET switch, the behavior of the XC6129 follows the timing chart in Fig. 4.

L level is fed to the MRB pin under the detect condition, the RESET switch will be kept.
H level is fed to the MRB pin under the detect condition, the RESET switch will be undefined.

Even though the voltage at the V_{SEN} pin changes from a higher voltage than the detect voltage to a lower voltage, as long as H level is fed to the MRB pin, the release condition is kept.

If H level or L level is fed to the Cd/MRB pin forcibly, then even though Cd is connected to the pin, the XC6129 can't have any delay time.

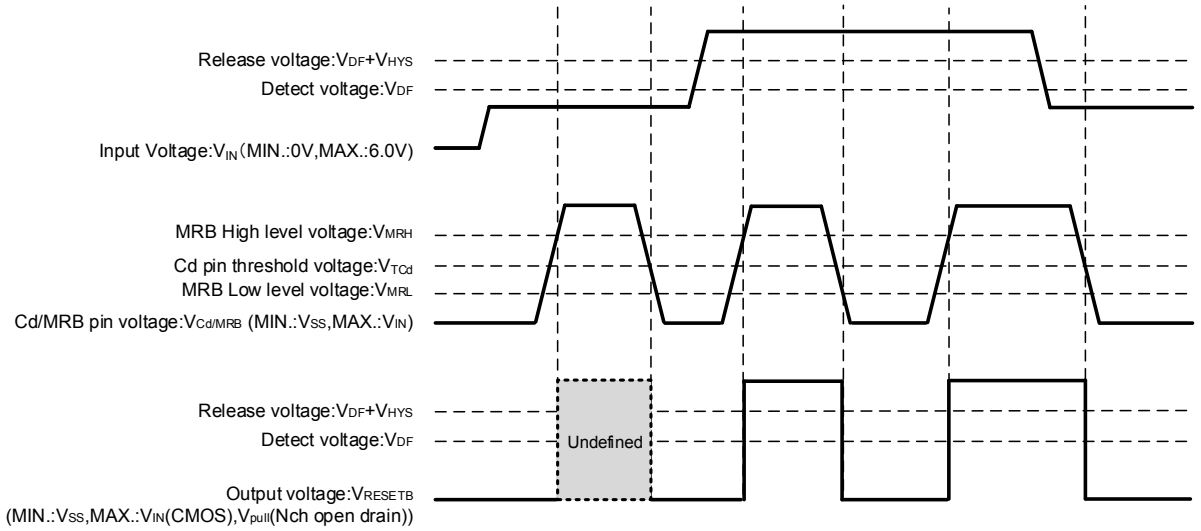


Fig. 4: Manual reset operation by the delay capacitance pin (Active Low product)

<Unstable operation prevention function>

Types B/D/F of the XC6129C series include an unstable operation prevention function.

When the power input pin voltage is less than the minimum operation voltage, the output pin voltage due to unstable operation is limited to 0.4V (MAX.) or less.

* Types A/C/E of the XC6129C series and each of the XC6129N series do not have an unstable operation prevention function.

■NOTE ON USE

1) Please use this IC within the stated maximum ratings. For temporary, transitional voltage drop or voltage rising phenomenon, the IC is liable to malfunction should the ratings be exceeded.

2) The power input pin voltage may fall due to the flow through current during IC operation and the resistance component between the power supply and the power input pin.
In the case of CMOS output, a drop in the power input pin voltage may occur in the same way due to the output current. When this happens, if the power input pin voltage drops below the minimum operating voltage, malfunctioning may occur.
In addition, when the power input pin voltage is below the detect voltage, the output pin voltage may oscillate. Exercise caution in particular if a resistor is connected to the power input pin.

3) Note that large, sharp changes of the power input pin voltage may cause malfunctioning.

4) Power supply noise is sometimes a cause of malfunctioning. Sufficiently test using the actual device, such as inserting a capacitor between V_{IN} and GND.

5) If a capacitor is connected to the delay capacitance pin and the power input pin voltage drops suddenly during release operation (for example, from 6.0V to 0V), there is a possibility that the delay capacitance pin voltage will exceed the absolute maximum rating. If there is a possibility that the power input pin voltage will drop suddenly during release operation, connect a Schottky diode between the power input pin and delay capacitance pin as shown in Fig. 5.

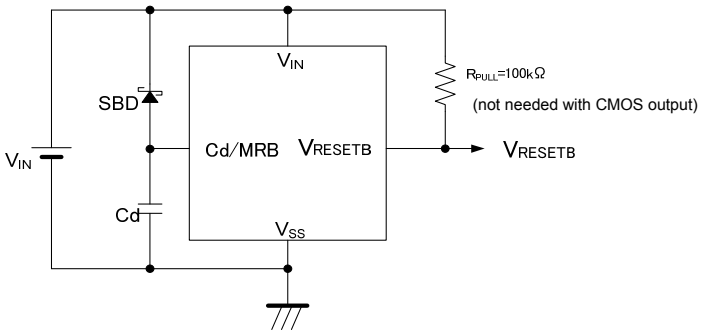


Fig. 5: Circuit example with a Schottky diode connected to the delay capacitance pin

6) When an N-ch open drain output is used, the V_{RESETB} voltage at detection and release is determined by the pull-up resistance connected to the output pin. Refer to the following when selecting the resistance value.

At detection:

$V_{RESETB}=V_{pull}/(1+R_{pull}/R_{ON})$
V_{pull} : Voltage after pull-up
R_{ON}(*1): ON resistance of N-ch driver M3 (calculated from V_{RESETB}/I_{RBOUT1} based on electrical characteristics)

Example: When V_{IN}=2.0V(*2), $R_{ON}=0.5/5.2\times10^{-3}=96\Omega$ (MAX.). If it is desired to make V_{RESETB} at detection 0.1V or less when V_{pull} is 3.0V,
$R_{pull}=(V_{pull}/V_{RESETB}-1)\times R_{ON}=(3/0.1-1)\times96\fallingdotseq2.8k\Omega$
Therefore, to make the output voltage at detection 0.1V or less under the above conditions, the pull-up resistance must be 2.8kΩ or higher.

(*1) Note that R_{ON} becomes larger as V_{IN} becomes smaller.
(*2) For V_{IN} in the calculation, use the lowest value of the input voltage range you will use.

At release:

$V_{RESETB}=V_{pull}/(1+R_{pull}/R_{off})$
V_{pull}: Voltage after pull-up
R_{off}: Resistance when N-ch driver M3 is OFF (calculated from V_{RESETB}/I_{LEAK} based on electrical characteristics)

Example: When V_{pull} is 6.0V, $R_{off}=6/(0.1\times10^{-6})=60M\Omega$ (MIN.). If it is desired to make V_{RESETB} 5.99V or higher,
$R_{pull}=(V_{pull}/V_{RESETB}-1)\times R_{off}=(6/5.99-1)\times60\times10^{6}\fallingdotseq100k\Omega$
Therefore, to make the output voltage at release 5.99V or higher under the above conditions, the pull-up resistance must be 100kΩ or less.

■NOTE ON USE (Continued)

7) If the discharge time of the delay capacitance Cd at detection is short and the delay capacitance Cd cannot be discharged to ground level, charging will take place at the next release operation with electric charge remaining in the delay capacitance Cd, and this may cause the release delay time to become noticeably short.

8) If the charging time of the delay capacitance Cd at release is short and the delay capacitance Cd cannot be charged to the V_{IN} level, the delay capacitance Cd will discharge from less than the V_{IN} level at the next detection operation, and this may cause the detect delay time to become noticeably short.

9) Even with a non-delay type, a delay time is added when a delay capacitance Cd is connected.

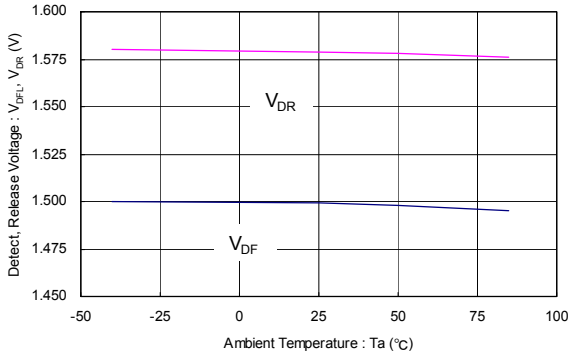
10) For a manual reset function, in case when the function is activated by feeding either MRB H level or MRB L level to Cd/MRB pin instead of using a reset switch, please note these phenomena below;
・The RESET output signal will be undefined when MRB H is fed to Cd/MRB pin under the detect condition.
・The RESET output signal will be undefined based on the voltage relationship between V_{SEN} pin and Cd/MRB pin.

11) Torex places an importance on improving our products and their reliability.
We request that users incorporate fail-safe designs and post-aging protection treatment when using Torex products in their systems.

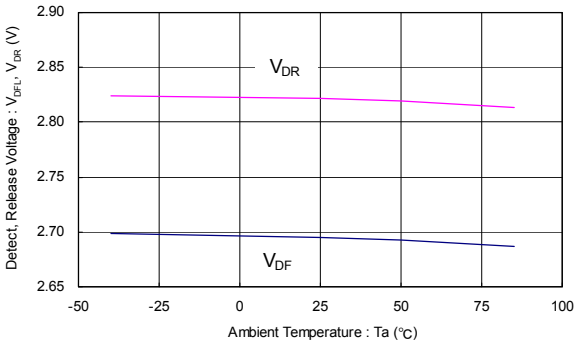
■TYPICAL PERFORMANCE CHARACTERISTICS

(1) Detect, Release Voltage vs. Ambient Temperature

XC6129 ($V_{DF(T)}$=1.5V)

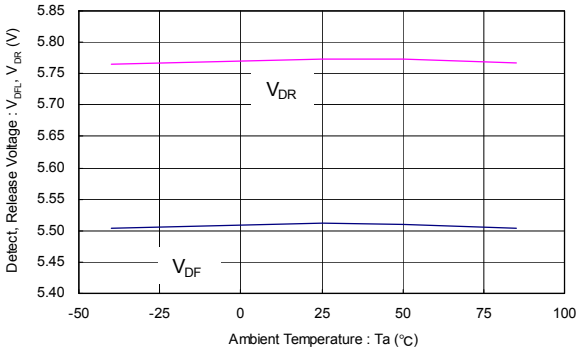


XC6129 ($V_{DF(T)}$=2.7V)

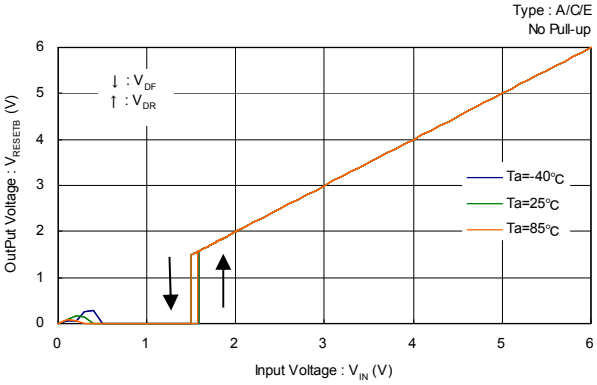


(2) Detect, Release Voltage vs. Input Voltage

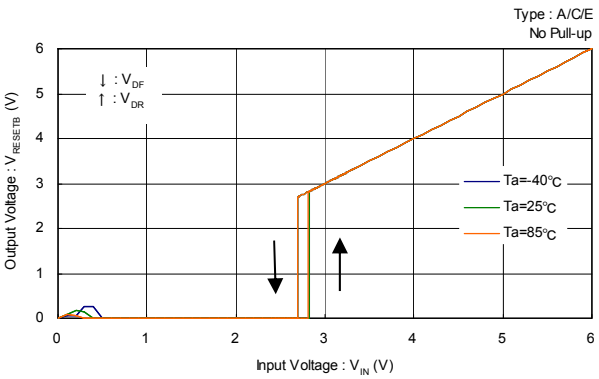
XC6129 ($V_{DF(T)}$=5.5V)



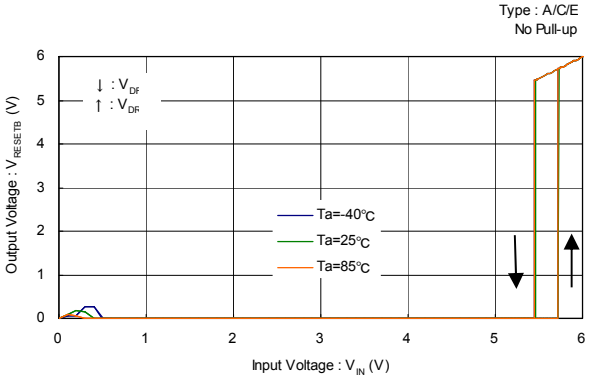
XC6129C ($V_{DF(T)}$=1.5V)



XC6129C ($V_{DF(T)}$=2.7V)



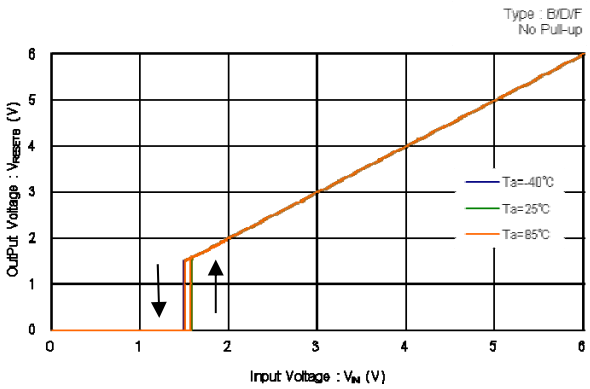
XC6129C ($V_{DF(T)}$=5.5V)



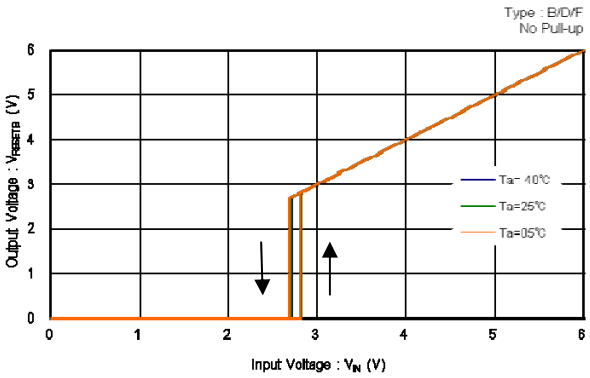
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(2) Detect, Release Voltage vs. Input Voltage (Continued)

XC6129C ($V_{DF(T)}$=1.5V)

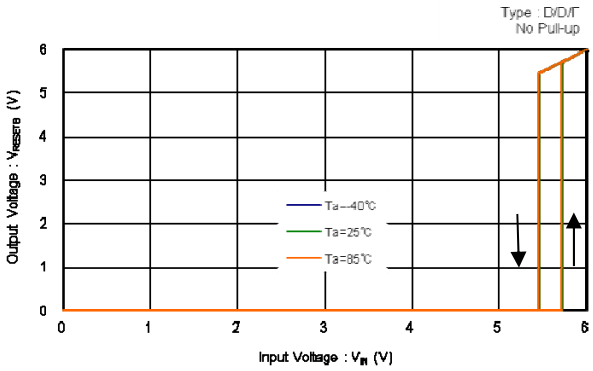


XC6129C ($V_{DF(T)}$=2.7V)

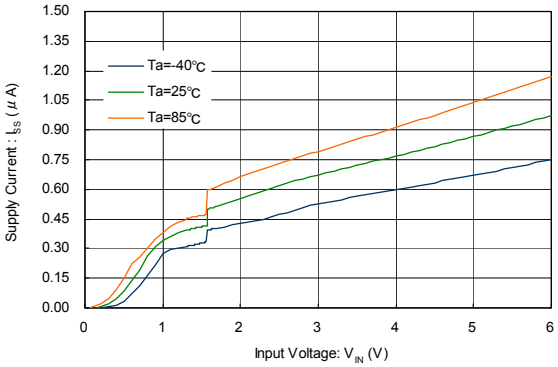


(3) Supply Current vs. Input Voltage

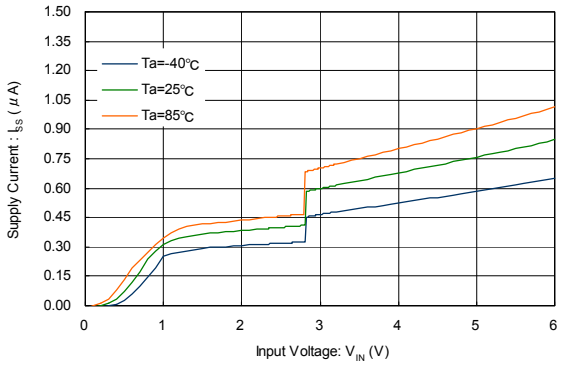
XC6129C ($V_{DF(T)}$=5.5V)



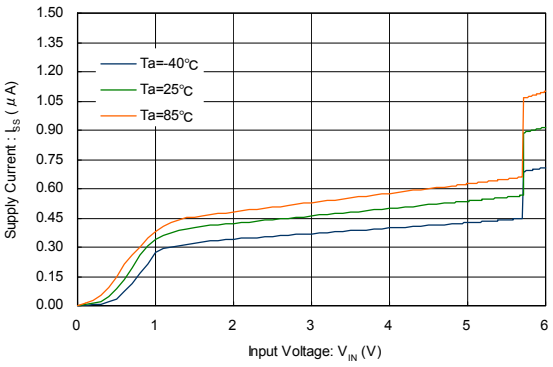
XC6129 ($V_{DF(T)}$=1.5V)



XC6129 ($V_{DF(T)}$=2.7V)



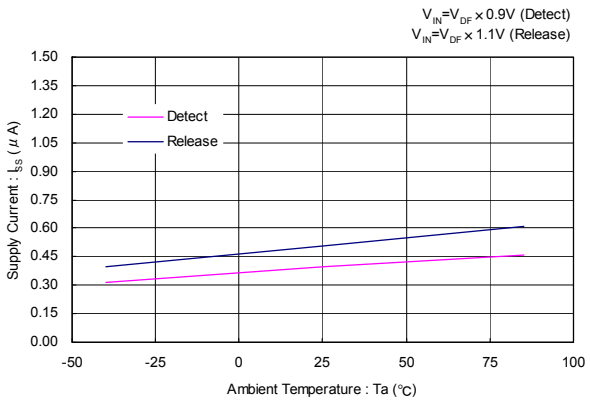
XC6129 ($V_{DF(T)}$=5.5V)



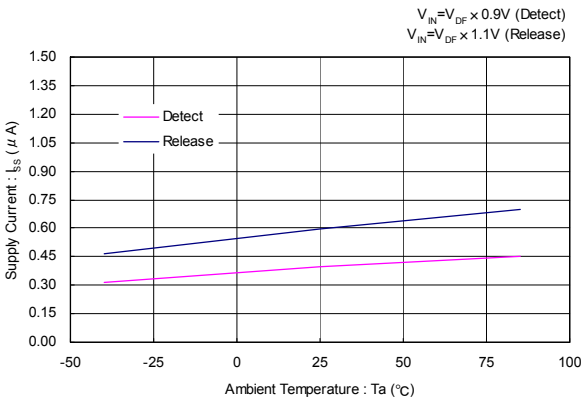
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(4) Supply Current vs. Ambient Temperature

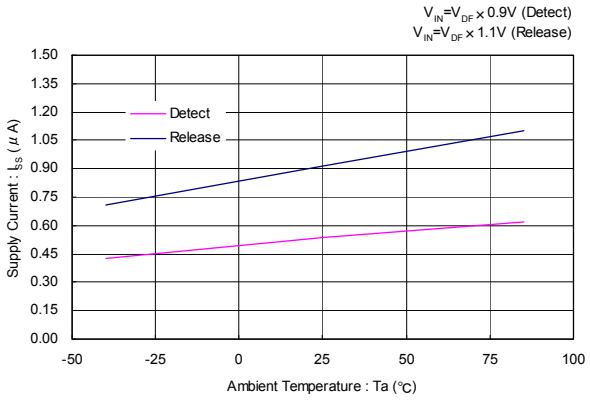
XC6129 ($V_{DF(T)}$=1.5V)



XC6129 ($V_{DF(T)}$=2.7V)

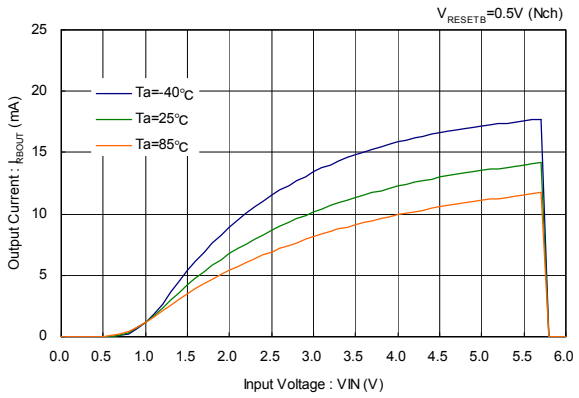


XC6129 ($V_{DF(T)}$=5.5V)

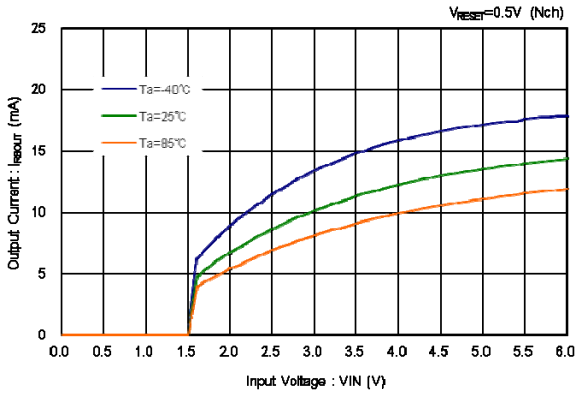


(5) Output Current vs. Input Voltage

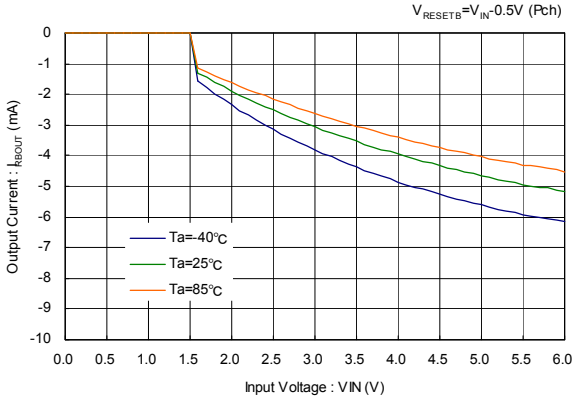
XC6129x55A



XC6129x15G

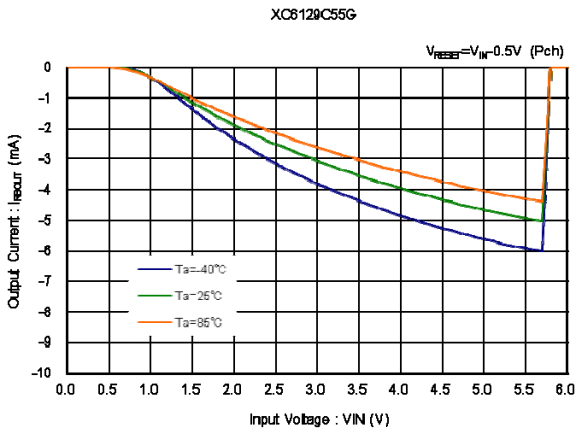


XC6129C15A

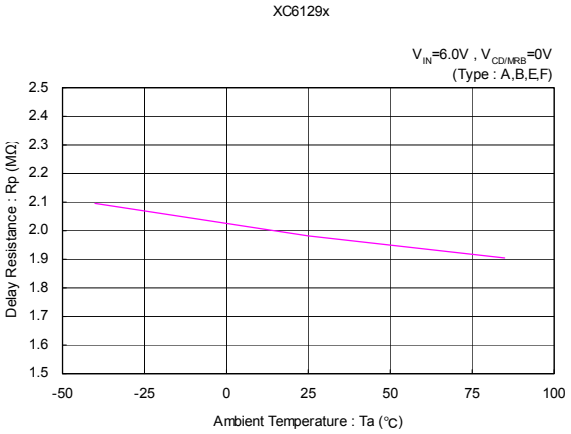


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

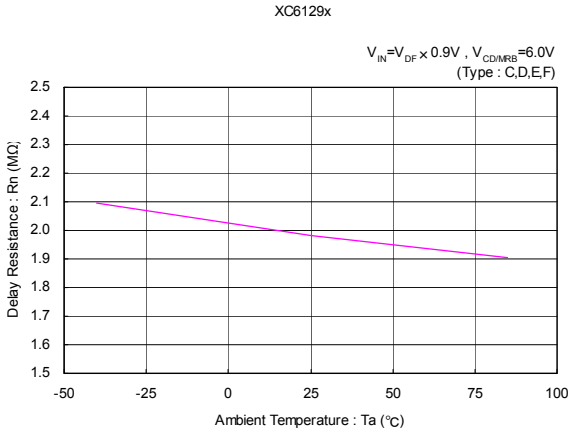
(5) Output Current vs. Input Voltage (Continued)

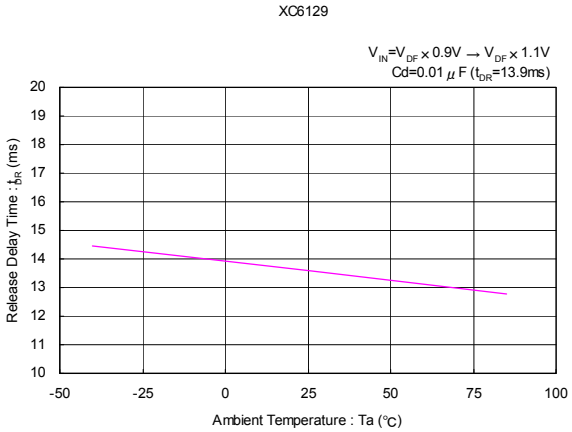


(6) Delay Resistance vs. Ambient Temperature

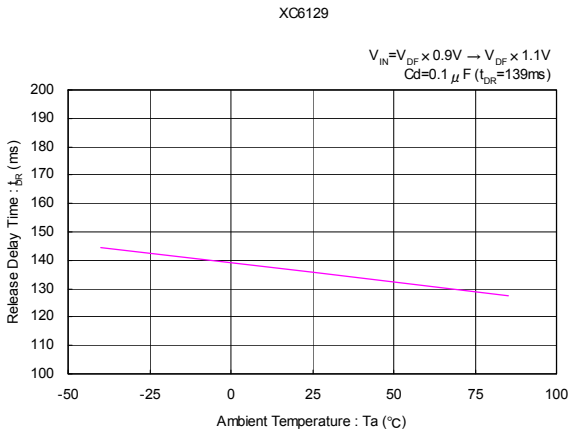


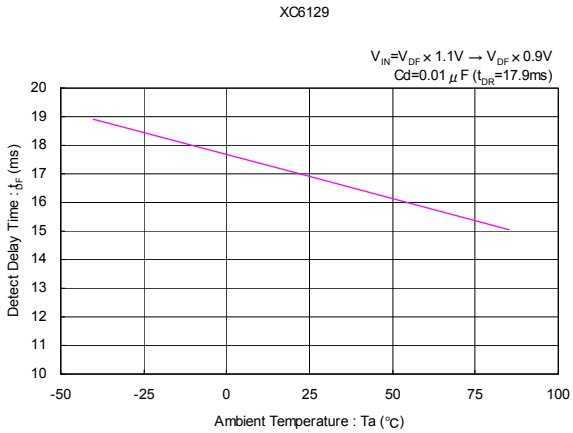
(7) Release Delay Time vs. Ambient Temperature





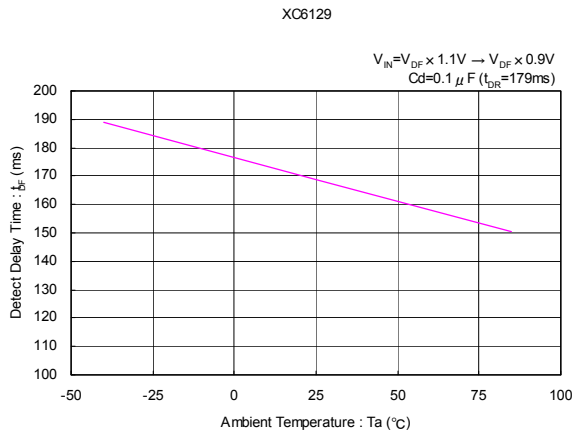
(8) Detect Delay Time vs. Ambient Temperature



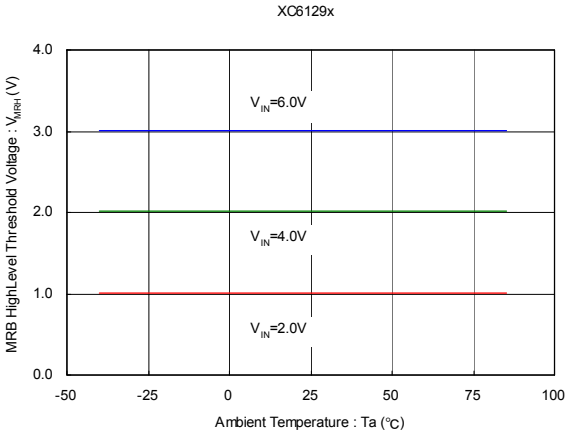


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

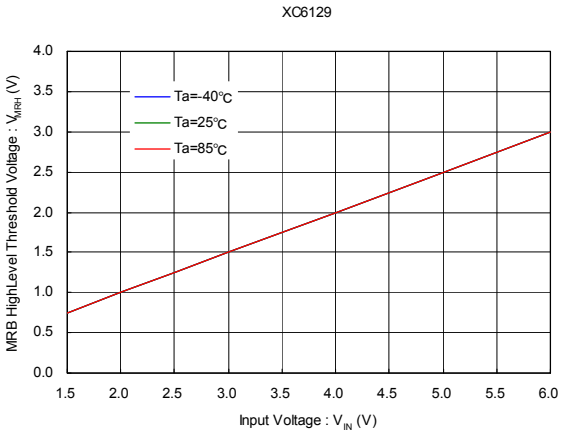
(8) Detect Delay Time vs. Ambient Temperature (Continued)



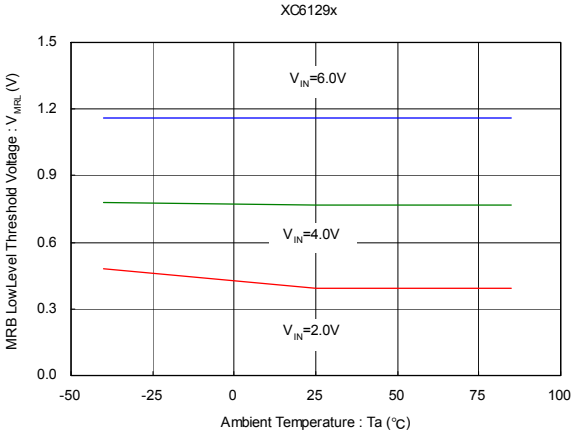
(9) Cd pin MRB High Level Voltage vs. Ambient Temperature



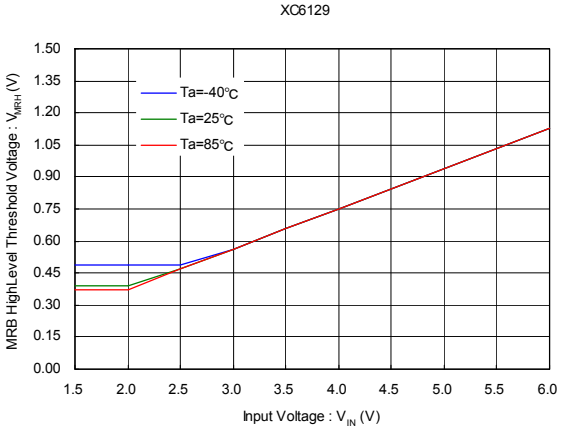
(10) Cd pin MRB High Level Voltage vs. Input Voltage



(11) Cd pin MRB Low Level Voltage vs. Ambient Temperature



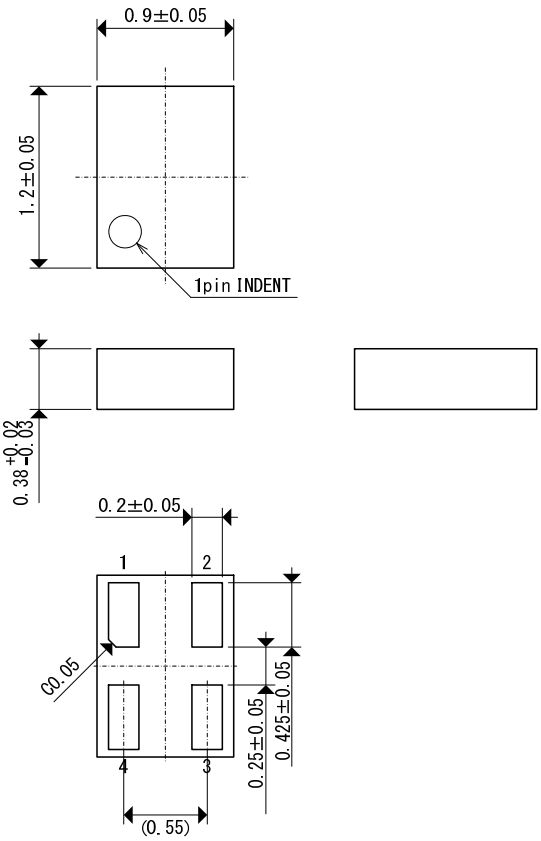
(12) Cd pin MRB Low Level Voltage vs. Input Voltage



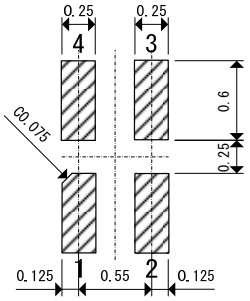
■PACKAGING INFORMATION

unit: mm

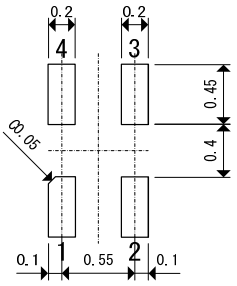
●USPN-4



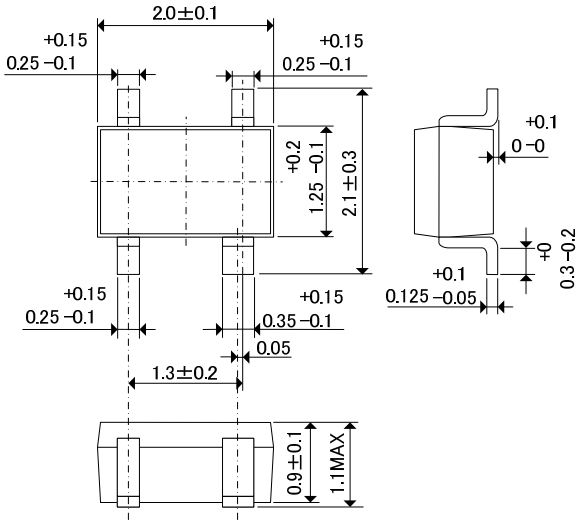
●USPN-4 Reference Pattern Layout



●USPN-4 Reference Metal Mask Design



●SSOT-24

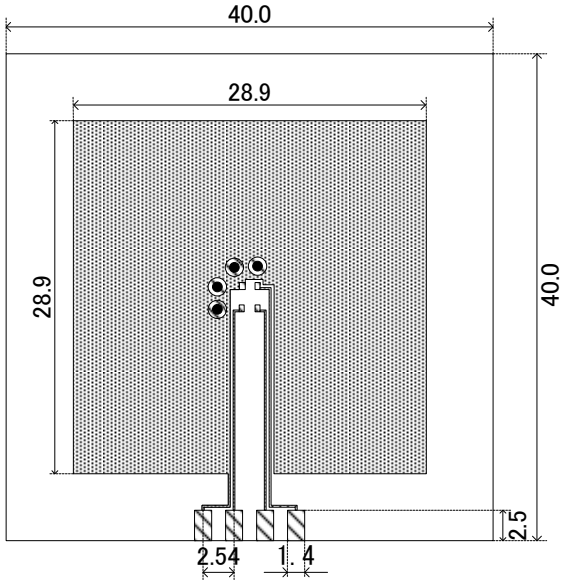


●SSOT-24 Power Dissipation

Power dissipation data for the SSOT-24 is shown in this page.
The value of power dissipation varies with the mount board conditions.
Please use this data as the reference data taken in the following condition.

1. Measurement Condition

Condition:	Mount on a board
Ambient:	Natural convection
Soldering:	Lead (Pb) free
Board:	Dimensions 40×40mm (1600mm^2 in one side)
	Copper (Cu) traces occupy 50% of the board area in top and back faces
	Package heat-sink is tied to the copper traces
Material:	Glass Epoxy (FR-4)
Thickness:	1.6mm
Through-hole:	4 x 0.8 Diameter

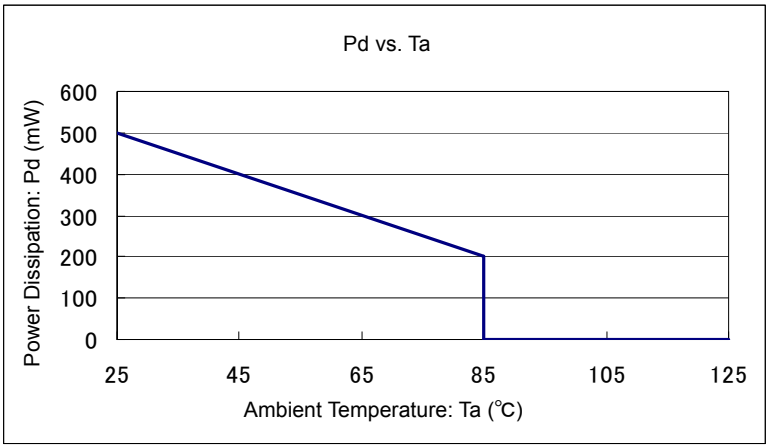


Evaluation Board (Unit: mm)

2. Power Dissipation vs. Ambient Temperature

Ambient Temperature (Tjmax=125℃)

Ambient Temperature (℃)	Power Dissipation Pd (mW)	Thermal Resistance (℃/W)
25	500	200.00
85	200	

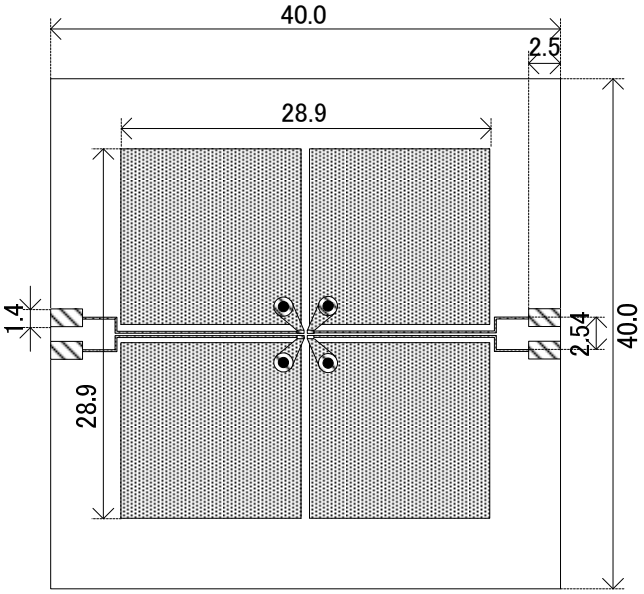


●USPN-4 Power Dissipation

Power dissipation data for the USPN-4 is shown in this page.
The value of power dissipation varies with the mount board conditions.
Please use this data as the reference data taken in the following condition.

1. Measurement Condition

Condition:	Mount on a board
Ambient:	Natural convection
Soldering:	Lead (Pb) free
Board:	Dimensions 40×40mm (1600mm^2 in one side) Copper (Cu) traces occupy 50% of the front and 50% of the back is 12.5% of total. The copper area is divided into four block, one block is 12.5% of total. The USPN-4 package has for terminals. Each terminal connects one copper block in the front and one in the back.
Material:	Glass Epoxy (FR-4)
Thickness:	1.6mm
Through-hole:	4 x 0.8 Diameter

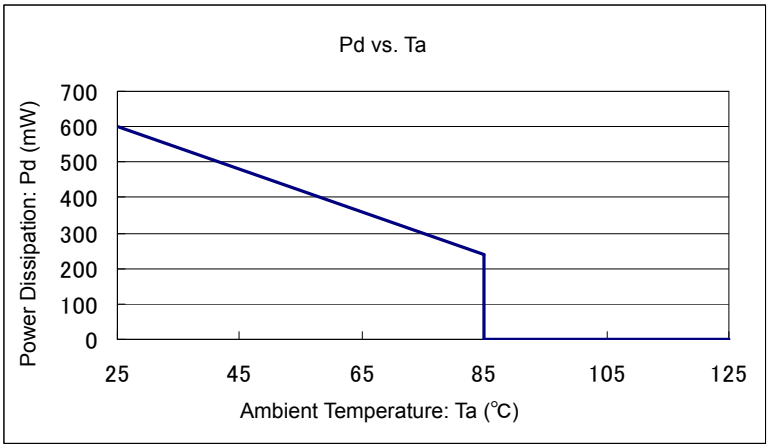


Evaluation Board (Unit: mm)

2. Power Dissipation vs. Ambient Temperature

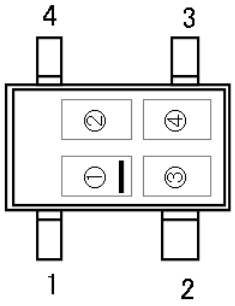
Board Mount (Tjmax=125℃)

Ambient Temperature (℃)	Power Dissipation Pd (mW)	Thermal Resistance (℃/W)
25	600	166.67
85	240	



■MARKING RULE

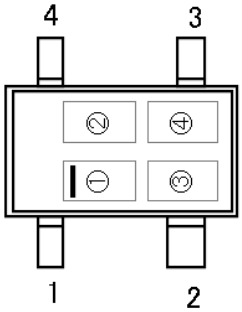
●SSOT-24
(with underline mark)



Indicates mark (1) product series. Indicates the detect voltage range and output type.
Mark (1)-1 (XC6129C*****-G is underline mark specification.)

MARK	OUTPUT	DETECT VOLTAGE RANGE (V)	TYPE	PRODUCT SERIES
0	CMOS	Odd number	A	XC6129C15A**-G to XC6129C55A**-G
1			B	XC6129C15B**-G to XC6129C55B**-G
2			C	XC6129C15C**-G to XC6129C55C**-G
3			D	XC6129C15D**-G to XC6129C55D**-G
4			E	XC6129C15E**-G to XC6129C55E**-G
5			F	XC6129C15F**-G to XC6129C55F**-G
6			G	XC6129C15G**-G to XC6129C55G**-G
8			J	XC6129C15J**-G to XC6129C55J**-G
A			L	XC6129C15L**-G to XC6129C55L**-G
C		Even number	A	XC6129C16A**-G to XC6129C54A**-G
D			B	XC6129C16B**-G to XC6129C54B**-G
E			C	XC6129C16C**-G to XC6129C54C**-G
F			D	XC6129C16D**-G to XC6129C54D**-G
H			E	XC6129C16E**-G to XC6129C54E**-G
K			F	XC6129C16F**-G to XC6129C54F**-G
L			G	XC6129C16G**-G to XC6129C54G**-G
N			J	XC6129C16J**-G to XC6129C54J**-G
R			L	XC6129C16L**-G to XC6129C54L**-G

●SSOT-24
(with overline mark)



Mark (1)-2 (XC6129N*****-G is overline mark specification.)

MARK	OUTPUT	DETECT VOLTAGE RANGE (V)	TYPE	PRODUCT SERIES
0	N-ch	Odd number	A	XC6129N15A**-G to XC6129N55A**-G
1			B	XC6129N15B**-G to XC6129N55B**-G
2			C	XC6129N15C**-G to XC6129N55C**-G
3			D	XC6129N15D**-G to XC6129N55D**-G
4			E	XC6129N15E**-G to XC6129N55E**-G
5			F	XC6129N15F**-G to XC6129N55F**-G
6			G	XC6129N15G**-G to XC6129N55G**-G
8			J	XC6129N15J**-G to XC6129N55J**-G
A			L	XC6129N15L**-G to XC6129N55L**-G
C		Even number	A	XC6129N16A**-G to XC6129N54A**-G
D			B	XC6129N16B**-G to XC6129N54B**-G
E			C	XC6129N16C**-G to XC6129N54C**-G
F			D	XC6129N16D**-G to XC6129N54D**-G
H			E	XC6129N16E**-G to XC6129N54E**-G
K			F	XC6129N16F**-G to XC6129N54F**-G
L			G	XC6129N16G**-G to XC6129N54G**-G
N			J	XC6129N16J**-G to XC6129N54J**-G
R			L	XC6129N16L**-G to XC6129N54L**-G

■MARKING RULE (Continued)

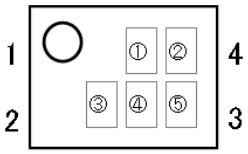
② represents detect voltage

MARK	DETECT VOLTEGE(V)		MARK	DETECT VOLTEGE(V)		MARK	DETECT VOLTEGE(V)	
A	1.5	1.6	K	2.9	3.0	T	4.3	4.4
B	1.7	1.8	L	3.1	3.2	U	4.5	4.6
C	1.9	2.0	M	3.3	3.4	V	4.7	4.8
D	2.1	2.2	N	3.5	3.6	X	4.9	5.0
E	2.3	2.4	P	3.7	3.8	Y	5.1	5.2
F	2.5	2.6	R	3.9	4.0	Z	5.3	5.4
H	2.7	2.8	S	4.1	4.2	0	5.5	-

③,④ represents production lot number
01～09, 0A～0Z, 11～9Z, A1～A9, AA～AZ, B1～ZZ repeated.
(G, I, J, O, Q, W excluded)
* No character inversion used.

■MARKING RULE (Continued)

●USPN-4



① represents detect voltage

MARK	OUTPUT	PRODUCT SERIES
K	CMOS	XC6129C*****-G
L	N-ch	XC6129N*****-G

② represents detect voltage range and product series

MARK	DETECT VOLTAGE RANGE (V)	TYPE	PRODUCT SERIES
0	Odd number	A	XC6129*15A**-G ～ XC6129*55A**-G
1		B	XC6129*15B**-G ～ XC6129*55B**-G
2		C	XC6129*15C**-G ～ XC6129*55C**-G
3		D	XC6129*15D**-G ～ XC6129*55D**-G
4		E	XC6129*15E**-G ～ XC6129*55E**-G
5		F	XC6129*15F**-G ～ XC6129*55F**-G
6		G	XC6129*15G**-G ～ XC6129*55G**-G
8		J	XC6129*15J**-G ～ XC6129*55J**-G
A		L	XC6129*15L**-G ～ XC6129*55L**-G
C	Even number	A	XC6129*16A**-G ～ XC6129*54A**-G
D		B	XC6129*16B**-G ～ XC6129*54B**-G
E		C	XC6129*16C**-G ～ XC6129*54C**-G
F		D	XC6129*16D**-G ～ XC6129*54D**-G
H		E	XC6129*16E**-G ～ XC6129*54E**-G
K		F	XC6129*16F**-G ～ XC6129*54F**-G
L		G	XC6129*16G**-G ～ XC6129*54G**-G
N		J	XC6129*16J**-G ～ XC6129*54J**-G
R		L	XC6129*16L**-G ～ XC6129*54L**-G

③ represents detect voltage

MARK	DETECT VOLTEGE(V)		MARK	DETECT VOLTEGE(V)		MARK	DETECT VOLTEGE(V)	
A	1.5	1.6	K	2.9	3.0	T	4.3	4.4
B	1.7	1.8	L	3.1	3.2	U	4.5	4.6
C	1.9	2.0	M	3.3	3.4	V	4.7	4.8
D	2.1	2.2	N	3.5	3.6	X	4.9	5.0
E	2.3	2.4	P	3.7	3.8	Y	5.1	5.2
F	2.5	2.6	R	3.9	4.0	Z	5.3	5.4
H	2.7	2.8	S	4.1	4.2	0	5.5	-

④,⑤ represents production lot number
01～09, 0A～0Z, 11～9Z, A1～A9, AA～AZ, B1～ZZ repeated.
(G, I, J, O, Q, W excluded)
* No character inversion used.

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