TC35678FSG-002
TC35678FXG-002
Bluetooth® low energy IC

Rev 1.20

Contents

1. General Description

1.1. Product Concept

TC35678FSG and TC35678FXG (Later omitted TC35678.) are compliant with Bluetooth® core specification 4.2. RF analog parts and baseband digital parts are built in them, and TC35678 provides Bluetooth® HCI (Host Control Interface) functions and Bluetooth® low energy GATT profile functions defined by Bluetooth® core specifications. Additionally, this IC works as an application using low power Bluetooth® communication by storing the application program into built-in flash ROM.

1.2. Features

- Compliant with Bluetooth® Ver4.2 low energy
  - Built-in ARM® Cortex®-M0 (13 MHz or 26 MHz operation frequency is able to select to run)
  - On-chip mask ROM for Bluetooth® program (384 KB)
  - On-chip work RAM for Bluetooth® Baseband process (192 KB)
  - On-chip Flash-ROM (256 KB, More than 100,000 erase and program cycles)
  - Supports patch program loader function
- General Purpose IO (TC35678FSG 17 ports,TC35678FXG 32 ports)
- General Purpose Serial Interfaces
  - SPI interface (1 ch assigned to a General Purpose IO)
  - I^2C interface (1 ch assigned to a General Purpose IO)
- Host CPU Interface
  - UART interface (9600 bps to 921.6 kbps, 2 ch - shared with GPIOs)
  - SPI interface
- Emulator debug control interface
  - SWD(Serial Wire Debug)2-wire (1 ch)
- Wake-up Interface (2 ch assigned to a General Purpose IO)
  - Wake-up input function from sleep and deep sleep
- PWM Interface (4 ch assigned to General Purpose IOs)
- Reference Clock Input (26 MHz)
  - Built-in oscillator for crystal oscillator connection
- Sleep Clock Input (32.768 kHz)
  - External oscillator input supported
  - Built-in oscillator for crystal oscillator connection
- Works as Standalone
- Sleep and Deep Sleep Functions
- Built-in DCDC converter and LDO
  - Wide range of input power supply voltages supported (Booting power supply voltage : 1.9 to 3.6 V, low battery voltage detection.)
- Built-in general purpose ADC
  - External analog inputs assigned to GPIOs (TC35678FSG-5 ch, TC35678FXG-7 ch)
  - Internal VDD monitoring (1 ch - connected inside)
- Package:
  - TC35678FSG: QFN Package [40 pin, 5 x5 mm, 0.4 mm pitch, 0.9 mm thickness]
  - TC35678FXG: QFN Package [60 pin, 7 x7 mm, 0.4 mm pitch, 0.9 mm thickness]

2. Pin Function

2.1. TC35678FSG Pin Assignment (Top View)

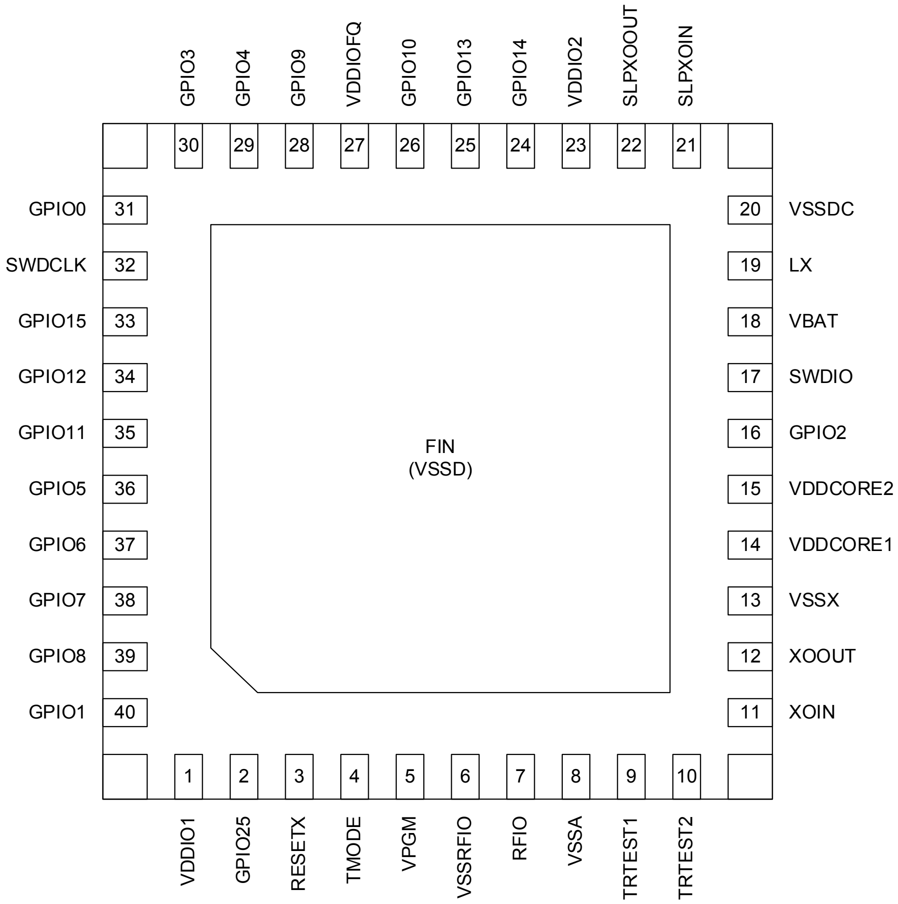


Figure 2-1 Pin Assignment (Top View)

2.2. TC35678FXG Pin Assignment (Top View)

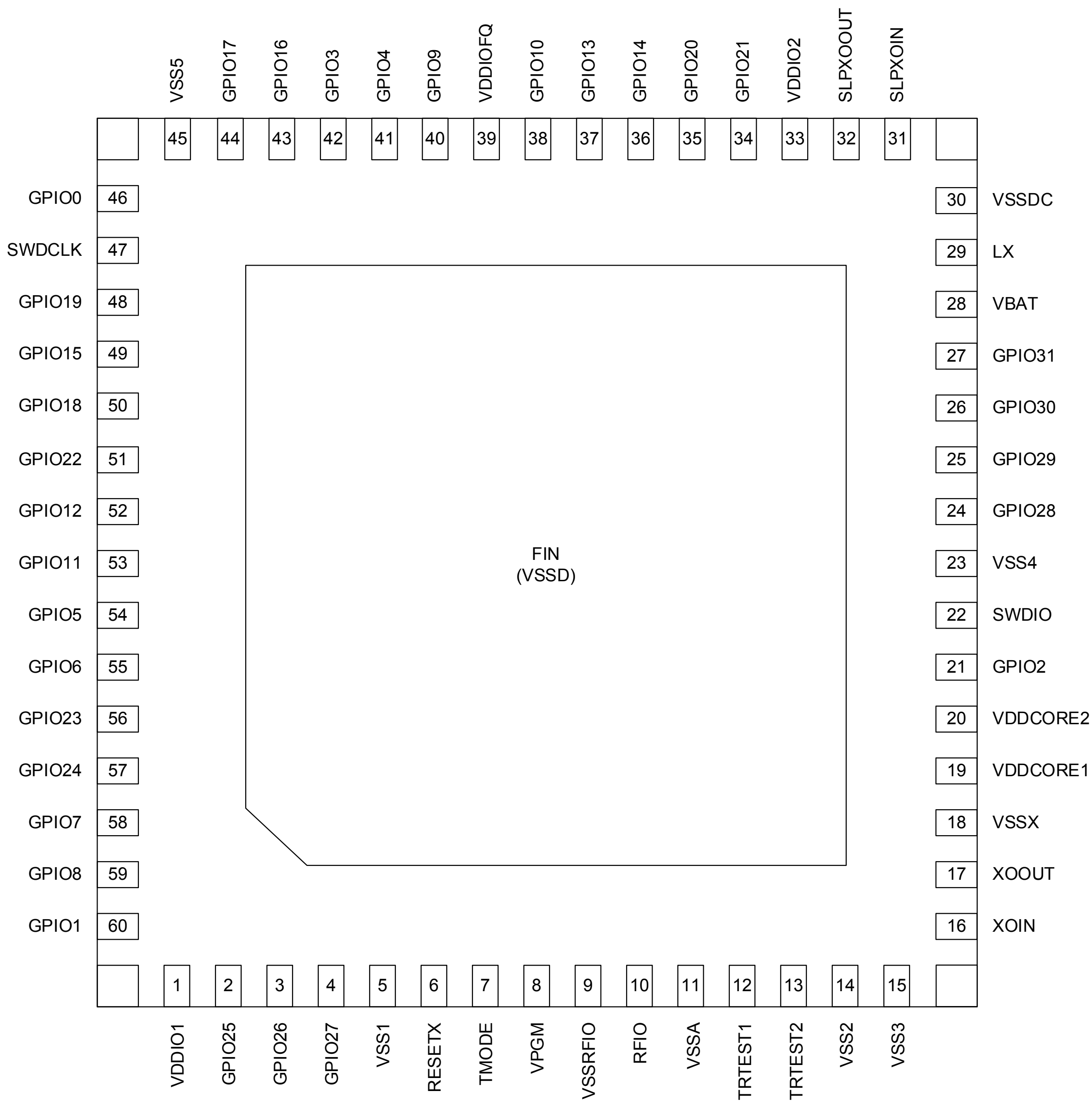


Figure 2-2 TC35678FXG Pin Assignment (Top View)

2.3. Pin Function Descriptions

Table 2-1 shows attributes, input/output states for operating modes and descriptions for pin functions. Table 2-4 shows descriptions about power supply pins.

Table 2-1 Pin Functions

Pin name	Pin No.		Attribute	Condition	Functional description
	QFN 40	QFN 60	VDD category Direction Type	Default (during reset)	
Reset interface					
RESETX	3	6	VDDIO IN Schmitt trigger	—	Hardware reset input pin. Setting this pin to Low level put the system at reset state.
Clock interface					
XOIN	11	16	VDDCORE IN OSC	IN	Reference clock input pin. Please use oscillator with 26 MHz and < 50 ppm accuracy. A feedback resistor is built in between XOIN pin and XOOUT pin and a capacity array which can set parameters in the crystal oscillation circuit is built-in, so that external feedback resistances and capacities are unnecessary.
XOOUT	12	17	VDDCORE OUT OSC	OUT	Oscillator output for Baseband and RF reference clock (26 MHz) pin. A feedback resistor is built in between XOIN pin and XOOUT pin and a capacity array which can set parameters in the crystal oscillation circuit is built-in, so that external feedback resistances and capacities are unnecessary.
SLPXOIN	21	31	VDDIO IN OSC	IN	Sleep clock input pin from oscillator. Please use an oscillator with 32.768 kHz and < 500 ppm accuracy. A feedback resistor is built in between SLPXOIN pin and SLPXOOUT pin and a capacity array which can set parameters in the crystal oscillation circuit is built-in, so that external feedback resistances and capacities are unnecessary. An external clock can be input from this pin. When the crystal oscillator is not used and do not supply a clock from the outside, this pin should be connected to the GND.
SLPXOOUT	22	32	VDDIO IN/OUT OSC	OUT	Sleep clock output pin from oscillator. A feedback resistor is built in between SLPXOIN pin and SLPXOOUT pin and a capacity array which can set parameters in the crystal oscillation circuit is built-in, so that external feedback resistances and capacities are unnecessary. When the crystal oscillator is not used, this pin should be connected to the GND.

Pin name	Pin No.		Attribute	Condition	Functional description
	QFN 40	QFN 60	VDD category Direction Type	Default (during reset)	
			RF interface		
RFIO	7	10	VDDCORE IN/OUT Analog	—	RF I/O pins. This product incorporates the 50 Ω matching circuit, so that external matching circuit is unnecessary. The RF output pattern should wire with the 50 Ω transmission line. For details, refer to the hardware application note of this product.
			General purpose I/O port		
GPIO0	31	46	VDDIO IN/OUT Pull-up Pull-down Schmitt trigger	Hi-Z	General purpose I/O pin. During reset, the pull-up and pull-down resistors are unconnected (input disable state). The same state continues just after the reset is released, and it will be controlled by software after that. After the pin configuration by software processing, it works as a GPIO pin of the input and output or Table 2-2 function. Pin processing when not using this function are listed in Table 2-2. (Note)
GPIO1 GPIO2 GPIO5 GPIO6 GPIO7 GPIO8 GPIO11 GPIO12 GPIO16 GPIO17 GPIO18 GPIO19 GPIO22 GPIO23 GPIO24 GPIO25 GPIO26 GPIO27 GPIO28 GPIO29 GPIO30 GPIO31	40 16 36 37 38 39 35 34 — — — — — — — 2 — — — — — —	60 21 54 55 58 59 53 52 43 44 50 48 51 56 57 2 3 4 24 25 26 27	VDDIO IN/OUT Pull-up Pull-down Schmitt trigger	Pull-up	General purpose I/O pin. During reset, the pull-up resistor is connected (input disable state). The pull-up resistor is connected (input state) just after the reset is released, and it will be controlled by software after that. After the pin configuration by software processing, it works as a GPIO pin of the input and output or Table 2-2 function. Pin processing when not using this function are listed in Table 2-2. In addition, GPIO1 pin is used in the case of switching operation modes. (Note)

Pin name	Pin No.		Attribute	Condition	Functional description
	QFN 40	QFN 60	VDD category Direction Type	Default (during reset)	
GPIO3 GPIO4 GPIO9 GPIO10 GPIO14 GPIO20 GPIO21	30 29 28 26 24 — —	42 41 40 38 36 35 34	VDDIO IN/OUT Pull-up Pull-down Schmitt trigger	Hi-Z	ADC input and general purpose I/O pin. During reset, the pull-up and pull-down resistors are unconnected (input disable state). The same state continues just after the reset is released, and it will be controlled by software after that. After reset, the software configures pull-up/pull-down resistors, and the pin can function as general purpose IO, or general ADC input. Pin processing when not using this function are listed in Table 2-2. (Note)
GPIO13	25	37	VDDIO IN/OUT Pull-up Pull-down Schmitt trigger	Pull-up	General purpose IO pin. During reset, the pull-up resistor is connected (input disable state). The pull-up and pull-down resistors are unconnected (input disable state) just after the reset is released, and it will be controlled by software after that. After the pin configuration by software processing, it works as a GPIO pin of the input and output or Table 2-2 function. (Note)
GPIO15	33	49	VDDIO IN/OUT Pull-up Pull-down Schmitt trigger	Hi-Z	General purpose I/O pin. During reset, the pull-up and pull-down resistors are unconnected (input disable state). The pull-up resistor is connected (input state) just after the reset is released, and it will be controlled by software after that. After the pin configuration by software processing, it works as a GPIO pin of the input and output or Table 2-2 function. Pin processing when not using this function are listed in Table 2-2. (Note)
SWDCLK	32	47	VDDIO IN Pull-up Pull-down Schmitt trigger	Pull-down	Serial Wire debugger clock pin. During reset, the pull-down resistor is connected (input state). After the reset is released, the serial wire debugger clock is inputted. When not used, this pin should be open.
SWDIO	17	22	VDDIO IN/OUT Pull-up Pull-down Schmitt trigger	Pull-up	Serial Wire Debugger data pin and operation switching pin. During reset, the pull-up resistor is connected (input state). After the reset is released, the serial wire debugger data is inputted and outputted. When not used, this pin should be open.

Pin name	Pin No.		Attribute	Condition	Functional description
	QFN 40	QFN 60	VDD category Direction Type	Default (during reset)	
IC test interface					
TMODE	4	7	VDDIO IN Schmitt trigger	—	Test mode setting pins. These pins are used for IC manufacturing test and need to be connected to GND when assembled on a board.
TRTEST1 TRTEST2	9 10	12 13	VDD12A IN/OUT Analog	—	Analog test pins. These pins are used for IC manufacturing test and need to be connected to GND when assembled on a board.

Note: The state of the GPIO pin corresponds to the usage state in the user application mode. Since states differ partially when the operation is powered on with the HCI mode, please refer to the software application note about the detailed state and its setting method of each pin.

2.4. GPIO function list

GPIO pins can be assigned to UART I/Fs, serial memory I/Fs and etc. by TC35678 firmware or command from external Hosts. Table 2-2 shows available functions for each GPIO pin, and Table 2-3 examples of GPIO function settings. About what function name shown in Table 2-2 is assigned to a plurality of pins in the same, please note that it cannot be assigned to select a plurality of pins at the same time.

Table 2-2 Available functions for GPIO

Pin name	Function 1	Function 2	Function 3	Function 4	Analog input	The pins of Unused
GPIO0	WakeUp0 Input	—	—	—	—	Open
GPIO1	PWM0 Output	—	—	—	—	Open (Note)
GPIO2	PWM1 Output	—	—	—	—	Open (Note)
GPIO3	PWM2 Output	SPI-DOUT Output	—	—	ADC1 Input	Open
GPIO4	PWM3 Output	SPI-DIN Input	—	—	ADC2 Input	Open
GPIO5	UART1-TX Output	SPI-DOUT Output	—	—	—	Open
GPIO6	UART1-RX Input	SPI-DIN Input	—	—	—	Open
GPIO7	I2C-SCL Output	UART2-TX Output	SPI-SCS Output	UART1-RTSX Output	—	Open
GPIO8	I2C-SDA I/O	UART2-RX Input	SPI-SCLK Output	UART1-CTSX Input	—	Open
GPIO9	—	—	—	—	ADC3 Input	Open
GPIO10	—	—	—	—	ADC4 Input	Open
GPIO11	I2C-SCL Output	SPI-DOUT Output	—	—	—	Open
GPIO12	I2C-SDA I/O	SPI-DIN Input	—	—	—	Open
GPIO13	UART1-RTSX Output	—	—	—	—	Open
GPIO14	UART1-CTSX Input	—	—	—	ADC5 Input	Open
GPIO15	WakeUp1 Input	—	—	—	—	Open
GPIO16	UART2-TX Output	—	—	—	—	Open
GPIO17	UART2-RX Input	—	—	—	—	Open
GPIO18	UART2-RTSX Output	—	—	—	—	Open
GPIO19	UART2-CTSX Input	—	—	—	—	Open
GPIO20	—	—	—	—	ADC6 Input	Open
GPIO21	—	—	—	—	ADC7 Input	Open
GPIO22	PWM2 Output	—	—	—	—	Open
GPIO23	PWM3 Output	—	—	—	—	Open
GPIO24 to 31	—	—	—	—	—	Open

Note: Handle with care because of using operation mode switching.

Table 2-3 GPIO function list (example)

Pin name	Basic example	Example of SPI unused	Example of SPI + I^2C	Example of UART + SPI + I^2C
GPIO0	WakeUp0	WakeUp0	WakeUp0	WakeUp0
GPIO1	PWM0	PWM0	PWM0	PWM0
GPIO2	PWM1	PWM1	PWM1	PWM1
GPIO3	SPI-DOUT	PWM2	PWM2	SPI-DOUT
GPIO4	SPI-DIN	ADC2	PWM3	SPI-DIN
GPIO5	UART1-TX	UART1-TX	SPI-DOUT	UART1-TX
GPIO6	UART1-RX	UART1-RX	SPI-DIN	UART1-RX
GPIO7	SPI-SCS	UART1-RTSX	SPI-SCS	SPI-SCS
GPIO8	SPI-SCLK	UART1-CTSX	SPI-SCLK	SPI-SCLK
GPIO9	ADC3	ADC3	ADC3	ADC3
GPIO10	ADC4	ADC4	ADC4	ADC4
GPIO11	I2C-SCL	I2C-SCL	I2C-SCL	I2C-SCL
GPIO12	I2C-SDA	I2C-SDA	I2C-SDA	I2C-SDA
GPIO13	UART1-RTSX	GPIO13	GPIO13	GPIO13
GPIO14	UART1-CTSX	ADC5	ADC5	ADC5
GPIO15	WakeUp1	WakeUp1	WakeUp1	WakeUp1
GPIO16	UART2-TX	UART2-TX	UART2-TX	UART2-TX
GPIO17	UART2-RX	UART2-RX	UART2-RX	UART2-RX
GPIO18	UART2-RTSX	UART2-RTSX	UART2-RTSX	UART2-RTSX
GPIO19	UART2-CTSX	UART2-CTSX	UART2-CTSX	UART2-CTSX
GPIO20	ADC6	ADC6	ADC6	ADC6
GPIO21	ADC7	ADC7	ADC7	ADC7
GPIO22	PWM2	GPIO22	GPIO22	GPIO22
GPIO23	PWM3	PWM3	GPIO23	GPIO23

Note: There are other functions than the above examples. About the detail of the other functions, refer to TC35678 firmware specification.

2.5. Power Supply Pins

Table 2-4 shows the attributes and descriptions of power supply pins for normal operations.

Table 2-4 Power supply pins

Pin name	Pin number		Attribute	Description
	QFN40	QFN60	Type VDD/GND	
				VDD/GND
VPGM	5	8	TEST —	Test pin Please connect VPGM to GND.
VBAT	18	28	VBAT VDD	Power supply pin for DCDC and sleep circuit. Connect the external power source for DCDC and LDO built into the IC.
LX	19	29	VBAT VDD	DCDC output pin. Please connect to external inductor for DCDC.
VDDCORE1	14	19	— VDD	DCDC for feedback input, analog circuit power supply pin. Please connect to external inductor for DCDC.
VDDCORE2	15	20	— VDD	DCDC for feedback input, digital circuit power supply pin. Please connect to external inductor for DCDC.
VDDIO1 VDDIO2	1 23	1 33	VDDIO VDD	IO power supply Power supply pin for GPIO.
VDDIOFQ	27	39	VDDIOFQ VDD	Flash ROM external capacitor connection pin. It has been connected to the power supply of the internal flash ROM of the IC. As the LDO load capacitor, a capacitor of 0.1 μF or more should be connected at the operation temperature.
VSS1 VSS2 VSS3 VSS4 VSS5	—	5 14 15 23 45	— GND	GND pin This pin is the unused inside the IC. Please connect to GND.
VSSA	8	11	Analog GND	GND pin for analog, this pin needs to be connected to GND.
VSSRFIO	6	9	Analog GND	GND pin for RFIO, this pin needs to be connected to GND.
VSSX	13	18	Analog GND	GND pin for OSC, this pin needs to be connected to GND.
VSSDC	20	30	Digital GND	GND pin for DCDC, this pin needs to be connected to GND.
VSSD	FIN	FIN	Digital GND	Die pad ground Fin. Connect the exposed Die Pad to GND because this pad is digital ground as well.

3. System Configuration

3.1. Block Diagram

Figure 3-1 shows block diagram of TC35678.

TC35678 is powered by single voltage between 1.9 V and 3.6 V.

The chip has built-in DCDC and LDO requiring external capacitors. It uses 26 MHz reference clock and 32.768 kHz sleep clock.

EEPROM Interface is SPI or I^2C, and host CPU interface is UART.

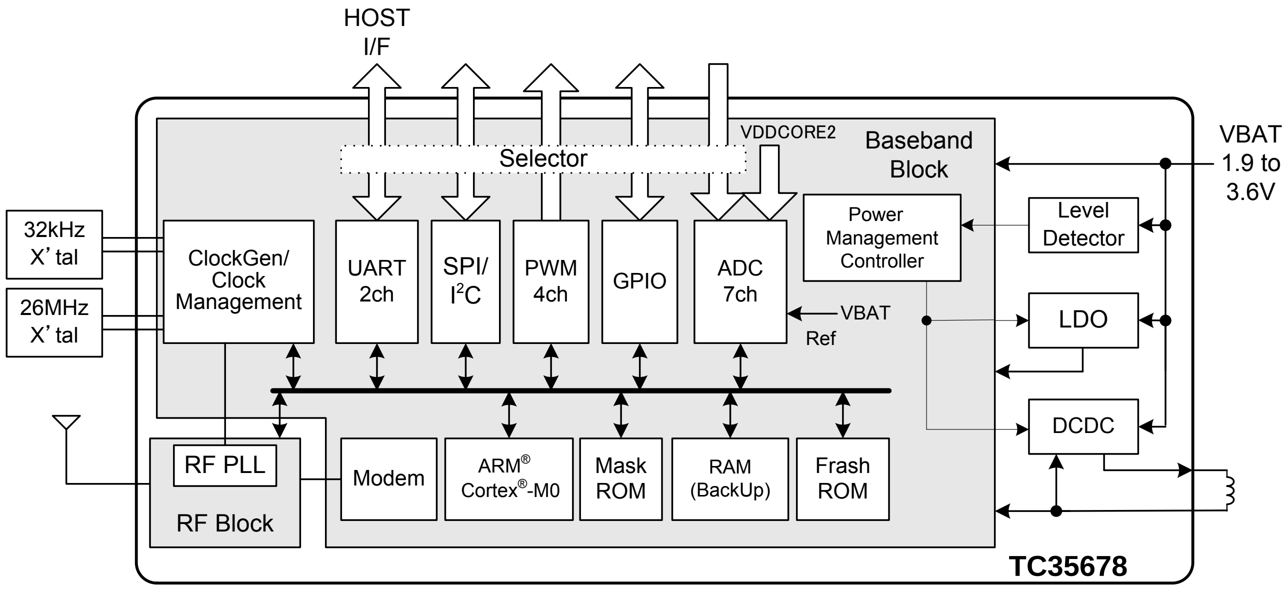


Figure 3-1 Example of TC35678 system configuration

4. Functional Specifications

4.1. Bluetooth® Function

The Bluetooth® function is realized by using the hardware which is configured with RF analog and baseband, and the software on a mask ROM. Only connecting a crystal oscillator and some discrete parts externally, the Bluetooth® wireless communication can work.

4.1.1. Supported Function

This function is compliant with Bluetooth® V4.2 low energy standard. Main supported functions are shown below.

Table 4-1 List of supported functions

Items	Description	Notes
Bluetooth® Core	4.2	LE is supported.
v4.0 features	Central	Supported
	Peripheral	Supported
	Multi Profile/point	Supported
	Connection Update	Supported
	Random Address	Supported
	WhiteList	Supported
	Security Property (Just Works)	Supported
	Security Property (PassKey Entry)	Supported
	Security Property (OOB)	Supported
	Security Property (Numeric Comparison)	Supported
	GATT-Client	Supported
	GATT-Server	Supported
	Broadcaster	Supported
	Observer	Supported
v4.1 features	Low Duty Cycle Directed Advertising	Supported
	32-bit UUID support in LE	Supported
	LE L2CAP Connection Oriented Channel Support	Supported
	LE Privacy v1.1	Supported
	Connection Parameter Request Procedure	Supported
	Extended Reject Indication	Supported
	Slave-initiated Features Exchange	Supported
	LE Ping	Supported
	Act as LE Master and LE Slave at the same time	Supported
	Act as LE Slave to more than one LE Master at the same time	Supported
v4.2 features	LE Data Packet Length Extension	Supported
	LE Secure Connections	Supported
	Link Layer Privacy	Supported
	Link Layer Extended Scanner Filter Policies	Supported

4.1.2. Support Protocol Layer

Following figure shows the Bluetooth Protocol and Profile Layer supported.

It has RF control, Link layer, internal HCI, L2CAP, ATT, SMP and GATT.

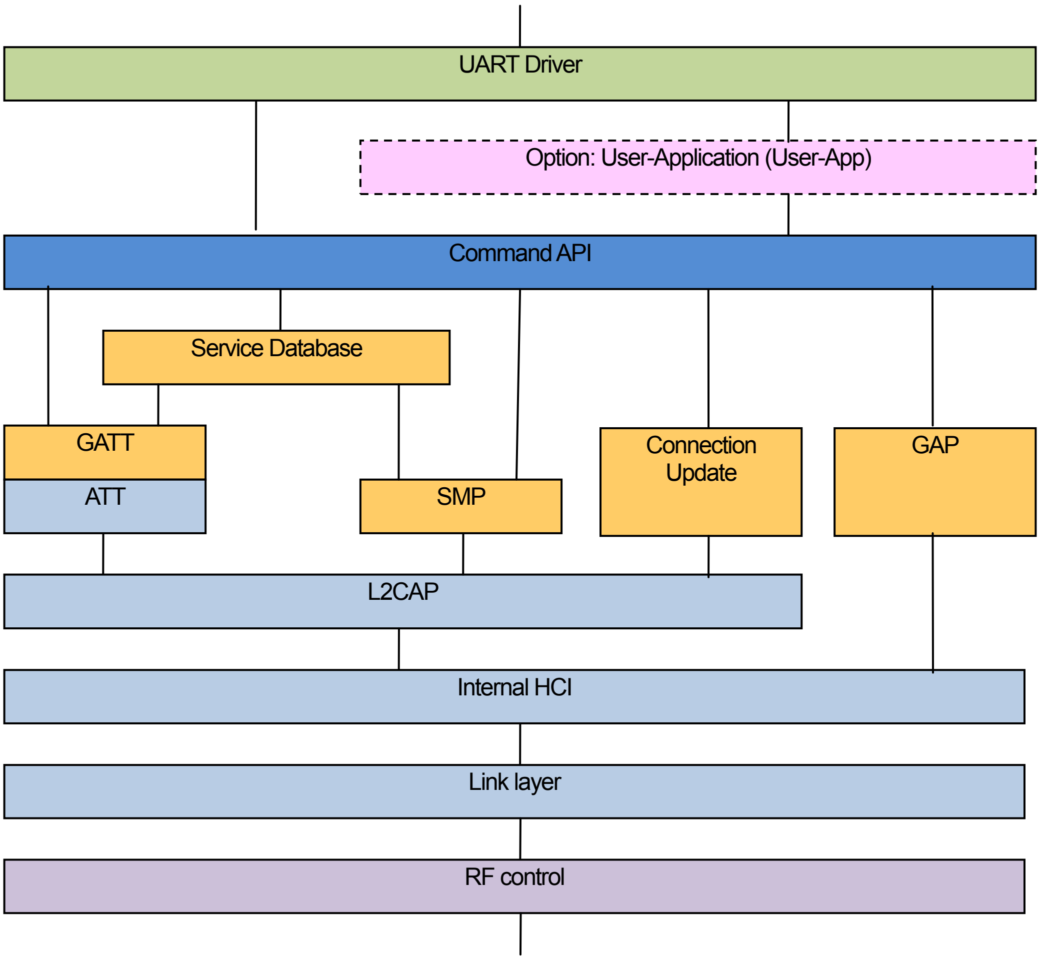


Figure 4-1 Protocol Layer

4.1.3. RF

Since the RF analog part of TC35678 builds in not only transmission and reception circuits but also the RF switch and the matching circuit, the RFIO pin which is a single I/O does not need an external matching circuit. The wireless device which suits for RF-PHY specifications of Bluetooth low energy can be realized easily by connecting to 50 Ω wiring.

The transmission power can be selected from intended power between 0 and -20 dBm (4 dB steps). Not only default transmission power but also transmission power to the specified destination can be set. The RSSI of reception block has an accuracy of ± 2 dB (typ.) to the input signal between -90 and -10 dBm.

4.1.4. Auto Advertise Function

Using an auto advertise function enables repeating transmissions of advertise packets with very small power. The auto advertise function is a function which transmits intended advertise packets without waking CPU up in Backup mode. Then, a scan request and a connection request can be also received. The response to the remote device can be preset in case of receiving a scan request, and when one connection request is received, this function wakes CPU up and leaves a subsequent process to the user software.

4.2. Reset Interface (Power up sequence)

4.2.1. Features

Reset interface has the following features.

- 1.9 to 3.6 V operation
- Level sensitive asynchronous reset (Low level: reset)

When the power supply is applied, the external reset signal connected to the TC35678 should be held the reset state (RESETX = Low). Please release the reset (RESETX = High) after the power supply voltage reaches 1.9 V and becomes stable.

Then, the oscillation of a crystal oscillator is started, and the internal reset is released by the internal timer after the oscillation-stable time of the crystal oscillator is passed.

4.2.2. Connection Example

Reset signal can be input by an RC time constant circuit or an asynchronous level sensitive reset IC. Figure 4-2 shows a connection example where TC35678 is power-supplied by an RC time constant circuit. Reset signal can be given by RC time constant circuit. Figure 4-3 shows the timings to reset and reset-release for the power supply.

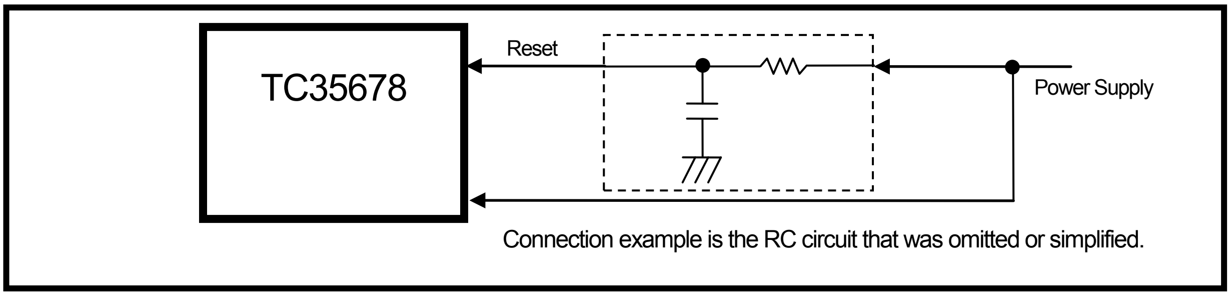


Figure 4-2 Reset signal connection example

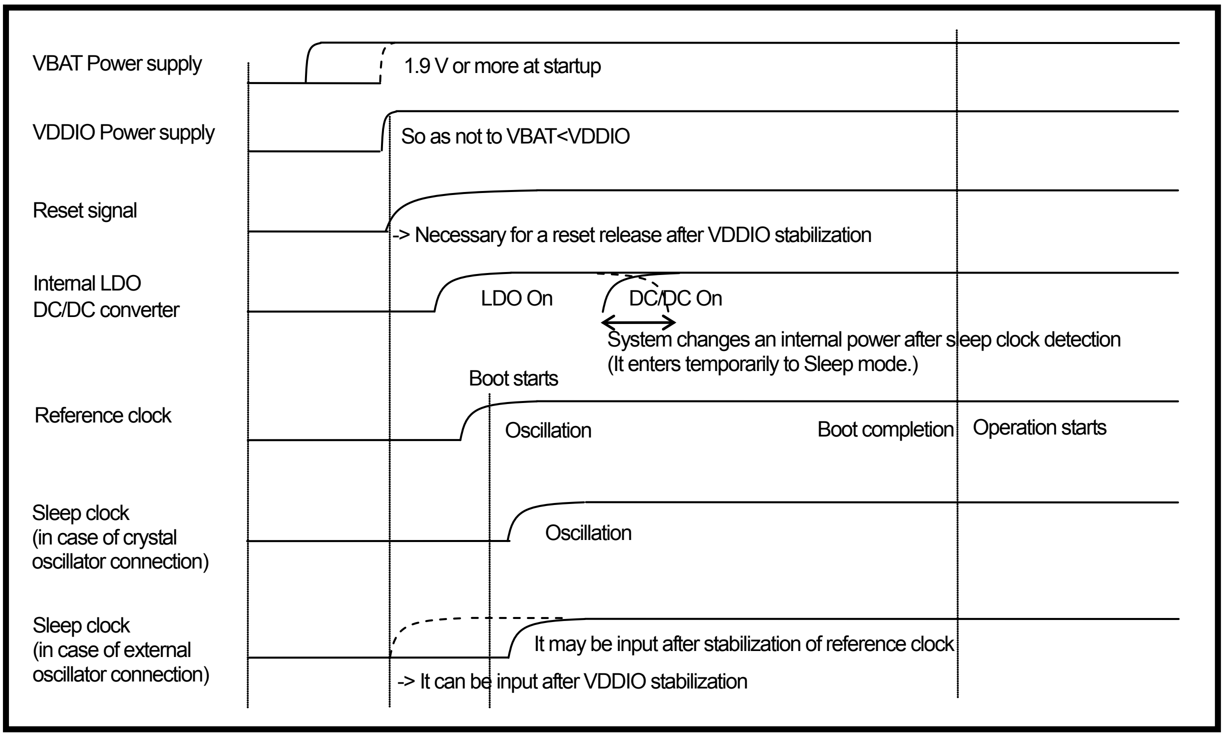


Figure 4-3 Power-on reset release sequence

4.3. UART Interface

4.3.1. Features

TC35678 UART interface has the following features.

- 1.8 to 3.6 V operation
- Full-duplex start-stop synchronization data transfer (RX, TX)
- Two-wire start-stop synchronization data transfer (RX, TX) or four-wire start-stop synchronization data transfer (RX, TX, CTSX, RTSX) are available depending on the settings.
- Start bit field (1 bit), data bit field (8 bit, LSB first), stop bit field (1 bit), no parity bit
- In HCI mode, UART TX/RX pins can be switched by commands (UART2).
- Programmable baud rate: 9600 bps to 921.6 kbps.
- More than 3 characters are inserted between TX messages. Interval can be changed on the command.
- Error detection (character timeout, overrun error, framing error)
- Host wake up function

TC35678 communicates commands, status, and data with a host CPU through UART interfaces. The UART interfaces are shared with GPIO pins, and during boot process after a reset, TC35678 firmware assigns UART functions to the GPIOs. The UART interfaces can operate at 1.8 to 3.6 V depending on the VDDIO power supply voltage. Sharing the power supply pin with other hardware interfaces, they cannot operate at a different voltage from the one other hardware interfaces operate at.

4.3.2. Connection Example

TC35678 UART can be connected with an UART interface on a host CPU. Figure 4-4 shows an example of two-wire start-stop synchronization data transfer connection with an external host CPU. Figure 4-5 shows the timing when UART is assigned to GPIO and activated.

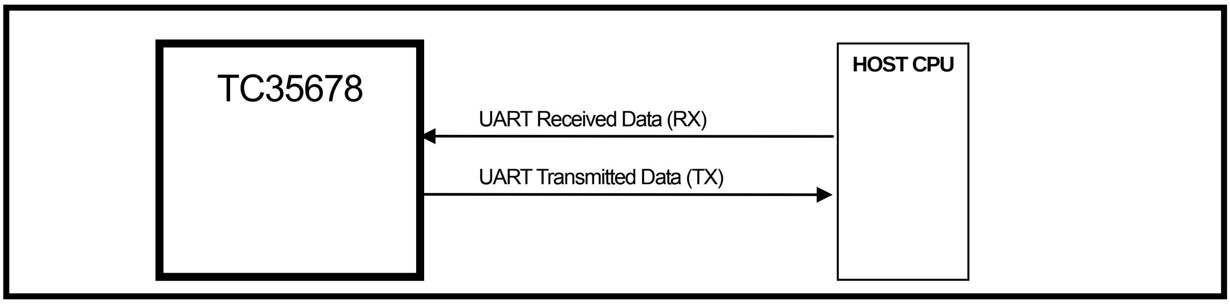


Figure 4-4 UART connection example

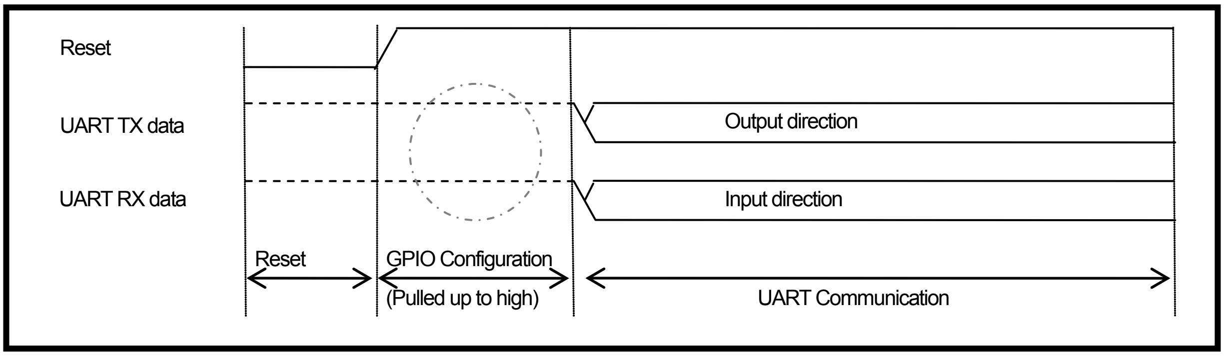


Figure 4-5 Timing for UART function assignment

4.3.3. Frame Format

TC35678 supports the following format:

- Number of data bits: 8 bits (LSB first)
- Parity bit: no parity
- Stop bit: 1 stop bit
- Flow control: RTSX/CTSX

Figure 4-6 shows UART data frame.

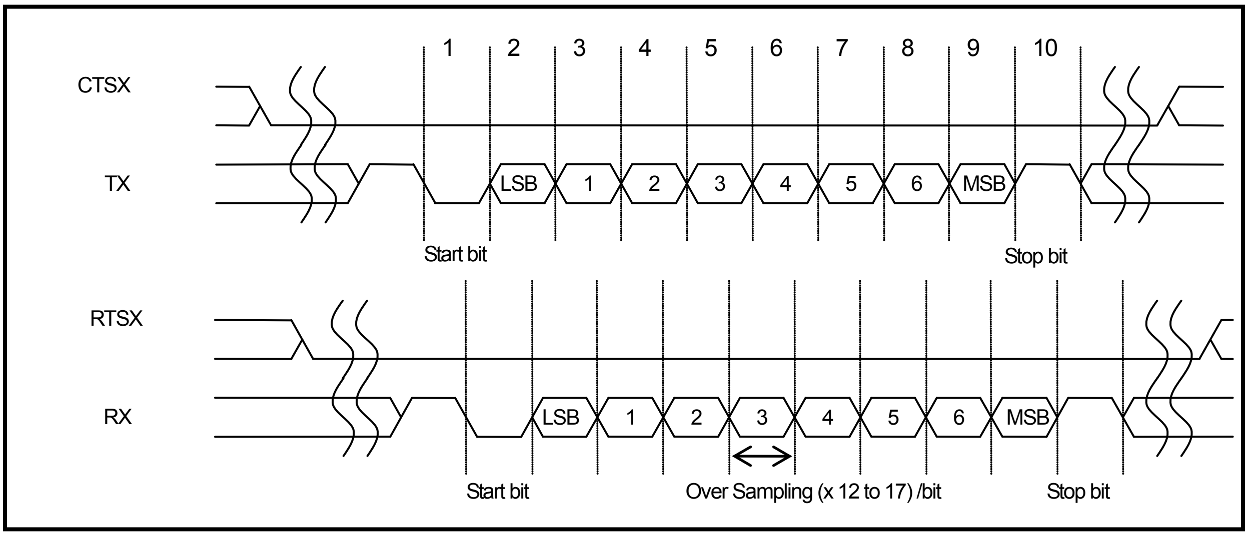


Figure 4-6 UART data frame

4.3.4. Flow Control Function

Hardware flow control is available when TC35678 UART interface is assigned to GPIO5 to GPIO8 (GPIO5, 6, 13, 14) as four-wire start-stop synchronization data transfer. Transmit flow control (CTSX) and receive flow control (RTSX). Figure 4-7 shows signals input and output direction.

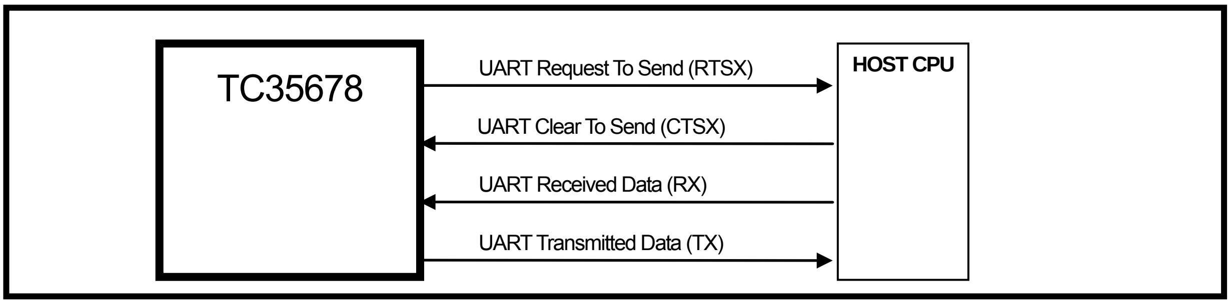


Figure 4-7 UART connection example

CTSX (Clear to Send) input signal is used for UART transmitting. Low input indicates the peer device (for example, the host in the Figure 4-7) is ready to receive data, and TC35678 sends data if it has data to transmit. On the other hand, TC35678 stops transmitting on the basis of UART unit frame when CTSX input is high.

RTSX (Request to Send) output signal is used for UART receiving. Low output indicates TC35678 is ready to receive data and requests data to the peer device. TC35678 outputs RTSX low when ready to receive data. When the UART becomes busy and cannot receive data, TC35678 outputs RTSX high, and stops UART communication on the basis of UART unit frame.

Response time of UART transmitting and receiving to flow control signals is between 1 frame to 4 frames depending on the baud rate and internal process status of frame.

4.3.5. UART Baud Rate Setting

TC35678 UART interface has a programmable baud rate setting function. The UART baud rate is generated from 26 MHz clock, and can be set according to the following equation depending on over sampling number and dividing ratio.

$$UART\,BaudRate = \frac{BaudRate\,Generating\,Clock\,Frequency}{Over\,Sampling\,Number \times Dividing\,Ratio}$$

Table 4-2 shows examples of UART Baud rate settings. If other target baud rates are required, please contact our engineering department.

Table 4-2 UART Baud rate settings

Target baud rate [bps]	Actual baud rate [bps]	Over sampling rate	Frequency dividing ratio
9600	9587.021	12	226
14400	14396.46	14	129
19200	19174.04	12	113
28800	28856.83	17	53
38400	38461.54	13	52
57600	57777.78	15	30
76800	76923.08	13	26
115200	115555.6	15	15
153600	153846.15	13	13
230400	232142.9	16	7
307200	305882.4	17	5
460800	464285.7	14	4
921600	928571.4	14	2

Note: Error of target baud rate and the actual baud rate is to be set to within 1%.

4.3.6. TX message spacing function

TC35678 spaces more than 12 time frames between different TX messages making less than 12 time frames between TX frames in a TX message when several TX frames belong to one TX message. Host CPU is able to know the boundaries between TX messages by measuring time frames between TX frames.

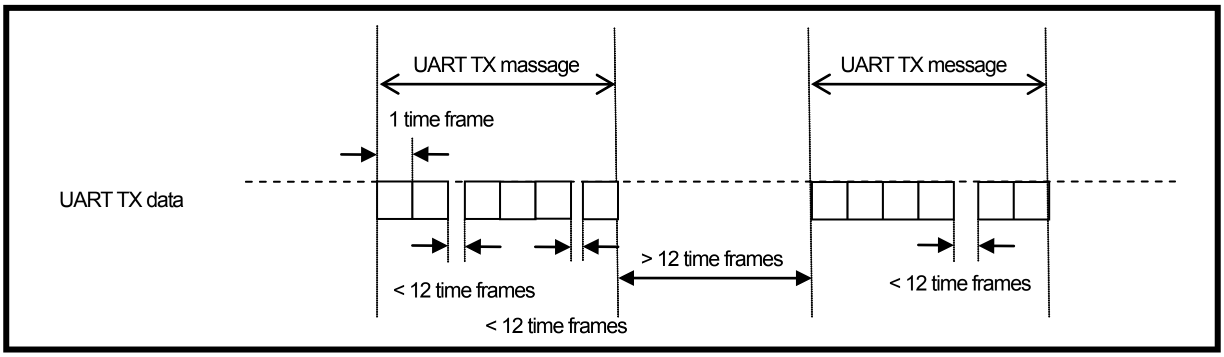


Figure 4-8 TX frames and TX messages

4.3.7. Error Detecting Functions

TC35678 UART interface has 3 kinds of error detecting functions.

- Receiver timeout error
- Receiver over run error
- Receiver frame error

Receiver timeout error detection judges an error if an UART RX message made from several RX frames has an RX frame interval longer than a certain value. The interval is counted by internal timer. Keep the interval between RX frames less than 12 time frames that belong to an RX message. For UART1, keep intervals between different RX messages more than 12 time frames. For example, 115200 bps has 0.087 ms for 1 frame, the interval between RX messages should be longer than 0.087 ms × 12 = 1.04 ms. RX messages that has intervals less than 12 time frames gives an error because TC35678 sees them as one UART RX message. Interval of the received frame is the default in the 12 time frame, but it can be changed by the command.
In the case of UART2, of different UART receive message interval is more than 14 ms.

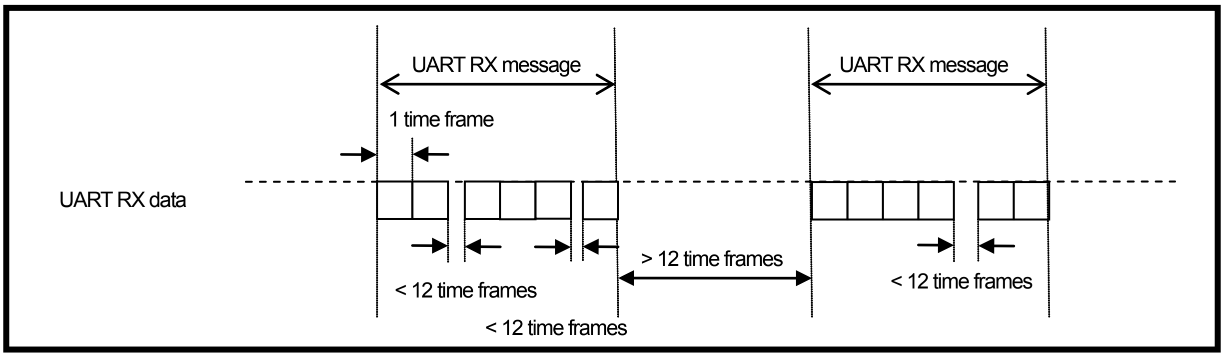


Figure 4-9 RX frames and RX messages

Receiver over run error judges if UART receive frame buffer internal TC35678 is overflowed. Normally, this overflow does not happen when the flow control mentioned in 4.2.4 is activated for data communication.
Receiver frame error judges if failing recognize the unit frame. A frame formation is judged as failure when its start bit is detected and the corresponding stop bit is detected as “0”.

4.3.8. Host Wake up Function

TC35678 can wakes up its host before sending UART data to the host. This function is disabled by default, but can be assigned to GPIO by command. Host wake up time can be changed by command (10 ms by default).

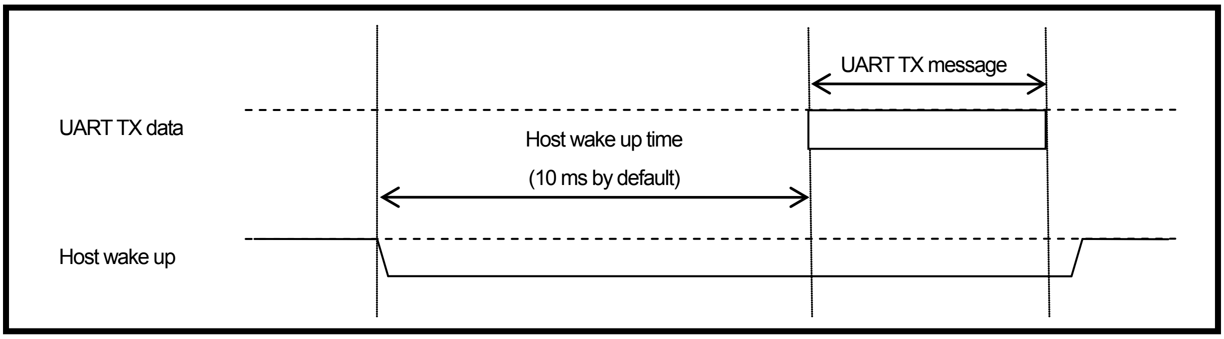


Figure 4-10 Host wake up

4.3.9. HCI mode

When TC35678 is used in the HCI mode, UART is the host interface to receive HCI commands. The Bluetooth® wireless performance can be tested in HCI mode by the measurement equipment which connects the UART directly.

4.3.9.1. HCI Reset

Sends a HCI reset command from the host, at least 150 μs from the command complete event can be processed the following command successfully.

4.4. SPI Interface

4.4.1. Features

TC35678 has the following main features for a serial memory interface

- Operation voltage: 1.8 to 3.6 V
- SPI interface
  - Chip select: 1 ch
  - Chip select polarity: Selectable: High-active and Low-active
  - Serial clock master operation: Polarity and phase are adjustable (4 combinations are selectable)
  - Serial clock frequency: 25 Hz to 6.5 MHz
  - Serial data transfer mode: MSB-first, LSB-first

SPI interface can operate at 1.8 to 3.6 V depending on VDDIO, however, cannot operate at different voltage from ones other interfaces are operate at.

4.4.2. Connection Example

TC35678 SPI interface can be connected to serial EEPROMs and serial Flash-ROMs and has 1 chip select port. Figure 4-11 shows a connection example, where a serial Flash-ROM is connected to TC35678 SPI interface.

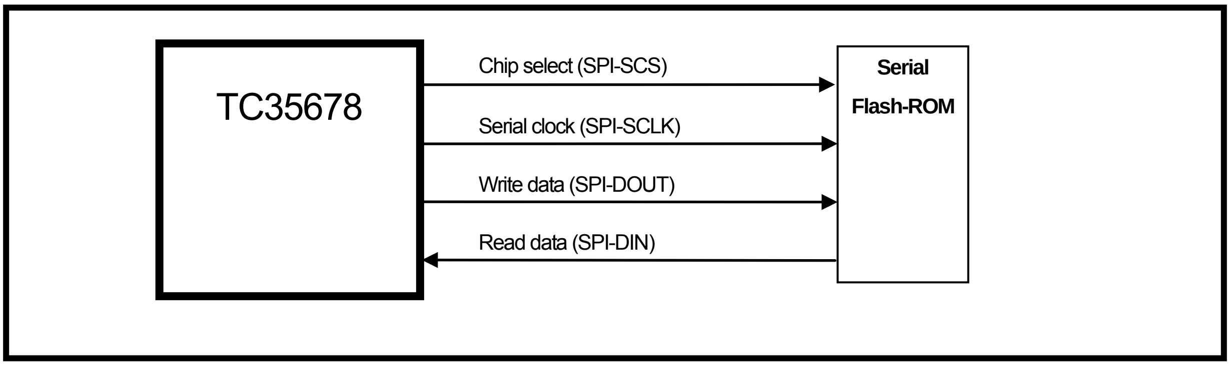


Figure 4-11 Connection example for serial Flash-ROM using SPI interface

4.4.3. Frame Format

When the SPI interface is connected to external ICs, the first 8 bit (X7 to X0) specifies the address and read or write mode. The command recognition code type and the address bit width should be determined by the external IC in use. For more information in detail, please refer to the technical documents for the external IC.

Figure 4-12 shows an example where 8-bit address is written and then 8-bit data is read. Figure 4-13 shows an example where 8-bit address is written and then 8-bit data is written.

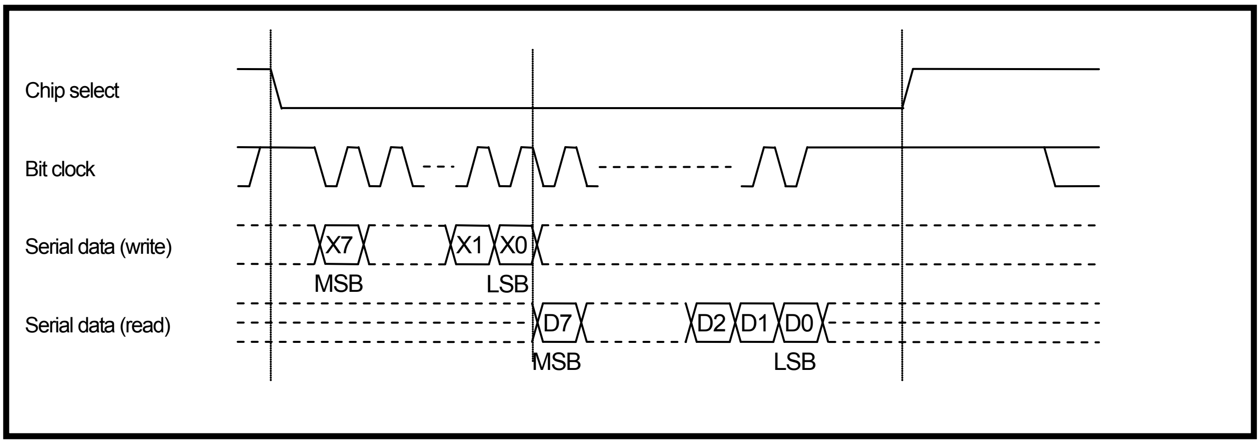


Figure 4-12 SPI format (single byte read)

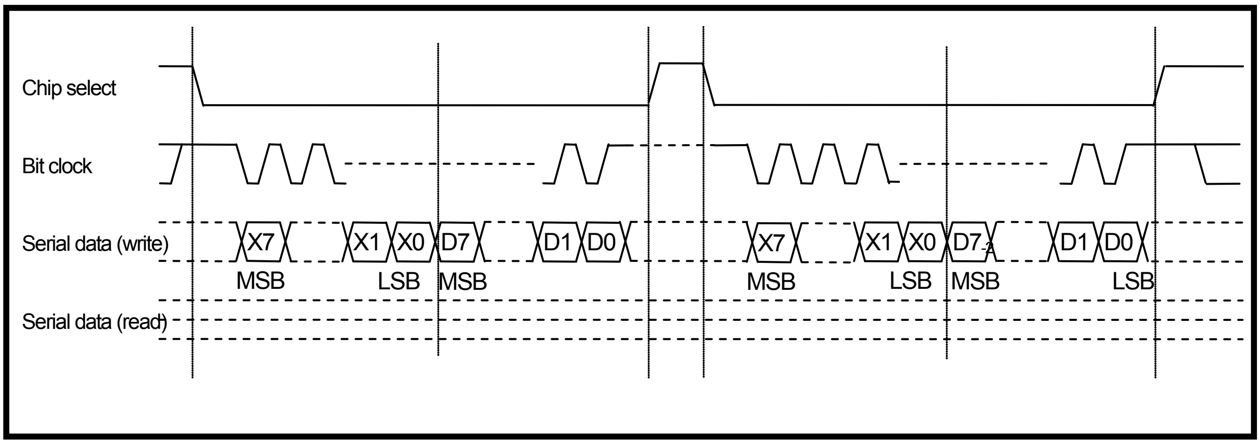


Figure 4-13 SPI format (single byte write)

4.5. I²C Interface

4.5.1. Features

I²C has the following main features for a serial interface.

- Operation voltage: 1.8 to 3.6 V
- I²C Interface
  - Operation mode: I²C bus master
  - Serial clock frequency: Standard mode (Max 100 kHz), Fast mode (Min 100 kHz to Max 400 kHz)
  - Output mode: Open-drain output, CMOS output
  - Device address format: 7-bit address (10-bit address is not supported)

I²C interface can operate at 1.8 to 3.6 V depending on VDDIO, however, cannot operate at different voltage from ones other interfaces are operate at.

4.5.2. Connection Example

Figure 4-14 shows a connection example of a serial EEPROM using I²C bus interface of the open-drain mode. External pull-up resistors (Rext) are necessary for both serial clock line and serial data line.
Figure 4-15 shows another connection example where I²C bus is in the CMOS output mode. Only the serial data line needs Rext because this line can be driven by neither TC35678 nor a serial EEPROM.

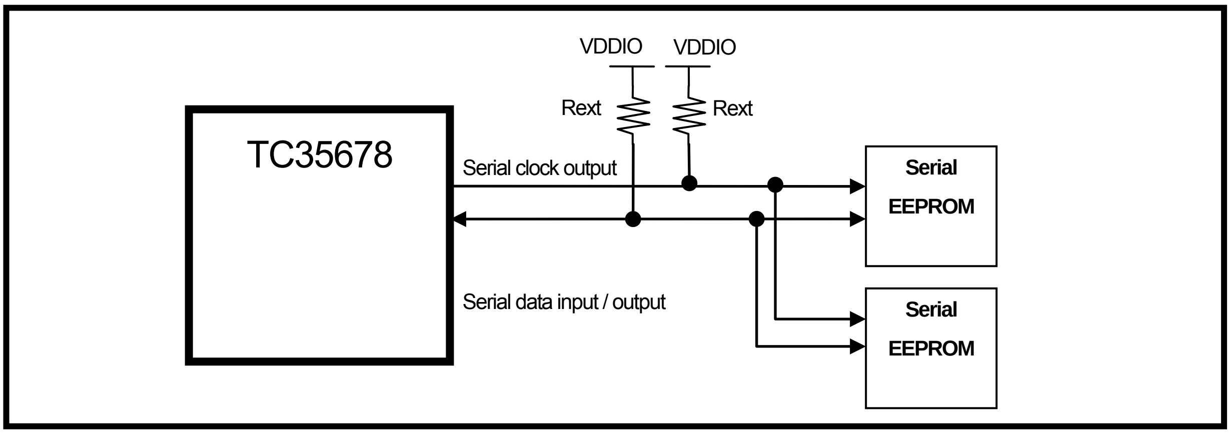


Figure 4-14 Connection example for serial EEPROM with I²C-bus interface (Open-drain output)

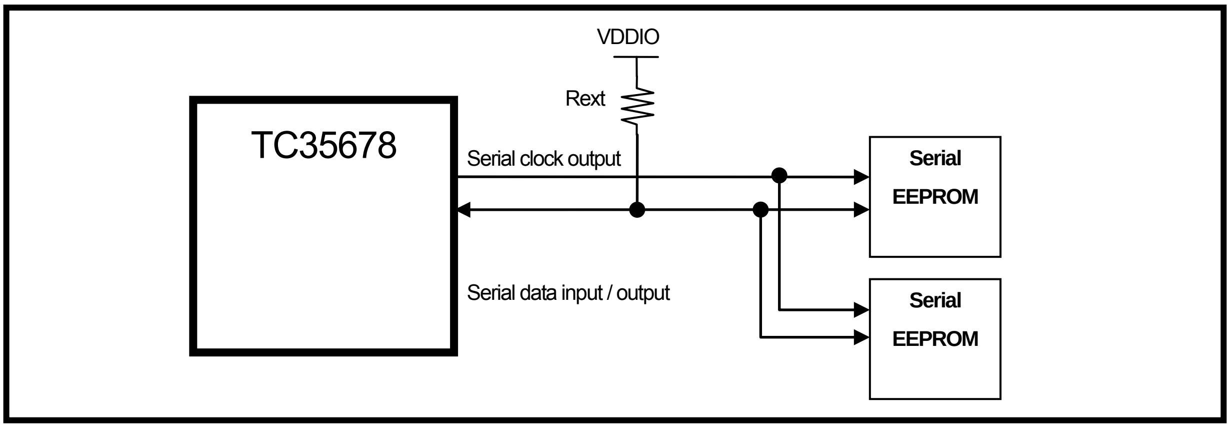


Figure 4-15 Connection example for serial EEPROM with I²C-bus interface (CMOS output)

4.5.3. Selection of External Pull-up Resistor Value

An external pull-up resistor value needs to be selected by the following equations in case of I^2C bus interface. Its maximum value is defined by equation (1), in which t_r is rise time of serial clock and data and C_b is I^2C bus capacity. Its minimum value is defined by equation (2), in which VDDIO is a supply voltage for TC35678, V_{ol_max} is the maximum value of low level output voltage, and I_{ol} is the low level output current. Please set the pull-up resistor value between these lower and upper limits.

$$R_{ext\_max} = \frac{t_r}{0.8473 \times C_b} \qquad (1)$$

$$R_{ext\_min} = \frac{VDDIO - V_{ol\_max}}{I_{ol}} \qquad (2)$$

TC35678 supports I^2C bus standard mode (Max 100 kHz) and I^2C bus fast mode (Min 100 kHz to Max 400 kHz). The rise time t_r is 1000 ns for the standard mode and it is 300 ns for the fast mode. C_b can vary depending on the IC board and how it is implemented. Table 4-3 and Table 4-4 show examples when I^2C bus capacity is 20 pF.

Table 4-3 External pull-up resistor value for I^2C standard mode (Cb = 20 pF)

I^2C bus frequency	Max 100 kHz								
tr [ns]	1000								
Cb [pF]	20								
VDDIO [V]	1.8			3.0			3.6		
Vol_max [V]	0.3			0.4			0.4		
Iol [mA]	1	2	4	1	2	4	1	2	4
Rext_min [kΩ]	1.50	0.75	0.38	2.60	1.30	0.65	3.20	1.60	0.80
Rext_max [kΩ]	59.01								

Table 4-4 External pull-up resistor value for I^2C fast mode (Cb = 20 pF)

I^2C bus frequency	Min 100 to Max 400 kHz								
tr [ns]	300								
Cb [pF]	20								
VDDIO [V]	1.8			3.0			3.6		
Vol_max [V]	0.3			0.4			0.4		
Iol [mA]	1	2	4	1	2	4	1	2	4
Rext_min [kΩ]	1.50	0.75	0.38	2.60	1.30	0.65	3.20	1.60	0.80
Rext_max [kΩ]	17.70								

4.5.4. Frame Format

For I^{2}C format, TC35678 first generates start condition. Then, it sends device recognition address (7 bit: [A6:A0]) and the first byte address ([B7:B0]) for the access target. Next, it goes for read or write sequence. For I^{2}C, every data is sent as MSB first. How to specify the value and byte address of the device identification address, and it has been determined in accordance with the device to be connected. In order to be connected, it must match the device to be connected. For read operation, TC35678 returns to the serial memory either receive acknowledge bit (ACK) or receive not acknowledge bit (NACK) every time it receives one byte. For write operation, TC35678 receives either ACK or NACK from the serial memory every time it sends one byte. It can handle not only one byte but also several bytes in a row. TC35678 generates stop condition when it has finished all the read or write of data.

Figure 4-16 shows an example where TC35678 reads two-byte data. Figure 4-17 shows an example where TC35678 writes two-byte data. In these examples, gray texts and lines indicate signals that are given by the serial memory. For read operation, after having read the final byte data, TC35678 returns NACK with which the serial memory gets to know the completion of the read operation.

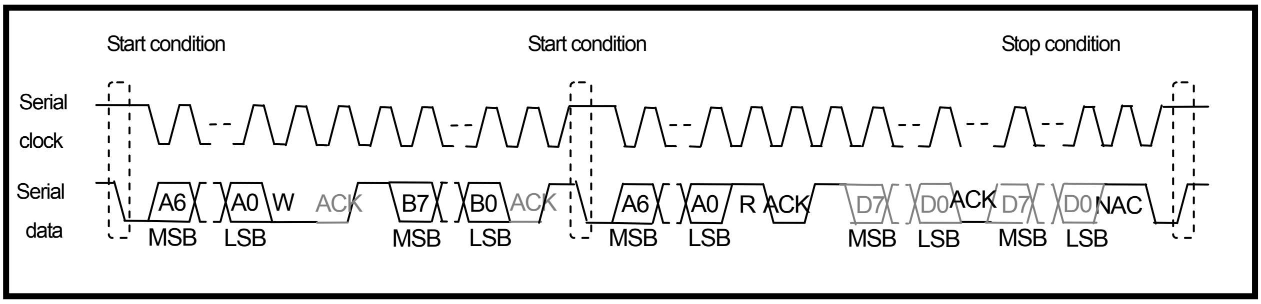


Figure 4-16 I^{2}C format (Serial memory, read)

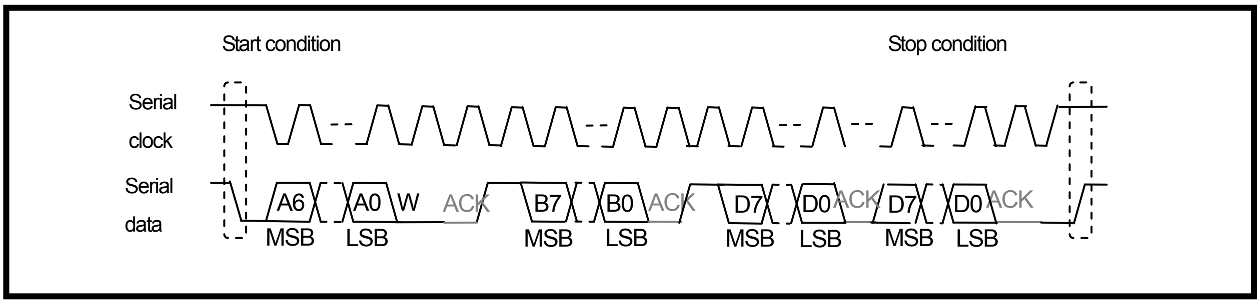


Figure 4-17 I^{2}C format (Serial memory, write)

4.6. PWM Interface

TC35678 has a PWM interface that can be used for LED, buzzer control, etc.

The PWM interface has the following features.

- Arbitrary pulse generation function
- It can select the source clock from 13 MHz and 32.768 kHz
- It has 12-bit clock division setting up to 1/4096: 8 Hz to 16.384 kHz (32.768 kHz), 3.17 kHz to 6.5 MHz (13 MHz)
- The pulse output can be masked by the regular pattern whose period is one second with 50 ms unit width (Rhythm function).
- It can generate an interrupt which is synchronized to the rhythm pattern period 1 s.
- It can switch the pulse output to Low / High active
- It can adjust the duty cycle of the pulse output.

4.6.1. Pulse Generation Function

Figure 4-18 shows a brief explanation of the pulse generation. TC35678 can adjust output pulse frequency by changing its cycle. Also it can adjust on/off ratio by changing its duty.

The cycle (frequency) can be set from 8 Hz to 16.384 kHz for 32.768 kHz clock, and from 3.17 kHz to 6.5 MHz for 13 MHz clock.

The duty can be set from 0% to 100%

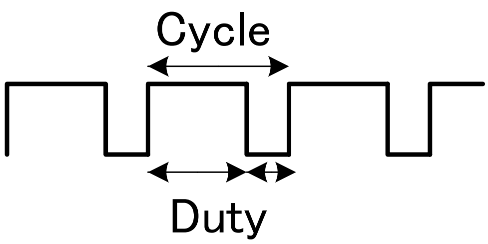


Figure 4-18 PWM pulse generation function

4.6.2. Rhythm Function (Output Masking)

Figure 4-19 shows the brief explanation of PWM rhythm function. In addition to the one for pulse generation, TC35678 has another timer that has 50 ms × 20 = 1 s (rhythm counter). That timer has 20-bit register (pattern register), each bit corresponds to the rhythm counter that counts down in every 50 ms. When the pattern register is zero, the PWM output is masked to zero or one. Using this function, LED or buzzer can be on with 1 s periodical pattern

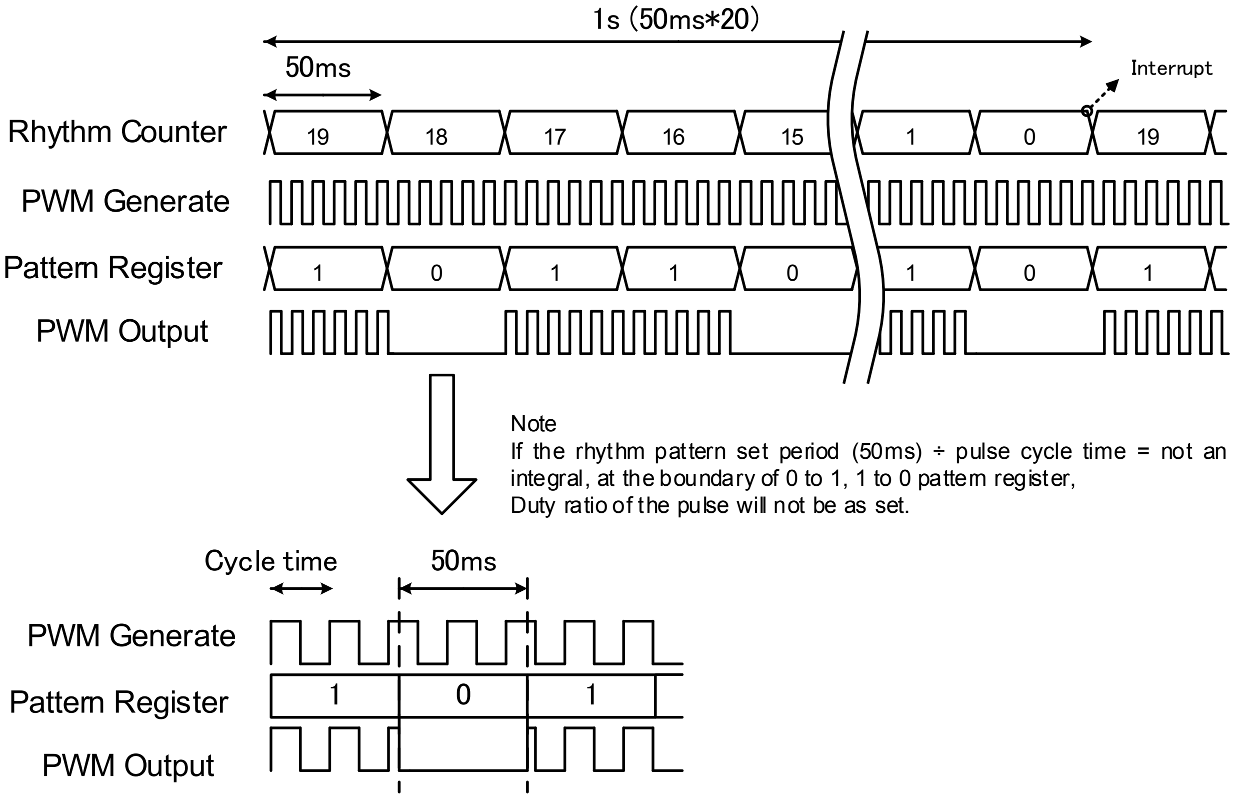


Figure 4-19 PWM Rhythm Function

4.7. ADC

4.7.1. Features

TC35678 has 8 ch of 10-bit ADCs for battery monitoring, analog inputs from external sensors, for example. The ADC has the following features. (Please note that the number of usable inputs is different for each package.)

- 7 ch for analog inputs (in case of 60 pin package) Note: Analog inputs are shared with GPIO pins.
- 1 ch for VBAT voltage monitor

  Note: The reference input is internally connected to VBAT, and the analog input is to built-in VDDCORE2 output. Please refer to 4.7.2 for how to calculate voltage value.
- Maximum conversion rate: 1 MS/s

4.7.2. Descriptions

The ADC has 10 bits conversion accuracy and can work for input voltages from 0 V to 3.6 V (VBAT). It has 8 ch of analog inputs, and the ch0 is connected to VDDCORE2 output, and the ch1 to ch7 are shared with GPIO pins.

When a battery is used as power source, the reference voltage can slide over time because the battery is connected as reference voltage. In that case, the VDDCORE2 output voltage connected to ch0 can be used as a reference voltage. The input voltage to ch1 to ch7 is converted by the reference voltage of ch0 and the converted value is used to calculate a correct digital value by the CPU. The following shows the conversion method of the input voltage.

Voltage A at time T can be calculated as follows

(1) VDDCORE2 output voltage (VDDCORE2) on Ch0 should be converted by the ADC. The converted digital value is X.

(2) The analog signal on Ch1 is converted and the converted digital value is Y.

(3) When the absolute value of the analog signal on Ch1 is defined as A (V), VDDCORE2 (V) / A (V) = X / Y. So,

A (V) = VDDCORE2 (V) × Y / X

Calculation example:

Suppose ch0 (for ex. VDDCORE2 output is 1.1 V) is converted to 0x0134, and ch1 (measurement target) is converted to 0x0188, the absolute voltage at ch1 A (V) is given by 1.1 × 0x0188 / 0x0134 = 1.1 × 392 / 308 = 1.4 (V).

Figure 4-20 shows conceptual of voltage conversion.

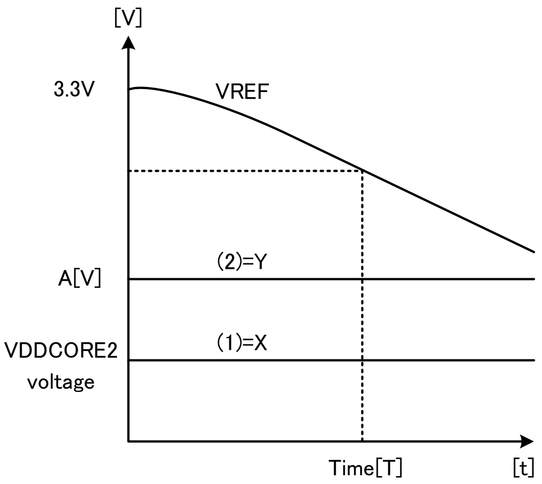


Figure 4-20 Voltage conversion concept

The ADC converts inputs from ch selected by register settings. When a conversion has finished, the CPU detects it by the interrupt or register polling, and then returns the results. The maximum sampling rate depends on software load on the CPU.

Note: The numerical values are expressed as follows.

Hexadecimal number: 0xABC

4.8. IC Reference Clock Interface

4.8.1. Features

TC35678 has the following features for IC reference clock interface.

- Clock frequency: 26 MHz (please adjust the accuracy to < 50 ppm at the temperature in use)

TC35678 doesn't require external feedback resistors and load capacitor because it has an internal feedback resistor and capacitor array. Please adjust capacitor array, based on the specification of the used oscillator and PCB layout and assembly.

4.8.2. Connection Example

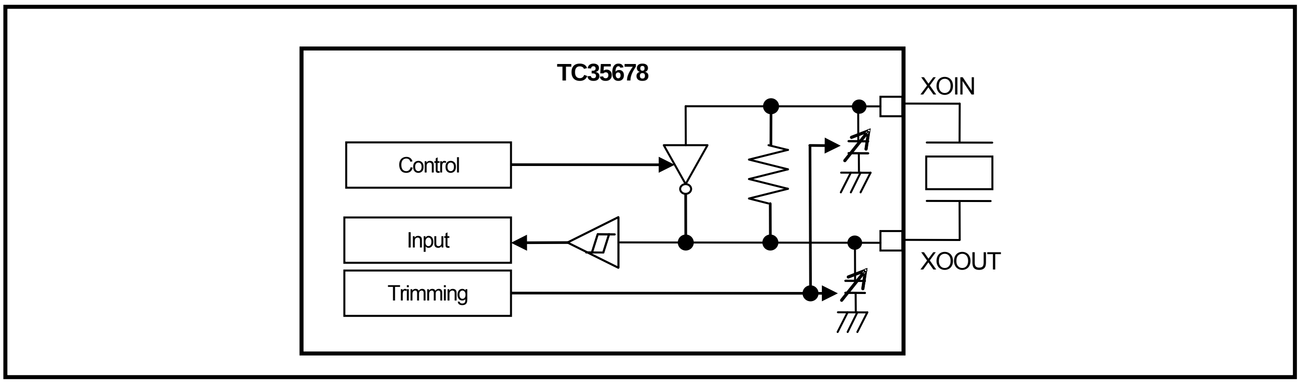


Figure 4-21 Crystal oscillator connection example

4.9. Sleep Clock Interface

TC35678 has the following features for sleep clock interface.

- Crystal oscillator can be connected.
- Clock frequency: 32.768 kHz (please adjust the frequency accuracy to less than or equal to ±500 ppm at the temperature in use.)

Crystal oscillator is connected between SLPXOIN pin and SLPXOOUT pin. TC35678 doesn't require external feedback resistors and load capacitor because it has an internal feedback resistor and capacitor array between SLPXOIN pin and SLPXOOUT pin. Please adjust capacitor array based on PCB layout and assembly if necessary within the range of the crystal's specification. When an external oscillator is connected, connect it to SLPXOIN and SLPXOOUT should be connected to the GND. When oscillator is not used and do not supply a clock from the outside, this pin needs to be connected to the GND.

4.9.1. Sleep Clock Connection Example

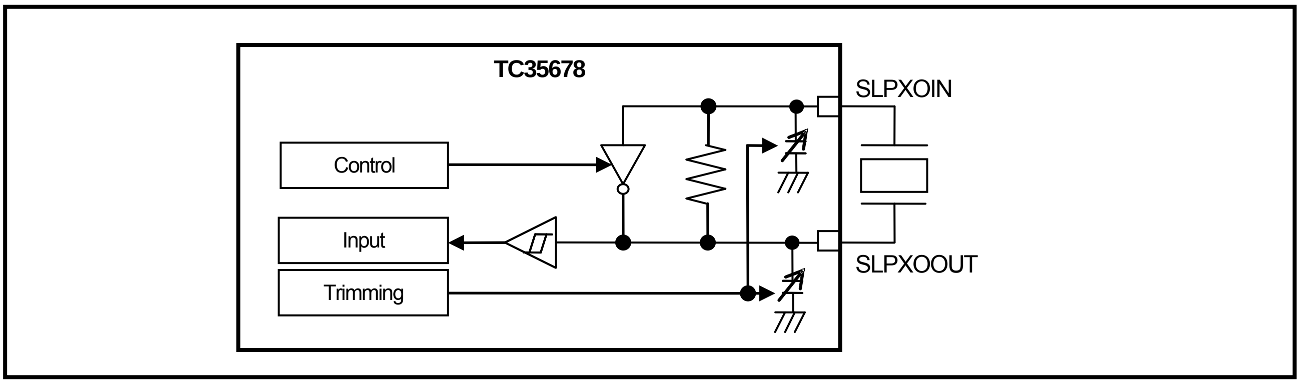


Figure 4-22 Crystal oscillator connection example

4.9.2. External Oscillator Connection Example

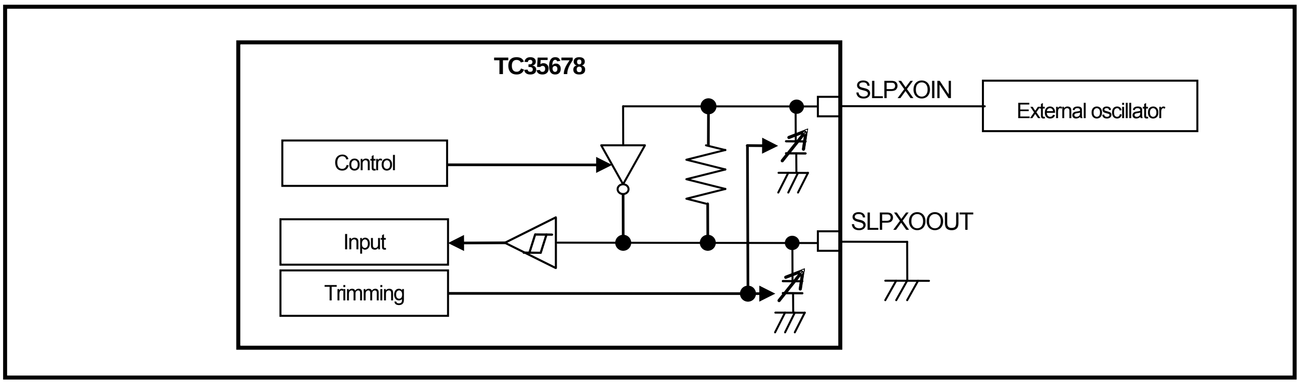


Figure 4-23 External oscillator connection example

5. Electric Characteristics

5.1. Absolute Maximum Ratings

Maximum ratings must not be exceeded even for a moment. Voltages, currents, and temperatures that exceed the maximum ratings can cause break-downs, degradations, and damages not only for ICs but also for other components and boards. Please make sure application designs not to exceed the maximum ratings in any situation.

Table 5-1 Maximum ratings (VSSA = VSSRFIO = VSSDC = VSSD = VSSX = 0 V)

Items	Symbols	Ratings		Units
		Min	Max	
Power supply	VBAT VDDIO (Note1)	-0.3	+3.9	V
Input voltage	VIN	-0.3	VDDIO + 0.3 (Note2)	V
Output voltage	VOUT	-0.3	VDDIO + 0.3 (Note2)	V
I/O pin Input current	IIN	-10	+10	mA
Input power	RFIO	—	+6	dBm
Storage temperature	Tstg	-40	+125	°C

Note1: Do not connect VBAT to GND while VDDIO is powered. Current from VDDIO to VBAT through IC may cause damages, break-downs, and degradations.

Note2: VDDIO+0.3 V should not be left more than 3.9 V.

5.2. Operating Conditions

TC35678 can operate normally with proven quality under the operating ranges. Any diversion from the operating ranges may cause false operation. Thus, please make sure application design to comply these operating ranges.

Table 5-2 Operating conditions (VSSA = VSSRFIO = VSSDC = VSSD = VSSX = 0 V)

Items		Symbols	Ratings Min	Ratings Typ.	Ratings Max	Units
	VBAT Operating Voltage1 (Note1)	VBATopr1	1.79	3.00	3.60	V
	VBAT Operating Voltage2 (Note2)	VBATopr2	1.90	3.00	3.60	V
	VDDIO Operating Voltage (Note3)	VDDIOopr	1.80	3.00	3.60	V
	VDDIOFQ Output Voltage (Note3)	VDDIOFQ	—	1.7	—	V
	VDDCORE Voltage (Note3)	VDDCORE1/ VDDCORE2	—	1.1 / 1.2 (Note4)	—	V
RF frequency		Fc	2400	—	2483.5	MHz
Clock frequencies		Reference clock Fck	25.99870	26.00000	26.00130	MHz
		Sleep clock fslclk	32.751616	32.768000	32.784384	kHz
Ambient temp.		Ta	-40	+25	+85	°C

Note1: The internal CPU powers on when the operating voltage rises to the minimum value of the VBAT operating voltage 1. However, please pay attention that the minimum voltage of the VBAT operating voltage 2 is required for the reading and writing operation of the flash ROM as indicated in the Note 2.

Note2: For reading and writing operation to the flash ROM in the digital block, the power in the range of VBAT operating voltage 3 should be supplied. In the booting process, please release RESET after the voltage rises to the minimum value (1.9 V) because of accessing to the flash ROM to confirm the existence of applications. Moreover, in case of operating in the Standalone mode or driving till the under voltage detection turns off the operation, please pay attention to the relation between R/W operation to the flash ROM and the voltage.

Note3: Please refer to other documents (application note) for our connection examples.
Please do not input external power supply and do connect external capacitors to VDDIOFQ because they are supplied by the internal LDO.

Note4: During RF block operation and 26 MHz operation of CPU, this voltage is 1.2 V (typ.).
In other operation it becomes 1.1 V (typ.).

5.3. DC electric characteristics

5.3.1. Current Consumption (Design value)

This section shows current consumption. When the operating temperature (Ta) is 25°C, and the operation of each power supply pin is in the recommendation connection state of our company, the current consumption is an average value.

Table 5-3 Current consumption (VBAT = VDDIO1 = VDDIO2 = 3.0 V, VSSA = VSSRFIO = VSSDC = VSSD = VSSX = 0 V)

Items	Symbols	Conditions	Pins (Note)	Ratings Min	Ratings Typ.	Ratings Max	Unit
Digital operation	IDD_{DIG} (Active1)	—	VBAT	—	0.7	—	mA
Flash read	IDD_{RD} (Flash Read)	—		—	2.4	—	
Flash write	IDD_{WR} (Flash Write)	—		—	15.6	—	
RX	IDD_{RX} (Active2)	—		—	3.3	—	
TX	IDD_{TX} (Active3)	Output Power= 0 dBm		—	3.3	—	
Low power mode With Connection	IDDS1 (Sleep)	26 MHz crystal oscillator disabled 32 kHz crystal oscillator enabled When 144 KB-RAM retention is performed	VBAT	—	1.8	—	μA
Low power mode Without Connection	IDDS2 (Backup)	26 MHz crystal oscillator disabled 32 kHz crystal oscillator enabled When 64 KB-RAM retention is performed		—	1.3	—	
Low power mode Without Connection	IDDS (Deep Sleep)	26 MHz crystal oscillator disabled 32 kHz crystal oscillator disabled		—	0.05	—	

Note: Power consumption for IO depends on its settings.

Table 5-4 shows DC electric characteristics for each pin under 25°C ambient temperature.

Table 5-4 DC Electric Characteristics (VBAT = VDDIO1 = VDDIO2 = 3.0 V, VSSD = VSSA = VSSRFIO = VSSDC = VSSX = 0 V)

Items	Symbols	Condition		Measuring Pin (Note 1)	Rating			Unit
		I/F Voltage	Other Condition		Min	Typ.	Max	
High Level Input Voltage	VIH	3.0 V	LVCMOS	VDDIO	0.8×VDDIO	—	—	V
Low Level Input Voltage	VIL	3.0 V	LVCMOS	VDDIO	—	—	0.2×VDDIO	V
High Level Input Current	IIH	VDDIO = Input Voltage of each pin	Pull-down Off	VDDIO	-10	—	10	μA
			Pull-down On		10	—	200	
Low Level Input Current	IIL		Pull-up Off		-10	—	10	
			Pull-up On		-200	—	-10	
High Level Output Voltage	VOH	3.0 V	IOH = 1 mA	VDDIO	VDDIO-0.6	—	—	V
Low Level Output Voltage	VOL	3.0 V	IOL = 1 mA	VDDIO	—	—	0.4	V
External 32 kHz Clock Input level (Note2)	VIH SLPCLK	3.0 V	—	SLPXOIN	0.8×VDDIO	—	—	V
	VIL SLPCLKL	3.0 V	—	SLPXOIN	—	—	0.2×VDDIO	V

Note 1: Please refer to Table 2-4 for power supply line for each pin.
Note 2: External oscillator is used for this case instead of crystal oscillator.

5.4. Built-in Regulator Characteristics

Table 5-5 Built-in regulator characteristics (VBAT = 1.9 to 3.6 V, VSSA = VSSRFIO = VSSDC = VSSD = VSSX = 0 V)

Items	Symbols	Pin names and conditions	Ratings			Units
			Min	Typ.	Max	
Output voltages	Vout1	VDDCORE1/ VDDCORE2	—	1.1 / 1.2 (Note)	—	V

Note: During RF block operation and 26 MHz operation of CPU, this voltage is 1.2 V (typ.).
In other operation it becomes 1.1 V (typ.).

Table 5-6 Built-in regulator characteristics (VBAT = 1.9 to 3.6 V, VSSA = VSSRFIO = VSSDC = VSSD = VSSX = 0 V)

Items	Symbols	Pin names and conditions	Ratings			Units
			Min	Typ.	Max	
Output voltages	Vout2	VDDIOFQ	—	1.7	—	V

5.5. ADC Characteristics

Table 5-7 ADC characteristics (VBAT = 1.9 to 3.6 V, VSSA = VSSRFIO = VSSDC = VSSD = VSSX = 0 V)

Items	Symbols	Condition	Ratings			Unit
			Min	Typ.	Max	
Analog reference voltage	VREFH	—	1.9	3.0	3.6	V
Analog input voltage	VAIN	—	VSSD	—	VREFH	V

5.6. RF Characteristics

The following conditions are applicable unless otherwise specified.

- Ta = 25°C
- VBAT = 3.0 V
- fx'tal = 26 MHz (Frequency accuracy is adjusted to ±2 ppm at normal temperature)
- PAOUT= 0 dBm

Table 5-8, Table 5-9 shows RF receiving characteristics and RF transmitting characteristics based on Bluetooth® Core Spec. V4.2 low energy.

About some the characteristics data here are design values.

Table 5-8 RF Characteristic

Test Item	Packet	bit	ch.	Condition	Spec.			Unit
					Min	Typ.	Max	
Output Power	255 octets	PRBS9	0,12, 19,39	peak	—	—	Pavg+ 3 dB	dBm
				average	—	0	—	
In-band Emissions	255 octets	PRBS9	0,12, 19,39	-5 MHz	—	-60	-30	dBm
				-4 MHz	—	-55	-30	
				-3 MHz	—	-53	-30	
				-2 MHz	—	-48	-20	
				2 MHz	—	-50	-20	
				3 MHz	—	-53	-30	
				4 MHz	—	-56	-30	
				5 MHz	—	-60	-30	
Modulation Characteristics	255 octets	11110000	0,12, 19,39	Δf1avg (11110000)	225	249.3	275	kHz
		10101010		Δf2max (99.9 %)	99.9	100	—	%
		—		Δf2avg /Δf1avg	0.8	0.90	—	Ratio
Carrier frequency offset (CFO)	255 octets	10101010	0,12, 19,39	average	—	4.4	—	kHz
				worst	-150	—	150	
Carrier frequency drift	255 octets	10101010		Absolute maximum	—	4.9	50	kHz
Carrier frequency drift Rate	255 octets	10101010		Absolute maximum	—	4.9	20	kHz/50 µs

Table 5-9 RF Characteristics

Test Item	Sub Item	Packet	bit	ch.	Condition	Min	Typ.	Max	Unit
Rx Sensitivity	—	37 octets	—	0,12, 19,3	PER=30.8 % at 1500 packets with dirty	—	-93.5	—	dBm
C/I and Receiver Selectivity Performance	PER=30.8 % at 1500 packets with dirty	255 octets	D wave: PRBS9 U wave: GFSK PRBS15	0,2,12, 19,37, 39	<=- -7 MHz	—	-38 or less	—	dB
					-6 MHz	—	-32	—	
					-5 MHz	—	-26	—	
					-4 MHz	—	-30	—	
					-3 MHz	—	-32	—	
					-2 MHz	—	-35	—	
					-1 MHz	—	-2	—	
					0 MHz	—	8	—	
					1 MHz	—	-2	—	
					2 MHz	—	-30	—	
					3 MHz	—	-38	—	
					4 MHz	—	-40	—	
					5 MHz	—	-44	—	
					=> 6 MHz	—	-38 or less	—	
Blocking Performance	—	255 octets	D wave: PRBS9 U wave: CW	12	30-2000 MHz	-30	—	—	dBm
					2003-2399 MHz	-35	—	—	
					2484-2997 MHz	-35	—	—	
					3000 M-12.75 GHz	-30	—	—	
Intermodulation Performance	1500 packets	255 octets	f1=-50 dBm with un-modulation f2=-50 dBm with PRBS15	0,12, 19,39	-4 MHz	30.8	0	—	%
					+4 MHz				
Maximum input signal level	PER	255 octets	PRBS9	0,12, 19,39	-10 dBm	30.8	0	—	%
PER Report Integrity	PER	255 octets	PRBS9	0,12, 19,39	-30 dBm	50	50	65.4	%

Note: C/I characteristic and blocking characteristic has the relief specs of the logo attestation test of Bluetooth® maybe applied. The blocking characteristic measures D wave as 12 ch.

5.7. AC Interface Characteristics (Design value)

5.7.1. UART Interface

Table 5-10 UART Interface AC characteristics

Symbols	Items	Min	Typ.	Max	Unit
tCLDTDLY	Transmit Data ON from CTSX Low level	192	—	—	ns
tCHDTDLY	Transmit Data OFF from CTSX High level	—	—	2	byte
tRLDTDLY	Received Data ON from RTSX Low level	0	—	—	ns
tRHDTDLY	Received Data OFF from RTSX High level	—	—	8	byte

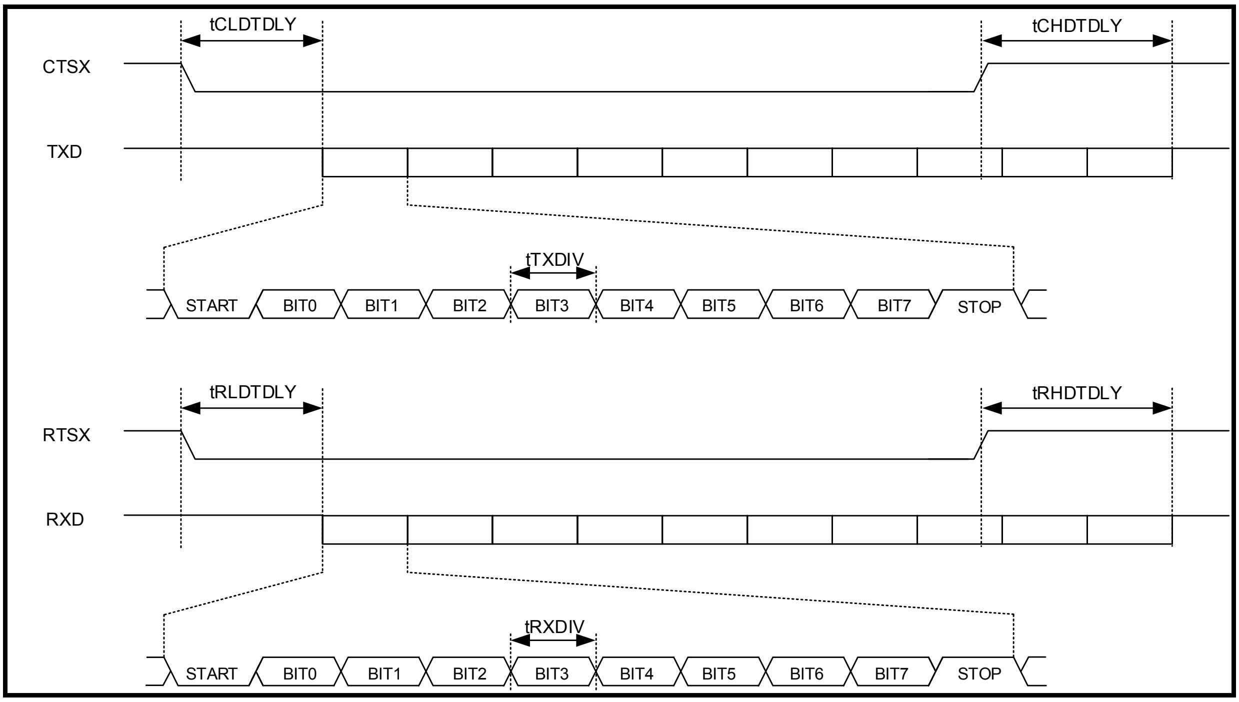


Figure 5-1 UART Interface Timing Diagram

5.7.2. I²C Interface

5.7.2.1. Normal Mode

Table 5-11 I²C Interface Normal mode AC Characteristics

Symbols	Items	Min	Typ.	Max	Unit
tDATS	Data set-up time	250	—	—	ns
tDATH	Data hold time	300	—	—	ns
tDATVD	Data validity period	—	—	3450	ns
tACKVD	ACK validity period	—	—	3450	ns
tSTAS	Restart condition set-up time	4700	—	—	ns
tSTAH	Restart condition hold time	4000	—	—	ns
tSTOS	Stop condition set-up time	4000	—	—	ns
tBUF	Bus open period from stop condition to start condition	4700	—	—	ns
tr	Rise up time	—	—	1000	ns
tf	Fall down time	—	—	300	ns
tHIGH	Serial clock period of High	4000	—	—	ns
tLOW	Serial clock period of Low	4700	—	—	ns
Cb	Bus load capacitance	—	—	400	pF

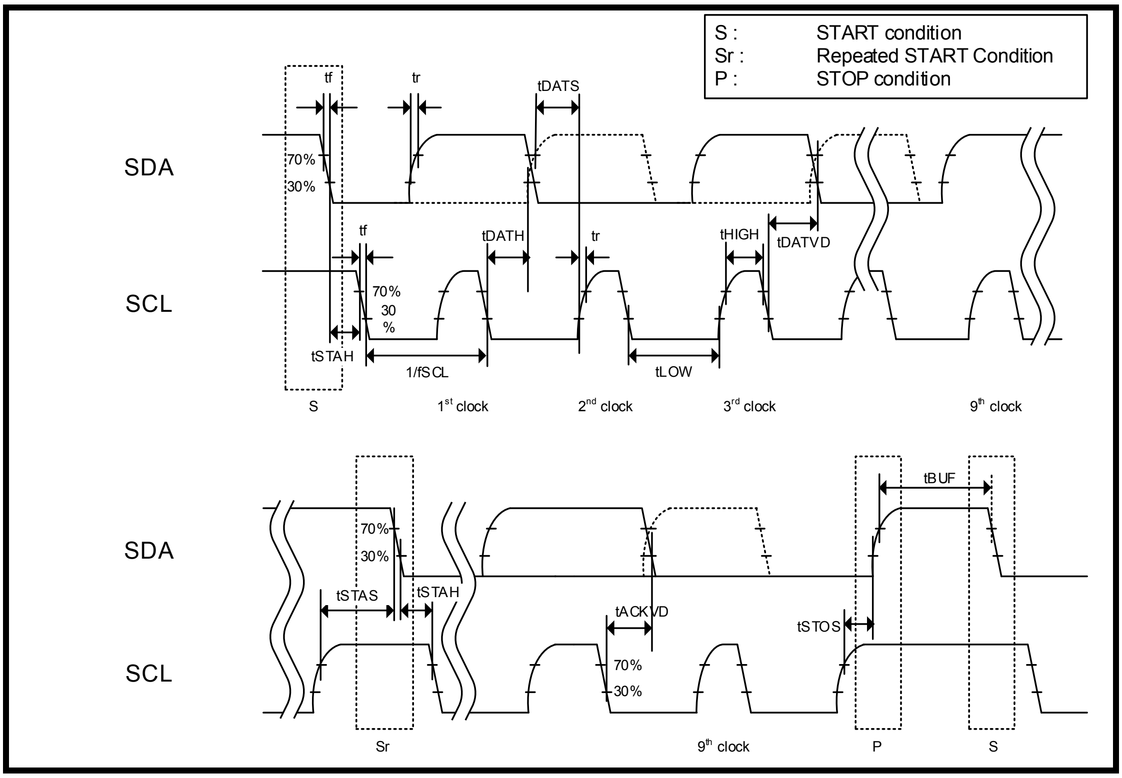


Figure 5-2 I²C Interface Normal mode Timing diagram

5.7.2.2. Fast mode

Table 5-12 I²C Interface Fast mode AC Characteristics

Symbols	Items	Min	Typ.	Max	Unit
tDATS	Data set-up time	100	—	—	ns
tDATH	Data hold time	300	—	—	ns
tDATVD	Datavalidity period	—	—	900	ns
tACKVD	ACKvalidity period	—	—	900	ns
tSTAS	Restart condition set-up time	600	—	—	ns
tSTAH	Restart condition hold time	600	—	—	ns
tSTOS	Stop condition set-up time	600	—	—	ns
tBUF	Bus open period from stop condition to start condition	1300	—	—	ns
tr	Rise up time	20 + 0.1Cb	—	300	ns
tf	Fall down time	20 + 0.1Cb	—	300	ns
tSP	Spike pulse width that can be removed	0	—	50	ns
tHIGH	Serial clock period of High	—	1423	—	ns
tLOW	Serial clock period of Low	—	1423	—	ns
Cb	Bus load capacitance	—	—	400	pF

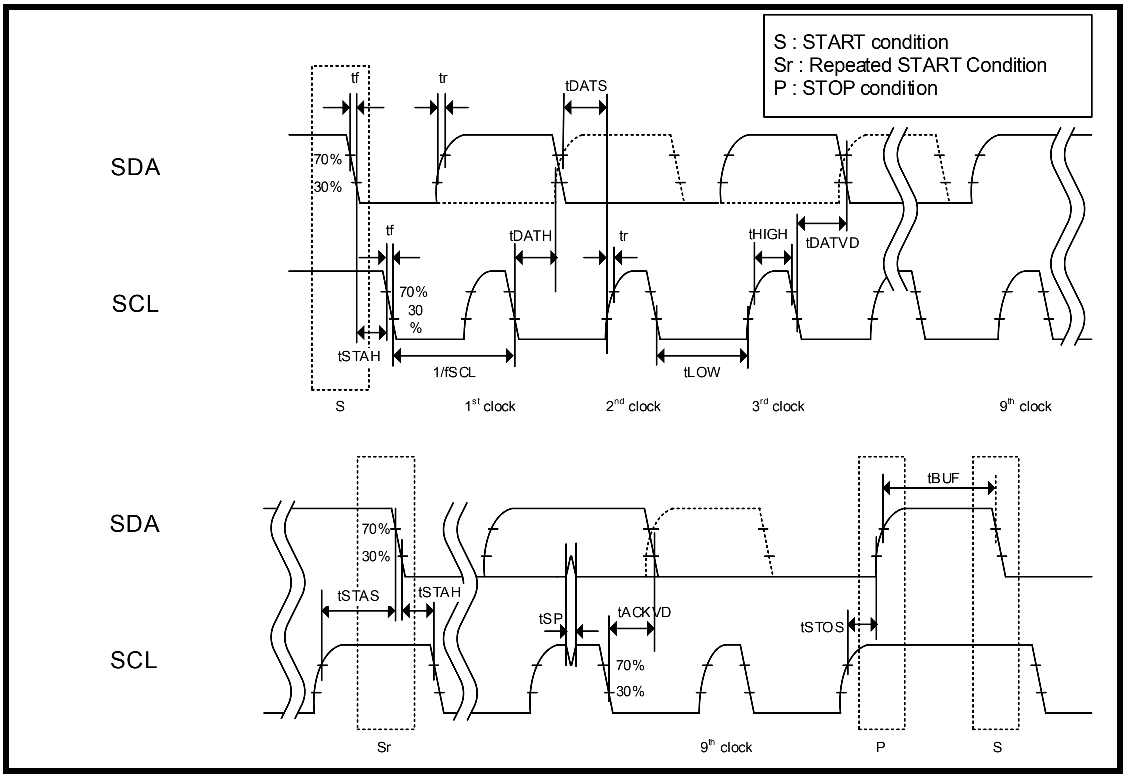


Figure 5-3 I²C Interface Fast mode Timing diagram

5.7.3. SPI Interface

Table 5-13 SPI Interface

Symbols	Items	Min	Typ.	Max	Unit
tSPICLKCYC	SPI clock cycle	154	—	—	ns
tSPICLKHPW	SPI clock high pulse width	77	—	—	ns
tSPICLKLPW	SPI clock low pulse width	77	—	—	ns
tSPICSS	SPI chip select setup time	38	—	—	ns
tSPICSH	SPI chip select hold time	77	—	—	ns
tSPIIW	SPI transfer idle pulse width	54	—	—	ns
tSPIAS	SPI address setup time	38	—	—	ns
tSPIAH	SPI address hold time	77	—	—	ns
tSPIDS	SPI data setup time	38	—	—	ns
tSPIDH	SPI data hold time	77	—	—	ns

Note: SPI Interface operates on the basis of 1/n frequency of half the frequency of ARM® Cortex®-M0 core clock (6.5 MHz for 13 MHz core clock)

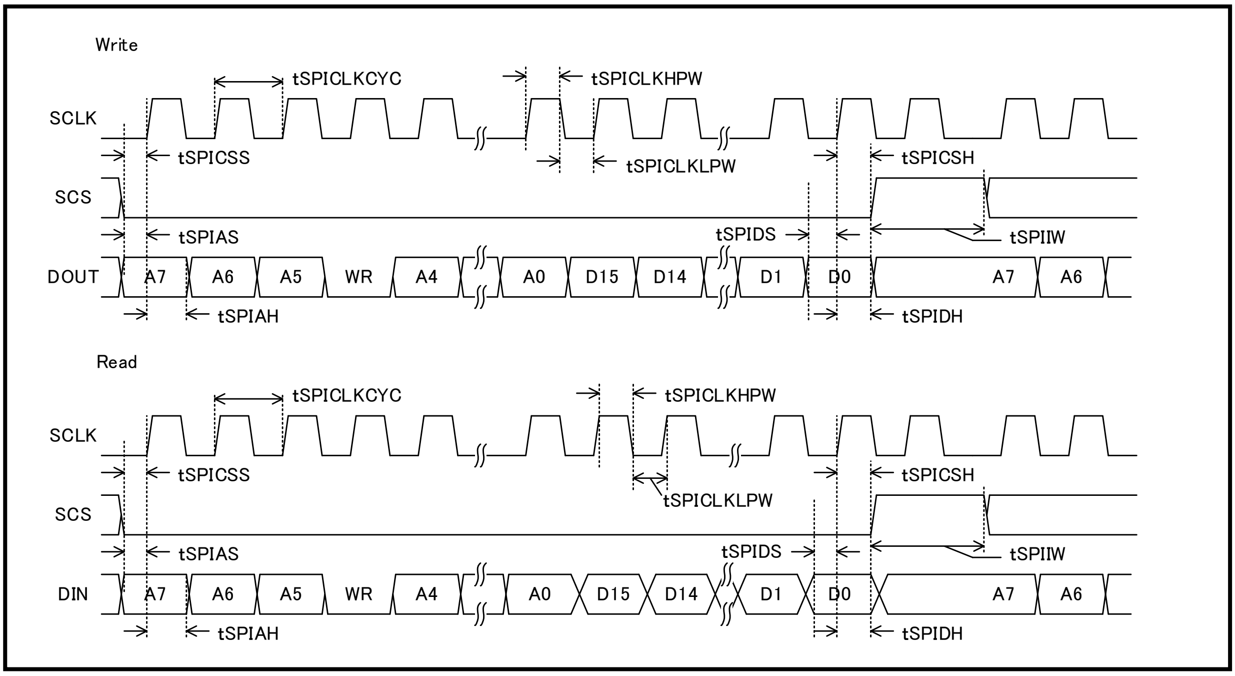


Figure 5-4 SPI Interface timing diagram

5.8. Characteristics of Flash-ROM block

Table 5-14 Characteristics of Flash-ROM block (VBAT=1.9 to 3.6 V, VSSA = VSSRFIO = VSSDC = VSSD = VSSX = 0 V)

Item	Symbol	Condition	Ratings			Unit
			Min	Typ.	Max	
Number of times of erase and program	—	Ta=25°C	10^5	—	—	times

6. System Configuration Example

An example of system configuration is shown in the following figures.

6.1. In case of Host CPU connection

- Host interface=UART and 26 MHz Reference Clock= XOSC Connection.
- XOSC (32.768 kHz) of the dotted line enclosure is unnecessary when the external input (HOST common use) is chosen.
- GPIO and SWD of connection is the connection example of when not in use.

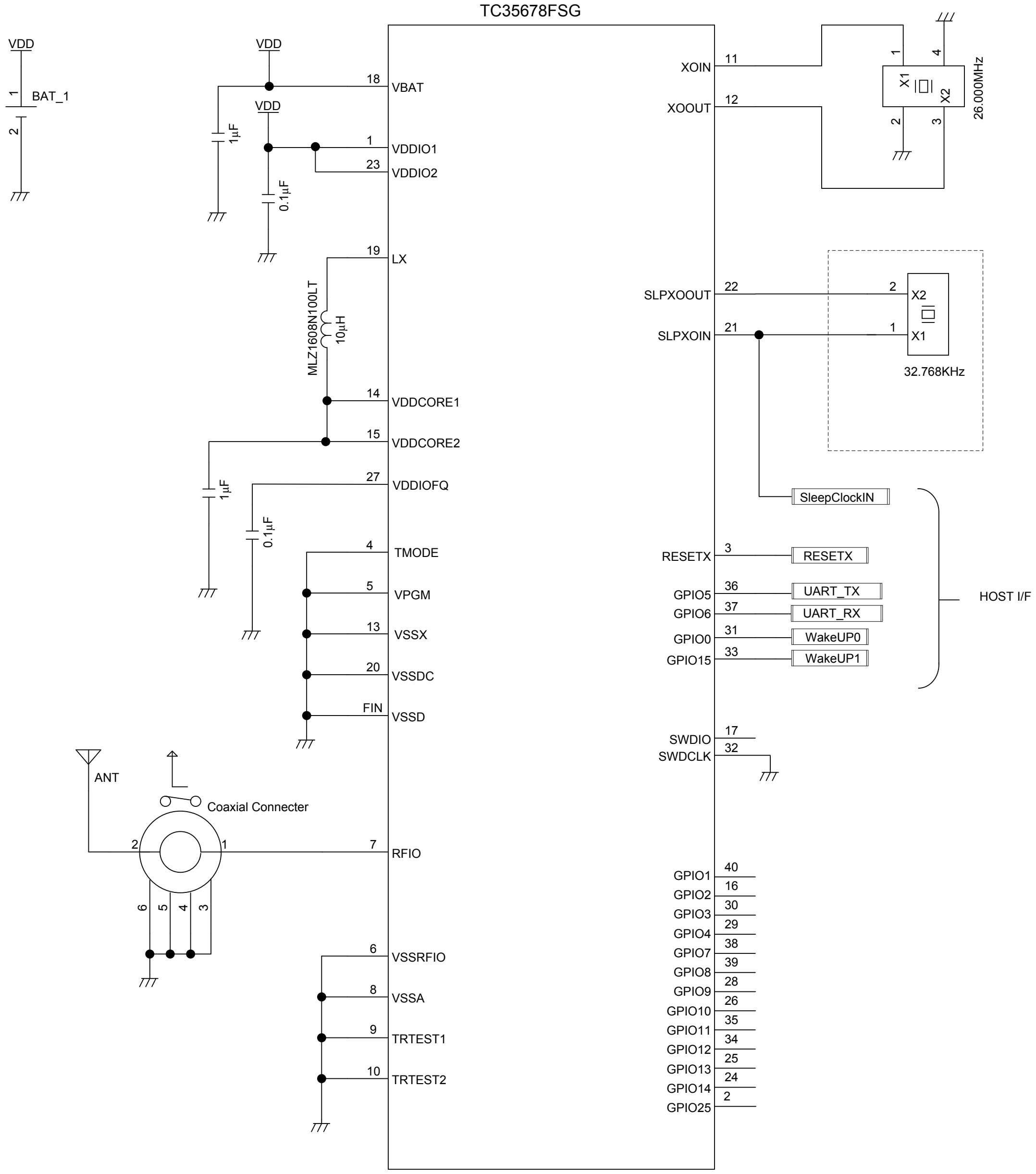


Figure 6-1 Example of TC35678FSG system configuration (HOST CPU connection)

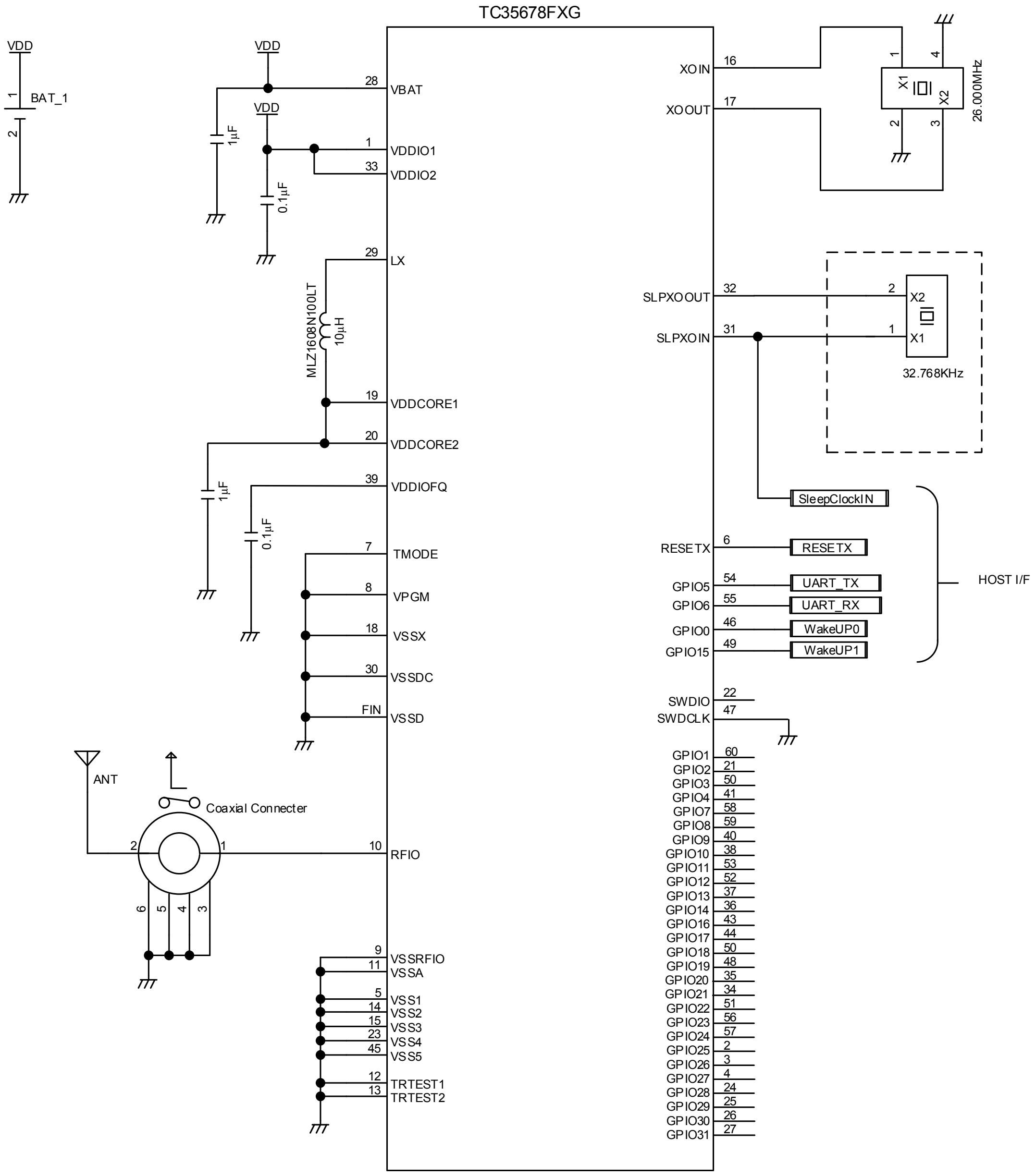


Figure 6-2 Example of TC35678FXG system configuration (HOST CPU connection)

6.2. In case of Standalone

- XOSC (32.768 kHz) of the dotted line enclosure is unnecessary when the external input (HOST common use) is chosen.
- GPIO and SWD of connection is the connection example of when not in use.

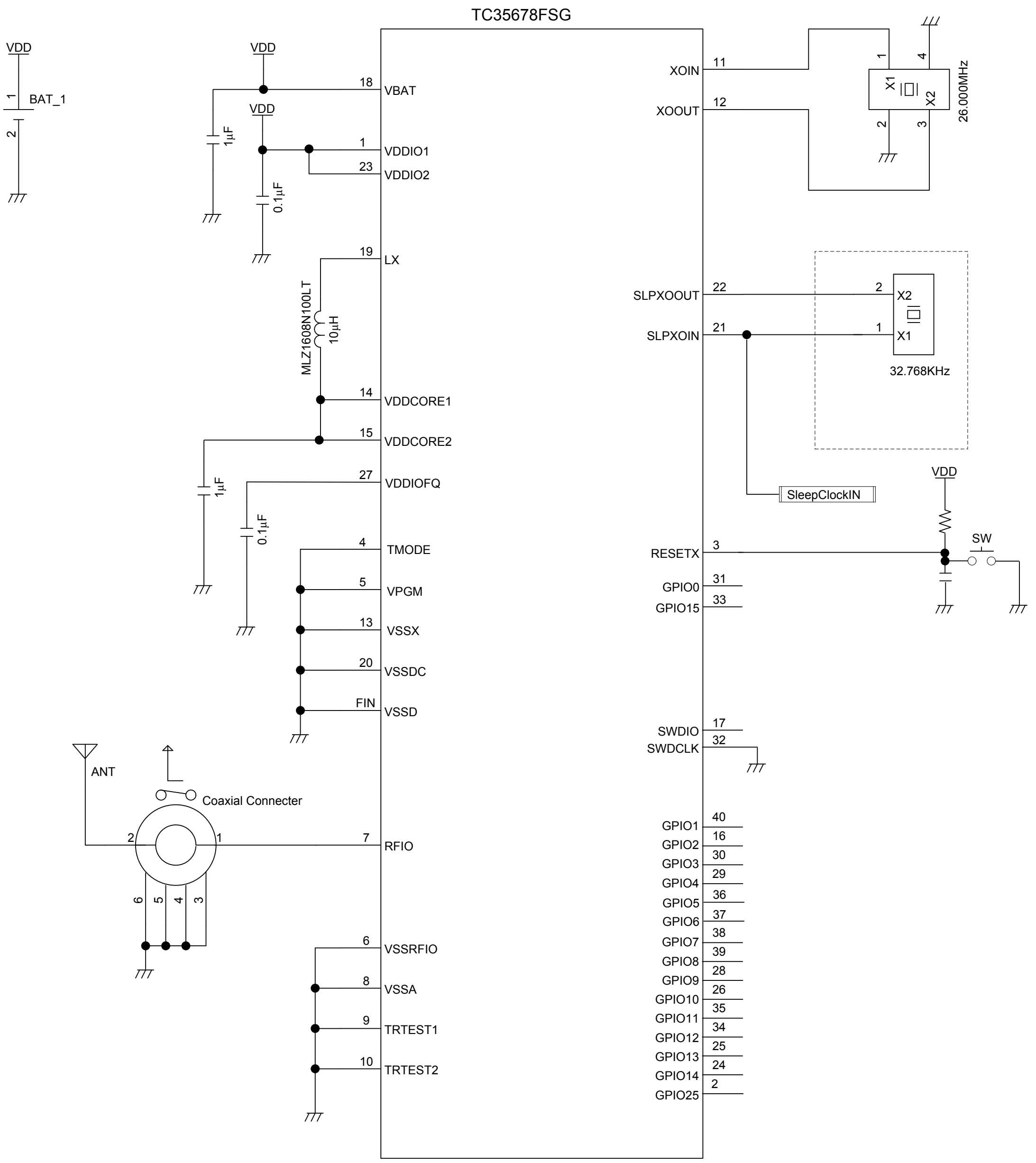


Figure 6-3 Example of TC35678FSG system configuration (Stand-alone)

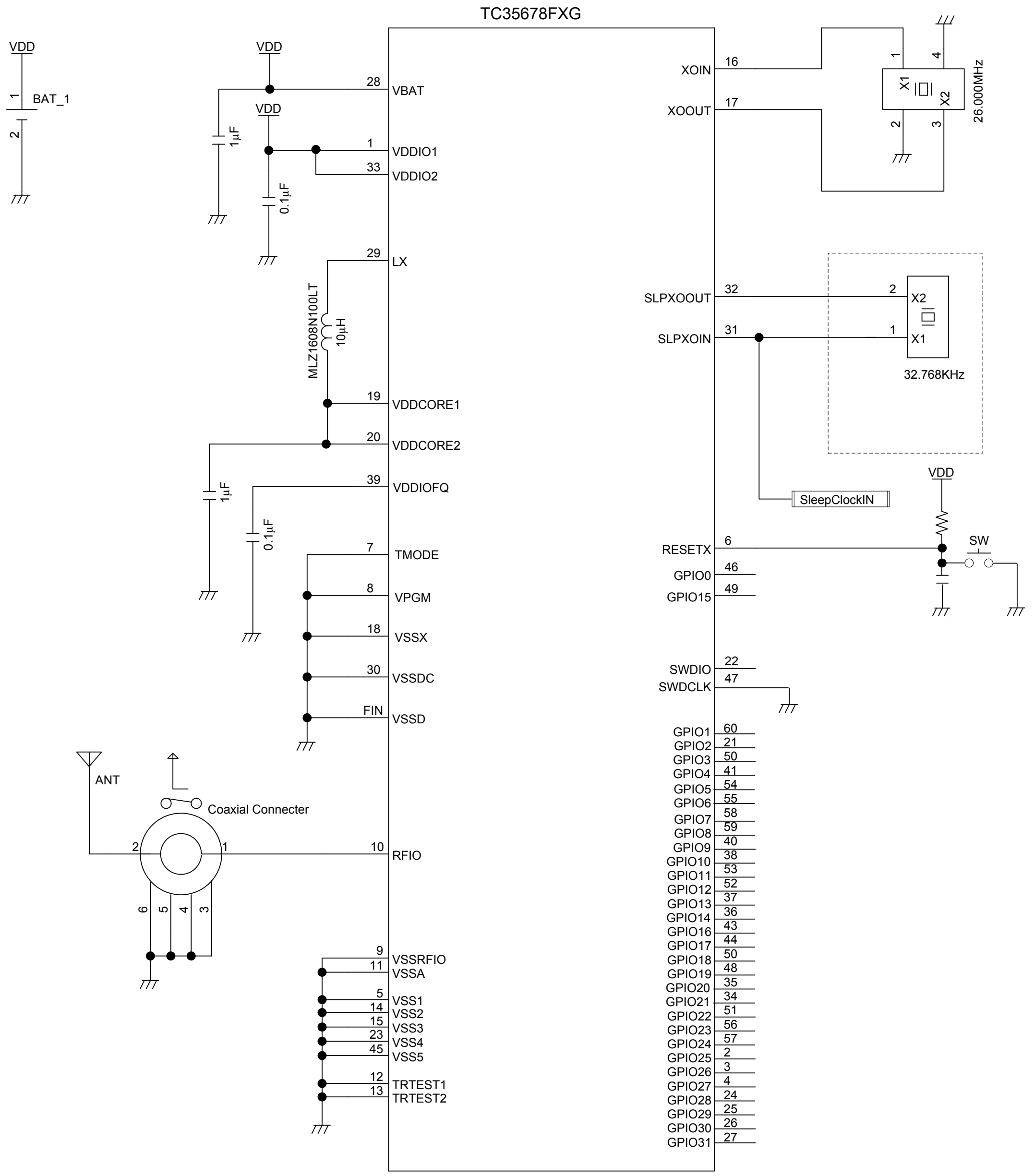
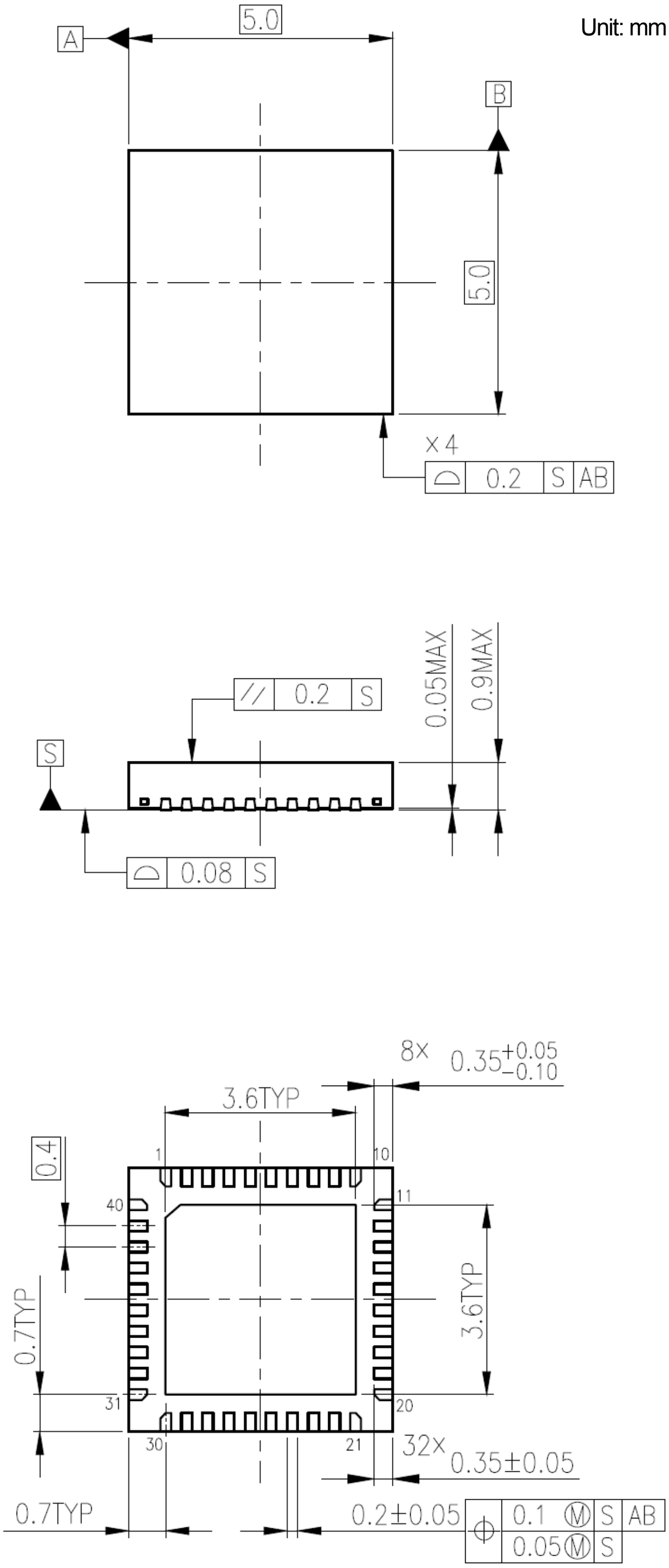


Figure 6-4 Example of TC35678FXG system configuration (Stand-alone)

7. Package outline

7.1. Outline dimensional drawing TC35678FSG-002(ELA (P-VQFN40-0505-0.40-005/F01)

Unit: mm

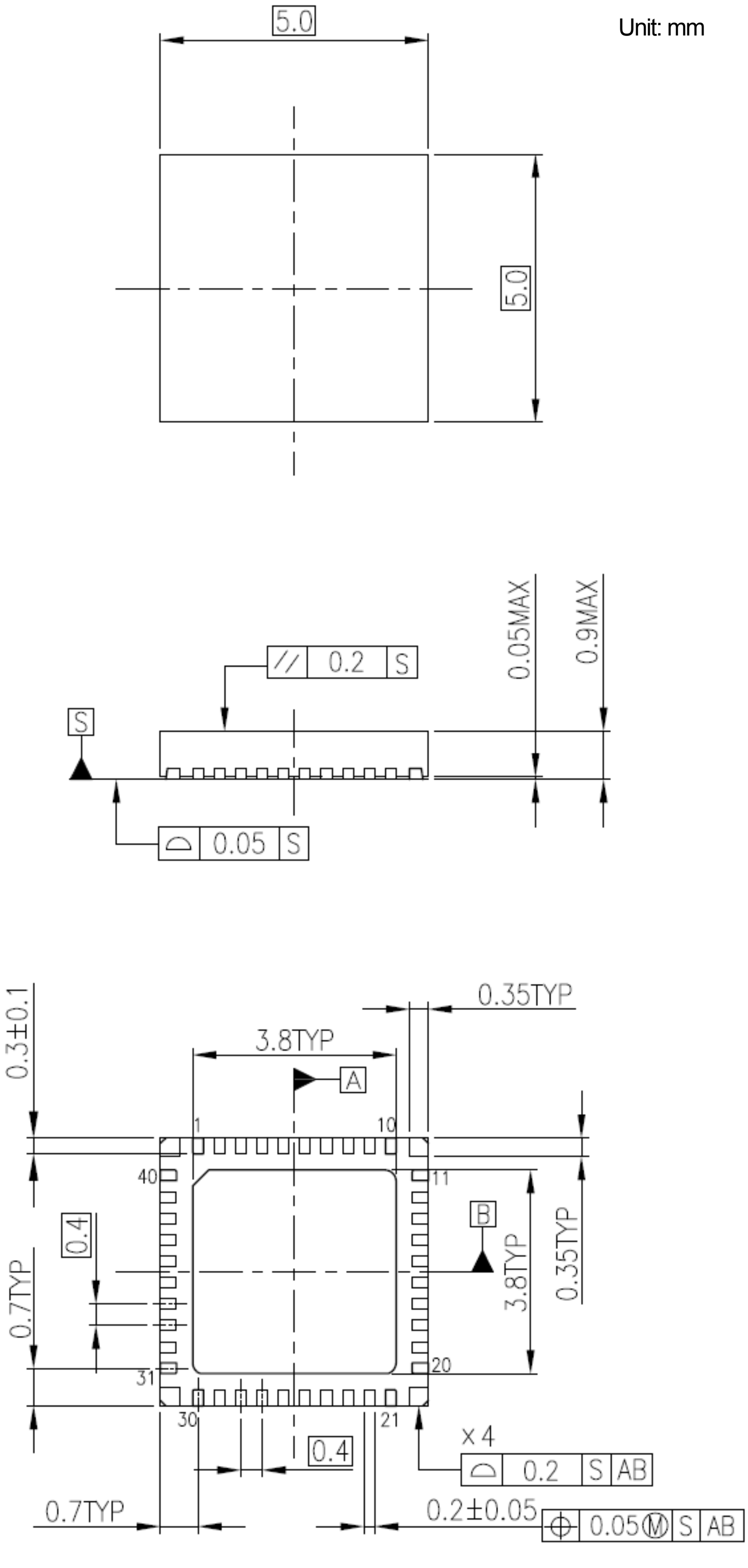


Weight: 0.068 g (Typ.)

Figure 7-1 Package outline (P-VQFN40-0505-0.40-005/F01)

7.2. Outline dimensional drawing TC35678FSG-002(EL) (P-VQFN40-0505-0.40-002)

Unit: mm

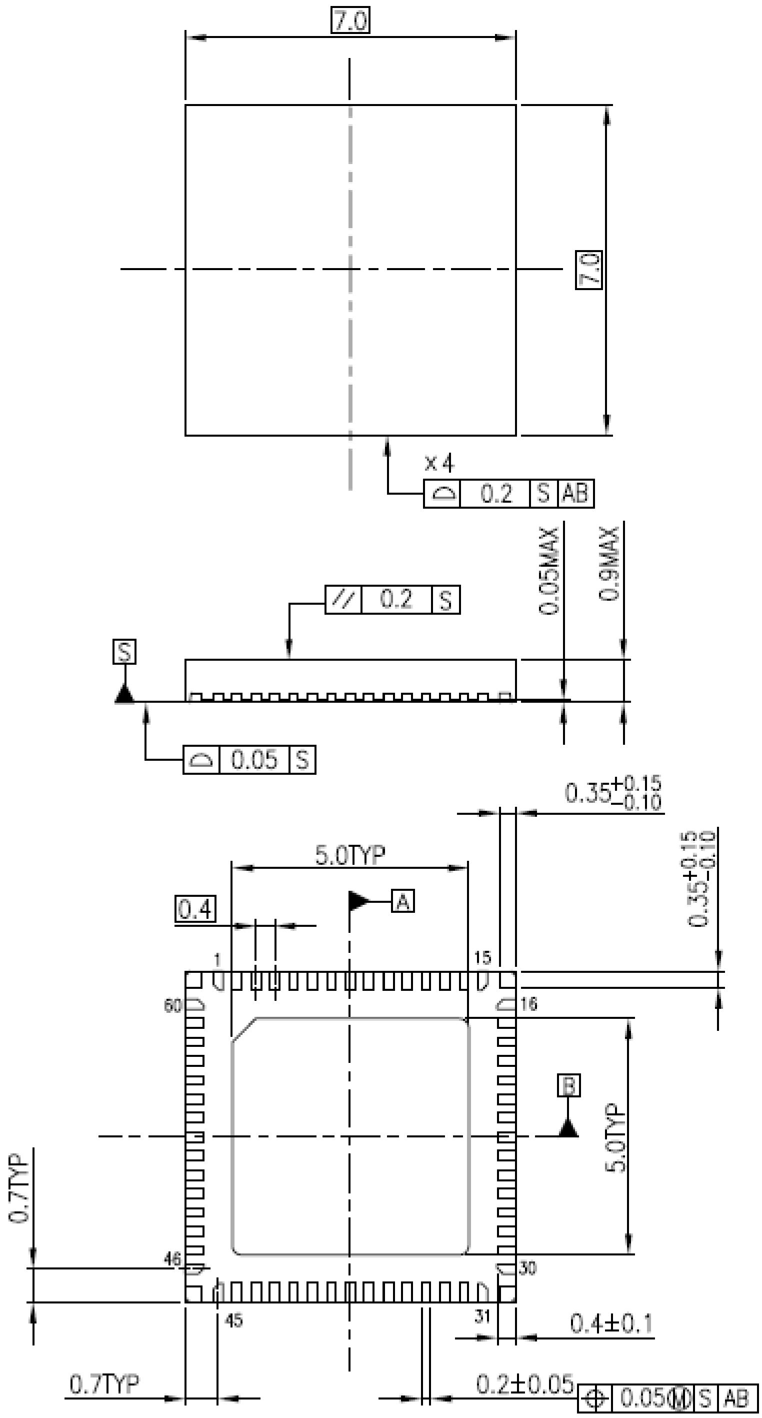


Weight: 0.068 g (Typ.)

Figure 7-2 Package outline (P-VQFN40-0505-0.40-002)

7.3. Outline dimensional drawing TC35678FXG-002(EL) (P-VQFN60-0707-0.40-001)

Unit: mm



Weight: 0.128 g (Typ.)

Figure 7-3 Package outline (P-VQFN60-0707-0.40-001)

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