

## Description

The 74AHCT164 is a serial input 8-bit edge-triggered shift register that has outputs from each of eight stages. The device features TTL compatible inputs.

### SERIAL DATA INPUT PINS

The serial input data is entered at pin SDA or pin SDB as these are logically ANDED. Either input could be used as an active HIGH enable with data entry on the other pin. If a single input is desired, the pins can be tied together or the unused input can be tied HIGH.

### DATA ENTRY

Data is shifted into Q0 from the serial input pins on each LOW to HIGH transition of the CP pin. Also during the CP edge the data is transferred from each Qn to Qn+1. The serial data on pins DSA and DSB must be stable before and after the CP rising edge to meet the set-up and hold timing requirements.

### RESET

When asserted LOW the Master Reset ( $\overline{MR}$ ) pin sets all Qn to LOW. This action does not depend on the condition of serial input or clock pins. The  $\overline{MR}$  must be asserted HIGH for a recovery time before the next CP positive edge pulse.

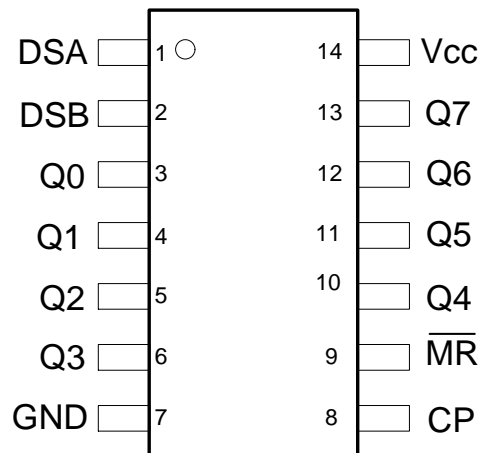
## Features

- Supply Voltage Range from 4.5V to 5.5V
- Sinks or Sources 8mA at V<sub>CC</sub> = 4.5V
- TTL Compatible Inputs
- CMOS Low Power Consumption
- Schmitt Trigger Action at All Inputs
- ESD Protection Exceeds JESD 22
  - 200-V Machine Model (A115)
  - 2000-V Human Body Model (A114)
  - 1000-V Charged Device Model (C101)
- Range of Package Options SO-14 and TSSOP-14
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
  2. See [http://www.diodes.com/quality/lead\\_free.html](http://www.diodes.com/quality/lead_free.html) for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

## Pin Assignments

### ( Top View )



### SO-14 / TSSOP-14 / PDIP-14\*

\*PDIP-14 is a Future Product

## Applications

- General Purpose Logic
- Wide Array of Products Such as:
  - PCs, Networking, Notebooks, Netbooks
  - Computer Peripherals, Hard Drives, CD/DVD ROM
  - TV, DVD, DVR, Set-Top Box

Device ordering information is on page 7

## Pin Descriptions

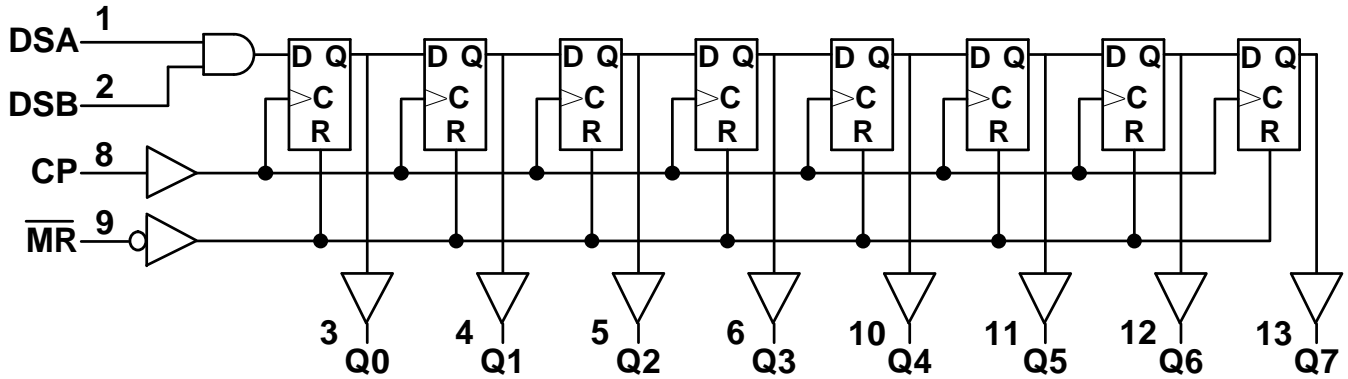
Pin Number	Pin Name	Function
1	DSA	Serial Data Input
2	DSB	Serial Data Input
3	Q0	Data Output
4	Q1	Data Output
5	Q2	Data Output
6	Q3	Data Output
7	GND	Ground
8	CP	Clock Pulse –Positive Edge Triggered
9	$\overline{\text{MR}}$	Master Reset - Asynchronous
10	Q4	Data Output
11	Q5	Data Output
12	Q6	Data Output
13	Q7	Data Output
14	V <sub>CC</sub>	Supply Voltage

## Function Table

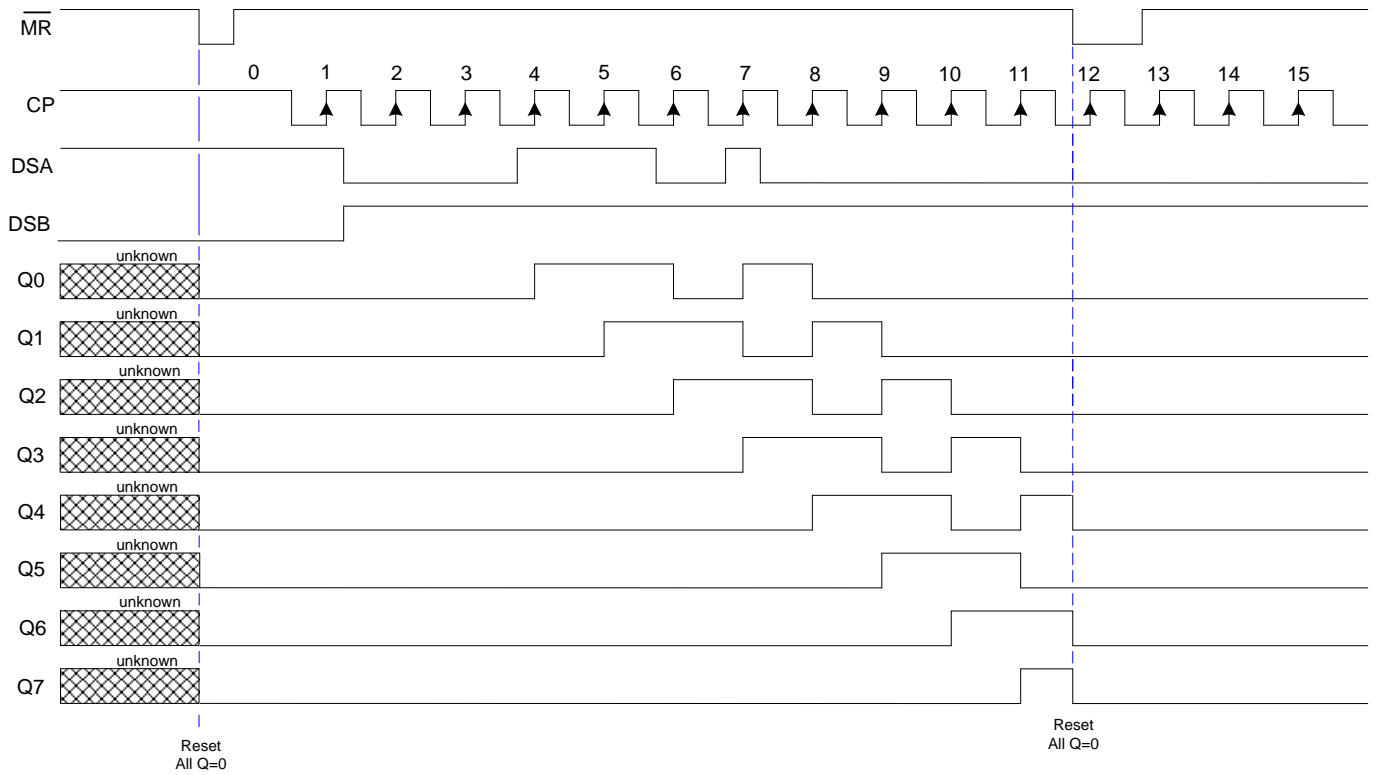
Mode	Input				Output	
	$\overline{\text{MR}}$	CP	DSA	DSB	Q0	Q1-Q7
Reset	L	X	X	X	L	L
Shift	H	↑	L	X	L	Q <sub>n</sub> ←Q <sub>n-1</sub> (n= 1 to7)
	H	↑	X	L	L	Q <sub>n</sub> ←Q <sub>n-1</sub> (n= 1 to7)
	H	↑	H	H	H	Q <sub>n</sub> ←Q <sub>n-1</sub> (n= 1 to7)

Note: 4. Signals asserted on DSA and DSB must be in place longer than T<sub>su</sub> (set up time) before CP occurs and remain in place T<sub>hold</sub> (hold time) after CP.

**Logic Diagram**



**Timing Diagram**



- Notes:
5. All Q values are reset to LOW when  $\overline{MR}$  goes low.  $\overline{MR}$  is asynchronous and overrides all other signals.
  6. Serial data supplied at DSA and DSB is ANDED and transferred to Q0 on positive edge of CP.

NEW PRODUCT

**Absolute Maximum Ratings** (Note 7) ( $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Symbol	Description	Rating	Unit
ESD HBM	Human Body Model ESD Protection	2	kV
ESD CDM	Charged Device Model ESD Protection	1	kV
ESD MM	Machine Model ESD Protection	200	V
$V_{CC}$	Supply Voltage Range	-0.5 to +7.0	V
$V_I$	Input Voltage Range (Note 8)	-0.5 to +7.0	V
$I_{IK}$	Input Clamp Current $V_I < -0.5\text{V}$	-20	mA
$I_{OK}$	Output Clamp Current $V_O < -0.5\text{V}$ or $V_O > V_{CC} + 0.5\text{V}$	$\pm 20$	mA
$I_O$	Continuous Output Current $-0.5\text{V} < V_O < V_{CC} + 0.5\text{V}$	$\pm 25$	mA
$I_{CC}$	Continuous Current Through $V_{CC}$	75	mA
$I_{GND}$	Continuous Current Through GND	-75	mA
$T_J$	Operating Junction Temperature	-40 to +150	$^\circ\text{C}$
$T_{STG}$	Storage Temperature	-65 to +150	$^\circ\text{C}$
$P_{TOT}$	Total Power Dissipation	500	mW

- Notes: 7. Stresses beyond the absolute maximum may result in immediate failure or reduced reliability. These are stress values and device operation should be within recommend values.  
 8. Input Voltage cannot exceed  $V_{CC}$  to the extent the Maximum clamp current is exceeded.

**Recommended Operating Conditions** (Note 9) ( $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	Supply Voltage	-	4.5	5.5	V
$V_I$	Input Voltage	-	0	5.5	V
$V_O$	Output Voltage	-	0	$V_{CC}$	V
$\Delta t/\Delta V$	Input transition rise or fall rate	$V_{CC} = 4.5\text{V}$ to $5.5\text{V}$	-	20	ns/V
$T_A$	Operating Free-Air Temperature	-	-40	+125	$^\circ\text{C}$

- Note: 9. Unused inputs should be held at  $V_{CC}$  or Ground.

**Electrical Characteristics** ( $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Symbol	Parameter	Test Conditions	$V_{CC}$	$T_A = +25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
$V_{IH}$	High-Level Input Voltage	-	4.5V to 5.5V	2.0	-	-	2.0	-	2.0	-	V
$V_{IL}$	Low-Level Input Voltage	-	4.5V to 5.5V	-	-	0.8	-	0.8	-	0.8	V
$V_{OH}$	High-Level Output Voltage	$I_{OH} = -50\mu\text{A}$	4.5V	4.4	4.5	-	4.4	-	4.4	-	V
		$I_{OH} = -8\text{mA}$	4.5V	3.94	-	3.80	-	3.70	-	-	V
$V_{OL}$	Low-Level Output Voltage	$I_{OL} = 50\mu\text{A}$	4.5V	-	0	0.1	-	0.1	-	0.1	V
		$I_{OL} = 8\text{mA}$	4.5V	-	-	0.36	-	0.44	-	0.55	V
$I_I$	Input Current	$V_I = \text{GND}$ or $5.5\text{V}$	0V or 5.5V	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 2$	$\mu\text{A}$
$I_{CC}$	Supply Current	$V_I = \text{GND}$ or $V_{CC}$ , $I_O = 0\text{A}$	5.5V	-	-	4.0	-	40	-	80	$\mu\text{A}$
$\Delta I_{CC}$	Additional Supply Current	$V_I = V_{CC} - 2.1\text{V}$ $I_O = 0$ Other inputs at $V_{CC}$ or GND	4.5V to 5.5V	-	-	1.35	-	1.5	-	1.5	mA

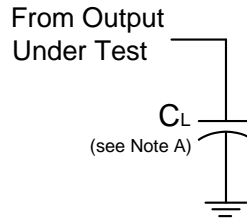
**Switching Characteristics**

Symbol / Parameter	Pins	Test Conditions Figure 1	V <sub>CC</sub>	T <sub>A</sub> = +25°C			-40°C to +85°C		-40°C to +125°C		Unit
				Min	Typ.	Max	Min	Max	Min	Max	
f <sub>MAX</sub> Maximum	CP	C <sub>L</sub> = 15pF	4.5V to 5.0V	125	175	-	105	-	85	-	MHz
		C <sub>L</sub> = 50pF	4.5V to 5.0V	85	115	-	75	-	65	-	
t <sub>w</sub> Pulse Width	CP HIGH or LOW	-	4.5V to 5.0V	5.0	-	-	5.0	-	5.0	-	ns
	$\overline{\text{MR}}$ LOW	-	4.5V to 5.0V	5.0	-	-	5.0	-	5.0	-	ns
t <sub>SU</sub> Set-up Time	DSA or DSB to CP	-	4.5V to 5.0V	4.5	-	-	4.5	-	4.5	-	ns
t <sub>H</sub> Hold Time	DSA or DSB to CP	-	4.5V to 5.0V	2.0	-	-	2.0	-	2.0	-	ns
t <sub>PD</sub> Propagation	CP to Qn	C <sub>L</sub> = 15pF	4.5V to 5.0V	-	3.4	9.0	1.0	10.5	1.0	11.5	ns
		C <sub>L</sub> = 50pF	4.5V to 5.0V	-	4.9	11.0	1.0	12.5	1.0	14.0	
t <sub>rec</sub> Recovery Time	$\overline{\text{MR}}$ to CP	-	4.5V to 5.0V	2.5	-	-	2.5	-	-	2.5	ns
t <sub>PHL</sub> HIGH to LOW	$\overline{\text{MR}}$ to Qn	C <sub>L</sub> = 15pF	4.5V to 5.0V	-	3.5	8.6	1.0	10.0	1.0	11.0	ns
		C <sub>L</sub> = 50pF	4.5V to 5.0V	-	5.0	10.6	1.0	12.0	1.0	13.5	

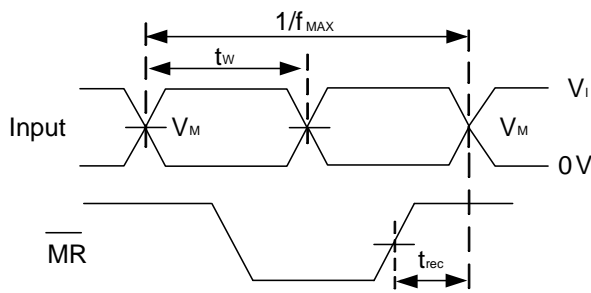
**Operating Characteristics** (T<sub>A</sub> = +25°C, unless otherwise specified.)

Parameter		Test Conditions	V <sub>CC</sub> = 5.5V		Unit
			Typ	Maximum	
C <sub>pd</sub>	Power Dissipation Capacitance per Gate	f = 1 MHz	51	-	pF
C <sub>i</sub>	Input Capacitance	V <sub>I</sub> = V <sub>CC</sub> – or GND	3.5	10	pF

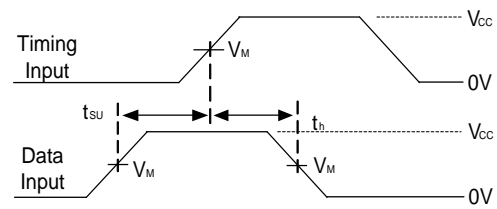
**Parameter Measurement Information**



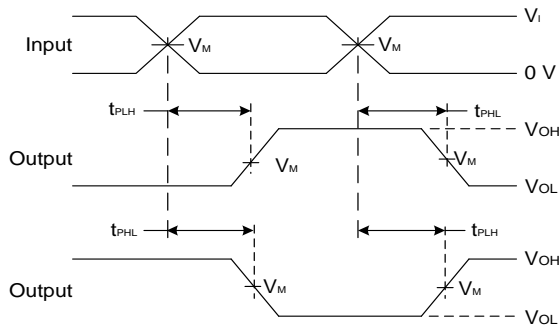
$V_{CC}$	Inputs		$V_M$		$C_L$
	$V_I$	$t_r/t_f$	Input	Output	
4.5V-5.5V	3.0V	$\leq 3\text{ns}$	1.5V	$V_{CC}/2$	15pF, 50pF



**Voltage Waveform  
Pulse Duration and Recovery Time**



**Voltage Waveform  
Set-up and Hold Times**

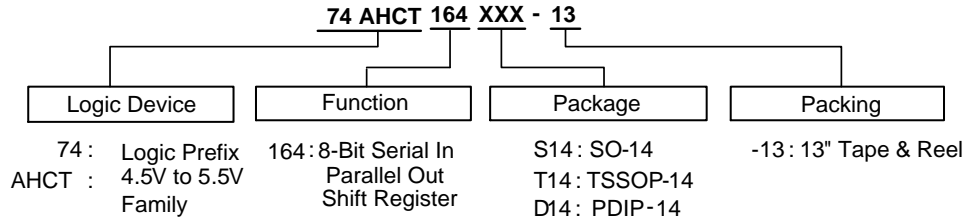


**Voltage Waveform  
Propagation Delay Times  
Inverting and Non Inverting Outputs**

- Notes:
- A. Includes test lead and test apparatus capacitance.
  - B. All pulses are supplied at pulse repetition rate  $\leq 10$  MHz
  - C. Inputs are measured separately one transition per measurement
  - D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{PD}$

**Figure 1 Load Circuit and Voltage Waveforms**

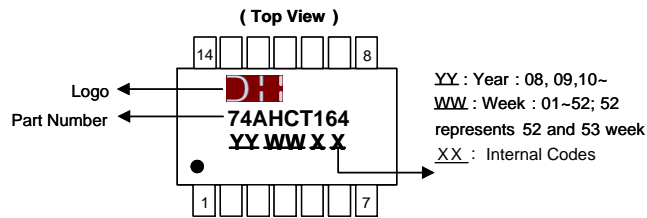
**Ordering Information**



Device	Package Code	Packaging	Packing	
			Quantity	Part Number Suffix
74AHCT164S14-13	S14	SO-14	2500/Tape & Reel	-13
74AHCT164T14-13	T14	TSSOP-14	2500/Tape & Reel	-13
74AHCT164D14 <b>Future Product</b>	D14	PDIP-14	Tube	-

**Marking Information**

(1) SO-14, TSSOP-14, PDIP-14

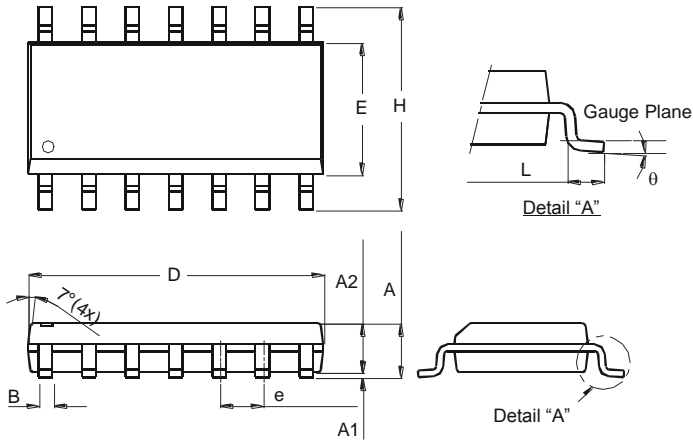


Part Number	Package
74AHCT164S14-13	SO-14
74AHCT164T14-13	TSSOP-14
74AHCT164D14	PDIP-14

**Package Outline Dimensions** (All dimensions in mm.)

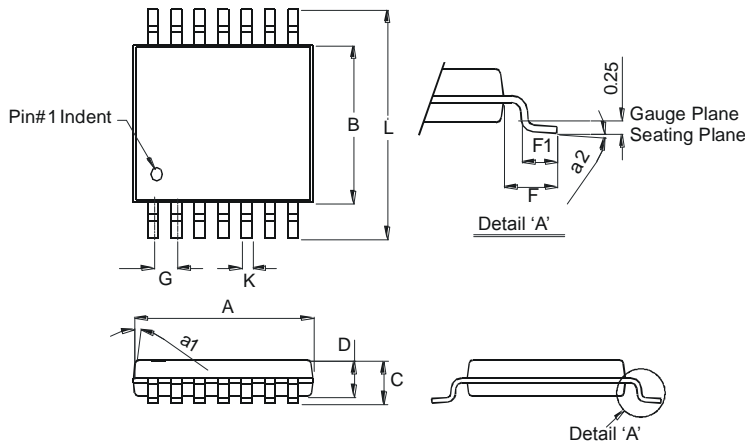
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.

**Package Type: SO-14**



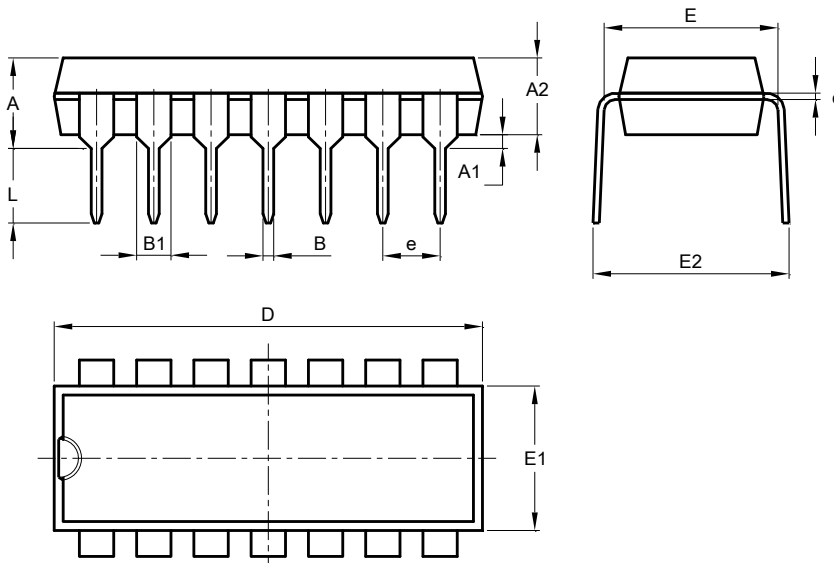
SO-14		
Dim	Min	Max
A	1.47	1.73
A1	0.10	0.25
A2	1.45 Typ	
B	0.33	0.51
D	8.53	8.74
E	3.80	3.99
e	1.27 Typ	
H	5.80	6.20
L	0.38	1.27
θ	0°	8°
All Dimensions in mm		

**Package Type: TSSOP-14**



TSSOP-14		
Dim	Min	Max
a1	7° (4X)	
a2	0°	8°
A	4.9	5.10
B	4.30	4.50
C	—	1.2
D	0.8	1.05
F	1.00 Typ	
F1	0.45	0.75
G	0.65 Typ	
K	0.19	0.30
L	6.40 Typ	
All Dimensions in mm		

**Package Type: PDIP-14**



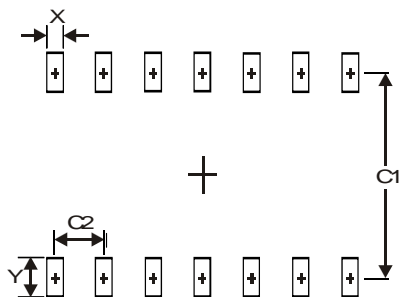
PDIP-14		
Dim	Min	Max
A	3.710	4.310
A1	0.510	-
A2	3.200	3.600
B	0.380	0.570
B1	1.524 (BSC)	
c	0.204	0.360
D	18.800	19.200
E	6.200	6.600
E1	7.320	7.920
E2	8.400	9.000
e	2.540 (BSC)	
L	3.000	3.600
All Dimensions in mm		



## Suggested Pad Layout

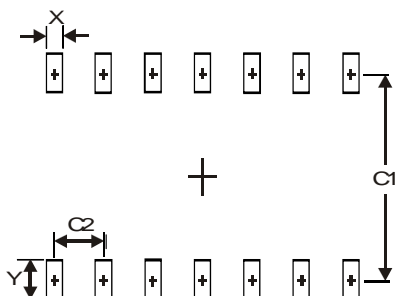
Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for latest version.

Package Type: SO-14



Dimensions	Value (in mm)
X	0.60
Y	1.50
C1	5.4
C2	1.27

Package Type: TSSOP-14



Dimensions	Value (in mm)
X	0.45
Y	1.45
C1	5.9
C2	0.65

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