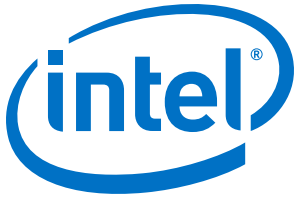

# Intel® MAX® 10 FPGA Device Datasheet

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# Contents

**Intel® MAX® 10 FPGA Device Datasheet ..... 3**
Electrical Characteristics ..... 3
Operating Conditions ..... 4
Switching Characteristics ..... 25
Core Performance Specifications ..... 26
Periphery Performance Specifications ..... 35
Configuration Specifications ..... 57
JTAG Timing Parameters ..... 58
Remote System Upgrade Circuitry Timing Specifications ..... 59
User Watchdog Internal Circuitry Timing Specifications ..... 59
Uncompressed Raw Binary File (.rbf) Sizes ..... 59
Internal Configuration Time ..... 60
Internal Configuration Timing Parameter ..... 61
I/O Timing ..... 61
Programmable IOE Delay ..... 62
Programmable IOE Delay On Row Pins ..... 62
Programmable IOE Delay for Column Pins ..... 63
Glossary ..... 64
Document Revision History for the Intel MAX 10 FPGA Device Datasheet ..... 67

# Intel® MAX® 10 FPGA Device Datasheet

This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and timing for Intel MAX® 10 devices.

**Table 1. Intel MAX 10 Device Grades and Speed Grades Supported**

| Device Grade | Speed Grade Supported |
|---|---|
| Commercial | • –C7<br>• –C8 (slowest) |
| Industrial | • –I6 (fastest)<br>• –I7 |
| Automotive | • –A6<br>• –A7 |

*Note:* The –I6 and –A6 speed grades of the Intel MAX 10 FPGA devices are not available by default in the Intel Quartus® Prime software. Contact your local Intel sales representatives for support.

### Related Information

Device Ordering Information, Intel MAX 10 FPGA Device Overview
Provides more information about the densities and packages of devices in the Intel MAX 10.

## Electrical Characteristics

The following sections describe the operating conditions and power consumption of Intel MAX 10 devices.

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# Operating Conditions

Intel MAX 10 devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Intel MAX 10 devices, you must consider the operating requirements described in this section.

## Absolute Maximum Ratings

This section defines the maximum operating conditions for Intel MAX 10 devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

***Caution:*** Conditions outside the range listed in the absolute maximum ratings tables may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

### Single Supply Devices Absolute Maximum Ratings

**Table 2. Absolute Maximum Ratings for Intel MAX 10 Single Supply Devices**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC_ONE}$ | Supply voltage for core and periphery through on-die voltage regulator | –0.5 | 3.9 | V |
| $V_{CCIO}$ | Supply voltage for input and output buffers | –0.5 | 3.9 | V |
| $V_{CCA}$ | Supply voltage for phase-locked loop (PLL) regulator and analog-to-digital converter (ADC) block (analog) | –0.5 | 3.9 | V |

### Dual Supply Devices Absolute Maximum Ratings

**Table 3. Absolute Maximum Ratings for Intel MAX 10 Dual Supply Devices**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage for core and periphery | –0.5 | 1.63 | V |
| $V_{CCIO}$ | Supply voltage for input and output buffers | –0.5 | 3.9 | V |
| $V_{CCA}$ | Supply voltage for PLL regulator (analog) | –0.5 | 3.41 | V |

*continued...*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CCD_PLL}$ | Supply voltage for PLL regulator (digital) | –0.5 | 1.63 | V |
| $V_{CCA_ADC}$ | Supply voltage for ADC analog block | –0.5 | 3.41 | V |
| $V_{CCINT}$ | Supply voltage for ADC digital block | –0.5 | 1.63 | V |

## Absolute Maximum Ratings

### Table 4. Absolute Maximum Ratings for Intel MAX 10 Devices

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_I$ | DC input voltage | –0.5 | 4.12 | V |
| $I_{OUT}$ | DC output current per pin | –25 | 25 | mA |
| $T_{STG}$ | Storage temperature | –65 | 150 | °C |
| $T_J$ | Operating junction temperature | –40 | 125 | °C |

## Maximum Allowed Overshoot During Transitions over a 11.4-Year Time Frame

During transitions, input signals may overshoot to the voltage listed in the following table and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

For example, a signal that overshoots to 4.17 V can only be at 4.17 V for ~11.7% over the lifetime of the device; for a device lifetime of 11.4 years, this amounts to 1.33 years.

### Table 5. Maximum Allowed Overshoot During Transitions over a 11.4-Year Time Frame for Intel MAX 10 Devices

| Condition (V) | Overshoot Duration as % of High Time | Unit |
|---|---|---|
| 4.12 | 100.0 | % |
| 4.17 | 11.7 | % |
| 4.22 | 7.1 | % |
| 4.27 | 4.3 | % |

*continued...*

| Condition (V) | Overshoot Duration as % of High Time | Unit |
|---|---|---|
| 4.32 | 2.6 | % |
| 4.37 | 1.6 | % |
| 4.42 | 1.0 | % |
| 4.47 | 0.6 | % |
| 4.52 | 0.3 | % |
| 4.57 | 0.2 | % |

## Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Intel MAX 10 devices. The tables list the steady-state voltage values expected from Intel MAX 10 devices. Power supply ramps must all be strictly monotonic, without plateaus.

### Single Supply Devices Power Supplies Recommended Operating Conditions

**Table 6. Power Supplies Recommended Operating Conditions for Intel MAX 10 Single Supply Devices**

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC_ONE}$(1) | Supply voltage for core and periphery through on-die voltage regulator | — | 2.85/3.135 | 3.0/3.3 | 3.15/3.465 | V |
| $V_{CCIO}$(2) | Supply voltage for input and output buffers | 3.3 V | 3.135 | 3.3 | 3.465 | V |
| | | 3.0 V | 2.85 | 3 | 3.15 | V |
| | | 2.5 V | 2.375 | 2.5 | 2.625 | V |
| | | 1.8 V | 1.71 | 1.8 | 1.89 | V |
| | | 1.5 V | 1.425 | 1.5 | 1.575 | V |
| | | 1.35 V | 1.2825 | 1.35 | 1.4175 | V |

*continued...*

(1) $V_{CCA}$ must be connected to $V_{CC_ONE}$ through a filter.

(2) $V_{CCIO}$ for all I/O banks must be powered up during user mode because $V_{CCIO}$ I/O banks are used for the ADC and I/O functionalities.

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | 1.2 V | 1.14 | 1.2 | 1.26 | V |
| | | 1.0 V | 0.95 | 1.0 | 1.05 | V |
| $V_{CCA}$ (1) | Supply voltage for PLL regulator and ADC block (analog) | — | 2.85/3.135 | 3.0/3.3 | 3.15/3.465 | V |

## Dual Supply Devices Power Supplies Recommended Operating Conditions

### Table 7. Power Supplies Recommended Operating Conditions for Intel MAX 10 Dual Supply Devices

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage for core and periphery | — | 1.15 | 1.2 | 1.25 | V |
| $V_{CCIO}$ (3) | Supply voltage for input and output buffers | 3.3 V | 3.135 | 3.3 | 3.465 | V |
| | | 3.0 V | 2.85 | 3 | 3.15 | V |
| | | 2.5 V | 2.375 | 2.5 | 2.625 | V |
| | | 1.8 V | 1.71 | 1.8 | 1.89 | V |
| | | 1.5 V | 1.425 | 1.5 | 1.575 | V |
| | | 1.35 V | 1.2825 | 1.35 | 1.4175 | V |
| | | 1.2 V | 1.14 | 1.2 | 1.26 | V |
| | | 1.0 V | 0.95 | 1.0 | 1.05 | V |
| $V_{CCA}$(4) | Supply voltage for PLL regulator (analog) | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCD_PLL}$(5) | Supply voltage for PLL regulator (digital) | — | 1.15 | 1.2 | 1.25 | V |
| $V_{CCA_ADC}$ | Supply voltage for ADC analog block | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCINT}$ | Supply voltage for ADC digital block | — | 1.15 | 1.2 | 1.25 | V |

(3) $V_{CCIO}$ for all I/O banks must be powered up during user mode because $V_{CCIO}$ I/O banks are used for the ADC and I/O functionalities.

(4) All $V_{CCA}$ pins must be powered to 2.5 V (even when PLLs are not used), and must be powered up and powered down at the same time.

(5) $V_{CCD_PLL}$ must always be connected to $V_{CC}$ through a decoupling capacitor and ferrite bead.

## Recommended Operating Conditions

### Table 8. Recommended Operating Conditions for Intel MAX 10 Devices

| Symbol | Parameter | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_I$ | DC input voltage | — | –0.5 | 3.6 | V |
| $V_O$ | Output voltage for I/O pins | — | 0 | $V_{CCIO}$ | V |
| $T_J$ | Operating junction temperature | Commercial | 0 | 85 | °C |
| | | Industrial | –40(6) | 100 | °C |
| | | Automotive | –40(6) | 125 | °C |
| $t_{RAMP}$ | Power supply ramp time | — | (7) | 10 | ms |
| $I_{Diode}$ | Magnitude of DC current across PCI* clamp diode when enabled | — | — | 10 | mA |

## Programming/Erasure Specifications

### Table 9. Programming/Erasure Specifications for Intel MAX 10 Devices

This table shows the programming cycles and data retention duration of the user flash memory (UFM) and configuration flash memory (CFM) blocks.

For more information about data retention duration with 10,000 programming cycles for automotive temperature devices, contact your Intel quality representative.

| Erase and reprogram cycles (E/P) (8) (Cycles/page) | Temperature (°C) | Data retention duration (Years) |
|---|---|---|
| 10,000 | 85 | 20 |
| 10,000 | 100 | 10 |

(6) –40°C is only applicable to Start of Test, when the device is powered-on. The device does not stay at the minimum junction temperature for a long time.

(7) There is no absolute minimum value for the ramp time requirement. Intel characterized the minimum ramp time at 200 µs.

(8) The number of E/P cycles applies to the smallest possible flash block that can be erased or programmed in each Intel MAX 10 device. Each Intel MAX 10 device has multiple flash pages per device.

# DC Characteristics

## Supply Current and Power Consumption

Intel offers two ways to estimate power for your design—the Excel-based Early Power Estimator (EPE) and the Intel Quartus Prime Power Analyzer feature.

Use the Excel-based EPE before you start your design to estimate the supply current for your design. The EPE provides a magnitude estimate of the device power because these currents vary greatly with the usage of the resources.

The Intel Quartus Prime Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yield very accurate power estimates.

### Related Information

- Early Power Estimator User Guide
  Provides more information about power estimation tools.
- Power Analysis chapter, Intel Quartus Prime Handbook
  Provides more information about power estimation tools.

## I/O Pin Leakage Current

The values in the table are specified for normal device operation. The values vary during device power-up. This applies for all $V_{CCIO}$ settings (3.3, 3.0, 2.5, 1.8, 1.5, 1.35, and 1.2 V).

10 µA I/O leakage current limit is applicable when the internal clamping diode is off. A higher current can be the observed when the diode is on.

Input channel leakage of ADC I/O pins due to hot socket is up to maximum of 1.8 mA. The input channel leakage occurs when the ADC IP core is enabled or disabled. This is applicable to all Intel MAX 10 devices with ADC IP core, which are 10M04, 10M08, 10M16, 10M25, 10M40, and 10M50 devices. The ADC I/O pins are in Bank 1A.

**Table 10. I/O Pin Leakage Current for Intel MAX 10 Devices**

| Symbol | Parameter | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $I_I$ | Input pin leakage current | $V_I$ = 0 V to $V_{CCIOMAX}$ | –10 | 10 | µA |
| $I_{OZ}$ | Tristated I/O pin leakage current | $V_O$ = 0 V to $V_{CCIOMAX}$ | –10 | 10 | µA |

### Table 11. ADC_VREF Pin Leakage Current for Intel MAX 10 Devices

| Symbol | Parameter | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $I_{adc_vref}$ | ADC_VREF pin leakage current | Single supply mode | — | 10 | µA |
| | | Dual supply mode | — | 20 | µA |

## Bus Hold Parameters

Bus hold retains the last valid logic state after the source driving it either enters the high impedance state or is removed. Each I/O pin has an option to enable bus hold in user mode. Bus hold is always disabled in configuration mode.

### Table 12. Bus Hold Parameters for Intel MAX 10 Devices

| Parameter | Condition | $V_{CCIO}$ (V) | | | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1.2 | | 1.5 | | 1.8 | | 2.5 | | 3.0 | | 3.3 | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Bus-hold low, sustaining current | $V_{IN} > V_{IL}$ (maximum) | 8 | — | 12 | — | 30 | — | 50 | — | 70 | — | 70 | — | µA |
| Bus-hold high, sustaining current | $V_{IN} < V_{IH}$ (minimum) | –8 | — | –12 | — | –30 | — | –50 | — | –70 | — | –70 | — | µA |
| Bus-hold low, overdrive current | $0 V < V_{IN} < V_{CCIO}$ | — | 125 | — | 175 | — | 200 | — | 300 | — | 500 | — | 500 | µA |
| Bus-hold high, overdrive current | $0 V < V_{IN} < V_{CCIO}$ | — | –125 | — | –175 | — | –200 | — | –300 | — | –500 | — | –500 | µA |
| Bus-hold trip point | — | 0.3 | 0.9 | 0.375 | 1.125 | 0.68 | 1.07 | 0.7 | 1.7 | 0.8 | 2 | 0.8 | 2 | V |

## Series OCT without Calibration Specifications

### Table 13. Series OCT without Calibration Specifications for Intel MAX 10 Devices

This table shows the variation of on-chip termination (OCT) without calibration across process, voltage, and temperature (PVT).

| Description | $V_{CCIO}$ (V) | Resistance Tolerance | | Unit |
|---|---|---|---|---|
| | | –C7, –I6, –I7, –A6, –A7 | –C8 | |
| Series OCT without calibration | 3.00 | ±35 | ±30 | % |
| | 2.50 | ±35 | ±30 | % |
| | 1.80 | ±40 | ±35 | % |
| | 1.50 | ±40 | ±40 | % |
| | 1.35 | ±40 | ±50 | % |
| | 1.20 | ±45 | ±60 | % |

## Series OCT with Calibration at Device Power-Up Specifications

### Table 14. Series OCT with Calibration at Device Power-Up Specifications for Intel MAX 10 Devices

OCT calibration is automatically performed at device power-up for OCT enabled I/Os.

| Description | $V_{CCIO}$ (V) | Calibration Accuracy | Unit |
|---|---|---|---|
| Series OCT with calibration at device power-up | 3.00 | ±12 | % |
| | 2.50 | ±12 | % |
| | 1.80 | ±12 | % |
| | 1.50 | ±12 | % |
| | 1.35 | ±12 | % |
| | 1.20 | ±12 | % |

## OCT Variation after Calibration at Device Power-Up

The OCT resistance may vary with the variation of temperature and voltage after calibration at device power-up.

Use the following table and equation to determine the final OCT resistance considering the variations after calibration at device power-up.

**Table 15. OCT Variation after Calibration at Device Power-Up for Intel MAX 10 Devices**

This table lists the change percentage of the OCT resistance with voltage and temperature.

| Description | Nominal Voltage | dR/dT (%/°C) | dR/dV (%/mV) |
|---|---|---|---|
| OCT variation after calibration at device power-up | 3.00 | 0.25 | –0.027 |
| | 2.50 | 0.245 | –0.04 |
| | 1.80 | 0.242 | –0.079 |
| | 1.50 | 0.235 | –0.125 |
| | 1.35 | 0.229 | –0.16 |
| | 1.20 | 0.197 | –0.208 |

**Figure 1. Equation for OCT Resistance after Calibration at Device Power-Up**

$$\Delta R_V = (V_2 - V_1) \times 1000 \times dR/dV$$

$$\Delta R_T = (T_2 - T_1) \times dR/dT$$

$$\text{For } \Delta R_X < 0; MF_X = 1/(|\Delta R_X|/100 + 1)$$

$$\text{For } \Delta R_X > 0; MF_X = \Delta R_X/100 + 1$$

$$MF = MF_V \times MF_T$$

$$R_{final} = R_{initial} \times MF$$

The definitions for equation are as follows:

- $T_1$ is the initial temperature.
- $T_2$ is the final temperature.
- MF is multiplication factor.
- $R_{initial}$ is initial resistance.
- $R_{final}$ is final resistance.

- Subscript x refers to both V and T.
- $\Delta R_V$ is variation of resistance with voltage.
- $\Delta R_T$ is variation of resistance with temperature.
- dR/dT is the change percentage of resistance with temperature after calibration at device power-up.
- dR/dV is the change percentage of resistance with voltage after calibration at device power-up.
- $V_1$ is the initial voltage.
- $V_2$ is final voltage.

The following figure shows the example to calculate the change of 50 Ω I/O impedance from 25°C at 3.0 V to 85°C at 3.15 V.

**Figure 2. Example for OCT Resistance Calculation after Calibration at Device Power-Up**

$$\Delta R_V = (3.15 - 3) \times 1000 \times -0.027 = -4.05$$

$$\Delta R_T = (85 - 25) \times 0.25 = 15$$

Because $\Delta R_V$ is negative,

$$MF_V = 1/(4.05/100 + 1) = 0.961$$

Because $\Delta R_T$ is positive,

$$MF_T = 15/100 + 1 = 1.15$$

$$MF = 0.961 \times 1.15 = 1.105$$

$$R_{final} = 50 \times 1.105 = 55.25\Omega$$

## Pin Capacitance

### Table 16. Pin Capacitance for Intel MAX 10 Devices

| Symbol | Parameter | Maximum | Unit |
|---|---|---|---|
| $C_{IOB}$ | Input capacitance on bottom I/O pins | 8 | pF |
| $C_{IOLRT}$ | Input capacitance on left/right/top I/O pins | 7 | pF |
| $C_{LVDSB}$ | Input capacitance on bottom I/O pins with dedicated LVDS output (9) | 8 | pF |
| $C_{ADCL}$ | Input capacitance on left I/O pins with ADC input (10) | 9 | pF |
| $C_{VREFLRT}$ | Input capacitance on left/right/top dual purpose $V_{REF}$ pin when used as $V_{REF}$ or user I/O pin (11) | 48 | pF |
| $C_{VREFB}$ | Input capacitance on bottom dual purpose $V_{REF}$ pin when used as $V_{REF}$ or user I/O pin | 50 | pF |
| $C_{CLKB}$ | Input capacitance on bottom dual purpose clock input pins (12) | 7 | pF |
| $C_{CLKLRT}$ | Input capacitance on left/right/top dual purpose clock input pins (12) | 6 | pF |

## Internal Weak Pull-Up Resistor

All I/O pins, except configuration, test, and JTAG pins, have an option to enable weak pull-up.

(9) Dedicated LVDS output buffer is only available at bottom I/O banks.

(10) ADC pins are only available at left I/O banks.

(11) When $V_{REF}$ pin is used as regular input or output, $F_{max}$ performance is reduced due to higher pin capacitance. Using the $V_{REF}$ pin capacitance specification from device datasheet, perform SI analysis on your board setup to determine the $F_{max}$ of your system.

(12) 10M40 and 10M50 devices have dual purpose clock input pins at top/bottom I/O banks.

### Table 17. Internal Weak Pull-Up Resistor for Intel MAX 10 Devices

Pin pull-up resistance values may be lower if an external source drives the pin higher than $V_{CCIO}$.

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{_PU}$ | Value of I/O pin (dedicated and dual-purpose) pull-up resistor before and during configuration, as well as user mode if the programmable pull-up resistor option is enabled | $V_{CCIO}$ = 3.3 V ± 5% | 7 | 12 | 34 | kΩ |
| | | $V_{CCIO}$ = 3.0 V ± 5% | 8 | 13 | 37 | kΩ |
| | | $V_{CCIO}$ = 2.5 V ± 5% | 10 | 15 | 46 | kΩ |
| | | $V_{CCIO}$ = 1.8 V ± 5% | 16 | 25 | 75 | kΩ |
| | | $V_{CCIO}$ = 1.5 V ± 5% | 20 | 36 | 106 | kΩ |
| | | $V_{CCIO}$ = 1.2 V ± 5% | 33 | 82 | 179 | kΩ |

## Hot-Socketing Specifications

### Table 18. Hot-Socketing Specifications for Intel MAX 10 Devices

| Symbol | Parameter | Maximum |
|---|---|---|
| $I_{IOPIN(DC)}$ | DC current per I/O pin | 300 µA |
| $I_{IOPIN(AC)}$ | AC current per I/O pin | 8 mA (13) |

## Hysteresis Specifications for Schmitt Trigger Input

Intel MAX 10 devices support Schmitt trigger input on all I/O pins. A Schmitt trigger feature introduces hysteresis to the input signal for improved noise immunity, especially for signal with slow edge rate.

(13) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}|$ = C dv/dt, in which C is I/O pin capacitance and dv/dt is the slew rate.

**Table 19. Hysteresis Specifications for Schmitt Trigger Input for Intel MAX 10 Devices**

| Symbol | Parameter | Condition | Minimum | Unit |
|---|---|---|---|---|
| $V_{HYS}$ | Hysteresis for Schmitt trigger input | $V_{CCIO}$ = 3.3 V | 180 | mV |
| | | $V_{CCIO}$ = 2.5 V | 150 | mV |
| | | $V_{CCIO}$ = 1.8 V | 120 | mV |
| | | $V_{CCIO}$ = 1.5 V | 110 | mV |

**Figure 3. LVTTL/LVCMOS Input Standard Voltage Diagram**

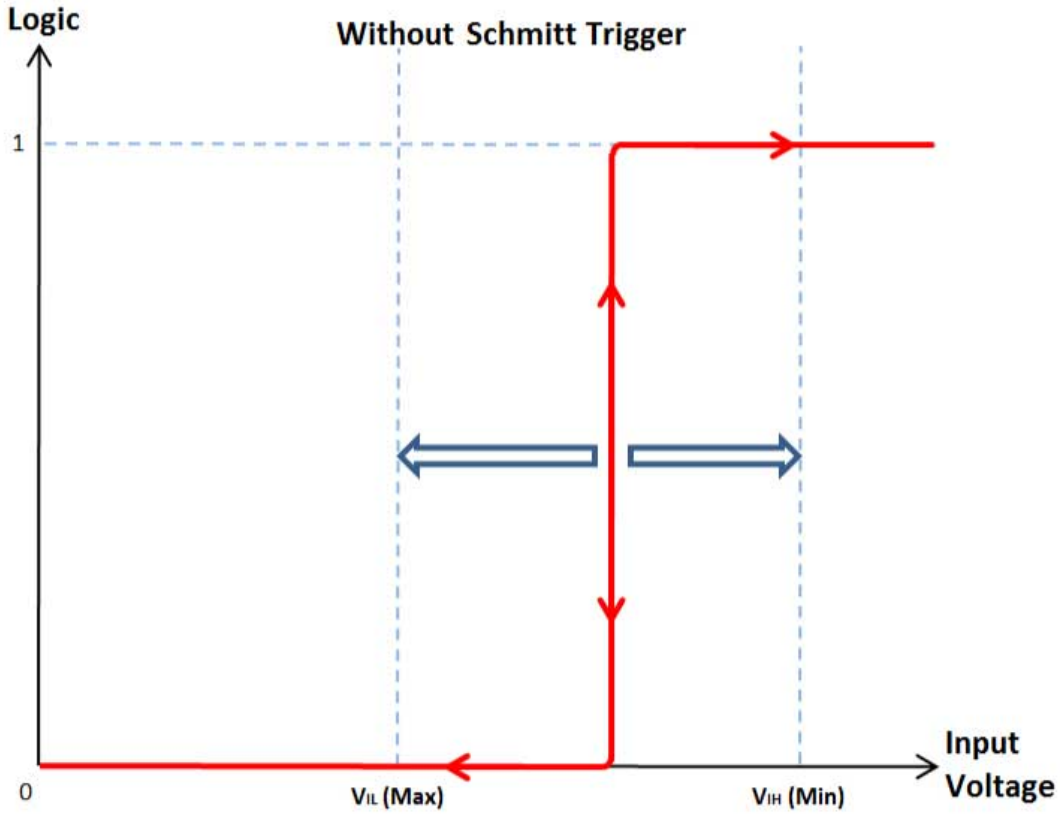
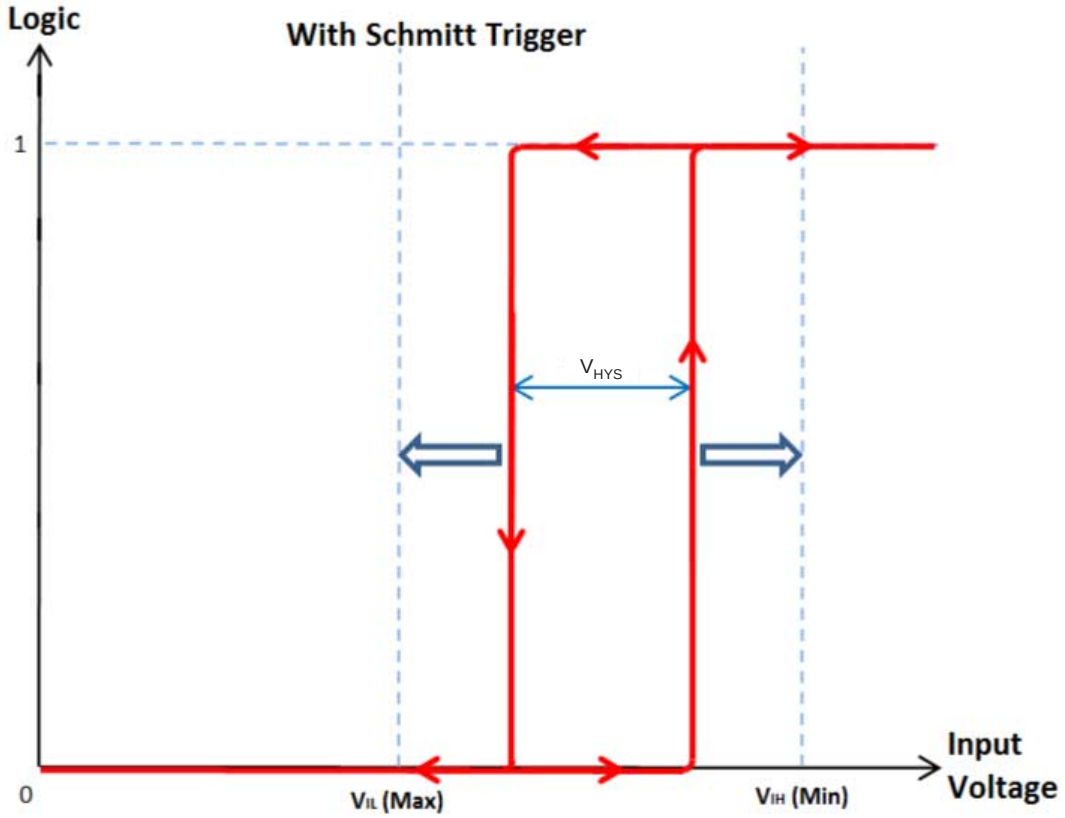


**Figure 4. Schmitt Trigger Input Standard Voltage Diagram**




## I/O Standards Specifications

Tables in this section list input voltage ($V_{IH}$ and $V_{IL}$), output voltage ($V_{OH}$ and $V_{OL}$), and current drive characteristics ($I_{OH}$ and $I_{OL}$) for various I/O standards supported by Intel MAX 10 devices.

For minimum voltage values, use the minimum $V_{CCIO}$ values. For maximum voltage values, use the maximum $V_{CCIO}$ values.

You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.

## Single-Ended I/O Standards Specifications

### Table 20. Single-Ended I/O Standards Specifications for Intel MAX 10 Devices

To meet the $I_{OL}$ and $I_{OH}$ specifications, you must set the current strength settings accordingly. For example, to meet the 3.3-V LVTTL specification (4 mA), you should set the current strength settings to 4 mA. Setting at lower current strength may not meet the $I_{OL}$ and $I_{OH}$ specifications in the datasheet.

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{IL}$ (V) | | $V_{IH}$ (V) | | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{OL}$ (mA) | $I_{OH}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Max | Max | Min | | |
| 3.3 V LVTTL | 3.135 | 3.3 | 3.465 | –0.3 | 0.8 | 1.7 | 3.6 | 0.45 | 2.4 | 4 | –4 |
| 3.3 V LVCMOS | 3.135 | 3.3 | 3.465 | –0.3 | 0.8 | 1.7 | 3.6 | 0.2 | $V_{CCIO}$ – 0.2 | 2 | –2 |
| 3.0 V LVTTL | 2.85 | 3 | 3.15 | –0.3 | 0.8 | 1.7 | $V_{CCIO}$ + 0.3 | 0.45 | 2.4 | 4 | –4 |
| 3.0 V LVCMOS | 2.85 | 3 | 3.15 | –0.3 | 0.8 | 1.7 | $V_{CCIO}$ + 0.3 | 0.2 | $V_{CCIO}$ – 0.2 | 0.1 | –0.1 |
| 2.5 V LVTTL and LVCMOS | 2.375 | 2.5 | 2.625 | –0.3 | 0.7 | 1.7 | $V_{CCIO}$ + 0.3 | 0.4 | 2 | 1 | –1 |
| 1.8 V LVTTL and LVCMOS | 1.71 | 1.8 | 1.89 | –0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | 2.25 | 0.45 | $V_{CCIO}$ – 0.45 | 2 | –2 |
| 1.5 V LVCMOS | 1.425 | 1.5 | 1.575 | –0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 2 | –2 |
| 1.2 V LVCMOS | 1.14 | 1.2 | 1.26 | –0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 2 | –2 |
| 1.0 V LVCMOS (14) | 0.95 | 1.0 | 1.05 | –0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 4 | –4 |
| 3.3 V Schmitt Trigger | 3.135 | 3.3 | 3.465 | –0.3 | 0.8 | 1.7 | $V_{CCIO}$ + 0.3 | — | — | — | — |
| 2.5 V Schmitt Trigger | 2.375 | 2.5 | 2.625 | –0.3 | 0.7 | 1.7 | $V_{CCIO}$ + 0.3 | — | — | — | — |

*continued...*

(14) The 1.0 V LVCMOS I/O standard is only supported on the following devices: 10M02SCU324C8G, 10M04SCU324C8G, 10M08SCU324C8G, 10M16SCU324C8G, 10M16SCU169C8G, 10M16SAU169C8G, 10M16DCF484C8G, 10M16DAF484C8G, 10M25DCF484C8G, 10M25DAF484C8G, 10M40DCF484C8G, 10M40DAF484C8G, 10M50DCF484C8G, 10M50DAF484C8G.

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{IL}$ (V) | | $V_{IH}$ (V) | | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{OL}$ (mA) | $I_{OH}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Max | Max | Min | | |
| 1.8 V Schmitt Trigger | 1.71 | 1.8 | 1.89 | –0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | — | — | — | — |
| 1.5 V Schmitt Trigger | 1.425 | 1.5 | 1.575 | –0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | — | — | — | — |
| 3.0 V PCI | 2.85 | 3 | 3.15 | — | 0.3 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.1 × $V_{CCIO}$ | 0.9 × $V_{CCIO}$ | 1.5 | –0.5 |

## Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

### Table 21. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Intel MAX 10 Devices

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{REF}$ (V) | | | $V_{TT}$ (V) (15) | | |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 1.19 | 1.25 | 1.31 | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| SSTL-18 Class I, II | 1.7 | 1.8 | 1.9 | 0.833 | 0.9 | 0.969 | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ |
| SSTL-135 Class I, II | 1.283 | 1.35 | 1.45 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.85 | 0.9 | 0.95 | 0.85 | 0.9 | 0.95 |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.71 | 0.75 | 0.79 | 0.71 | 0.75 | 0.79 |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.48 × $V_{CCIO}$ (16) | 0.5 × $V_{CCIO}$ (16) | 0.52 × $V_{CCIO}$ (16) | — | 0.5 × $V_{CCIO}$ | — |
| | | | | 0.47 × $V_{CCIO}$ (17) | 0.5 × $V_{CCIO}$ (17) | 0.53 × $V_{CCIO}$ (17) | | | |
| HSUL-12 | 1.14 | 1.2 | 1.3 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | — | — | — |

(15) $V_{TT}$ of transmitting device must track $V_{REF}$ of the receiving device.

(16) Value shown refers to DC input reference voltage, $V_{REF(DC)}$.

(17) Value shown refers to AC input reference voltage, $V_{REF(AC)}$.

## Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications

### Table 22. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Intel MAX 10 Devices

To meet the $I_{OL}$ and $I_{OH}$ specifications, you must set the current strength settings accordingly. For example, to meet the SSTL-15 Class I specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the $I_{OL}$ and $I_{OH}$ specifications in the datasheet.

| I/O Standard | $V_{IL(DC)}$ (V) | | $V_{IH(DC)}$ (V) | | $V_{IL(AC)}$ (V) | | $V_{IH(AC)}$ (V) | | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{OL}$ (mA) | $I_{OH}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | Max | Min | | |
| SSTL-2 Class I | — | $V_{REF}$ – 0.18 | $V_{REF}$ + 0.18 | — | — | $V_{REF}$ – 0.31 | $V_{REF}$ + 0.31 | — | $V_{TT}$ – 0.57 | $V_{TT}$ + 0.57 | 8.1 | –8.1 |
| SSTL-2 Class II | — | $V_{REF}$ – 0.18 | $V_{REF}$ + 0.18 | — | — | $V_{REF}$ – 0.31 | $V_{REF}$ + 0.31 | — | $V_{TT}$ – 0.76 | $V_{TT}$ + 0.76 | 16.4 | –16.4 |
| SSTL-18 Class I | — | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | — | — | $V_{REF}$ – 0.25 | $V_{REF}$ + 0.25 | — | $V_{TT}$ – 0.475 | $V_{TT}$ + 0.475 | 6.7 | –6.7 |
| SSTL-18 Class II | — | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | — | — | $V_{REF}$ – 0.25 | $V_{REF}$ + 0.25 | — | 0.28 | $V_{CCIO}$ – 0.28 | 13.4 | –13.4 |
| SSTL-15 Class I | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | — | $V_{REF}$ – 0.175 | $V_{REF}$ + 0.175 | — | 0.2 × $V_{CCIO}$ | 0.8 × $V_{CCIO}$ | 8 | –8 |
| SSTL-15 Class II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | — | $V_{REF}$ – 0.175 | $V_{REF}$ + 0.175 | — | 0.2 × $V_{CCIO}$ | 0.8 × $V_{CCIO}$ | 16 | –16 |
| SSTL-135 | — | $V_{REF}$ – 0.09 | $V_{REF}$ + 0.09 | — | — | $V_{REF}$ – 0.16 | $V_{REF}$ + 0.16 | — | 0.2 × $V_{CCIO}$ | 0.8 × $V_{CCIO}$ | — | — |
| HSTL-18 Class I | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | — | 0.4 | $V_{CCIO}$ – 0.4 | 8 | –8 |
| HSTL-18 Class II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | — | 0.4 | $V_{CCIO}$ – 0.4 | 16 | –16 |
| HSTL-15 Class I | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | — | 0.4 | $V_{CCIO}$ – 0.4 | 8 | –8 |
| HSTL-15 Class II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | — | 0.4 | $V_{CCIO}$ – 0.4 | 16 | –16 |

*continued...*

| I/O Standard | $V_{IL(DC)}$ (V) | | $V_{IH(DC)}$ (V) | | $V_{IL(AC)}$ (V) | | $V_{IH(AC)}$ (V) | | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{OL}$ (mA) | $I_{OH}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | Max | Min | | |
| HSTL-12 Class I | –0.15 | $V_{REF}$ – 0.08 | $V_{REF}$ + 0.08 | $V_{CCIO}$ + 0.15 | –0.24 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | $V_{CCIO}$ + 0.24 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 8 | –8 |
| HSTL-12 Class II | –0.15 | $V_{REF}$ – 0.08 | $V_{REF}$ + 0.08 | $V_{CCIO}$ + 0.15 | –0.24 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | $V_{CCIO}$ + 0.24 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 14 | –14 |
| HSUL-12 | — | $V_{REF}$ – 0.13 | $V_{REF}$ + 0.13 | — | — | $V_{REF}$ – 0.22 | $V_{REF}$ + 0.22 | — | 0.1 × $V_{CCIO}$ | 0.9 × $V_{CCIO}$ | — | — |

## Differential SSTL I/O Standards Specifications

Differential SSTL requires a $V_{REF}$ input.

### Table 23. Differential SSTL I/O Standards Specifications for Intel MAX 10 Devices

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{Swing(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{Swing(AC)}$ (V) | |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max[18] | Min | Typ | Max | Min | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 0.36 | $V_{CCIO}$ | $V_{CCIO}/2$ – 0.2 | — | $V_{CCIO}/2$+ 0.2 | 0.7 | $V_{CCIO}$ |
| SSTL-18 Class I, II | 1.7 | 1.8 | 1.9 | 0.25 | $V_{CCIO}$ | $V_{CCIO}/2$ – 0.175 | — | $V_{CCIO}/2$+ 0.175 | 0.5 | $V_{CCIO}$ |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | — | $V_{CCIO}/2$ – 0.15 | — | $V_{CCIO}/2$ + 0.15 | $2(V_{IH(AC)} – V_{REF})$ | $2(V_{IL(AC)} – V_{REF})$ |
| SSTL-135 | 1.283 | 1.35 | 1.45 | 0.18 | — | $V_{REF}$ – 0.135 | 0.5 × $V_{CCIO}$ | $V_{REF}$ + 0.135 | $2(V_{IH(AC)} – V_{REF})$ | $2(V_{IL(AC)} – V_{REF})$ |

## Differential HSTL and HSUL I/O Standards Specifications

Differential HSTL requires a $V_{REF}$ input.

(18) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

### Table 24. Differential HSTL and HSUL I/O Standards Specifications for Intel MAX 10 Devices

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{DIF(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{CM(DC)}$ (V) | | | $V_{DIF(AC)}$ (V) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Typ | Max | Min |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.2 | — | 0.85 | — | 0.95 | 0.85 | — | 0.95 | 0.4 |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | — | 0.71 | — | 0.79 | 0.71 | — | 0.79 | 0.4 |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.16 | $V_{CCIO}$ | 0.48 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.52 × $V_{CCIO}$ | 0.48 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.52 × $V_{CCIO}$ | 0.3 |
| HSUL-12 | 1.14 | 1.2 | 1.3 | 0.26 | — | 0.5 × $V_{CCIO}$ – 0.12 | 0.5 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ + 0.12 | 0.4 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.6 × $V_{CCIO}$ | 0.44 |

## Differential I/O Standards Specifications

### Table 25. Differential I/O Standards Specifications for Intel MAX 10 Devices

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{ID}$ (mV) | | $V_{ICM}$ (V) (19) | | | $V_{OD}$ (mV) (20)(21) | | | $V_{OS}$ (V) (20) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Condition | Max | Min | Typ | Max | Min | Typ | Max |
| LVPECL (22) | 2.375 | 2.5 | 2.625 | 100 | — | 0.05 | $D_{MAX}$ ≤ 500 Mbps | 1.8 | — | — | — | — | — | — |
| | | | | | | 0.55 | 500 Mbps ≤ $D_{MAX}$ ≤ 700 Mbps | 1.8 | | | | | | |
| | | | | | | 1.05 | $D_{MAX}$ > 700 Mbps | 1.55 | | | | | | |
| LVDS | 2.375 | 2.5 | 2.625 | 100 | — | 0.05 | $D_{MAX}$ ≤ 500 Mbps | 1.8 | 247 | — | 600 | 1.125 | 1.25 | 1.375 |
| | | | | | | 0.55 | 500 Mbps ≤ $D_{MAX}$ ≤ 700 Mbps | 1.8 | | | | | | |

*continued...*

(19) $V_{IN}$ range: 0 V ≤ $V_{IN}$ ≤ 1.85 V.

(20) $R_L$ range: 90 ≤ $R_L$ ≤ 110 Ω.

(21) Low $V_{OD}$ setting is only supported for RSDS standard.

(22) LVPECL input standard is only supported at clock input. Output standard is not supported.

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{ID}$ (mV) | | $V_{ICM}$ (V) (19) | | | $V_{OD}$ (mV) (20)(21) | | | $V_{OS}$ (V) (20) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Condition | Max | Min | Typ | Max | Min | Typ | Max |
| | | | | | | 1.05 | $D_{MAX}$ > 700 Mbps | 1.55 | | | | | | |
| BLVDS (23) | 2.375 | 2.5 | 2.625 | 100 | — | — | — | — | — | — | — | — | — | — |
| mini-LVDS (24) | 2.375 | 2.5 | 2.625 | — | — | — | — | — | 300 | — | 600 | 1 | 1.2 | 1.4 |
| RSDS (24) | 2.375 | 2.5 | 2.625 | — | — | — | — | — | 100 | 200 | 600 | 0.5 | 1.2 | 1.5 |
| PPDS (Row I/Os) (24) | 2.375 | 2.5 | 2.625 | — | — | — | — | — | 100 | 200 | 600 | 0.5 | 1.2 | 1.4 |
| TMDS(25) | 2.375 | 2.5 | 2.625 | 100 | — | 0.05 | $D_{MAX}$ ≤ 500 Mbps | 1.8 | — | — | — | — | — | — |
| | | | | | | 0.55 | 500 Mbps ≤ $D_{MAX}$ ≤ 700 Mbps | 1.8 | | | | | | |
| | | | | | | 1.05 | $D_{MAX}$ > 700 Mbps | 1.55 | | | | | | |
| Sub-LVDS (26) | 1.71 | 1.8 | 1.89 | 100 | — | 0.55 | — | 1.25 | (27) | | | 0.8 | 0.9 | 1 |
| SLVS | 2.375 | 2.5 | 2.625 | 100 | — | 0.05 | — | 1.1 | (27) | | | (28) | | |

continued...

(19) $V_{IN}$ range: 0 V ≤ $V_{IN}$ ≤ 1.85 V.
(20) $R_L$ range: 90 ≤ $R_L$ ≤ 110 Ω.
(21) Low $V_{OD}$ setting is only supported for RSDS standard.

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{ID}$ (mV) | | $V_{ICM}$ (V) (19) | | | $V_{OD}$ (mV) (20)(21) | | | $V_{OS}$ (V) (20) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Condition | Max | Min | Typ | Max | Min | Typ | Max |
| HiSpi | 2.375 | 2.5 | 2.625 | 100 | — | 0.05 | $D_{MAX}$ ≤ 500 Mbps | 1.8 | — | — | — | — | — | — |
| | | | | | | 0.55 | 500 Mbps ≤ $D_{MAX}$ ≤ 700 Mbps | 1.8 | | | | | | |
| | | | | | | 1.05 | $D_{MAX}$ > 700 Mbps | 1.55 | | | | | | |

**Related Information**

Intel MAX 10 LVDS SERDES I/O Standards Support, Intel MAX 10 High-Speed LVDS I/O User Guide
Provides the list of I/O standards supported in single supply and dual supply devices.

## Switching Characteristics

This section provides the performance characteristics of Intel MAX 10 core and periphery blocks.

(19) $V_{IN}$ range: 0 V ≤ $V_{IN}$ ≤ 1.85 V.
(20) $R_L$ range: 90 ≤ $R_L$ ≤ 110 Ω.
(21) Low $V_{OD}$ setting is only supported for RSDS standard.

(23) No fixed $V_{IN}$ , $V_{OD}$ , and $V_{OS}$ specifications for Bus LVDS (BLVDS). They are dependent on the system topology.

(24) Mini-LVDS, RSDS, and Point-to-Point Differential Signaling (PPDS) standards are only supported at the output pins for Intel MAX 10 devices.

(25) Supported with requirement of an external level shift

(26) Sub-LVDS input buffer is using 2.5 V differential buffer.

(27) Differential output depends on the values of the external termination resistors.

(28) Differential output offset voltage depends on the values of the external termination resistors.

# Core Performance Specifications

## Clock Tree Specifications

### Table 26. Clock Tree Specifications for Intel MAX 10 Devices

| Device | Performance | | | | | Unit |
|---|---|---|---|---|---|---|
| | –I6 | –A6, –C7 | –I7 | –A7 | –C8 | |
| 10M02 | 450 | 416 | 416 | 382 | 402 | MHz |
| 10M04 | 450 | 416 | 416 | 382 | 402 | MHz |
| 10M08 | 450 | 416 | 416 | 382 | 402 | MHz |
| 10M16 | 450 | 416 | 416 | 382 | 402 | MHz |
| 10M25 | 450 | 416 | 416 | 382 | 402 | MHz |
| 10M40 | 450 | 416 | 416 | 382 | 402 | MHz |
| 10M50 | 450 | 416 | 416 | 382 | 402 | MHz |

## PLL Specifications

### Table 27. PLL Specifications for Intel MAX 10 Devices

$V_{CCD_PLL}$ should always be connected to $V_{CCINT}$ through decoupling capacitor and ferrite bead.

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{IN}$ (29) | Input clock frequency | — | 5 | — | 472.5 | MHz |
| $f_{INPFD}$ | Phase frequency detector (PFD) input frequency | — | 5 | — | 325 | MHz |

*continued...*

(29) This parameter is limited in the Intel Quartus Prime software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{VCO}$ (30) | PLL internal voltage-controlled oscillator (VCO) operating range | — | 600 | — | 1300 | MHz |
| $f_{INDUTY}$ | Input clock duty cycle | — | 40 | — | 60 | % |
| $t_{INJITTER_CCJ}$ (31) | Input clock cycle-to-cycle jitter | $F_{INPFD}$ ≥ 100 MHz | — | — | 0.15 | UI |
| | | $F_{INPFD}$ < 100 MHz | — | — | ±750 | ps |
| $f_{OUT_EXT}$ (29) | PLL output frequency for external clock output | — | — | — | 472.5 | MHz |
| $f_{OUT}$ | PLL output frequency to global clock | –6 speed grade | — | — | 472.5 | MHz |
| | | –7 speed grade | — | — | 450 | MHz |
| | | –8 speed grade | — | — | 402.5 | MHz |
| $t_{OUTDUTY}$ | Duty cycle for external clock output | Duty cycle set to 50% | 45 | 50 | 55 | % |
| $t_{LOCK}$ | Time required to lock from end of device configuration | — | — | — | 1 | ms |
| $t_{DLOCK}$ | Time required to lock dynamically | After switchover, reconfiguring any non-post-scale counters or delays, or when `areset` is deasserted | — | — | 1 | ms |
| $t_{OUTJITTER_PERIOD_IO}$ (32) | Regular I/O period jitter | $F_{OUT}$ ≥ 100 MHz | — | — | 650 | ps |
| | | $F_{OUT}$ < 100 MHz | — | — | 75 | mUI |
| $t_{OUTJITTER_CCJ_IO}$ (32) | Regular I/O cycle-to-cycle jitter | $F_{OUT}$ ≥ 100 MHz | — | — | 650 | ps |
| | | $F_{OUT}$ < 100 MHz | — | — | 75 | mUI |

***continued...***

(30) The VCO frequency reported by the Intel Quartus Prime software in the PLL summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the $f_{VCO}$ specification.

(31) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source, which is less than 200 ps.

(32) Peak-to-peak jitter with a probability level of $10^{-12}$ (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied.

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{PLL_PSERR}$ | Accuracy of PLL phase shift | — | — | — | ±50 | ps |
| $t_{ARESET}$ | Minimum pulse width on areset signal. | — | 10 | — | — | ns |
| $t_{CONFIGPLL}$ | Time required to reconfigure scan chains for PLLs | — | — | 3.5 (33) | — | SCANCLK cycles |
| $f_{SCANCLK}$ | scanclk frequency | — | — | — | 100 | MHz |

## Table 28. PLL Specifications for Intel MAX 10 Single Supply Devices

For V36 package, the PLL specification is based on single supply devices.

| Symbol | Parameter | Condition | Max | Unit |
|---|---|---|---|---|
| $t_{OUTJITTER_PERIOD_DEDCLK}$ (32) | Dedicated clock output period jitter | $F_{OUT} \geq 100$ MHz | 660 | ps |
| | | $F_{OUT} < 100$ MHz | 66 | mUI |
| $t_{OUTJITTER_CCJ_DEDCLK}$ (32) | Dedicated clock output cycle-to-cycle jitter | $F_{OUT} \geq 100$ MHz | 660 | ps |
| | | $F_{OUT} < 100$ MHz | 66 | mUI |

## Table 29. PLL Specifications for Intel MAX 10 Dual Supply Devices

| Symbol | Parameter | Condition | Max | Unit |
|---|---|---|---|---|
| $t_{OUTJITTER_PERIOD_DEDCLK}$ (32) | Dedicated clock output period jitter | $F_{OUT} \geq 100$ MHz | 300 | ps |
| | | $F_{OUT} < 100$ MHz | 30 | mUI |
| $t_{OUTJITTER_CCJ_DEDCLK}$ (32) | Dedicated clock output cycle-to-cycle jitter | $F_{OUT} \geq 100$ MHz | 300 | ps |
| | | $F_{OUT} < 100$ MHz | 30 | mUI |

(33) With 100 MHz scanclk frequency.

## Embedded Multiplier Specifications

### Table 30. Embedded Multiplier Specifications for Intel MAX 10 Devices

| Mode | Number of Multipliers | Power Supply Mode | Performance | | | Unit |
|---|---|---|---|---|---|---|
| | | | –I6 | –A6, –C7, –I7, –A7 | –C8 | |
| 9 × 9-bit multiplier | 1 | Single supply mode | 198 | 183 | 160 | MHz |
| | | Dual supply mode | 310 | 260 | 210 | MHz |
| 18 × 18-bit multiplier | 1 | Single supply mode | 198 | 183 | 160 | MHz |
| | | Dual supply mode | 265 | 240 | 190 | MHz |

## Memory Block Performance Specifications

### Table 31. Memory Block Performance Specifications for Intel MAX 10 Devices

| Memory | Mode | Resources Used | | Power Supply Mode | Performance | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | LEs | M9K Memory | | –I6 | –A6, –C7, –I7, –A7 | –C8 | |
| M9K Block | FIFO 256 × 36 | 47 | 1 | Single supply mode | 232 | 219 | 204 | MHz |
| | | | | Dual supply mode | 330 | 300 | 250 | MHz |
| | Single-port 256 × 36 | 0 | 1 | Single supply mode | 232 | 219 | 204 | MHz |
| | | | | Dual supply mode | 330 | 300 | 250 | MHz |
| | Simple dual-port 256 × 36 CLK | 0 | 1 | Single supply mode | 232 | 219 | 204 | MHz |
| | | | | Dual supply mode | 330 | 300 | 250 | MHz |
| | True dual port 512 × 18 single CLK | 0 | 1 | Single supply mode | 232 | 219 | 204 | MHz |
| | | | | Dual supply mode | 330 | 300 | 250 | MHz |

## Internal Oscillator Specifications

### Table 32. Internal Oscillator Frequencies for Intel MAX 10 Devices

You can access to the internal oscillator frequencies in this table. The duty cycle of internal oscillator is approximately 45%–55%.

| Device | Frequency | | | Unit |
|---|---|---|---|---|
| | Minimum | Typical | Maximum | |
| 10M02 | 55 | 82 | 116 | MHz |
| 10M04 | | | | |
| 10M08 | | | | |
| 10M16 | | | | |
| 10M25 | | | | |
| 10M40 | 35 | 52 | 77 | MHz |
| 10M50 | | | | |

## UFM Performance Specifications

### Table 33. UFM Performance Specifications for Intel MAX 10 Devices

| Block | Mode | Interface | Device | Frequency | | Unit |
|---|---|---|---|---|---|---|
| | | | | Minimum | Maximum | |
| UFM | Avalon®-MM slave | Parallel (34) | 10M02 (35) | 3.43 | 7.25 | MHz |
| | | | 10M04, 10M08, 10M16, 10M25, 10M40, 10M50 | 5 | 116 | MHz |
| | | Serial (35) | 10M02, 10M04, 10M08, 10M16, 10M25 | 3.43 | 7.25 | MHz |
| | | | 10M40, 10M50 | 2.18 | 4.81 | MHz |

(34) Clock source is derived from user, except for 10M02 device.

(35) Clock source is derived from 1/16 of the frequency of the internal oscillator.

# ADC Performance Specifications

## Single Supply Devices ADC Performance Specifications

### Table 34. ADC Performance Specifications for Intel MAX 10 Single Supply Devices

| Parameter | | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| ADC resolution | | — | — | — | — | 12 | bits |
| ADC supply voltage | | $V_{CC_ONE}$ | — | 2.85 | 3.0/3.3 | 3.465 | V |
| External reference voltage | | $V_{REF}$ | — | $V_{CC_ONE}$ – 0.5 | — | $V_{CC_ONE}$ | V |
| Sampling rate | | $F_S$ | Accumulative sampling rate | — | — | 1 | MSPS |
| Operating junction temperature range | | $T_J$ | — | –40 | 25 | 125 | °C |
| Analog input voltage | | $V_{IN}$ | Prescalar disabled | 0 | — | $V_{REF}$ | V |
| | | | Prescalar enabled (36) | 0 | — | 3.6 | V |
| Input resistance | | $R_{IN}$ | — | — | (37) | — | — |
| Input capacitance | | $C_{IN}$ | — | — | (37) | — | — |
| DC Accuracy | Offset error and drift | $E_{offset}$ | Prescalar disabled | –0.2 | — | 0.2 | %FS |
| | | | Prescalar enabled | –0.5 | — | 0.5 | %FS |
| | Gain error and drift | $E_{gain}$ | Prescalar disabled | –0.5 | — | 0.5 | %FS |
| | | | Prescalar enabled | –0.75 | — | 0.75 | %FS |
| | Differential non linearity | DNL | External $V_{REF}$, no missing code | –0.9 | — | 0.9 | LSB |
| | | | Internal $V_{REF}$, no missing code | –1 | — | 1.7 | LSB |

*continued...*

(36) Prescalar function divides the analog input voltage by half. The analog input handles up to 3.6 V for the Intel MAX 10 single supply devices.

(37) Download the SPICE models for simulation.

| Parameter | | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| | Integral non linearity | INL | — | –2 | — | 2 | LSB |
| AC Accuracy | Total harmonic distortion | THD | $F_{IN}$ = 50 kHz, $F_S$ = 1 MHz, PLL | –65 (38) | — | — | dB |
| | Signal-to-noise ratio | SNR | $F_{IN}$ = 50 kHz, $F_S$ = 1 MHz, PLL | 54 (39) | — | — | dB |
| | Signal-to-noise and distortion | SINAD | $F_{IN}$ = 50 kHz, $F_S$ = 1 MHz, PLL | 53 (40) | — | — | dB |
| On-Chip Temperature Sensor | Temperature sampling rate | $T_S$ | — | — | — | 50 | kSPS |
| | Absolute accuracy | — | –40 to 125°C, with 64 samples averaging (41) | — | — | ±10 | °C |
| Conversion Rate (42) | Conversion time | — | Single measurement | — | — | 1 | Cycle |
| | | | Continuous measurement | — | — | 1 | Cycle |
| | | | Temperature measurement | — | — | 1 | Cycle |

**Related Information**

SPICE Models for Intel FPGAs

(38) THD with prescalar enabled is 6dB less than the specification.

(39) SNR with prescalar enabled is 6dB less than the specification.

(40) SINAD with prescalar enabled is 6dB less than the specification.

(41) For the Intel Quartus Prime software version 15.0 and later, Modular ADC Core Intel FPGA IP and Modular Dual ADC Core Intel FPGA IP cores handle the 64 samples averaging. For the Intel Quartus Prime software versions prior to 14.1, you need to implement your own averaging calculation.

(42) For more detailed description, refer to the Timing section in the *Intel MAX 10 Analog-to-Digital Converter User Guide*.

## Dual Supply Devices ADC Performance Specifications

### Table 35. ADC Performance Specifications for Intel MAX 10 Dual Supply Devices

| Parameter | | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| ADC resolution | | — | — | — | — | 12 | bits |
| Analog supply voltage | | $V_{CCA_ADC}$ | — | 2.375 | 2.5 | 2.625 | V |
| Digital supply voltage | | $V_{CCINT}$ | — | 1.15 | 1.2 | 1.25 | V |
| External reference voltage | | $V_{REF}$ | — | $V_{CCA_ADC}$ – 0.5 | — | $V_{CCA_ADC}$ | V |
| Sampling rate | | $F_S$ | Accumulative sampling rate | — | — | 1 | MSPS |
| Operating junction temperature range | | $T_J$ | — | –40 | 25 | 125 | °C |
| Analog input voltage | | $V_{IN}$ | Prescalar disabled | 0 | — | $V_{REF}$ | V |
| | | | Prescalar enabled (43) | 0 | — | 3 | V |
| Analog supply current (DC) | | $I_{ACC_ADC}$ | Average current | — | 275 | 450 | µA |
| Digital supply current (DC) | | $I_{CCINT}$ | Average current | — | 65 | 150 | µA |
| Input resistance | | $R_{IN}$ | — | — | (44) | — | — |
| Input capacitance | | $C_{IN}$ | — | — | (44) | — | — |
| DC Accuracy | Offset error and drift | $E_{offset}$ | Prescalar disabled | –0.2 | — | 0.2 | %FS |
| | | | Prescalar enabled | –0.5 | — | 0.5 | %FS |
| | Gain error and drift | $E_{gain}$ | Prescalar disabled | –0.5 | — | 0.5 | %FS |
| | | | Prescalar enabled | –0.75 | — | 0.75 | %FS |
| | Differential non linearity | DNL | External $V_{REF}$, no missing code | –0.9 | — | 0.9 | LSB |

*continued...*

(43) Prescalar function divides the analog input voltage by half. The analog input handles up to 3 V input for the Intel MAX 10 dual supply devices.

(44) Download the SPICE models for simulation.

| Parameter | | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| | | | Internal $V_{REF}$, no missing code | –1 | — | 1.7 | LSB |
| | Integral non linearity | INL | — | –2 | — | 2 | LSB |
| AC Accuracy | Total harmonic distortion | THD | $F_{IN}$ = 50 kHz, $F_S$ = 1 MHz, PLL | –70 (45)(46)(47) | — | — | dB |
| | Signal-to-noise ratio | SNR | $F_{IN}$ = 50 kHz, $F_S$ = 1 MHz, PLL | 62 (48)(49)(47) | — | — | dB |
| | Signal-to-noise and distortion | SINAD | $F_{IN}$ = 50 kHz, $F_S$ = 1 MHz, PLL | 61.5 (50)(51)(47) | — | — | dB |
| On-Chip Temperature Sensor | Temperature sampling rate | $T_S$ | — | — | — | 50 | kSPS |
| | Absolute accuracy | — | –40 to 125°C, with 64 samples averaging (52) | — | — | ±5 | °C |

continued...

(45) Total harmonic distortion is –65 dB for dual function pin.

(46) THD with prescalar enabled is 6dB less than the specification.

(47) When using internal $V_{REF}$, THD = 66 dB, SNR = 58 dB and SINAD = 57.5 dB for dedicated ADC input channels.

(48) Signal-to-noise ratio is 54 dB for dual function pin.

(49) SNR with prescalar enabled is 6dB less than the specification.

(50) Signal-to-noise and distortion is 53 dB for dual function pin.

(51) SINAD with prescalar enabled is 6dB less than the specification.

(52) For the Intel Quartus Prime software version 15.0 and later, Modular ADC Core and Modular Dual ADC Core IP cores handle the 64 samples averaging. For the Intel Quartus Prime software versions prior to 14.1, you need to implement your own averaging calculation.

| Parameter | | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Conversion Rate (53) | Conversion time | — | Single measurement | — | — | 1 | Cycle |
| | | | Continuous measurement | — | — | 1 | Cycle |
| | | | Temperature measurement | — | — | 1 | Cycle |

**Related Information**

SPICE Models for Intel FPGAs

## Periphery Performance Specifications

This section describes the periphery performance, high-speed I/O, and external memory interface.

Actual achievable frequency depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

## High-Speed I/O Specifications

For more information about the high-speed and low-speed I/O performance pins, refer to the respective device pin-out files.

**Related Information**

Documentation: Pin-Out Files for Intel FPGAs

(53) For more detailed description, refer to the Timing section in the *Intel MAX 10 Analog-to-Digital Converter User Guide*.

## True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications

### Table 36. True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices

True **PPDS** transmitter is only supported at bottom I/O banks. Emulated **PPDS** transmitter is supported at the output pin of all I/O banks.

| Symbol | Parameter | Mode | –I6, –A6, –C7, –I7 | | | –A7 | | | –C8 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSCLK}$ | Input clock frequency (high-speed I/O performance pin) | ×10 | 5 | — | 155 | 5 | — | 155 | 5 | — | 155 | MHz |
| | | ×8 | 5 | — | 155 | 5 | — | 155 | 5 | — | 155 | MHz |
| | | ×7 | 5 | — | 155 | 5 | — | 155 | 5 | — | 155 | MHz |
| | | ×4 | 5 | — | 155 | 5 | — | 155 | 5 | — | 155 | MHz |
| | | ×2 | 5 | — | 155 | 5 | — | 155 | 5 | — | 155 | MHz |
| | | ×1 | 5 | — | 310 | 5 | — | 310 | 5 | — | 310 | MHz |
| HSIODR | Data rate (high-speed I/O performance pin) | ×10 | 100 | — | 310 | 100 | — | 310 | 100 | — | 310 | Mbps |
| | | ×8 | 80 | — | 310 | 80 | — | 310 | 80 | — | 310 | Mbps |
| | | ×7 | 70 | — | 310 | 70 | — | 310 | 70 | — | 310 | Mbps |
| | | ×4 | 40 | — | 310 | 40 | — | 310 | 40 | — | 310 | Mbps |
| | | ×2 | 20 | — | 310 | 20 | — | 310 | 20 | — | 310 | Mbps |
| | | ×1 | 10 | — | 310 | 10 | — | 310 | 10 | — | 310 | Mbps |
| $f_{HSCLK}$ | Input clock frequency (low-speed I/O performance pin) | ×10 | 5 | — | 150 | 5 | — | 150 | 5 | — | 150 | MHz |
| | | ×8 | 5 | — | 150 | 5 | — | 150 | 5 | — | 150 | MHz |
| | | ×7 | 5 | — | 150 | 5 | — | 150 | 5 | — | 150 | MHz |
| | | ×4 | 5 | — | 150 | 5 | — | 150 | 5 | — | 150 | MHz |
| | | ×2 | 5 | — | 150 | 5 | — | 150 | 5 | — | 150 | MHz |
| | | ×1 | 5 | — | 300 | 5 | — | 300 | 5 | — | 300 | MHz |
| HSIODR | Data rate (low-speed I/O performance pin) | ×10 | 100 | — | 300 | 100 | — | 300 | 100 | — | 300 | Mbps |
| | | ×8 | 80 | — | 300 | 80 | — | 300 | 80 | — | 300 | Mbps |
| | | ×7 | 70 | — | 300 | 70 | — | 300 | 70 | — | 300 | Mbps |

*continued...*

| Symbol | Parameter | Mode | –I6, –A6, –C7, –I7 | | | –A7 | | | –C8 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| | | ×4 | 40 | — | 300 | 40 | — | 300 | 40 | — | 300 | Mbps |
| | | ×2 | 20 | — | 300 | 20 | — | 300 | 20 | — | 300 | Mbps |
| | | ×1 | 10 | — | 300 | 10 | — | 300 | 10 | — | 300 | Mbps |
| $t_{DUTY}$ | Duty cycle on transmitter output clock | — | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | % |
| TCCS(54) | Transmitter channel-to-channel skew | — | — | — | 300 | — | — | 300 | — | — | 300 | ps |
| $t_{x\ Jitter}$(55) | Output jitter (high-speed I/O performance pin) | — | — | — | 425 | — | — | 425 | — | — | 425 | ps |
| | Output jitter (low-speed I/O performance pin) | — | — | — | 470 | — | — | 470 | — | — | 470 | ps |
| $t_{RISE}$ | Rise time | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{FALL}$ | Fall time | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{LOCK}$ | Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration | — | — | — | 1 | — | — | 1 | — | — | 1 | ms |

(54) TCCS specifications apply to I/O banks from the same side only.

(55) TX jitter is the jitter induced from core noise and I/O switching noise.

## True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications

### Single Supply Devices True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications

**Table 37. True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices**

True **RSDS** transmitter is only supported at bottom I/O banks. Emulated **RSDS** transmitter is supported at the output pin of all I/O banks.

| Symbol | Parameter | Mode | –I6, –A6, –C7, –I7 | | | –A7 | | | –C8 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSCLK}$ | Input clock frequency (high-speed I/O performance pin) | ×10 | 5 | — | 50 | 5 | — | 50 | 5 | — | 50 | MHz |
| | | ×8 | 5 | — | 50 | 5 | — | 50 | 5 | — | 50 | MHz |
| | | ×7 | 5 | — | 50 | 5 | — | 50 | 5 | — | 50 | MHz |
| | | ×4 | 5 | — | 50 | 5 | — | 50 | 5 | — | 50 | MHz |
| | | ×2 | 5 | — | 50 | 5 | — | 50 | 5 | — | 50 | MHz |
| | | ×1 | 5 | — | 100 | 5 | — | 100 | 5 | — | 100 | MHz |
| HSIODR | Data rate (high-speed I/O performance pin) | ×10 | 100 | — | 100 | 100 | — | 100 | 100 | — | 100 | Mbps |
| | | ×8 | 80 | — | 100 | 80 | — | 100 | 80 | — | 100 | Mbps |
| | | ×7 | 70 | — | 100 | 70 | — | 100 | 70 | — | 100 | Mbps |
| | | ×4 | 40 | — | 100 | 40 | — | 100 | 40 | — | 100 | Mbps |
| | | ×2 | 20 | — | 100 | 20 | — | 100 | 20 | — | 100 | Mbps |
| | | ×1 | 10 | — | 100 | 10 | — | 100 | 10 | — | 100 | Mbps |
| $f_{HSCLK}$ | Input clock frequency (low-speed I/O performance pin) | ×10 | 5 | — | 50 | 5 | — | 50 | 5 | — | 50 | MHz |
| | | ×8 | 5 | — | 50 | 5 | — | 50 | 5 | — | 50 | MHz |
| | | ×7 | 5 | — | 50 | 5 | — | 50 | 5 | — | 50 | MHz |
| | | ×4 | 5 | — | 50 | 5 | — | 50 | 5 | — | 50 | MHz |
| | | ×2 | 5 | — | 50 | 5 | — | 50 | 5 | — | 50 | MHz |
| | | ×1 | 5 | — | 100 | 5 | — | 100 | 5 | — | 100 | MHz |
| HSIODR | Data rate (low-speed I/O performance pin) | ×10 | 100 | — | 100 | 100 | — | 100 | 100 | — | 100 | Mbps |

*continued...*

| Symbol | Parameter | Mode | –I6, –A6, –C7, –I7 | | | –A7 | | | –C8 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| | | ×8 | 80 | — | 100 | 80 | — | 100 | 80 | — | 100 | Mbps |
| | | ×7 | 70 | — | 100 | 70 | — | 100 | 70 | — | 100 | Mbps |
| | | ×4 | 40 | — | 100 | 40 | — | 100 | 40 | — | 100 | Mbps |
| | | ×2 | 20 | — | 100 | 20 | — | 100 | 20 | — | 100 | Mbps |
| | | ×1 | 10 | — | 100 | 10 | — | 100 | 10 | — | 100 | Mbps |
| $t_{DUTY}$ | Duty cycle on transmitter output clock | — | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | % |
| TCCS[56] | Transmitter channel-to-channel skew | — | — | — | 300 | — | — | 300 | — | — | 300 | ps |
| $t_{x\ Jitter}$[57] | Output jitter (high-speed I/O performance pin) | — | — | — | 425 | — | — | 425 | — | — | 425 | ps |
| | Output jitter (low-speed I/O performance pin) | — | — | — | 470 | — | — | 470 | — | — | 470 | ps |
| $t_{RISE}$ | Rise time | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{FALL}$ | Fall time | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{LOCK}$ | Time required for the PLL to lock, after `CONF_DONE` signal goes high, indicating the completion of device configuration | — | — | — | 1 | — | — | 1 | — | — | 1 | ms |

(56) TCCS specifications apply to I/O banks from the same side only.

(57) TX jitter is the jitter induced from core noise and I/O switching noise.

## Dual Supply Devices True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications

### Table 38. True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices

True **RSDS** transmitter is only supported at bottom I/O banks. Emulated **RSDS** transmitter is supported at the output pin of all I/O banks.

| Symbol | Parameter | Mode | –I6, –A6, –C7, –I7 | | | –A7 | | | –C8 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSCLK}$ | Input clock frequency (high-speed I/O performance pin) | ×10 | 5 | — | 155 | 5 | — | 155 | 5 | — | 155 | MHz |
| | | ×8 | 5 | — | 155 | 5 | — | 155 | 5 | — | 155 | MHz |
| | | ×7 | 5 | — | 155 | 5 | — | 155 | 5 | — | 155 | MHz |
| | | ×4 | 5 | — | 155 | 5 | — | 155 | 5 | — | 155 | MHz |
| | | ×2 | 5 | — | 155 | 5 | — | 155 | 5 | — | 155 | MHz |
| | | ×1 | 5 | — | 310 | 5 | — | 310 | 5 | — | 310 | MHz |
| HSIODR | Data rate (high-speed I/O performance pin) | ×10 | 100 | — | 310 | 100 | — | 310 | 100 | — | 310 | Mbps |
| | | ×8 | 80 | — | 310 | 80 | — | 310 | 80 | — | 310 | Mbps |
| | | ×7 | 70 | — | 310 | 70 | — | 310 | 70 | — | 310 | Mbps |
| | | ×4 | 40 | — | 310 | 40 | — | 310 | 40 | — | 310 | Mbps |
| | | ×2 | 20 | — | 310 | 20 | — | 310 | 20 | — | 310 | Mbps |
| | | ×1 | 10 | — | 310 | 10 | — | 310 | 10 | — | 310 | Mbps |
| $f_{HSCLK}$ | Input clock frequency (low-speed I/O performance pin) | ×10 | 5 | — | 150 | 5 | — | 150 | 5 | — | 150 | MHz |
| | | ×8 | 5 | — | 150 | 5 | — | 150 | 5 | — | 150 | MHz |
| | | ×7 | 5 | — | 150 | 5 | — | 150 | 5 | — | 150 | MHz |
| | | ×4 | 5 | — | 150 | 5 | — | 150 | 5 | — | 150 | MHz |
| | | ×2 | 5 | — | 150 | 5 | — | 150 | 5 | — | 150 | MHz |
| | | ×1 | 5 | — | 300 | 5 | — | 300 | 5 | — | 300 | MHz |
| HSIODR | Data rate (low-speed I/O performance pin) | ×10 | 100 | — | 300 | 100 | — | 300 | 100 | — | 300 | Mbps |
| | | ×8 | 80 | — | 300 | 80 | — | 300 | 80 | — | 300 | Mbps |
| | | ×7 | 70 | — | 300 | 70 | — | 300 | 70 | — | 300 | Mbps |

*continued...*

| Symbol | Parameter | Mode | –I6, –A6, –C7, –I7 | | | –A7 | | | –C8 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| | | ×4 | 40 | — | 300 | 40 | — | 300 | 40 | — | 300 | Mbps |
| | | ×2 | 20 | — | 300 | 20 | — | 300 | 20 | — | 300 | Mbps |
| | | ×1 | 10 | — | 300 | 10 | — | 300 | 10 | — | 300 | Mbps |
| $t_{DUTY}$ | Duty cycle on transmitter output clock | — | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | % |
| TCCS[58] | Transmitter channel-to-channel skew | — | — | — | 300 | — | — | 300 | — | — | 300 | ps |
| $t_{x\ Jitter}$[59] | Output jitter (high-speed I/O performance pin) | — | — | — | 425 | — | — | 425 | — | — | 425 | ps |
| | Output jitter (low-speed I/O performance pin) | — | — | — | 470 | — | — | 470 | — | — | 470 | ps |
| $t_{RISE}$ | Rise time | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{FALL}$ | Fall time | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{LOCK}$ | Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration | — | — | — | 1 | — | — | 1 | — | — | 1 | ms |

(58) TCCS specifications apply to I/O banks from the same side only.

(59) TX jitter is the jitter induced from core noise and I/O switching noise.

## Emulated RSDS_E_1R Transmitter Timing Specifications

### Table 39. Emulated RSDS_E_1R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices

Emulated **RSDS_E_1R** transmitter is supported at the output pin of all I/O banks.

| Symbol | Parameter | Mode | –I6, –A6, –C7, –I7 | | | –A7 | | | –C8 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSCLK}$ | Input clock frequency (high-speed I/O performance pin) | ×10 | 5 | — | 85 | 5 | — | 85 | 5 | — | 85 | MHz |
| | | ×8 | 5 | — | 85 | 5 | — | 85 | 5 | — | 85 | MHz |
| | | ×7 | 5 | — | 85 | 5 | — | 85 | 5 | — | 85 | MHz |
| | | ×4 | 5 | — | 85 | 5 | — | 85 | 5 | — | 85 | MHz |
| | | ×2 | 5 | — | 85 | 5 | — | 85 | 5 | — | 85 | MHz |
| | | ×1 | 5 | — | 170 | 5 | — | 170 | 5 | — | 170 | MHz |
| HSIODR | Data rate (high-speed I/O performance pin) | ×10 | 100 | — | 170 | 100 | — | 170 | 100 | — | 170 | Mbps |
| | | ×8 | 80 | — | 170 | 80 | — | 170 | 80 | — | 170 | Mbps |
| | | ×7 | 70 | — | 170 | 70 | — | 170 | 70 | — | 170 | Mbps |
| | | ×4 | 40 | — | 170 | 40 | — | 170 | 40 | — | 170 | Mbps |
| | | ×2 | 20 | — | 170 | 20 | — | 170 | 20 | — | 170 | Mbps |
| | | ×1 | 10 | — | 170 | 10 | — | 170 | 10 | — | 170 | Mbps |
| $f_{HSCLK}$ | Input clock frequency (low-speed I/O performance pin) | ×10 | 5 | — | 85 | 5 | — | 85 | 5 | — | 85 | MHz |
| | | ×8 | 5 | — | 85 | 5 | — | 85 | 5 | — | 85 | MHz |
| | | ×7 | 5 | — | 85 | 5 | — | 85 | 5 | — | 85 | MHz |
| | | ×4 | 5 | — | 85 | 5 | — | 85 | 5 | — | 85 | MHz |
| | | ×2 | 5 | — | 85 | 5 | — | 85 | 5 | — | 85 | MHz |
| | | ×1 | 5 | — | 170 | 5 | — | 170 | 5 | — | 170 | MHz |
| HSIODR | Data rate (low-speed I/O performance pin) | ×10 | 100 | — | 170 | 100 | — | 170 | 100 | — | 170 | Mbps |
| | | ×8 | 80 | — | 170 | 80 | — | 170 | 80 | — | 170 | Mbps |
| | | ×7 | 70 | — | 170 | 70 | — | 170 | 70 | — | 170 | Mbps |

*continued...*

| Symbol | Parameter | Mode | –I6, –A6, –C7, –I7 | | | –A7 | | | –C8 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| | | ×4 | 40 | — | 170 | 40 | — | 170 | 40 | — | 170 | Mbps |
| | | ×2 | 20 | — | 170 | 20 | — | 170 | 20 | — | 170 | Mbps |
| | | ×1 | 10 | — | 170 | 10 | — | 170 | 10 | — | 170 | Mbps |
| $t_{DUTY}$ | Duty cycle on transmitter output clock | — | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | % |
| TCCS[60] | Transmitter channel-to-channel skew | — | — | — | 300 | — | — | 300 | — | — | 300 | ps |
| $t_{x\ Jitter}$[61] | Output jitter (high-speed I/O performance pin) | — | — | — | 425 | — | — | 425 | — | — | 425 | ps |
| | Output jitter (low-speed I/O performance pin) | — | — | — | 470 | — | — | 470 | — | — | 470 | ps |
| $t_{RISE}$ | Rise time | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{FALL}$ | Fall time | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{LOCK}$ | Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration | — | — | — | 1 | — | — | 1 | — | — | 1 | ms |

(60) TCCS specifications apply to I/O banks from the same side only.

(61) TX jitter is the jitter induced from core noise and I/O switching noise.

## True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications

### Table 40. True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices

True **mini-LVDS** transmitter is only supported at the bottom I/O banks. Emulated **mini-LVDS_E_3R** transmitter is supported at the output pin of all I/O banks.

| Symbol | Parameter | Mode | –I6, –A6, –C7, –I7 | | | –A7 | | | –C8 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSCLK}$ | Input clock frequency (high-speed I/O performance pin) | ×10 | 5 | — | 155 | 5 | — | 155 | 5 | — | 155 | MHz |
| | | ×8 | 5 | — | 155 | 5 | — | 155 | 5 | — | 155 | MHz |
| | | ×7 | 5 | — | 155 | 5 | — | 155 | 5 | — | 155 | MHz |
| | | ×4 | 5 | — | 155 | 5 | — | 155 | 5 | — | 155 | MHz |
| | | ×2 | 5 | — | 155 | 5 | — | 155 | 5 | — | 155 | MHz |
| | | ×1 | 5 | — | 310 | 5 | — | 310 | 5 | — | 310 | MHz |
| HSIODR | Data rate (high-speed I/O performance pin) | ×10 | 100 | — | 310 | 100 | — | 310 | 100 | — | 310 | Mbps |
| | | ×8 | 80 | — | 310 | 80 | — | 310 | 80 | — | 310 | Mbps |
| | | ×7 | 70 | — | 310 | 70 | — | 310 | 70 | — | 310 | Mbps |
| | | ×4 | 40 | — | 310 | 40 | — | 310 | 40 | — | 310 | Mbps |
| | | ×2 | 20 | — | 310 | 20 | — | 310 | 20 | — | 310 | Mbps |
| | | ×1 | 10 | — | 310 | 10 | — | 310 | 10 | — | 310 | Mbps |
| $f_{HSCLK}$ | Input clock frequency (low-speed I/O performance pin) | ×10 | 5 | — | 150 | 5 | — | 150 | 5 | — | 150 | MHz |
| | | ×8 | 5 | — | 150 | 5 | — | 150 | 5 | — | 150 | MHz |
| | | ×7 | 5 | — | 150 | 5 | — | 150 | 5 | — | 150 | MHz |
| | | ×4 | 5 | — | 150 | 5 | — | 150 | 5 | — | 150 | MHz |
| | | ×2 | 5 | — | 150 | 5 | — | 150 | 5 | — | 150 | MHz |
| | | ×1 | 5 | — | 300 | 5 | — | 300 | 5 | — | 300 | MHz |
| HSIODR | Data rate (low-speed I/O performance pin) | ×10 | 100 | — | 300 | 100 | — | 300 | 100 | — | 300 | Mbps |
| | | ×8 | 80 | — | 300 | 80 | — | 300 | 80 | — | 300 | Mbps |

*continued...*

| Symbol | Parameter | Mode | –I6, –A6, –C7, –I7 | | | –A7 | | | –C8 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| | | ×7 | 70 | — | 300 | 70 | — | 300 | 70 | — | 300 | Mbps |
| | | ×4 | 40 | — | 300 | 40 | — | 300 | 40 | — | 300 | Mbps |
| | | ×2 | 20 | — | 300 | 20 | — | 300 | 20 | — | 300 | Mbps |
| | | ×1 | 10 | — | 300 | 10 | — | 300 | 10 | — | 300 | Mbps |
| $t_{DUTY}$ | Duty cycle on transmitter output clock | — | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | % |
| TCCS(62) | Transmitter channel-to-channel skew | — | — | — | 300 | — | — | 300 | — | — | 300 | ps |
| $t_{x\ Jitter}$(63) | Output jitter (high-speed I/O performance pin) | — | — | — | 425 | — | — | 425 | — | — | 425 | ps |
| | Output jitter (low-speed I/O performance pin) | — | — | — | 470 | — | — | 470 | — | — | 470 | ps |
| $t_{RISE}$ | Rise time | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{FALL}$ | Fall time | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{LOCK}$ | Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration | — | — | — | 1 | — | — | 1 | — | — | 1 | ms |

(62) TCCS specifications apply to I/O banks from the same side only.

(63) TX jitter is the jitter induced from core noise and I/O switching noise.

## True LVDS Transmitter Timing

### Single Supply Devices True LVDS Transmitter Timing Specifications

### Table 41. True LVDS Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices

True **LVDS** transmitter is only supported at the bottom I/O banks.

| Symbol | Parameter | Mode | –C7, –I7 | | | –A7 | | | –C8 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSCLK}$ | Input clock frequency | ×10 | 5 | — | 145 | 5 | — | 100 | 5 | — | 100 | MHz |
| | | ×8 | 5 | — | 145 | 5 | — | 100 | 5 | — | 100 | MHz |
| | | ×7 | 5 | — | 145 | 5 | — | 100 | 5 | — | 100 | MHz |
| | | ×4 | 5 | — | 145 | 5 | — | 100 | 5 | — | 100 | MHz |
| | | ×2 | 5 | — | 145 | 5 | — | 100 | 5 | — | 100 | MHz |
| | | ×1 | 5 | — | 290 | 5 | — | 200 | 5 | — | 200 | MHz |
| HSIODR | Data rate | ×10 | 100 | — | 290 | 100 | — | 200 | 100 | — | 200 | Mbps |
| | | ×8 | 80 | — | 290 | 80 | — | 200 | 80 | — | 200 | Mbps |
| | | ×7 | 70 | — | 290 | 70 | — | 200 | 70 | — | 200 | Mbps |
| | | ×4 | 40 | — | 290 | 40 | — | 200 | 40 | — | 200 | Mbps |
| | | ×2 | 20 | — | 290 | 20 | — | 200 | 20 | — | 200 | Mbps |
| | | ×1 | 10 | — | 290 | 10 | — | 200 | 10 | — | 200 | Mbps |
| $t_{DUTY}$ | Duty cycle on transmitter output clock | — | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | % |
| TCCS[64] | Transmitter channel-to-channel skew | — | — | — | 300 | — | — | 300 | — | — | 300 | ps |
| $t_{x\ Jitter}$[65] | Output jitter | — | — | — | 1,000 | — | — | 1,000 | — | — | 1,000 | ps |

*continued...*

(64) TCCS specifications apply to I/O banks from the same side only.

(65) TX jitter is the jitter induced from core noise and I/O switching noise.

| Symbol | Parameter | Mode | –C7, –I7 | | | –A7 | | | –C8 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $t_{RISE}$ | Rise time | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{FALL}$ | Fall time | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{LOCK}$ | Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration | — | — | — | 1 | — | — | 1 | — | — | 1 | ms |

## Dual Supply Devices True LVDS Transmitter Timing Specifications

### Table 42. True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices

True **LVDS** transmitter is only supported at the bottom I/O banks.

| Symbol | Parameter | Mode | –I6 | | | –A6, –C7, –I7 | | | –A7 | | | –C8 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSCLK}$ | Input clock frequency | ×10 | 5 | — | 360 | 5 | — | 340 | 5 | — | 310 | 5 | — | 300 | MHz |
| | | ×8 | 5 | — | 360 | 5 | — | 360 | 5 | — | 320 | 5 | — | 320 | MHz |
| | | ×7 | 5 | — | 360 | 5 | — | 340 | 5 | — | 310 | 5 | — | 300 | MHz |
| | | ×4 | 5 | — | 360 | 5 | — | 350 | 5 | — | 320 | 5 | — | 320 | MHz |
| | | ×2 | 5 | — | 360 | 5 | — | 350 | 5 | — | 320 | 5 | — | 320 | MHz |
| | | ×1 | 5 | — | 360 | 5 | — | 350 | 5 | — | 320 | 5 | — | 320 | MHz |
| HSIODR | Data rate | ×10 | 100 | — | 720 | 100 | — | 680 | 100 | — | 620 | 100 | — | 600 | Mbps |
| | | ×8 | 80 | — | 720 | 80 | — | 720 | 80 | — | 640 | 80 | — | 640 | Mbps |
| | | ×7 | 70 | — | 720 | 70 | — | 680 | 70 | — | 620 | 70 | — | 600 | Mbps |
| | | ×4 | 40 | — | 720 | 40 | — | 700 | 40 | — | 640 | 40 | — | 640 | Mbps |
| | | ×2 | 20 | — | 720 | 20 | — | 700 | 20 | — | 640 | 20 | — | 640 | Mbps |

*continued...*

| Symbol | Parameter | Mode | –I6 | | | –A6, –C7, –I7 | | | –A7 | | | –C8 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| | | ×1 | 10 | — | 360 | 10 | — | 350 | 10 | — | 320 | 10 | — | 320 | Mbps |
| $t_{DUTY}$ | Duty cycle on transmitter output clock | — | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | % |
| TCCS(66) | Transmitter channel-to-channel skew | — | — | — | 300 | — | — | 300 | — | — | 300 | — | — | 300 | ps |
| $t_{x\ Jitter}$(67) | Output jitter | — | — | — | 380 | — | — | 380 | — | — | 380 | — | — | 380 | ps |
| $t_{RISE}$ | Rise time | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{FALL}$ | Fall time | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{LOCK}$ | Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration | — | — | — | 1 | — | — | 1 | — | — | 1 | — | — | 1 | ms |

(66) TCCS specifications apply to I/O banks from the same side only.

(67) TX jitter is the jitter induced from core noise and I/O switching noise.

## Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications

### Single Supply Devices Emulated LVDS_E_3R Transmitter Timing Specifications

**Table 43. Emulated LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices**

Emulated **LVDS_E_3R** transmitters are supported at the output pin of all I/O banks.

| Symbol | Parameter | Mode | –C7, –I7 | | | –A7 | | | –C8 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSCLK}$ | Input clock frequency (high-speed I/O performance pin) | ×10 | 5 | — | 142.5 | 5 | — | 100 | 5 | — | 100 | MHz |
| | | ×8 | 5 | — | 142.5 | 5 | — | 100 | 5 | — | 100 | MHz |
| | | ×7 | 5 | — | 142.5 | 5 | — | 100 | 5 | — | 100 | MHz |
| | | ×4 | 5 | — | 142.5 | 5 | — | 100 | 5 | — | 100 | MHz |
| | | ×2 | 5 | — | 142.5 | 5 | — | 100 | 5 | — | 100 | MHz |
| | | ×1 | 5 | — | 285 | 5 | — | 200 | 5 | — | 200 | MHz |
| HSIODR | Data rate (high-speed I/O performance pin) | ×10 | 100 | — | 285 | 100 | — | 200 | 100 | — | 200 | Mbps |
| | | ×8 | 80 | — | 285 | 80 | — | 200 | 80 | — | 200 | Mbps |
| | | ×7 | 70 | — | 285 | 70 | — | 200 | 70 | — | 200 | Mbps |
| | | ×4 | 40 | — | 285 | 40 | — | 200 | 40 | — | 200 | Mbps |
| | | ×2 | 20 | — | 285 | 20 | — | 200 | 20 | — | 200 | Mbps |
| | | ×1 | 10 | — | 285 | 10 | — | 200 | 10 | — | 200 | Mbps |
| $f_{HSCLK}$ | Input clock frequency (low-speed I/O performance pin) | ×10 | 5 | — | 100 | 5 | — | 100 | 5 | — | 100 | MHz |
| | | ×8 | 5 | — | 100 | 5 | — | 100 | 5 | — | 100 | MHz |
| | | ×7 | 5 | — | 100 | 5 | — | 100 | 5 | — | 100 | MHz |
| | | ×4 | 5 | — | 100 | 5 | — | 100 | 5 | — | 100 | MHz |
| | | ×2 | 5 | — | 100 | 5 | — | 100 | 5 | — | 100 | MHz |
| | | ×1 | 5 | — | 200 | 5 | — | 200 | 5 | — | 200 | MHz |
| HSIODR | Data rate (low-speed I/O performance pin) | ×10 | 100 | — | 200 | 100 | — | 200 | 100 | — | 200 | Mbps |

*continued...*

| Symbol | Parameter | Mode | –C7, –I7 | | | –A7 | | | –C8 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| | | ×8 | 80 | — | 200 | 80 | — | 200 | 80 | — | 200 | Mbps |
| | | ×7 | 70 | — | 200 | 70 | — | 200 | 70 | — | 200 | Mbps |
| | | ×4 | 40 | — | 200 | 40 | — | 200 | 40 | — | 200 | Mbps |
| | | ×2 | 20 | — | 200 | 20 | — | 200 | 20 | — | 200 | Mbps |
| | | ×1 | 10 | — | 200 | 10 | — | 200 | 10 | — | 200 | Mbps |
| $t_{DUTY}$ | Duty cycle on transmitter output clock | — | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | % |
| TCCS[68] | Transmitter channel-to-channel skew | — | — | — | 300 | — | — | 300 | — | — | 300 | ps |
| $t_{x\ Jitter}$[69] | Output jitter | — | — | — | 1,000 | — | — | 1,000 | — | — | 1,000 | ps |
| $t_{RISE}$ | Rise time | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{FALL}$ | Fall time | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{LOCK}$ | Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration | — | — | — | 1 | — | — | 1 | — | — | 1 | ms |

(68) TCCS specifications apply to I/O banks from the same side only.

(69) TX jitter is the jitter induced from core noise and I/O switching noise.

## Dual Supply Devices Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications

### Table 44. Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices

Emulated **LVDS_E_3R**, **SLVS**, and **Sub-LVDS** transmitters are supported at the output pin of all I/O banks.

| Symbol | Parameter | Mode | –I6, –A6, –C7, –I7 | | | –A7 | | | –C8 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSCLK}$ | Input clock frequency (high-speed I/O performance pin) | ×10 | 5 | — | 300 | 5 | — | 275 | 5 | — | 275 | MHz |
| | | ×8 | 5 | — | 300 | 5 | — | 275 | 5 | — | 275 | MHz |
| | | ×7 | 5 | — | 300 | 5 | — | 275 | 5 | — | 275 | MHz |
| | | ×4 | 5 | — | 300 | 5 | — | 275 | 5 | — | 275 | MHz |
| | | ×2 | 5 | — | 300 | 5 | — | 275 | 5 | — | 275 | MHz |
| | | ×1 | 5 | — | 300 | 5 | — | 275 | 5 | — | 275 | MHz |
| HSIODR | Data rate (high-speed I/O performance pin) | ×10 | 100 | — | 600 | 100 | — | 550 | 100 | — | 550 | Mbps |
| | | ×8 | 80 | — | 600 | 80 | — | 550 | 80 | — | 550 | Mbps |
| | | ×7 | 70 | — | 600 | 70 | — | 550 | 70 | — | 550 | Mbps |
| | | ×4 | 40 | — | 600 | 40 | — | 550 | 40 | — | 550 | Mbps |
| | | ×2 | 20 | — | 600 | 20 | — | 550 | 20 | — | 550 | Mbps |
| | | ×1 | 10 | — | 300 | 10 | — | 275 | 10 | — | 275 | Mbps |
| $f_{HSCLK}$ | Input clock frequency (low-speed I/O performance pin) | ×10 | 5 | — | 150 | 5 | — | 150 | 5 | — | 150 | MHz |
| | | ×8 | 5 | — | 150 | 5 | — | 150 | 5 | — | 150 | MHz |
| | | ×7 | 5 | — | 150 | 5 | — | 150 | 5 | — | 150 | MHz |
| | | ×4 | 5 | — | 150 | 5 | — | 150 | 5 | — | 150 | MHz |
| | | ×2 | 5 | — | 150 | 5 | — | 150 | 5 | — | 150 | MHz |
| | | ×1 | 5 | — | 300 | 5 | — | 300 | 5 | — | 300 | MHz |
| HSIODR | Data rate (low-speed I/O performance pin) | ×10 | 100 | — | 300 | 100 | — | 300 | 100 | — | 300 | Mbps |
| | | ×8 | 80 | — | 300 | 80 | — | 300 | 80 | — | 300 | Mbps |

*continued...*

| Symbol | Parameter | Mode | –I6, –A6, –C7, –I7 | | | –A7 | | | –C8 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| | | ×7 | 70 | — | 300 | 70 | — | 300 | 70 | — | 300 | Mbps |
| | | ×4 | 40 | — | 300 | 40 | — | 300 | 40 | — | 300 | Mbps |
| | | ×2 | 20 | — | 300 | 20 | — | 300 | 20 | — | 300 | Mbps |
| | | ×1 | 10 | — | 300 | 10 | — | 300 | 10 | — | 300 | Mbps |
| $t_{DUTY}$ | Duty cycle on transmitter output clock | — | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | % |
| TCCS[70] | Transmitter channel-to-channel skew | — | — | — | 300 | — | — | 300 | — | — | 300 | ps |
| $t_{x\ Jitter}$[71] | Output jitter (high-speed I/O performance pin) | — | — | — | 425 | — | — | 425 | — | — | 425 | ps |
| | Output jitter (low-speed I/O performance pin) | — | — | — | 470 | — | — | 470 | — | — | 470 | ps |
| $t_{RISE}$ | Rise time | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{FALL}$ | Fall time | 20 – 80%, $C_{LOAD}$ = 5 pF | — | 500 | — | — | 500 | — | — | 500 | — | ps |
| $t_{LOCK}$ | Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration | — | — | — | 1 | — | — | 1 | — | — | 1 | ms |

(70) TCCS specifications apply to I/O banks from the same side only.

(71) TX jitter is the jitter induced from core noise and I/O switching noise.

## LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications

### Single Supply Devices LVDS Receiver Timing Specifications

### Table 45. LVDS Receiver Timing Specifications for Intel MAX 10 Single Supply Devices

**LVDS** receivers are supported at all banks.

| Symbol | Parameter | Mode | –C7, –I7 | | –A7 | | –C8 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| $f_{HSCLK}$ | Input clock frequency (high-speed I/O performance pin) | ×10 | 5 | 145 | 5 | 100 | 5 | 100 | MHz |
| | | ×8 | 5 | 145 | 5 | 100 | 5 | 100 | MHz |
| | | ×7 | 5 | 145 | 5 | 100 | 5 | 100 | MHz |
| | | ×4 | 5 | 145 | 5 | 100 | 5 | 100 | MHz |
| | | ×2 | 5 | 145 | 5 | 100 | 5 | 100 | MHz |
| | | ×1 | 5 | 290 | 5 | 200 | 5 | 200 | MHz |
| HSIODR | Data rate (high-speed I/O performance pin) | ×10 | 100 | 290 | 100 | 200 | 100 | 200 | Mbps |
| | | ×8 | 80 | 290 | 80 | 200 | 80 | 200 | Mbps |
| | | ×7 | 70 | 290 | 70 | 200 | 70 | 200 | Mbps |
| | | ×4 | 40 | 290 | 40 | 200 | 40 | 200 | Mbps |
| | | ×2 | 20 | 290 | 20 | 200 | 20 | 200 | Mbps |
| | | ×1 | 10 | 290 | 10 | 200 | 10 | 200 | Mbps |
| $f_{HSCLK}$ | Input clock frequency (low-speed I/O performance pin) | ×10 | 5 | 100 | 5 | 100 | 5 | 100 | MHz |
| | | ×8 | 5 | 100 | 5 | 100 | 5 | 100 | MHz |
| | | ×7 | 5 | 100 | 5 | 100 | 5 | 100 | MHz |
| | | ×4 | 5 | 100 | 5 | 100 | 5 | 100 | MHz |
| | | ×2 | 5 | 100 | 5 | 100 | 5 | 100 | MHz |
| | | ×1 | 5 | 200 | 5 | 200 | 5 | 200 | MHz |
| HSIODR | Data rate (low-speed I/O performance pin) | ×10 | 100 | 200 | 100 | 200 | 100 | 200 | Mbps |

*continued...*

| Symbol | Parameter | Mode | –C7, –I7 | | –A7 | | –C8 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| | | ×8 | 80 | 200 | 80 | 200 | 80 | 200 | Mbps |
| | | ×7 | 70 | 200 | 70 | 200 | 70 | 200 | Mbps |
| | | ×4 | 40 | 200 | 40 | 200 | 40 | 200 | Mbps |
| | | ×2 | 20 | 200 | 20 | 200 | 20 | 200 | Mbps |
| | | ×1 | 10 | 200 | 10 | 200 | 10 | 200 | Mbps |
| SW | Sampling window (high-speed I/O performance pin) | — | — | 910 | — | 910 | — | 910 | ps |
| | Sampling window (low-speed I/O performance pin) | — | — | 1,110 | — | 1,110 | — | 1,110 | ps |
| $t_{x\ Jitter}$(72) | Input jitter | — | — | 1,000 | — | 1,000 | — | 1,000 | ps |
| $t_{LOCK}$ | Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration | — | — | 1 | — | 1 | — | 1 | ms |

## Dual Supply Devices LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications

### Table 46. LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices

**LVDS**, **TMDS**, **HiSpi**, **SLVS**, and **Sub-LVDS** receivers are supported at all banks.

| Symbol | Parameter | Mode | –I6, –A6, –C7, –I7 | | –A7 | | –C8 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| $f_{HSCLK}$ | Input clock frequency (high-speed I/O performance pin) | ×10 | 5 | 350 | 5 | 320 | 5 | 320 | MHz |
| | | ×8 | 5 | 360 | 5 | 320 | 5 | 320 | MHz |
| | | ×7 | 5 | 350 | 5 | 320 | 5 | 320 | MHz |
| | | ×4 | 5 | 360 | 5 | 320 | 5 | 320 | MHz |

*continued...*

(72) TX jitter is the jitter induced from core noise and I/O switching noise.

| Symbol | Parameter | Mode | –I6, –A6, –C7, –I7 | | –A7 | | –C8 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| | | ×2 | 5 | 360 | 5 | 320 | 5 | 320 | MHz |
| | | ×1 | 5 | 360 | 5 | 320 | 5 | 320 | MHz |
| HSIODR | Data rate (high-speed I/O performance pin) | ×10 | 100 | 700 | 100 | 640 | 100 | 640 | Mbps |
| | | ×8 | 80 | 720 | 80 | 640 | 80 | 640 | Mbps |
| | | ×7 | 70 | 700 | 70 | 640 | 70 | 640 | Mbps |
| | | ×4 | 40 | 720 | 40 | 640 | 40 | 640 | Mbps |
| | | ×2 | 20 | 720 | 20 | 640 | 20 | 640 | Mbps |
| | | ×1 | 10 | 360 | 10 | 320 | 10 | 320 | Mbps |
| $f_{HSCLK}$ | Input clock frequency (low-speed I/O performance pin) | ×10 | 5 | 150 | 5 | 150 | 5 | 150 | MHz |
| | | ×8 | 5 | 150 | 5 | 150 | 5 | 150 | MHz |
| | | ×7 | 5 | 150 | 5 | 150 | 5 | 150 | MHz |
| | | ×4 | 5 | 150 | 5 | 150 | 5 | 150 | MHz |
| | | ×2 | 5 | 150 | 5 | 150 | 5 | 150 | MHz |
| | | ×1 | 5 | 300 | 5 | 300 | 5 | 300 | MHz |
| HSIODR | Data rate (low-speed I/O performance pin) | ×10 | 100 | 300 | 100 | 300 | 100 | 300 | Mbps |
| | | ×8 | 80 | 300 | 80 | 300 | 80 | 300 | Mbps |
| | | ×7 | 70 | 300 | 70 | 300 | 70 | 300 | Mbps |
| | | ×4 | 40 | 300 | 40 | 300 | 40 | 300 | Mbps |
| | | ×2 | 20 | 300 | 20 | 300 | 20 | 300 | Mbps |
| | | ×1 | 10 | 300 | 10 | 300 | 10 | 300 | Mbps |
| SW | Sampling window (high-speed I/O performance pin) | — | — | 510 | — | 510 | — | 510 | ps |

*continued...*

| Symbol | Parameter | Mode | –I6, –A6, –C7, –I7 | | –A7 | | –C8 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| | Sampling window (low-speed I/O performance pin) | — | — | 910 | — | 910 | — | 910 | ps |
| $t_{x\ Jitter}$[73] | Input jitter | — | — | 500 | — | 500 | — | 500 | ps |
| $t_{LOCK}$ | Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration | — | — | 1 | — | 1 | — | 1 | ms |

## Memory Standards Supported by the Soft Memory Controller

### Table 47. Memory Standards Supported by the Soft Memory Controller for Intel MAX 10 Devices

Contact your local sales representatives for access to the -I6 or -A6 speed grade devices in the Intel Quartus Prime software.

| External Memory Interface Standard | Rate Support | Speed Grade | Voltage (V) | Max Frequency (MHz) |
|---|---|---|---|---|
| DDR3 SDRAM | Half | –I6 | 1.5 | 303 |
| DDR3L SDRAM | Half | –I6 | 1.35 | 303 |
| DDR2 SDRAM | Half | –I6 | 1.8 | 200 |
| | | –I7 and –C7 | | 167 |
| LPDDR2[74] | Half | –I6 | 1.2 | 200[75] |

#### Related Information

External Memory Interface Spec Estimator
Provides the specific details of the memory standards supported.

(73) TX jitter is the jitter induced from core noise and I/O switching noise.

(74) Intel MAX 10 devices support only single-die LPDDR2.

(75) To achieve the specified performance, constrain the memory device I/O and core power supply variation to within ±3%. By default, the frequency is 167 MHz.

## Memory Output Clock Jitter Specifications

Intel MAX 10 devices support external memory interfaces up to 303 MHz. The external memory interfaces for Intel MAX 10 devices calibrate automatically.

The memory output clock jitter measurements are for 200 consecutive clock cycles.

The clock jitter specification applies to memory output clock pins generated using DDIO circuits clocked by a PLL output routed on a PHY clock network.

DDR3 and LPDDR2 SDRAM memory interfaces are only supported on the fast speed grade device.

**Table 48. Memory Output Clock Jitter Specifications for Intel MAX 10 Devices**

| Parameter | Symbol | –6 Speed Grade | | –7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| Clock period jitter | $t_{JIT(per)}$ | –127 | 127 | –215 | 215 | ps |
| Cycle-to-cycle period jitter | $t_{JIT(cc)}$ | — | 242 | — | 360 | ps |

### Related Information

Literature: External Memory Interfaces
Provides more information about external memory system performance specifications, board design guidelines, timing analysis, simulation, and debugging information.

# Configuration Specifications

This section provides configuration specifications and timing for Intel MAX 10 devices.

# JTAG Timing Parameters

## Table 49. JTAG Timing Parameters for Intel MAX 10 Devices

The values are based on $C_L$ = 10 pF of TDO.

The affected Boundary Scan Test (BST) instructions are SAMPLE/PRELOAD, EXTEST, INTEST, and CHECK_STATUS.

| Symbol | Parameter | Non-BST and non-CONFIG_IO Operation | | BST and CONFIG_IO Operation | | Unit |
|---|---|---|---|---|---|---|
| | | Minimum | Maximum | Minimum | Maximum | |
| $t_{JCP}$ | TCK clock period | 40 | — | 50 | — | ns |
| $t_{JCH}$ | TCK clock high time | 20 | — | 25 | — | ns |
| $t_{JCL}$ | TCK clock low time | 20 | — | 25 | — | ns |
| $t_{JPSU_TDI}$ | JTAG port setup time | 2 | — | 2 | — | ns |
| $t_{JPSU_TMS}$ | JTAG port setup time | 3 | — | 3 | — | ns |
| $t_{JPH}$ | JTAG port hold time | 10 | — | 10 | — | ns |
| $t_{JPCO}$ | JTAG port clock to output | — | • 15 (for $V_{CCIO}$ = 3.3, 3.0, and 2.5 V)<br>• 17 (for $V_{CCIO}$ = 1.8 and 1.5 V) | — | • 18 (for $V_{CCIO}$ = 3.3, 3.0, and 2.5 V)<br>• 20 (for $V_{CCIO}$ = 1.8 and 1.5 V) | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output | — | • 15 (for $V_{CCIO}$ = 3.3, 3.0, and 2.5 V)<br>• 17 (for $V_{CCIO}$ = 1.8 and 1.5 V) | — | • 15 (for $V_{CCIO}$ = 3.3, 3.0, and 2.5 V)<br>• 17 (for $V_{CCIO}$ = 1.8 and 1.5 V) | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | — | • 15 (for $V_{CCIO}$ = 3.3, 3.0, and 2.5 V)<br>• 17 (for $V_{CCIO}$ = 1.8 and 1.5 V) | — | • 15 (for $V_{CCIO}$ = 3.3, 3.0, and 2.5 V)<br>• 17 (for $V_{CCIO}$ = 1.8 and 1.5 V) | ns |

## Remote System Upgrade Circuitry Timing Specifications

### Table 50. Remote System Upgrade Circuitry Timing Specifications for Intel MAX 10 Devices

| Parameter | Device | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{MAX_RU_CLK}$ | All | — | 40 | MHz |
| $t_{RU_nCONFIG}$ | 10M02, 10M04, 10M08, 10M16, 10M25 | 250 | — | ns |
| | 10M40, 10M50 | 350 | — | ns |
| $t_{RU_nRSTIMER}$ | 10M02, 10M04, 10M08, 10M16, 10M25 | 300 | — | ns |
| | 10M40, 10M50 | 500 | — | ns |

## User Watchdog Internal Circuitry Timing Specifications

### Table 51. User Watchdog Timer Specifications for Intel MAX 10 Devices

The specifications are subject to PVT changes.

| Parameter | Device | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| User watchdog frequency | 10M02, 10M04, 10M08, 10M16, 10M25 | 3.4 | 5.1 | 7.3 | MHz |
| | 10M40, 10M50 | 2.2 | 3.3 | 4.8 | MHz |

## Uncompressed Raw Binary File (.rbf) Sizes

### Table 52. Uncompressed .rbf Sizes for Intel MAX 10 Devices

| Device | CFM Data Size (bits) | |
|---|---|---|
| | Without Memory Initialization | With Memory Initialization |
| 10M02/10M02SCU324 | 554,000/1,540,000 | — |
| 10M04 | 1,540,000 | 1,880,000 |
| 10M08 | 1,540,000 | 1,880,000 |
| 10M16 | 2,800,000 | 3,430,000 |

*continued...*

| Device | CFM Data Size (bits) | |
|---|---|---|
| | Without Memory Initialization | With Memory Initialization |
| 10M25 | 4,140,000 | 4,780,000 |
| 10M40 | 7,840,000 | 9,670,000 |
| 10M50 | 7,840,000 | 9,670,000 |

## Internal Configuration Time

The internal configuration time measurement is from the rising edge of nSTATUS signal to the rising edge of CONF_DONE signal.

**Table 53. Internal Configuration Time for Intel MAX 10 Devices (Uncompressed .rbf)**

| Device | Internal Configuration Time (ms) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | Unencrypted | | | | Encrypted | | | |
| | Without Memory Initialization | | With Memory Initialization | | Without Memory Initialization | | With Memory Initialization | |
| | Min | Max | Min | Max | Min | Max | Min | Max |
| 10M02/ 10M02SCU324 | 0.3/0.6 | 1.7/2.7 | — | — | 1.7/5.0 | 5.4/15.0 | — | — |
| 10M04 | 0.6 | 2.7 | 1.0 | 3.4 | 5.0 | 15.0 | 6.8 | 19.6 |
| 10M08 | 0.6 | 2.7 | 1.0 | 3.4 | 5.0 | 15.0 | 6.8 | 19.6 |
| 10M16 | 1.1 | 3.7 | 1.4 | 4.5 | 9.3 | 25.3 | 11.7 | 31.5 |
| 10M25 | 1.0 | 3.7 | 1.3 | 4.4 | 14.0 | 38.1 | 16.9 | 45.7 |
| 10M40 | 2.6 | 6.9 | 3.2 | 9.8 | 41.5 | 112.1 | 51.7 | 139.6 |
| 10M50 | 2.6 | 6.9 | 3.2 | 9.8 | 41.5 | 112.1 | 51.7 | 139.6 |

### Table 54. Internal Configuration Time for Intel MAX 10 Devices (Compressed .rbf)

Compression ratio depends on design complexity. The minimum value is based on the best case (25% of original `.rbf` sizes) and the maximum value is based on the typical case (70% of original `.rbf` sizes).

| Device | Internal Configuration Time (ms) | | | |
|---|---|---|---|---|
| | Unencrypted/Encrypted | | | |
| | Without Memory Initialization | | With Memory Initialization | |
| | Min | Max | Min | Max |
| 10M02/10M02SCU324 | 0.3/0.6 | 5.2/10.7 | — | — |
| 10M04 | 0.6 | 10.7 | 1.0 | 13.9 |
| 10M08 | 0.6 | 10.7 | 1.0 | 13.9 |
| 10M16 | 1.1 | 17.9 | 1.4 | 22.3 |
| 10M25 | 1.1 | 26.9 | 1.4 | 32.2 |
| 10M40 | 2.6 | 66.1 | 3.2 | 82.2 |
| 10M50 | 2.6 | 66.1 | 3.2 | 82.2 |

## Internal Configuration Timing Parameter

### Table 55. Internal Configuration Timing Parameter for Intel MAX 10 Devices

| Symbol | Parameter | Device | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| $t_{CD2UM}$ | `CONF_DONE` high to user mode | 10M02, 10M04, 10M08, 10M16, 10M25 | 182.8 | 385.5 | µs |
| | | 10M40, 10M50 | 275.3 | 605.7 | µs |

# I/O Timing

The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

The Intel Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specific device and design after you complete place-and-route.

### Table 56. I/O Timing for Intel MAX 10 Devices

These I/O timing parameters are for the 3.3-V LVTTL I/O standard with the maximum drive strength and fast slew rate for 10M08DAF484 device.

| Symbol | Parameter | –C7, –I7 | –C8 | Unit |
|---|---|---|---|---|
| $T_{su}$ | Global clock setup time | –0.750 | –0.808 | ns |
| $T_h$ | Global clock hold time | 1.180 | 1.215 | ns |
| $T_{co}$ | Global clock to output delay | 5.131 | 5.575 | ns |
| $T_{pd}$ | Best case pin-to-pin propagation delay through one LUT | 4.907 | 5.467 | ns |

# Programmable IOE Delay

## Programmable IOE Delay On Row Pins

### Table 57. IOE Programmable Delay on Row Pins for Intel MAX 10 Devices

The incremental values for the settings are generally linear. For exact values of each setting, refer to the **Assignment Name** column in the latest version of the Intel Quartus Prime software.

The minimum and maximum offset timing numbers are in reference to setting '0' as available in the Intel Quartus Prime software.

| Parameter | Paths Affected | Number of Settings | Minimum Offset | Maximum Offset | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Fast Corner | | Slow Corner | | | | | |
| | | | | –I7 | –C8 | –A6 | –C7 | –C8 | –I7 | –A7 | |
| Input delay from pin to internal cells | Pad to I/O dataout to core | 7 | 0 | 0.815 | 0.873 | 1.831 | 1.811 | 1.874 | 1.871 | 1.922 | ns |
| Input delay from pin to input register | Pad to I/O input register | 8 | 0 | 0.924 | 0.992 | 2.081 | 2.055 | 2.125 | 2.127 | 2.185 | ns |
| Delay from output register to output pin | I/O output register to pad | 2 | 0 | 0.479 | 0.514 | 1.069 | 1.070 | 1.117 | 1.105 | 1.134 | ns |

# Programmable IOE Delay for Column Pins

## Table 58. IOE Programmable Delay on Column Pins for Intel MAX 10 Devices

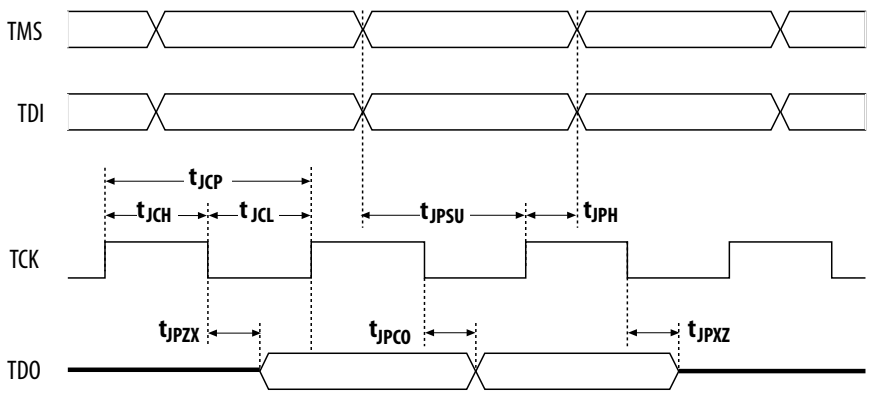
The incremental values for the settings are generally linear. For exact values of each setting, refer to the **Assignment Name** column in the latest version of the Intel Quartus Prime software.

The minimum and maximum offset timing numbers are in reference to setting '0' as available in the Intel Quartus Prime software.

| Parameter | Paths Affected | Number of Settings | Minimum Offset | Maximum Offset | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Fast Corner | | Slow Corner | | | | | |
| | | | | –I7 | –C8 | –A6 | –C7 | –C8 | –I7 | –A7 | |
| Input delay from pin to internal cells | Pad to I/O dataout to core | 7 | 0 | 0.81 | 0.868 | 1.823 | 1.802 | 1.864 | 1.862 | 1.912 | ns |
| Input delay from pin to input register | Pad to I/O input register | 8 | 0 | 0.914 | 0.981 | 2.06 | 2.032 | 2.101 | 2.102 | 2.161 | ns |
| Delay from output register to output pin | I/O output register to pad | 2 | 0 | 0.435 | 0.466 | 0.971 | 0.97 | 1.013 | 1.001 | 1.028 | ns |

# Glossary

## Table 59. Glossary

| Term | Definition |
|---|---|
| JTAG Timing Specifications |  |
| $R_L$ | Receiver differential input discrete resistor (external to Intel MAX 10 devices). |
| RSKM (Receiver input skew margin) | HIGH-SPEED I/O block: The total margin left after accounting for the sampling window and TCCS. RSKM = (TUI – SW – TCCS) / 2. |
| Sampling window (SW) | HIGH-SPEED I/O Block: The period of time during which the data must be valid to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window. |
| Single-ended voltage referenced I/O standard | The AC input signal values indicate the voltage levels at which the receiver must meet its timing specifications. The DC input signal values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input crosses the AC value, the receiver changes to the new logic state.<br>The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing. |
| $t_C$ | High-speed receiver/transmitter input and output clock period. |
| TCCS (Channel-to- channel-skew) | HIGH-SPEED I/O block: The timing difference between the fastest and slowest output edges, including $t_{CO}$ variation and clock skew. The clock is included in the TCCS measurement. |
| $t_{cin}$ | Delay from clock pad to I/O input register. |
| $t_{CO}$ | Delay from clock pad to I/O output. |
| $t_{cout}$ | Delay from clock pad to I/O output register. |

*continued...*

| Term | Definition |
|---|---|
| $t_{DUTY}$ | HIGH-SPEED I/O Block: Duty cycle on high-speed transmitter output clock. |
| $t_{FALL}$ | Signal high-to-low transition time (80–20%). |
| $t_H$ | Input register hold time. |
| Timing Unit Interval (TUI) | HIGH-SPEED I/O block: The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = $t_C$/w). |
| $t_{INJITTER}$ | Period jitter on PLL clock input. |
| $t_{OUTJITTER_DEDCLK}$ | Period jitter on dedicated clock output driven by a PLL. |
| $t_{OUTJITTER_IO}$ | Period jitter on general purpose I/O driven by a PLL. |
| $t_{plicin}$ | Delay from PLL inclk pad to I/O input register. |
| $t_{plicout}$ | Delay from PLL inclk pad to I/O output register. |
| $t_{RISE}$ | Signal low-to-high transition time (20–80%). |
| $t_{SU}$ | Input register setup time. |
| $V_{CM(DC)}$ | DC common mode input voltage. |
| $V_{DIF(AC)}$ | AC differential input voltage: The minimum AC input differential voltage required for switching. |
| $V_{DIF(DC)}$ | DC differential input voltage: The minimum DC input differential voltage required for switching. |
| $V_{HYS}$ | Hysteresis for Schmitt trigger input. |
| $V_{ICM}$ | Input common mode voltage: The common mode of the differential signal at the receiver. |
| $V_{ID}$ | Input differential Voltage Swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver. |
| $V_{IH}$ | Voltage input high: The minimum positive voltage applied to the input which is accepted by the device as a logic high. |
| $V_{IH(AC)}$ | High-level AC input voltage. |
| $V_{IH(DC)}$ | High-level DC input voltage. |
| $V_{IL}$ | Voltage input low: The maximum positive voltage applied to the input which is accepted by the device as a logic low. |
| $V_{IL\ (AC)}$ | Low-level AC input voltage. |
| $V_{IL\ (DC)}$ | Low-level DC input voltage. |
| $V_{IN}$ | DC input voltage. |

***continued...***

| Term | Definition |
|---|---|
| $V_{OCM}$ | Output common mode voltage: The common mode of the differential signal at the transmitter. |
| $V_{OD}$ | Output differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission line at the transmitter. $V_{OD} = V_{OH} – V_{OL}$. |
| $V_{OH}$ | Voltage output high: The maximum positive voltage from an output which the device considers is accepted as the minimum positive high level. |
| $V_{OL}$ | Voltage output low: The maximum positive voltage from an output which the device considers is accepted as the maximum positive low level. |
| $V_{OS}$ | Output offset voltage: $V_{OS} = (V_{OH} + V_{OL}) / 2$. |
| $V_{OX\ (AC)}$ | AC differential Output cross point voltage: The voltage at which the differential output signals must cross. |
| $V_{REF}$ | Reference voltage for SSTL, HSTL, and HSUL I/O Standards. |
| $V_{REF(AC)}$ | AC input reference voltage for SSTL, HSTL, and HSUL I/O Standards. $V_{REF(AC)} = V_{REF(DC)}$ + noise. The peak-to-peak AC noise on $V_{REF}$ should not exceed 2% of $V_{REF(DC)}$. |
| $V_{REF(DC)}$ | DC input reference voltage for SSTL, HSTL, and HSUL I/O Standards. |
| $V_{SWING\ (AC)}$ | AC differential input voltage: AC Input differential voltage required for switching. |
| $V_{SWING\ (DC)}$ | DC differential input voltage: DC Input differential voltage required for switching. |
| $V_{TT}$ | Termination voltage for SSTL, HSTL, and HSUL I/O Standards. |
| $V_{X\ (AC)}$ | AC differential Input cross point voltage: The voltage at which the differential input signals must cross. |

# Document Revision History for the Intel MAX 10 FPGA Device Datasheet

| Document Version | Changes |
|---|---|
| 2020.06.30 | • Added $V_{CCIO}$ specifications for 1.0 V in the following tables:<br>— *Power Supplies Recommended Operating Conditions for Intel MAX 10 Single Supply Devices*<br>— *Power Supplies Recommended Operating Conditions for Intel MAX 10 Dual Supply Devices*<br>• Added 1.0 V LVCMOS specifications in the *Single-Ended I/O Standards Specifications for Intel MAX 10 Devices* table.<br>• Added specifications for 10M02SCU324 device in the following tables:<br>— *Uncompressed .rbf Sizes for Intel MAX 10 Devices*<br>— *Internal Configuration Time for Intel MAX 10 Devices (Uncompressed .rbf)*<br>— *Internal Configuration Time for Intel MAX 10 Devices (Compressed .rbf)* |
| 2018.06.29 | • Removed links on instant-on feature.<br>• Added JTAG timing specifications term in *Glossary*.<br>• Renamed the following IP cores as per Intel rebranding:<br>— Renamed Altera Modular ADC IP core to Modular ADC core Intel FPGA IP core.<br>— Renamed Altera Modular Dual ADC IP core to Modular Dual ADC core Intel FPGA IP core. |

| Date | Version | Changes |
|---|---|---|
| December 2017 | 2017.12.15 | • Removed the units for "Input resistance" and "Input capacitance" parameters in the following tables:<br>— *ADC Performance Specifications for Intel MAX 10 Single Supply Devices*<br>— *ADC Performance Specifications for Intel MAX 10 Dual Supply Devices*<br>• Removed the specification with memory initialization for 10M02 device in the *Uncompressed .rbf Sizes for Intel MAX 10 Devices* table. |
| June 2017 | 2017.06.16 | • Added notes for $T_J$ for Industrial and Automotive devices in Recommended Operating Conditions for Intel MAX 10 Devices table.<br>• Updated the parameter in Internal Weak Pull-Up Resistor for Intel MAX 10 Devices table.<br>• Changed "Performance" to "Frequency" in UFM Performance Specifications for Intel MAX 10 Devices table.<br>• Removed PowerPlay text from tool name. |
| February 2017 | 2017.02.21 | • Rebranded as Intel. |
| October 2016 | 2016.10.31 | • Updated the note to the Intel MAX 10 Device Grades and Speed Grades Supported table.<br>• Updated the Memory Standards Supported by the Soft Memory Controller for Intel MAX 10 Devices table. |

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| Date | Version | Changes |
|---|---|---|
| May 2016 | 2016.05.02 | • Updated $t_{RAMP}$ specifications in Recommended Operating Conditions for Intel MAX 10 Devices table.<br>— Removed standard POR and fast POR specifications.<br>— Updated maximum value from 3 ms to 10 ms and added a not for the minimum value.<br>• Added Supply Current and Power Consumption section.<br>• Added the following tables:<br>— Memory Standards Supported by the Soft Memory Controller for Intel MAX 10 Devices<br>— Internal Configuration Timing Parameter for Intel MAX 10 Devices<br>• Removed POR Delay Specifications for Intel MAX 10 Devices table.<br>• Updated the description in the Internal Configuration Time section.<br>• Updated the following tables:<br>— Internal Configuration Time for Intel MAX 10 Devices (Uncompressed `.rbf`)<br>— Internal Configuration Time for Intel MAX 10 Devices (Compressed `.rbf`) |
| January 2016 | 2016.01.22 | • Added description about automotive temperature devices in the Programming/Erasure Specifications table.<br>• Changed the pin capacitance to maximum values.<br>• Updated maximum TCCS specifications from 410 ps to 300 ps in the following tables:<br>— True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— Emulated RSDS_E_1R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— True LVDS Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices<br>— True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— Emulated LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices<br>— Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>• Added new table: True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices.<br>• Updated maximum $f_{HSCLK}$ and HSIODR specifications for –A6, –C7, and –I7 speed grades in True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices table.<br>• Updated SW specifications in the following tables:<br>— LVDS Receiver Timing Specifications for Intel MAX 10 Single Supply Devices<br>— LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices<br>• Updated maximum $f_{HSCLK}$ and HSIODR (high-speed I/O performance pin) specifications for –I6, –A6, –C7, –I7 speed grades in LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices table.<br>• Removed Internal Configuration Time information in the Uncompressed .rbf Sizes for Intel MAX 10 Devices table.<br>• Added Internal Configuration Time tables for uncompressed `.rbf` files and compressed `.rbf` files.<br>• Removed Preliminary tags for all tables. |

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| Date | Version | Changes |
|---|---|---|
| November 2015 | 2015.11.02 | • Added description to *Maximum Allowed Overshoot During Transitions over a 11.4-Year Time Frame* topic.<br>• Added ADC_VREF Pin Leakage Current for Intel MAX 10 Devices table.<br>• Updated the condition for "Bus-hold high, sustaining current" parameter from "$V_{IN}$ < $V_{IL}$ (minimum)" to "$V_{IN}$ < $V_{IH}$ (minimum)" in Bus Hold Parameters table.<br>• Added –A6 speed grade in the following tables:<br>— Intel MAX 10 Device Grades and Speed Grades Supported<br>— Series OCT without Calibration Specifications for Intel MAX 10 Devices<br>— Clock Tree Specifications for Intel MAX 10 Devices<br>— Embedded Multiplier Specifications for Intel MAX 10 Devices<br>— Memory Block Performance Specifications for Intel MAX 10 Devices<br>— True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— Emulated RSDS_E_1R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— IOE Programmable Delay on Row Pins for Intel MAX 10 Devices<br>— IOE Programmable Delay on Column Pins for Intel MAX 10 Devices<br>• Updated the maximum value for input clock cycle-to-cycle jitter ($t_{INJITTER_CCJ}$) with $F_{INPFD}$ < 100 MHz condition from 750 ps to ±750 ps in PLL Specifications for Intel MAX 10 Devices table.<br>• Updated the dual supply mode performance in Embedded Multiplier Specifications for Intel MAX 10 Devices table.<br>• Updated the dual supply mode performance in Memory Block Performance Specifications for Intel MAX 10 Devices table.<br>• Added typical specifications in Internal Oscillator Frequencies for Intel MAX 10 Devices table.<br>• Updated specifications in UFM Performance Specifications for Intel MAX 10 Devices table.<br>• Updated sampling window specifications in LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices table.<br>• Updated IOE programmable delay for row and column pins.<br>• Changed instances of *Quartus II* to *Quartus Prime*. |
| June 2015 | 2015.06.12 | • Updated the maximum values in Internal Weak Pull-Up Resistor for Intel MAX 10 Devices table.<br>• Removed Internal Weak Pull-Up Resistor equation.<br>• Updated the note for input resistance and input capacitance parameters in the ADC Performance Specifications table for both single supply and dual supply devices. Note: Download the SPICE models for simulation.<br>• Added a note to AC Accuracy - THD, SNR, and SINAD parameters in the ADC Performance Specifications for Intel MAX 10 Dual Supply Devices table. Note: When using internal $V_{REF}$, THD = 66 dB, SNR = 58 dB and SINAD = 57.5 dB for dedicated ADC input channels.<br>• Updated clock period jitter and cycle-to-cycle period jitter parameters in the Memory Output Clock Jitter Specifications for Intel MAX 10 Devices table. |

***continued...***

| Date | Version | Changes |
|---|---|---|
| May 2015 | 2015.05.04 | • Updated a note to $V_{CCIO}$ for both single supply and dual supply power supplies recommended operating conditions tables. Note updated: $V_{CCIO}$ for all I/O banks must be powered up during user mode because $V_{CCIO}$ I/O banks are used for the ADC and I/O functionalities.<br>• Updated Example for OCT Resistance Calculation after Calibration at Device Power-Up.<br>• Removed a note to BLVDS in Differential I/O Standards Specifications for Intel MAX 10 Devices table. BLVDS is now supported in Intel MAX 10 single supply devices. Note removed: BLVDS TX is not supported in single supply devices.<br>• Updated ADC Performance Specifications for both single supply and dual supply devices.<br>— Changed the symbol for Operating junction temperature range parameter from $T_A$ to $T_J$.<br>— Edited sampling rate maximum value from 1000 kSPS to 1 MSPS.<br>— Added a note to analog input voltage parameter.<br>— Removed input frequency, $f_{IN}$ specification.<br>— Updated the condition for DNL specification: External $V_{REF}$, no missing code. Added DNL specification for condition: Internal $V_{REF}$, no missing code.<br>— Added notes to AC accuracy specifications that the value with prescalar enabled is 6dB less than the specification.<br>— Added a note to On-Chip Temperature Sensor (absolute accuracy) parameter about the averaging calculation.<br>• Updated ADC Performance Specifications for Intel MAX 10 Single Supply Devices table.<br>— Added condition for On-Chip Temperature Sensor (absolute accuracy) parameter: with 64 samples averaging.<br>• Updated ADC Performance Specifications for Intel MAX 10 Dual Supply Devices table.<br>— Updated Digital Supply Voltage minimum value from 1.14 V to 1.15 V and maximum value from 1.26 V to 1.25 V.<br>• Updated $f_{HSCLK}$ and HSIODR specifications for –A7 speed grade in the following tables:<br>— True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— True LVDS Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices<br>— True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— Emulated LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices<br>— Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— LVDS Receiver Timing Specifications for Intel MAX 10 Single Supply Devices<br>— LVDS, TMDS, HiSpi, SLVS, and Sub-LVDS Receiver Timing Specifications for Intel MAX 10 Dual Supply Devices |

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| | | • Updated TCCS specifications in the following tables:<br>— True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— Emulated RSDS_E_1R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— True LVDS Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices<br>— True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— Emulated LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Single Supply Devices<br>— Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>• Updated $t_{x\ Jitter}$ specifications in the following tables:<br>— True PPDS and Emulated PPDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— True RSDS and Emulated RSDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— Emulated RSDS_E_1R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— True Mini-LVDS and Emulated Mini-LVDS_E_3R Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>— Emulated LVDS_E_3R, SLVS, and Sub-LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices<br>• Updated SW specifications in LVDS Receiver Timing Specifications for Intel MAX 10 Single Supply Devices table.<br>• Added a note to $t_{x\ Jitter}$ for all LVDS tables. Note: TX jitter is the jitter induced from core noise and I/O switching noise.<br>• Updated the description for $t_{LOCK}$ for all LVDS tables: Time required for the PLL to lock, after CONF_DONE signal goes high, indicating the completion of device configuration.<br>• Updated Memory Output Clock Jitter Specifications section.<br>— Updated maximum external memory interfaces frequency from 300 MHz to 303 MHz.<br>— Updated PLL output routing from global clock network to PHY clock network.<br>• Added I/O Timing for Intel MAX 10 Devices table.<br>• Added $V_{HYS}$ in the Glossary table. |
| January 2015 | 2015.01.23 | • Removed a note to $V_{CCA}$ in Power Supplies Recommended Operating Conditions for Intel MAX 10 Dual Supply Devices table. This note is not valid: All $V_{CCA}$ pins must be connected together for EQFP package.<br>• Corrected the maximum value for $t_{OUTJITTER_CCJ_IO}$ ($F_{OUT} \geq 100$ MHz) from 60 ps to 650 ps in PLL Specifications for Intel MAX 10 Devices table. |
| December 2014 | 2014.12.15 | • Restructured Programming/Erasure Specifications for Intel MAX 10 Devices table to add temperature specifications that affect the data retention duration.<br>• Added statements in the I/O Pin Leakage Current section: Input channel leakage of ADC I/O pins due to hot socket is up to maximum of 1.8 mA. The input channel leakage occurs when the ADC IP core is enabled or disabled. This is applicable to all Intel MAX 10 devices with ADC IP core, which are 10M04, 10M08, 10M16, 10M25, 10M40, and 10M50 devices. The ADC I/O pins are in Bank 1A.<br>• Added a statement in the I/O Standards Specifications section: You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards. |

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| | | • Updated SSTL-2 Class I and II I/O standard specifications for JEDEC compliance as follows:<br>— VIL(AC) Max: Updated from $V_{REF}$ – 0.35 to $V_{REF}$ – 0.31<br>— VIH(AC) Min: Updated from $V_{REF}$ + 0.35 to $V_{REF}$ + 0.31<br>• Added a note to BLVDS in Differential I/O Standards Specifications for Intel MAX 10 Devices table: BLVDS TX is not supported in single supply devices.<br>• Added a link to MAX 10 High-Speed LVDS I/O User Guide for the list of I/O standards supported in single supply and dual supply devices.<br>• Added a statement in PLL Specifications for Intel MAX 10 Single Supply Device table: For V36 package, the PLL specification is based on single supply devices.<br>• Added Internal Oscillator Specifications from Intel MAX 10 Clocking and PLL User Guide.<br>• Added UFM specifications for serial interface.<br>• Updated total harmonic distortion (THD) specifications as follows:<br>— Single supply devices: Updated from 65 dB to –65 dB<br>— Dual supply devices: Updated from 70 dB to –70 dB (updated from 65 dB to –65 dB for dual function pin)<br>• Added condition for On-Chip Temperature Sensor—Absolute accuracy parameter in ADC Performance Specifications for Intel MAX 10 Dual Supply Devices table. The condition is: with 64 samples averaging.<br>• Updated the description in Periphery Performance Specifications to mention that proper timing closure is required in design.<br>• Updated HSIODR and $f_{HSCLK}$ specifications for x10 and x7 modes in True LVDS Transmitter Timing Specifications for Intel MAX 10 Dual Supply Devices.<br>• Added specifications for low-speed I/O performance pin sampling window in LVDS Receiver Timing Specifications for Intel MAX 10 Single Supply Devices table: Max = 900 ps for –C7, –I7, –A7, and –C8 speed grades.<br>• Added $t_{RU_nCONFIG}$ and $t_{RU_nRSTIMER}$ specifications for different devices in Remote System Upgrade Circuitry Timing Specifications for Intel MAX 10 Devices table.<br>• Removed the word "internal oscillator" in User Watchdog Timer Specifications for Intel MAX 10 Devices table to avoid confusion.<br>• Added IOE programmable delay specifications. |
| September 2014 | 2014.09.22 | Initial release. |