GaAs, pHEMT, MMIC,1/2 W, 20 GHz to 44 GHz, Power Amplifier

Data Sheet **ADPA7002CHIP**

FEATURES

Output P1dB: 28 dBm (typical at 34 GHz to 44 GHz)
P_{SAT}: 30 dBm (typical at 20 GHz to 34 GHz)
Gain: 15 dB (typical at 34 GHz to 44 GHz)
IP3: 40 dBm (typical)
Supply voltage: 5 V at 600 mA
Die size: 2.75 mm × 1.805 mm × 0.1 mm

APPLICATIONS

Military and space
Test instrumentation

FUNCTIONAL BLOCK DIAGRAM

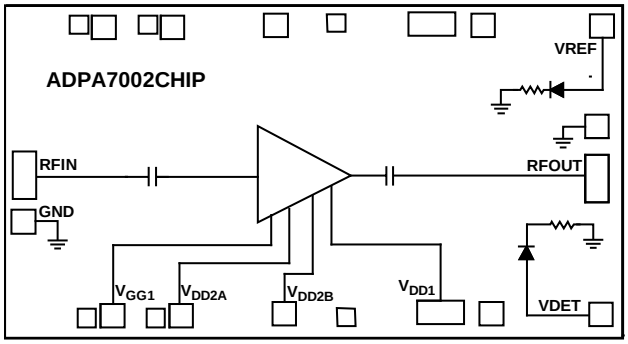

Figure 1.

GENERAL DESCRIPTION

The ADPA7002CHIP is a gallium arsenide (GaAs), monolithic microwave integrated circuit (MMIC), pseudomorphic high electron mobility transistor (pHEMT), distributed power amplifier that operates from 20 GHz to 44 GHz. The amplifier provides 15 dB of small signal gain, 28 dBm output power at 1 dB gain compression (P1dB), and a typical output third-order intercept (IP3) of 40 dBm. The amplifier requires 600 mA from a 5 V supply on V_{DD2A}, V_{DD2B}, and V_{DD1}. The ADPA7002CHIP also features inputs/outputs (I/Os) that are internally matched to 50 Ω, and facilitates integration into multichip modules (MCMs). All data is taken with the on substrate chip connected via two wire bonds that are 0.025 mm (1 mil) wide and 0.31 mm (12 mils) long.

Rev. A Document Feedback

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Technical Support www.analog.com

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REVISION HISTORY

7/2019—Rev. 0 to Rev. A

Added Thermal Resistance Section and Table 4; Renumbered Sequentially 4
Changes to Figure 10 7

2/2019—Revision 0: Initial Version

SPECIFICATIONS

FREQUENCY RANGE: 20 GHz TO 34 GHz

T_A = 25°C, V_{DD} = 5 V, quiescent drain supply current (I_{DQ}) = 600 mA, for nominal operation, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		20		34	GHz	
GAIN		15	17		dB	
Gain Flatness			±0.5		dB	
Gain Variation over Temperature			0.012		dB/°C	
NOISE FIGURE			6		dB	
RETURN LOSS						
Input			20		dB	
Output			20		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB	26	28.5		dBm	
Saturated Output Power	P_{SAT}		30		dBm	
Output Third-Order Intercept	IP3		40		dBm	Measurement taken at saturated output power (P_{OUT}) per tone = 14 dBm
SUPPLY						
Quiescent Drain Supply Current	I_{DQ}		600		mA	Adjust the gate bias voltage (V_{GG1}) between −2 V to 0 V to achieve the desired I_{DQ}
Voltage	V_{DD}	4	5		V	

FREQUENCY RANGE: 34 GHz TO 44 GHz

T_A = 25°C, V_{DD} = 5 V, I_{DQ} = 600 mA, for nominal operation, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		34		44	GHz	
GAIN		12	15		dB	
Gain Flatness			±0.7		dB	
Gain Variation over Temperature			0.024		dB/°C	
NOISE FIGURE			5		dB	
RETURN LOSS						
Input			25		dB	
Output			16		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB	25	28		dBm	
Saturated Output Power	P_{SAT}		28.5		dBm	
Output Third-Order Intercept	IP3		40		dBm	Measurement taken at P_{OUT} per tone = 14 dBm
SUPPLY						
Quiescent Drain Supply Current	I_{DQ}		600		mA	Adjust the gate bias voltage (V_{GG1}) between −2 V to 0 V to achieve the desired I_{DQ}
Voltage	V_{DD}	4	5		V	

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Drain Bias Voltage (V_{DD})	6.0 V
Gate Bias Voltage (V_{GG1})	−1.5 to 0 V
Radio Frequency Input Power (RFIN)	25 dBm
Continuous Power Dissipation (P_{DISS}), T = 85°C (Derate 75.2 mW/°C above 85°C)	6.77 W
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +85°C
Nominal Junction Temperature (T = 85°C, V_{DD} = 5 V, I_{DQ} = 600 mA)	124.9°C
Junction Temperature to Maintain 1,000,000 Hour Mean Time to Failure (MTTF)	175°C
Electrostatic Discharge (ESD) Sensitivity Human Body Model (HBM)	Class 1A (passed 500 V)

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to system design and operating environment. Careful attention to printed circuit board (PCB) thermal design is required.

θ_{JC} is the channel to case thermal resistance, channel to bottom of die.

Table 4. Thermal Resistance

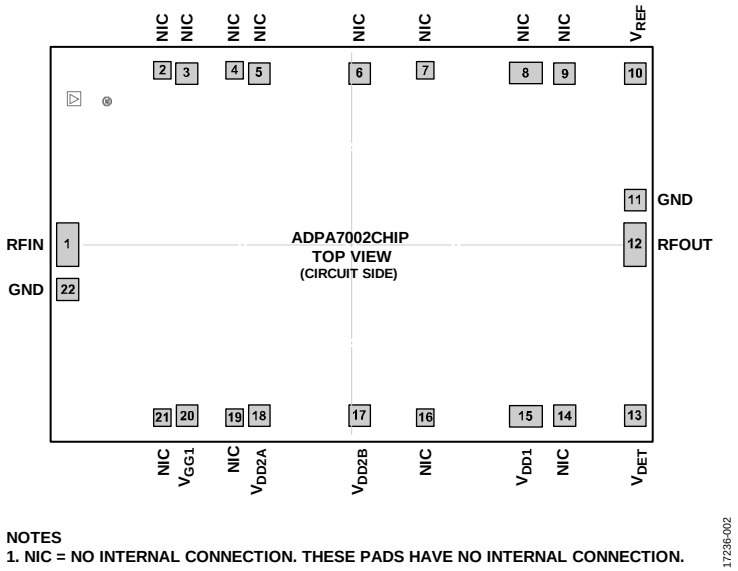
Package Type	θ_{JC}	Unit
C-22-3[1]	13.3	°C/W

[1] θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to thermal conduction from the channel through the ground pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NIC = NO INTERNAL CONNECTION. THESE PADS HAVE NO INTERNAL CONNECTION.

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RFIN	Radio Frequency (RF) Signal Input. This pad is ac-coupled and matched to 50 Ω.
2 to 9, 14, 16, 19, 21	NIC	No Internal Connection. These pads have no internal connections.
10	V_{REF}	Reference Diode for Temperature Compensation of V_{DET} RF Output Power Measurements.
11, 22, Die Bottom	GND	Ground. These pads and the die bottom must be connected to RF and dc ground.
12	RFOUT	RF Signal Output. This pad is ac-coupled and matched to 50 Ω.
13	V_{DET}	Detector Diode to Measure RF Output Power. Output power detection via this pin requires the application of a dc bias voltage through an external series resistor. Used in combination with the V_{REF} pin, the difference voltage (V_{REF} – V_{DET}) is a temperature compensated dc voltage that is proportional to the RF output power.
15, 17, 18	V_{DD1}, V_{DD2A}, V_{DD2B}	Drain Biases for Amplifier. External bypass capacitors of 4.7 µF and 0.01 µF are required.
20	V_{GG1}	Gate Control for Amplifier. External bypass capacitors of 4.7 µF and 0.01 µF are required.

INTERFACE SCHEMATICS

Figure 3. GND Interface Schematic

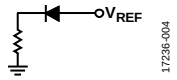


Figure 4. V_{REF} Interface Schematic

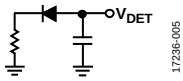


Figure 5. V_{DET} Interface Schematic

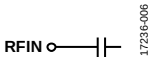


Figure 6. RFIN Interface Schematic

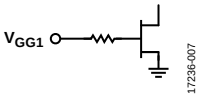


Figure 7. V_{GG1} Schematic

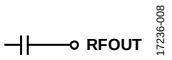


Figure 8. RFOUT Interface Schematic

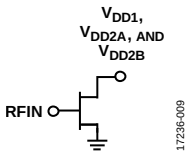


Figure 9. V_{DD1}, V_{DD2A}, and V_{DD2B} Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

Where I_{DQ} = quiescent drain supply current and I_{DD} (drain current) = RF signal applied to I_{DQ}.

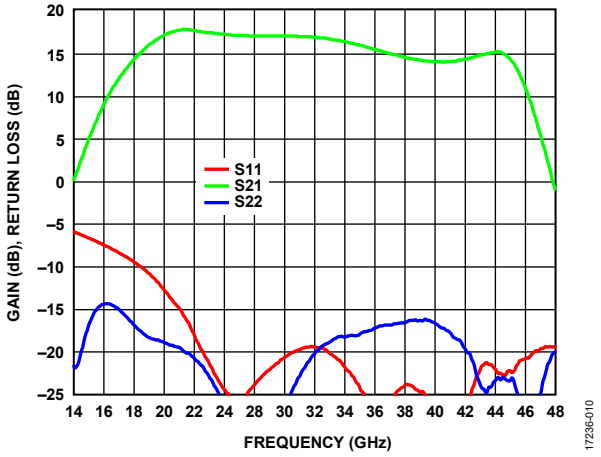


Figure 10. Gain and Return Loss vs. Frequency

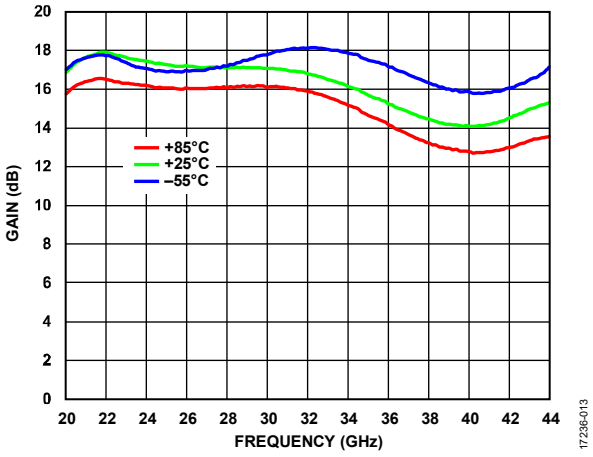


Figure 13. Gain vs. Frequency for Various Temperatures

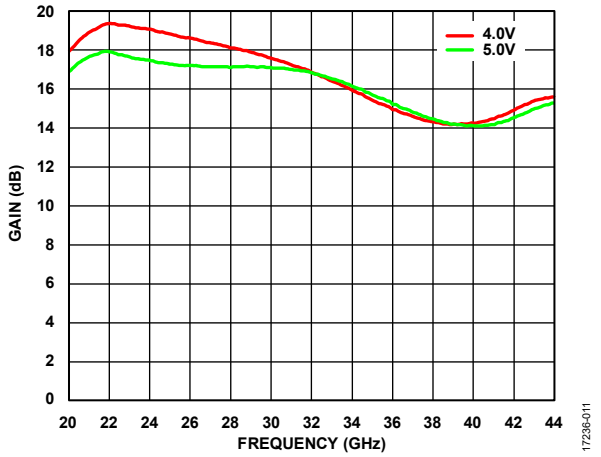


Figure 11. Gain vs. Frequency for Various Supply Voltages (V_{DD})

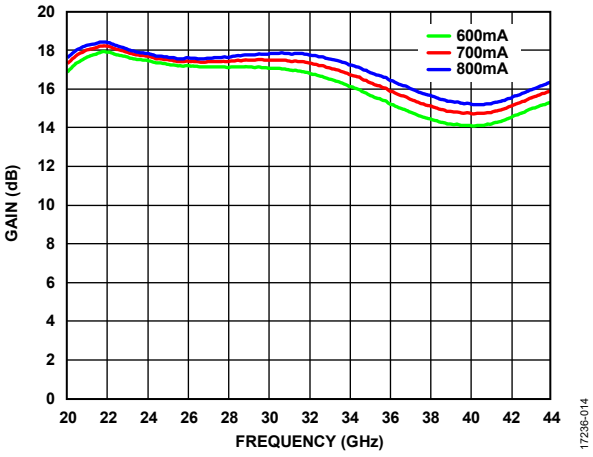


Figure 14. Gain vs. Frequency for Various Quiescent Drain Supply Current (I_{DQ})

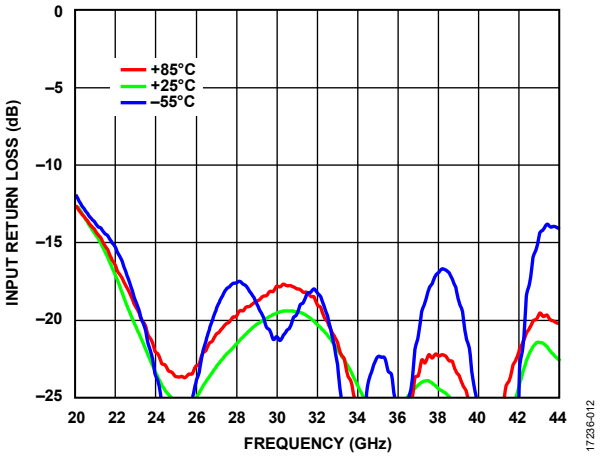


Figure 12. Input Return Loss vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 600 mA

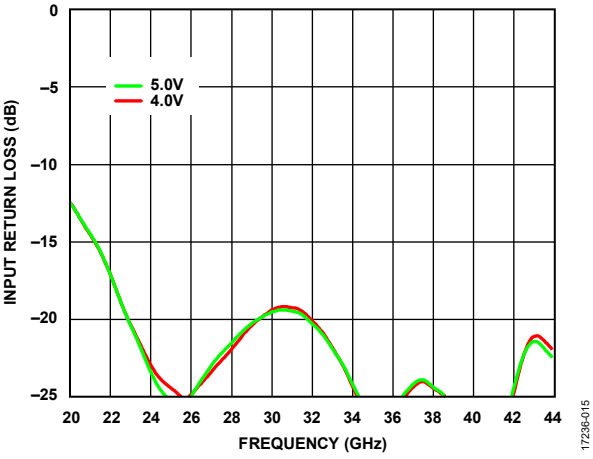


Figure 15. Input Return Loss vs. Frequency for Various Supply Voltages (V_{DD})

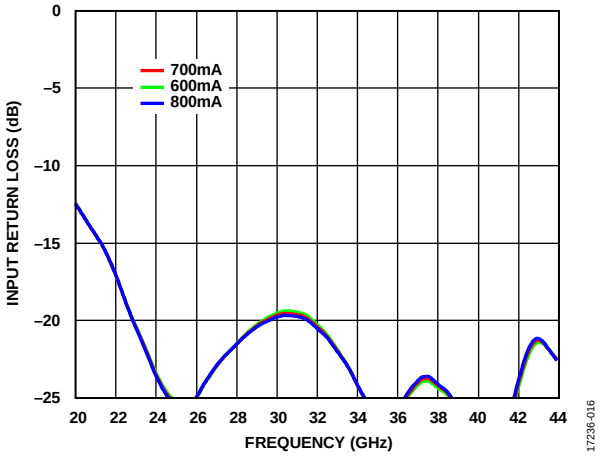


Figure 16. Input Return Loss vs. Frequency for Various Quiescent Drain Supply Current (I_{DQ})

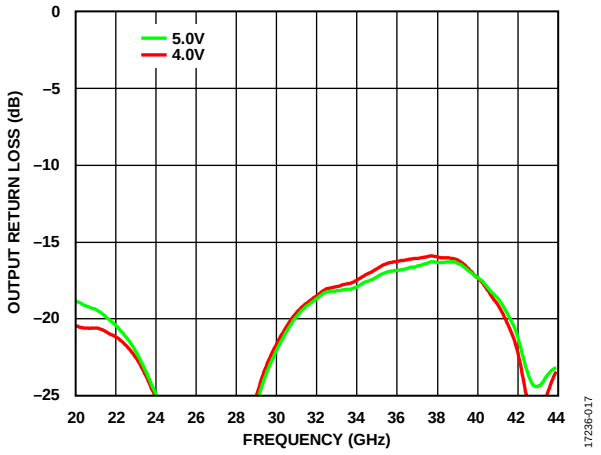


Figure 17. Output Return Loss vs. Frequency for Various Supply Voltages (V_{DD})

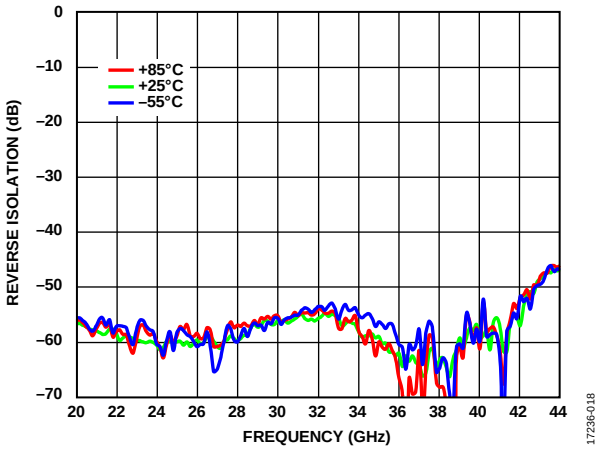


Figure 18. Reverse Isolation vs. Frequency for Various Temperatures

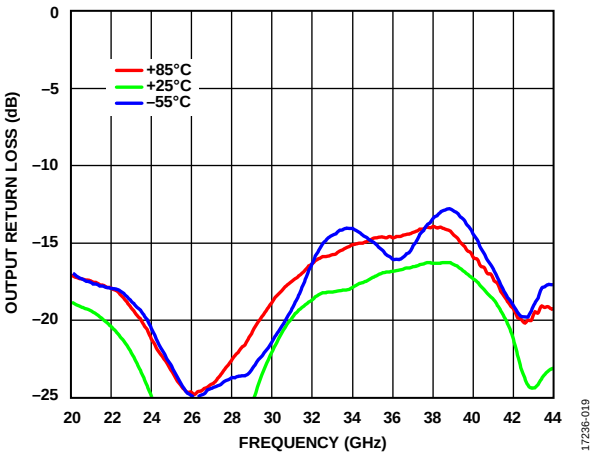


Figure 19. Output Return Loss vs. Frequency for Various Temperatures

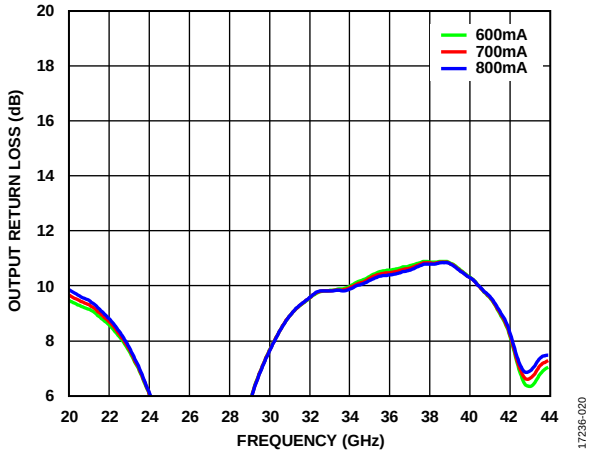


Figure 20. Output Return Loss vs. Frequency for Various Quiescent Drain Supply Current (I_{DQ})

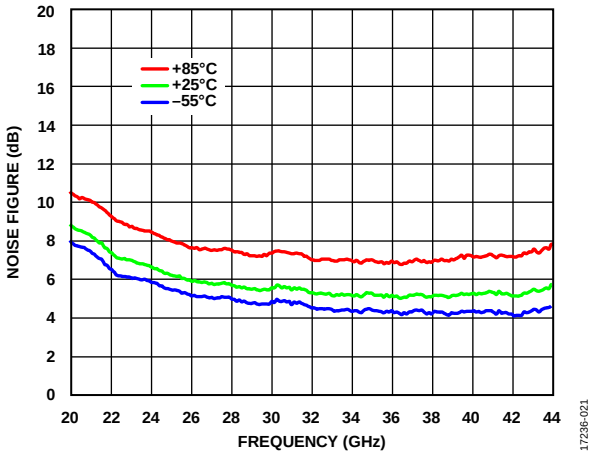


Figure 21. Noise Figure vs. Frequency for Various Temperatures

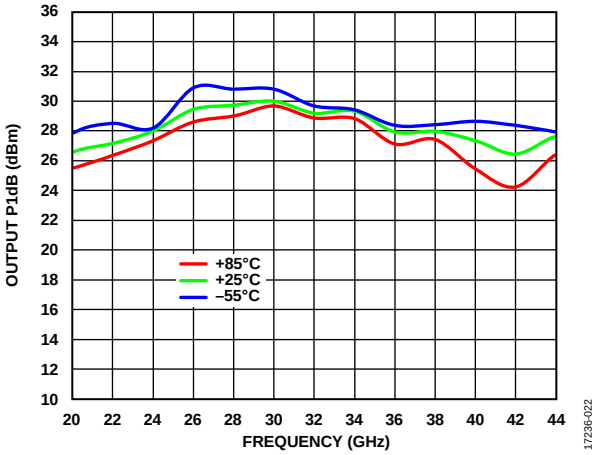


Figure 22. Output P1dB vs. Frequency for Various Temperatures

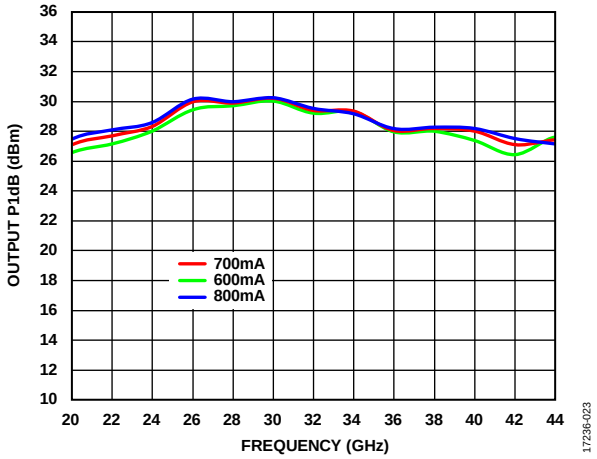


Figure 23. Output P1dB vs. Frequency for Various Supply Currents

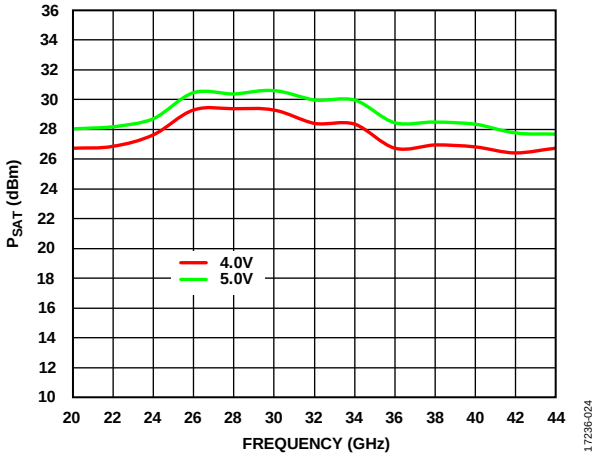


Figure 24. P_{SAT} vs. Frequency for Various Supply Voltages

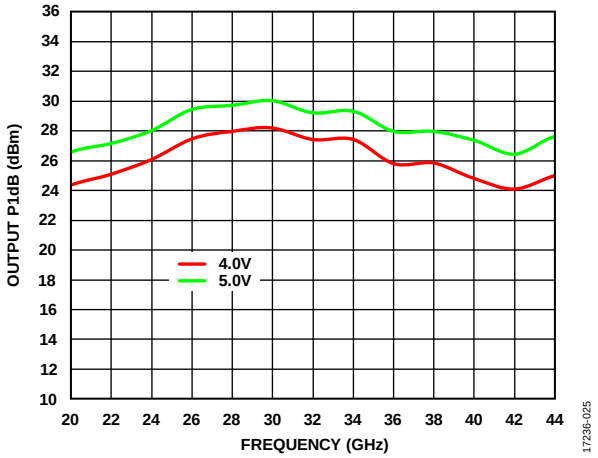


Figure 25. Output P1dB vs. Frequency for Various Supply Voltages

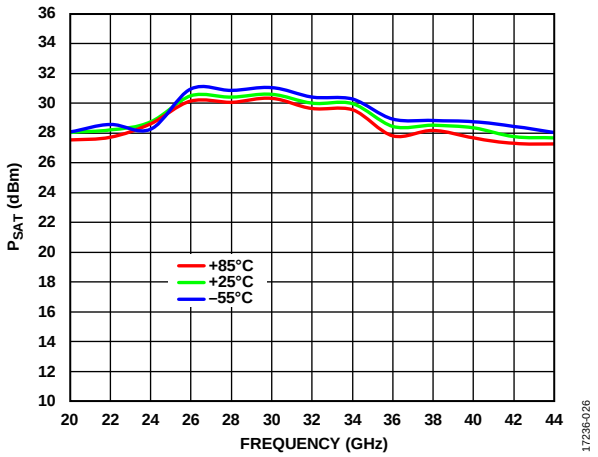


Figure 26. P_{SAT} vs. Frequency for Various Temperatures

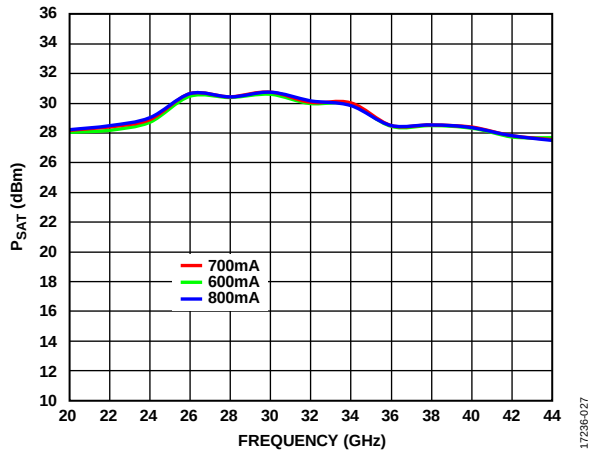


Figure 27. P_{SAT} vs. Frequency for Various Supply Currents

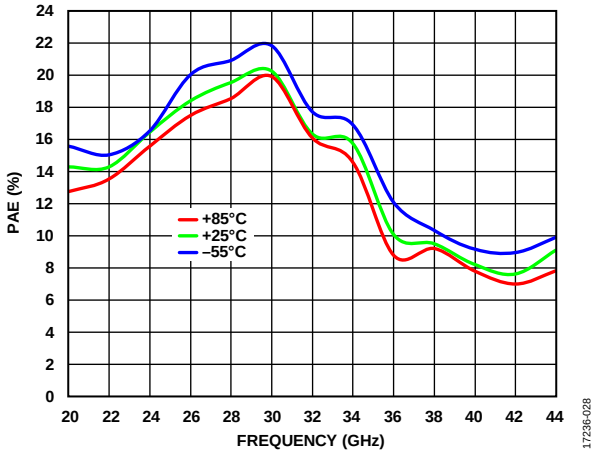


Figure 28. Power Added Efficiency (PAE) vs. Frequency over Temperature, PAE Measured at P_{SAT}

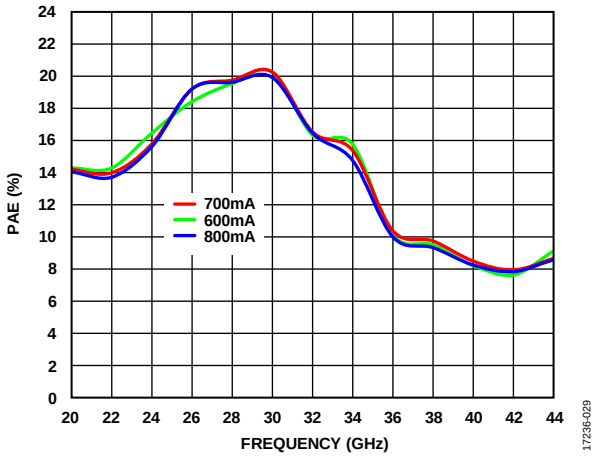


Figure 29. PAE vs. Frequency for Various Drain Currents (I_{DD}), PAE Measured at P_{SAT}

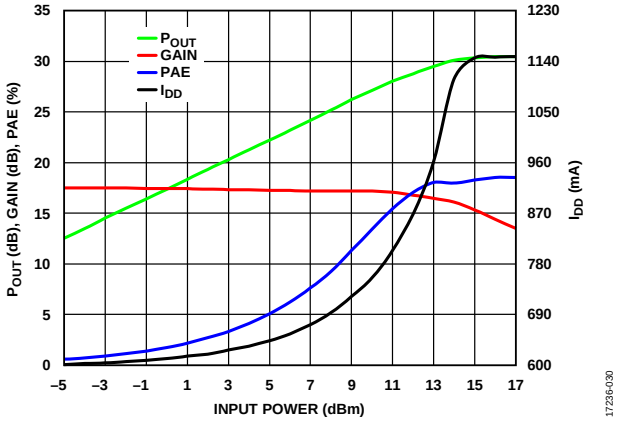


Figure 30. P_{OUT}, Gain, PAE, and Drain Current (I_{DD}) vs. Input Power, Frequency = 26 GHz

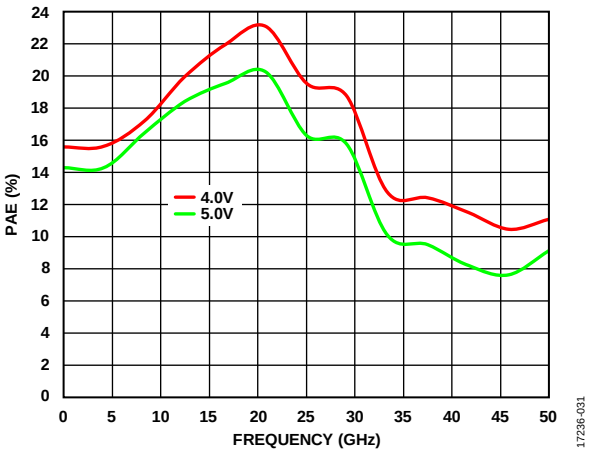


Figure 31. PAE vs. Frequency for Various Supply Voltages (V_{DD}), PAE Measured at P_{SAT}

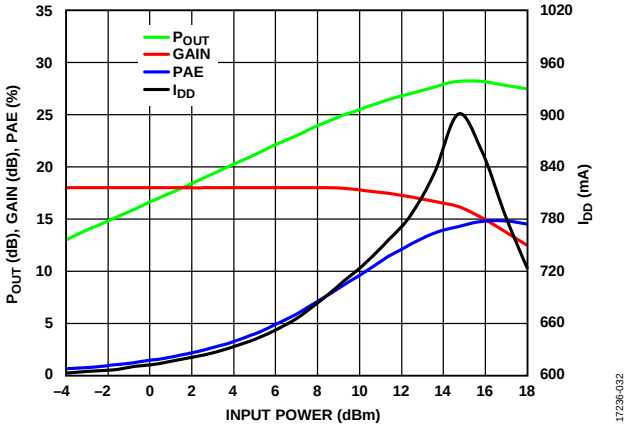


Figure 32. P_{OUT}, Gain, PAE, and Drain Current (I_{DD}) vs. Input Power, Frequency = 22 GHz

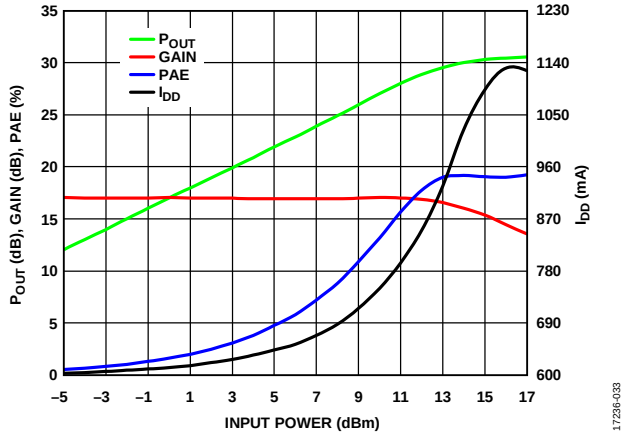


Figure 33. P_{OUT}, Gain, PAE, and Drain Current (I_{DD}) vs. Input Power, Frequency = 30 GHz

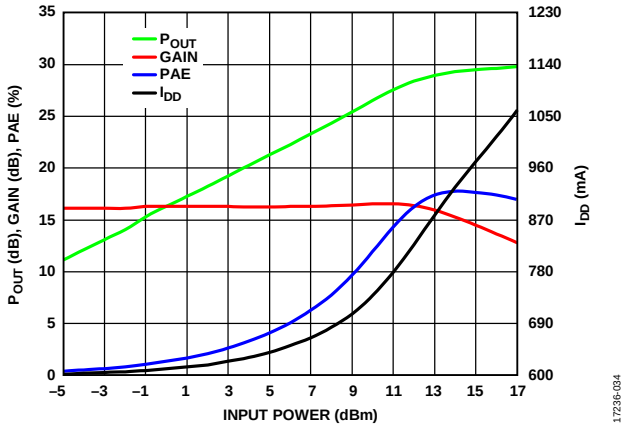


Figure 34. P_{OUT}, Gain, PAE, and Drain Current (I_{DD}) vs. Input Power, Frequency = 34 GHz

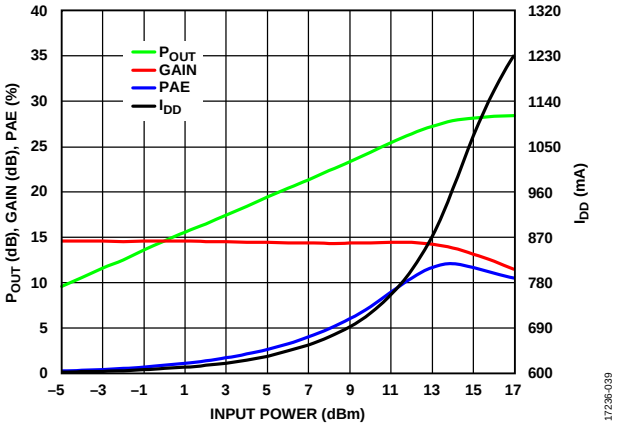


Figure 37. P_{OUT}, Gain, PAE, and Drain Current (I_{DD}) vs. Input Power, Frequency = 38 GHz

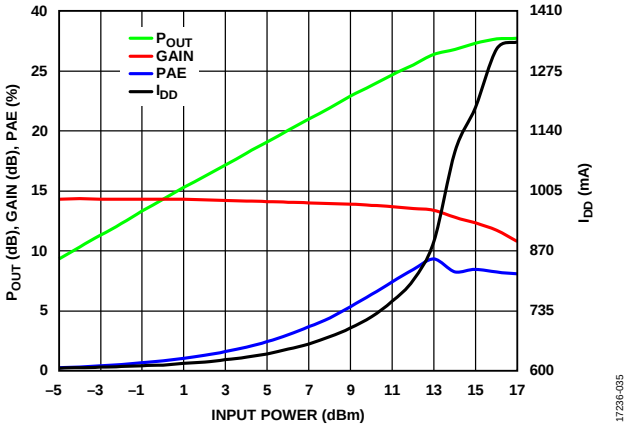


Figure 35. P_{OUT}, Gain, PAE, and Drain Current (I_{DD}) vs. Input Power, Frequency = 42 GHz

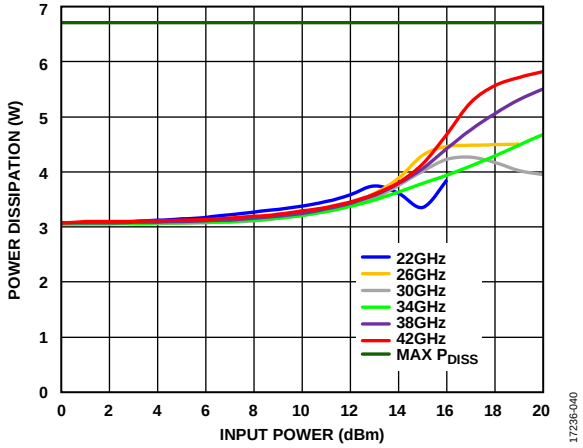


Figure 38. Power Dissipation (P_{DISS}) vs. Input Power, T_A = 85°C

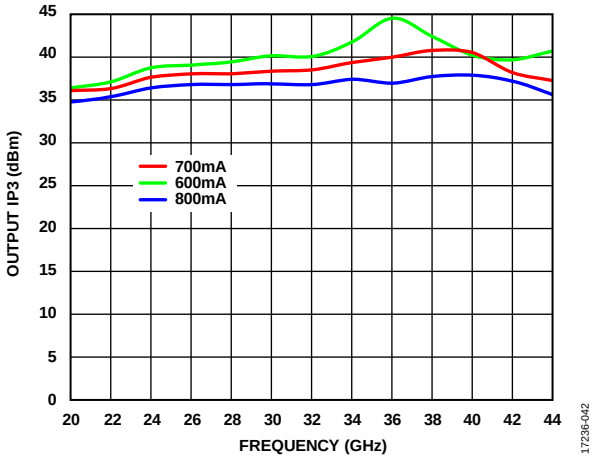


Figure 36. Output IP3 vs. Frequency for Various Drain Currents (I_{DD}), P_{OUT} per Tone = 12 dBm

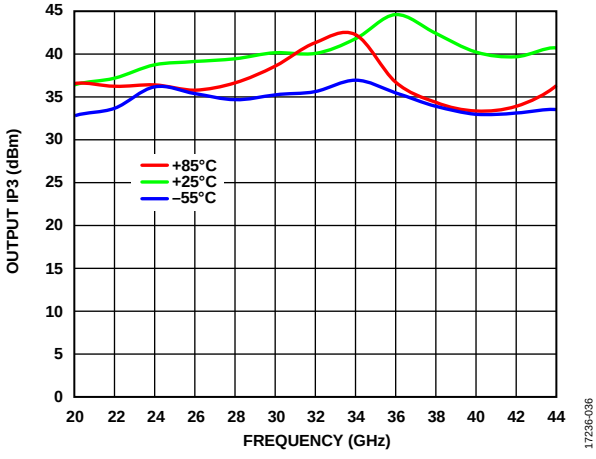


Figure 39. Output IP3 vs. Frequency for Various Temperatures, P_{OUT} per Tone = 12 dBm, I_{DD} = 600 mA

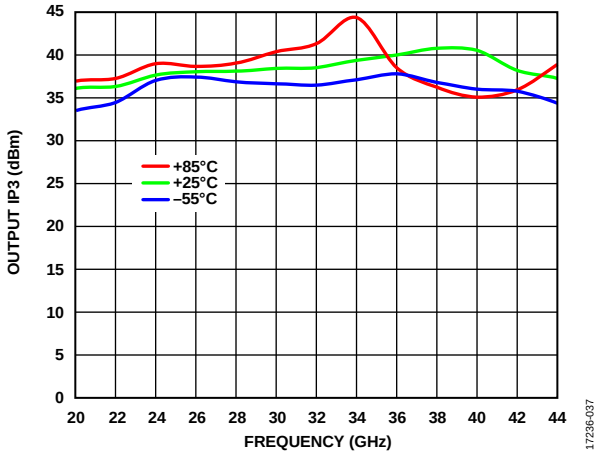


Figure 40. Output IP3 vs. Frequency for Various Temperatures, P_{OUT} per Tone = 12 dBm, I_{DD} = 700 mA

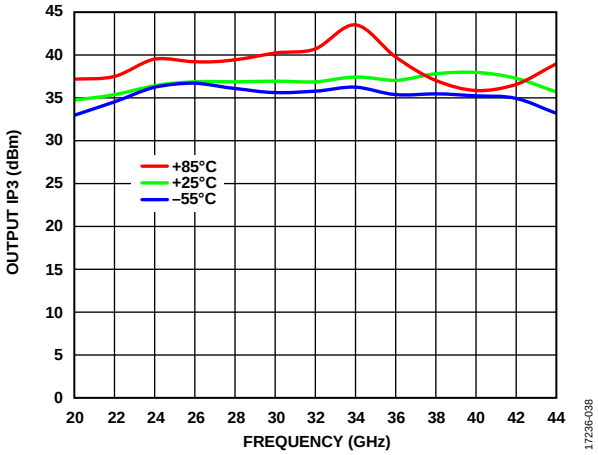


Figure 43. Output IP3 vs. Frequency for Various Temperatures, P_{OUT} per Tone = 12 dBm, I_{DD} = 800 mA

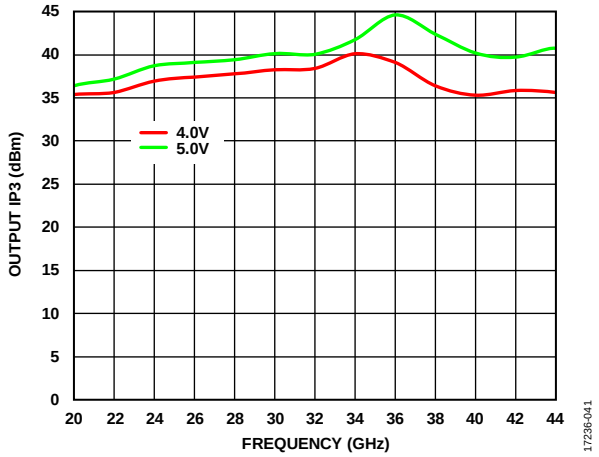


Figure 41. Output IP3 vs. Frequency for Various Supply Voltages (V_{DD}), P_{OUT} per Tone = 12 dBm

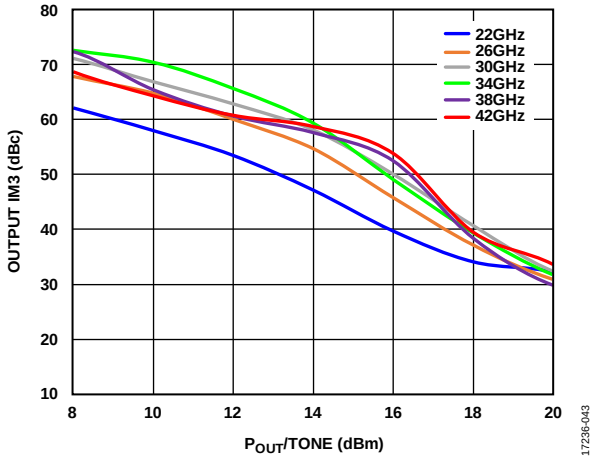


Figure 44. Output Third-Order Intermodulation (IM3) vs. P_{OUT} per Tone for Various Frequencies at V_{DD} = 5 V

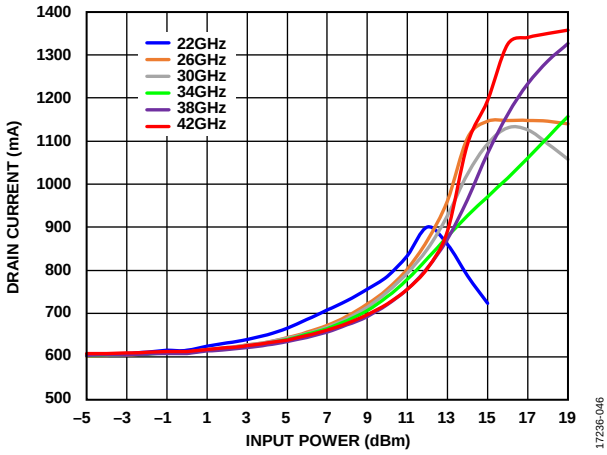


Figure 42. Drain Current (I_{DD}) vs. Input Power over Various Frequencies

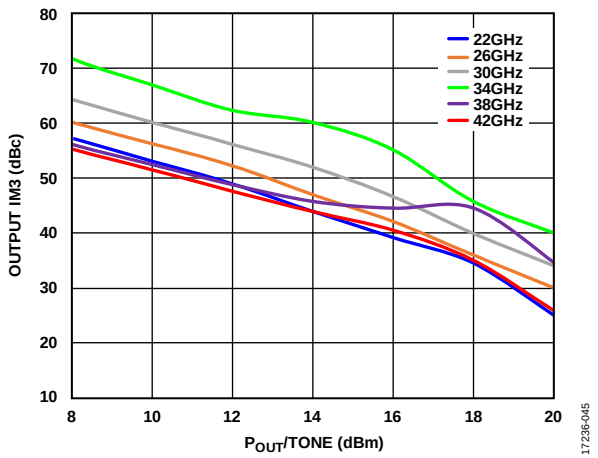


Figure 45. Output IM3 vs. P_{OUT} per Tone for Various Frequencies at V_{DD} = 4 V (Specifically Tested at Minimum Voltage)

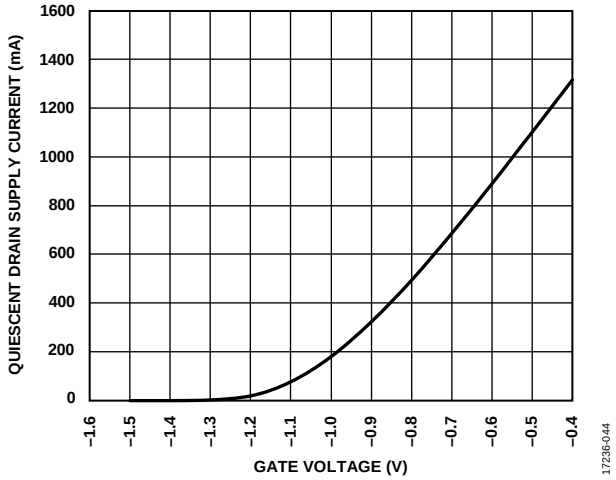


Figure 46. Quiescent Drain Supply Current (I_{DQ}) vs. Gate Voltage (V_{GG1})

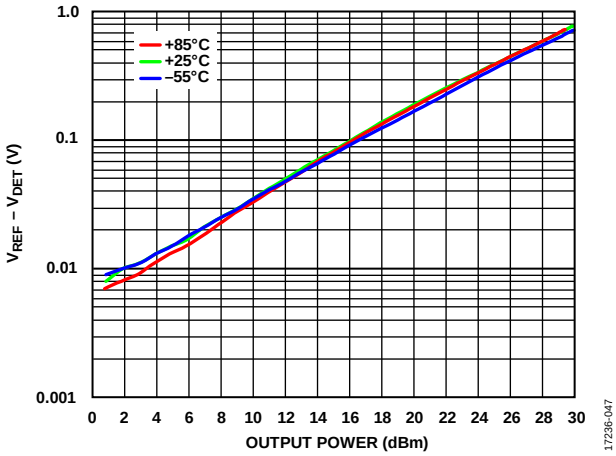


Figure 47. $V_{REF} - V_{DET}$ vs. Output Power at Various Temperatures, Frequency = 32 GHz

CONSTANT DRAIN CURRENT (I_{DD}) OPERATION

T_A = 25°C, V_{DD} = 5 V, I_{DD} = 800 mA, for nominal operation, unless otherwise noted. Figure 48 through Figure 51 are biased with the HMC980LP4E active bias controller. See the Biasing the ADPA7002CHIP with the HMC980LP4E section for biasing details.

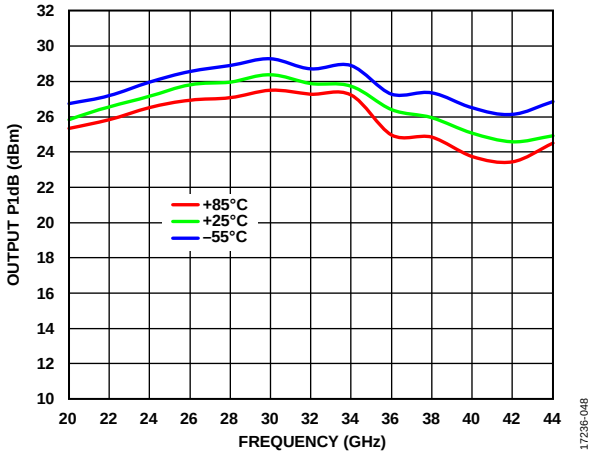


Figure 48. Output P1dB vs. Frequency for Various Temperatures, Data Measured with Constant Drain Current (I_{DD})

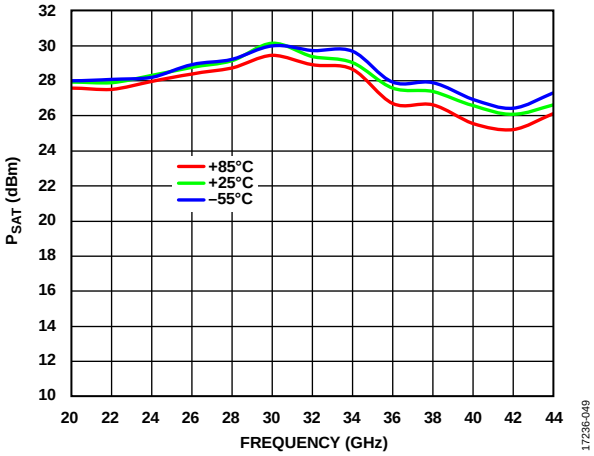


Figure 49. P_{SAT} vs. Frequency for Various Temperatures, Data Measured with Constant Drain Current (I_{DD})

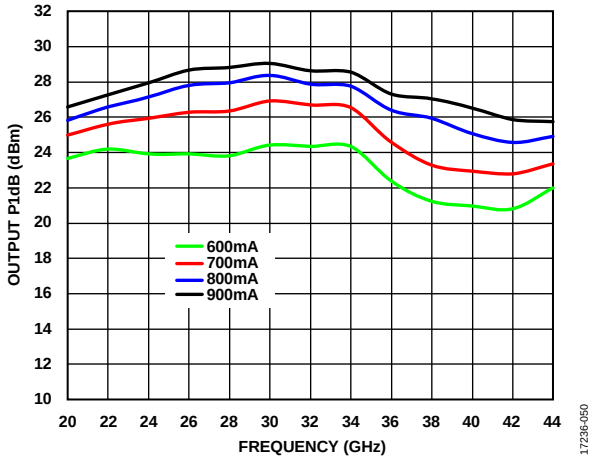


Figure 50. Output P1dB vs. Frequency for Various Supply Currents, Data Measured with Constant Drain Current (I_{DD})

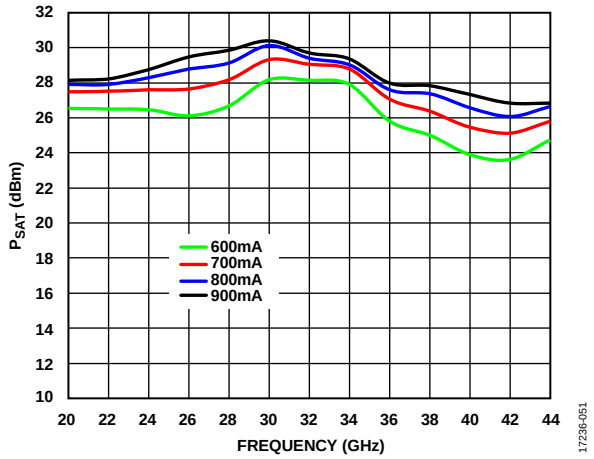


Figure 51. P_{SAT} vs. Frequency for Various Supply Currents Data Measured with Constant Drain Current (I_{DD})

THEORY OF OPERATION

The architecture of the ADPA7002CHIP, a medium power amplifier, is shown in Figure 52. The ADPA7002CHIP uses a cascaded, three-stage amplifier operating in quadrature between two 90° hybrids.

The input signal is evenly divided into two. Each input signal is amplified through three independent gain stages and the amplified signals are combined at the output. This balanced amplifier approach creates an amplifier with a combined gain of 15 dB and a P_{SAT} value of 30 dBm.

A portion of the RF output signal is directionally coupled to a diode to detect the RF output power (see Figure 52). When the diode is dc biased, the diode rectifies the RF power and makes the RF power available for measurement as a dc voltage at the V_{DET} pin. Temperature compensation is accomplished by referencing a symmetrical diode circuit that is not coupled to the RF output, which contains a dc voltage output, at the V_{REF} pin as shown in Figure 56. The difference of $V_{REF} - V_{DET}$ provides a temperature compensated signal that is proportional to the RF output.

The 90° hybrids ensure that the input and output return losses are >12 dB. See the application circuits in Figure 53 and Figure 54 for further details on biasing the various blocks.

To obtain optimal performance from the ADPA7002CHIP and avoid damaging the device, follow the recommended biasing sequences described in the Biasing Procedures section.

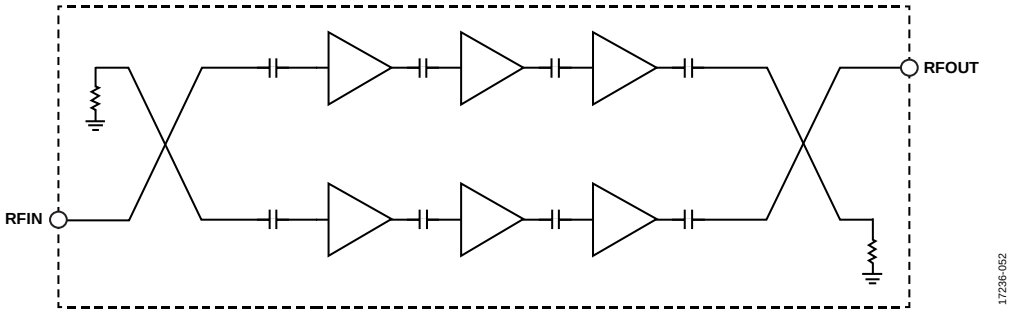


Figure 52. Fundamental Cell Schematic

ADPA7002CHIP ASSEMBLY AND CIRCUIT DIAGRAMS

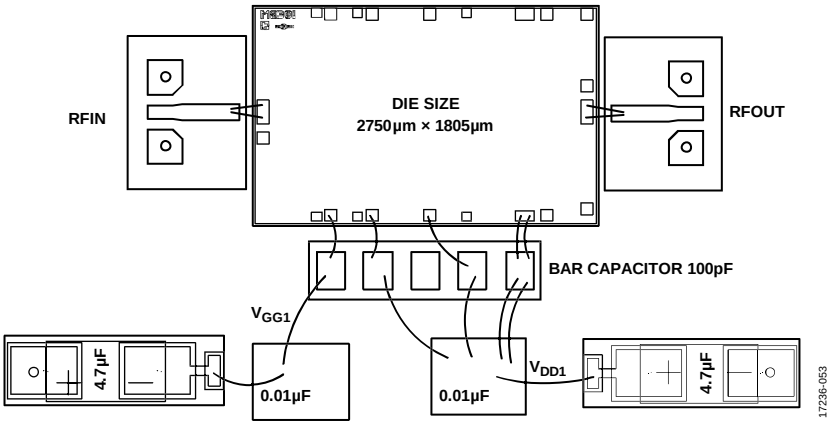


Figure 53. Assembly Diagram

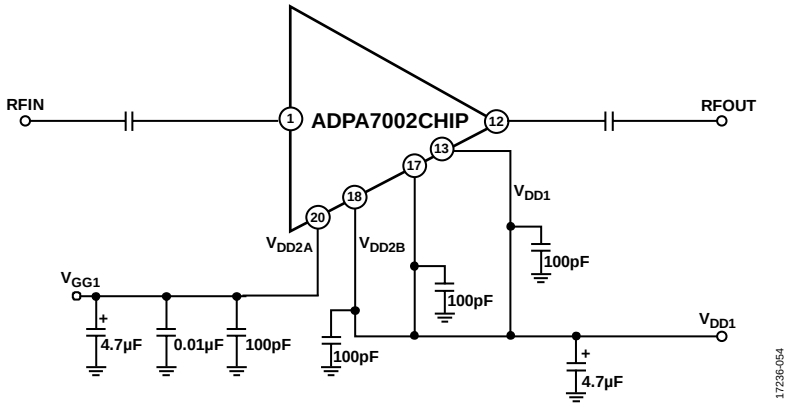
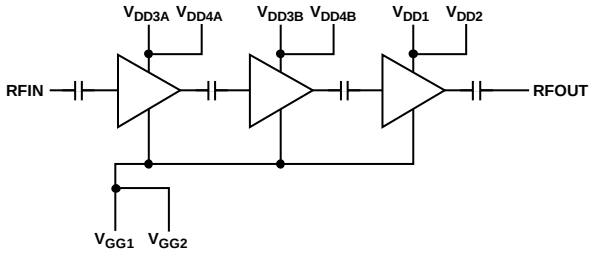


Figure 54. Typical Application Circuit



NOTES
1. V_{DD3A} IS A DRAIN BIAS PAD FOR THE FIRST STAGE.
   V_{DD3B} IS A DRAIN BIAS PAD FOR THE SECOND STAGE.
   V_{DD4A} AND V_{DD4B} ARE A COMBINED DRAIN BIAS PAD FOR THE THIRD STAGE.

17236-055

Figure 55. Simplified Internal ADPA7002CHIP Block Diagram

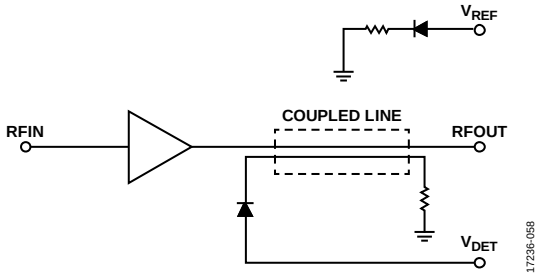


Figure 56. Power Detector Circuit

ALTERNATE ASSEMBLY DIAGRAM

The ADPA7002CHIP die is symmetric and can be biased from either the north side or the south side (see Figure 57) with equivalent performance.

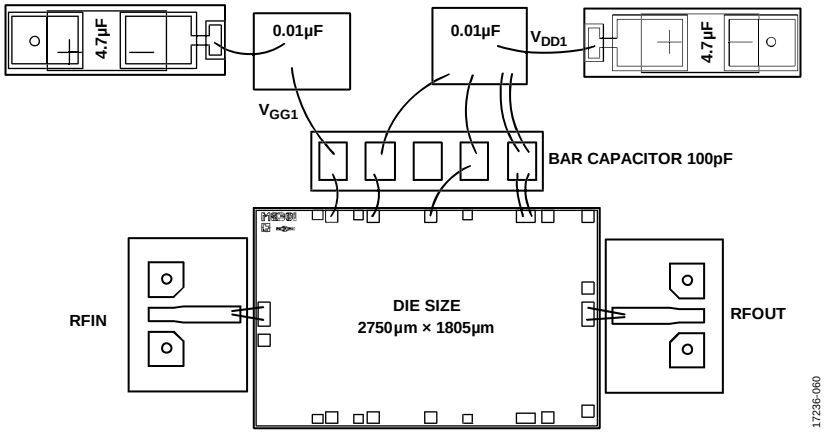


Figure 57. Alternate Assembly Diagram

BIASING PROCEDURES

The ADPA7002CHIP is a GaAs, pHEMT, MMIC power amplifier. Capacitive bypassing is required for all V_{GGx} and V_{DDx} pads (see Figure 54). The internal connections of the bypass capacitors are shown in Figure 56.

V_{GG1} and V_{GG2} are gate bias pads. V_{DD2A} and V_{DD3A} are drain bias pads for the first stage. V_{DD2B} and V_{DD3B} are drain bias pads for the second stage. V_{DD1} and V_{DD2} are drain bias pads for the third stage.

All measurements for this device are taken using the typical application circuit (see Figure 54) and configured as shown in the assembly diagram (see Figure 53).

Adhere to the following bias sequence during power-up:

1. Connect GND to RF and dc ground.
2. Set the V_{GG1} and V_{GG2} voltage to −2 V.
3. Set all the drain bias voltages, V_{DDX} = 5 V.
4. Increase the gate bias voltage to achieve a quiescent current, I_{DQ} = 600 mA.
5. Apply the RF signal.

Adhere to the following bias sequence during power-down:

1. Turn off the RF signal.
2. Decrease the gate bias, V_{GG1}, and V_{GG2} voltages to −2 V to achieve I_{DQ} = 0 mA (approximately).
3. Decrease all drain bias voltages to 0 V.
4. Decrease the gate bias voltage to 0 V.

Simplified bias pad connections to dedicated gain stages, as well as dependence and independence among pads are shown in Figure 54.

Table 6. Power Selection Table[1, 2]

I_{DQ} (mA)	Gain (dB)	P1dB (dBm)	Output IP3 (dBm)	P_{DISS} (W)	V_{GG} (V)
600	17.2	30.04	40.6	3	−0.73
700	17.7	30.24	38.7	3.5	−0.67
800	18.0	30.25	37.0	4	−0.62

[1] Data taken at the following nominal bias conditions: V_{DD} = 5 V, T_A = 25°C.
[2] Adjust V_{GG1} and V_{GG2} from −2 V to 0 V to achieve the desired drain current.

The V_{DD} = 5 V and I_{DQ} = 600 mA bias conditions are recommended to optimize overall performance. Unless otherwise noted, the data shown in the Typical Performance Characteristics section is taken using the recommended bias conditions. Operating the ADPA7002CHIP at different bias conditions can provide performance that differs from what is shown in Table 1 and Table 2. Biasing the ADPA7002CHIP for higher drain current typically results in higher P1dB, output IP3, and signal gain at the expense of increased power consumption (see Table 6 for bias selection per performance).

BIASING THE ADPA7002CHIP WITH THE HMC980LP4E

The HMC980LP4E is an active bias controller that is designed to meet the bias requirement for enhancement mode and depletion mode amplifiers like the ADPA7002CHIP. The HMC980LP4E provides constant current biasing over temperature and device to device variation. Additionally, the HMC980LP4E properly sequences gate and drain voltages to ensure safe amplifier operation, and offers self protection in the event of a short circuit. The active bias controller contains an internal charge pump that generates negative voltage that is needed for the ADPA7002CHIP gate and that can also be used as an external negative voltage source.

For more information regarding the usage of HMC980LP4E, refer to the HMC980LP4E data sheet and the AN-1363 application note.

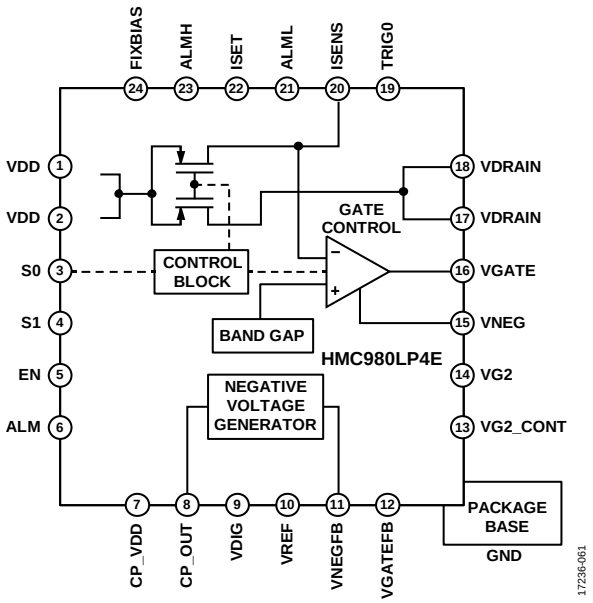


Figure 58. Functional Diagram of HMC980LP4E

Application Circuit Setup

Figure 59 shows a schematic of an application circuit of the HMC980LP4E used with the ADPA7002CHIP. Refer to Figure 60 for an application circuit diagram if using external negative supply for the VNEG pin.

In the application circuit, the ADPA7002CHIP drain voltage and drain current are set by the following equations:

$$VDRAIN\ (5\ V) = V_{DD}\ (5.68\ V) - IDRAIN\ (800\ mA) \times 0.85\ \Omega$$

$$IDRAIN = 150\ \Omega \times R10\ (187\ \Omega)$$

where:
V_{DD} is the supply voltage to the HMC980LP4E.
IDRAIN is the output current from Pin 17 and Pin 18 on the HMC980LP4E.

Limiting VGATE to Meet ADPA7002CHIP V_{GGx} AMR Requirement

When using the ADPA7002CHIP with the HMC980LP4E, the minimum voltages for VNEG and VGATE need to be limited to −1.5 V to keep them within the absolute maximum ratings (AMR) limit for the ADPA7002CHIP V_{GGx} pad. This is accomplished by setting the R15 resistor and the R16 resistor to the values shown in Figure 59 and Figure 60. Refer to the AN-1363 application note for more information and calculations for R15 and R16.

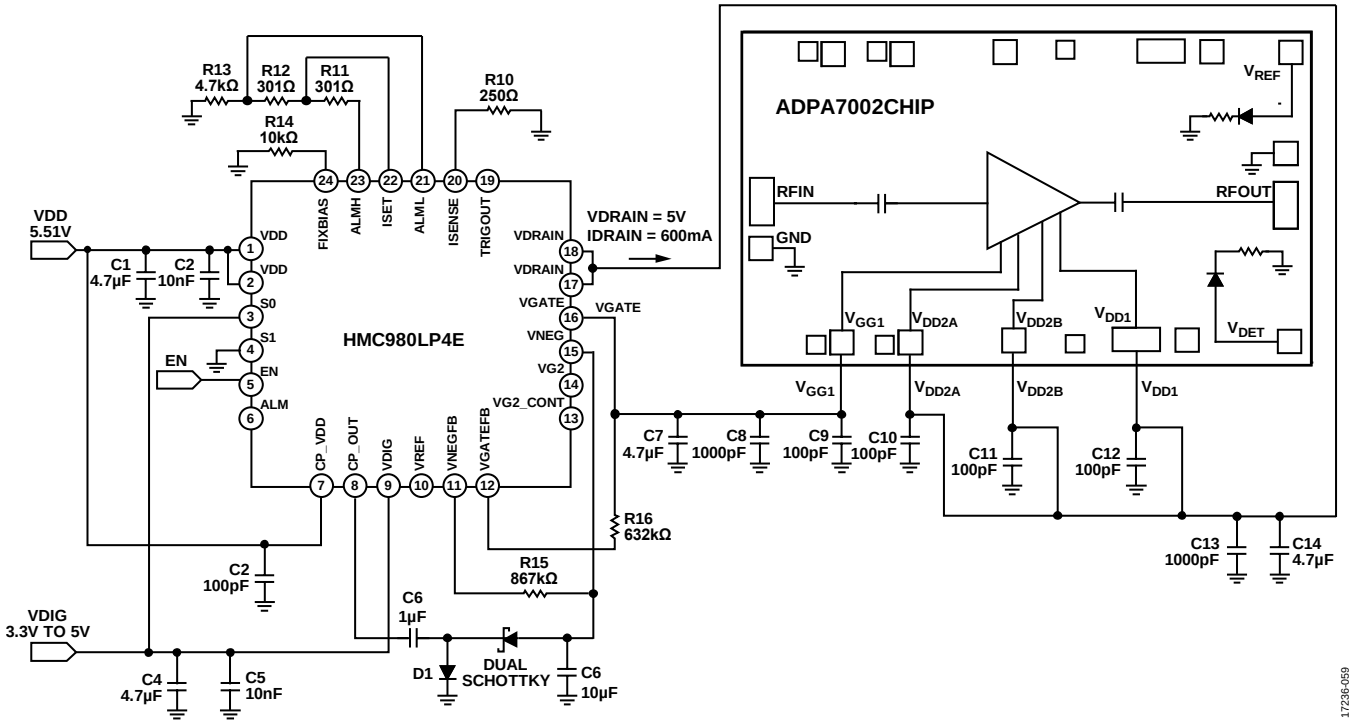


Figure 59. Application Circuit using the HMC980LP4E with the ADPA7002CHIP

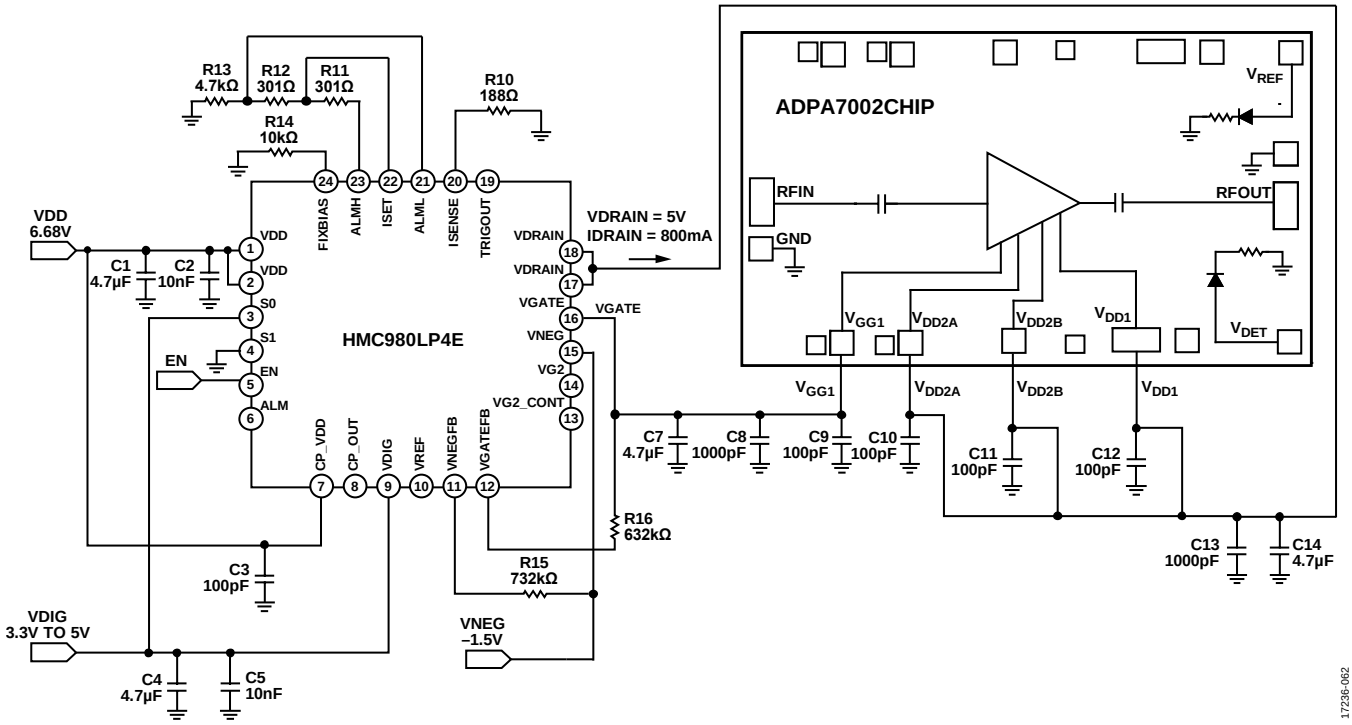


Figure 60. Application Circuit using the HMC980LP4E with the ADPA7002CHIP as an External Negative Voltage Source

HMC980LP4E Bias Sequence

Proper dc supply sequencing is required to prevent damage to HMC980LP4E. Adhere to the following power-up sequence steps:

1. Set VDIG, the voltage supply input (Pin 9) for the HMC980LP4E digital circuit (see Figure 60) to 3.3 V.
2. Set S0, the digital control pin (Pin 3) that sets the internal field effect transistor (FET) and the internal HMC980LP4E resistor (RDS) resistance (see Figure 60) to 3.3 V.
3. Set the V_{DD} pin to 5.68 V.
4. Set VNEG to −1.5 V. This step is not needed if using internally generated voltage.
5. Set the EN pad to 3.3 V. Transitioning from 0 V to 3.3 V turns on the VGATE and VDRAIN pads.

Adhere to the following power-down sequence steps:

1. Set the EN pad to 0 V. Transitioning from 3.3 V to 0 V turns off the VDRAIN and VGATE pads.
2. Set VNEG to 0 V. This step is not required if using internally generated voltage.
3. Set the V_{DD} pin to 0 V.
4. Set S0 to 0 V.
5. Set VDIG to 0 V.

When the HMC980LP4E bias control circuit has been set up, the ADPA7002CHIP bias can be toggled on and off by applying 3.3 V or 0 V to the EN pad. If EN is set to +3.3 V, VGATE drops to −1.5 V and VDRAIN is turned on at +5 V. VGATE rises in voltage until IDRAIN equals 800 mA. The closed control loop then regulates IDRAIN at 800 mA. When the EN pad equals 0 V, VGATE is automatically set to −1.5 V and VDRAIN is set to 0 V (see Figure 61 and Figure 62).

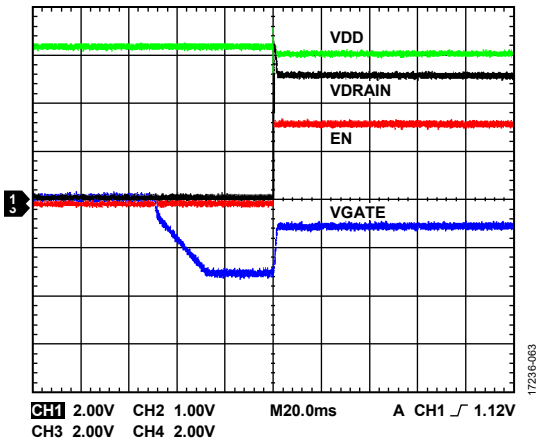


Figure 61. Turn On—HMC980LP4E Outputs to the ADPA7002CHIP

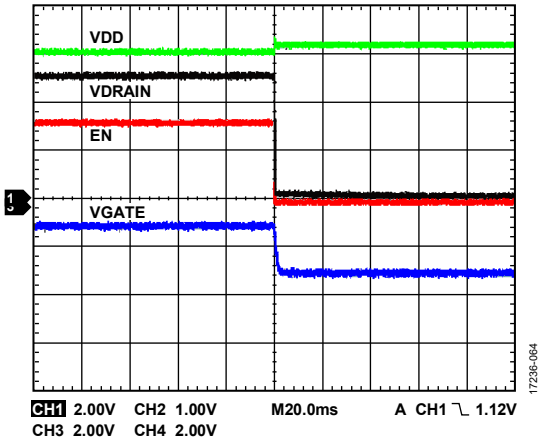


Figure 62. Turn Off—HMC980LP4E Outputs to the ADPA7002CHIP

Constant Drain Current Biasing vs. Constant Gate Voltage Biasing

The HMC980LP4E uses closed loop feedback to continuously adjust VGATE to maintain a constant gate current bias over dc supply variation, temperature and part to part variation. Constant drain current bias is an excellent method for reducing time in calibration procedures and to maintain consistent performance over time.

In comparison to a constant gate voltage bias, where the current increases when RF power is applied, a constant drain current has a slightly lower output P1dB. This effect can be seen in Figure 64 and Figure 66, where RF performance is slightly lower than constant gate voltage bias operation. RF performance is lower due to a lower drain current at high input power levels as the HMC980LP4E reaches 1 dB compression.

The output P1dB performance for the constant drain current bias improves if the constant gate voltage bias is increased. By increasing the set current towards I_{DD}, the output P1dB increases up to the RF drive in the constant gate voltage bias condition shown in Figure 64.

The current and temperature limit of I_{DD} under the constant current operation is usually set by the thermal limitations found in the table from the Absolute Maximum Ratings section along with the maximum power dissipation specification. Increasing the I_{DD} does not indefinitely increase the actual output P1dB and the power dissipation increases. Therefore, consider the trade-off between power dissipation and output P1dB performance when using constant drain current biasing.

Testing the HMC980LP4E

After biasing the ADPA7002CHIP with the HMC980LP4E at the application nodes, compare the results to Figure 63 to Figure 66 to verify that the biasing procedure is correct.

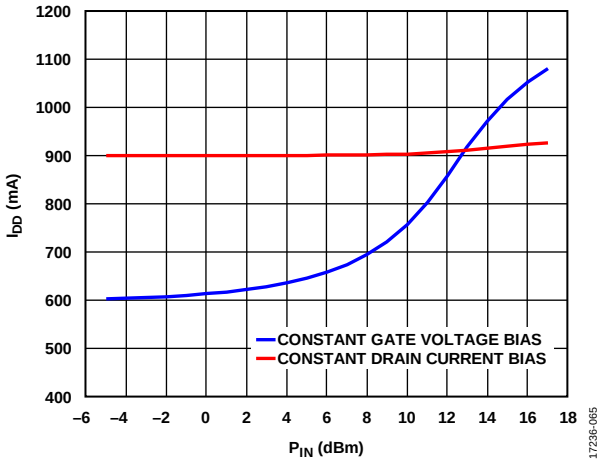


Figure 63. I_{DD} vs. Input Power (P_{IN}), V_{DD} = 5 V, Frequency = 32 GHz, Constant Current Bias and Constant Voltage Bias

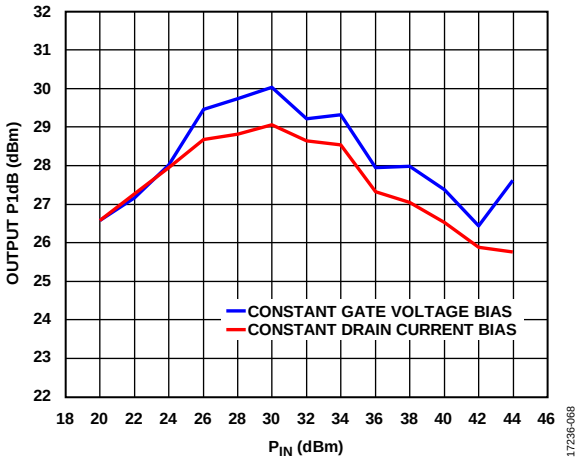


Figure 66. Output P1dB vs. P_{IN}, V_{DD} = 5 V, Frequency = 32 GHz Constant Current Bias and Constant Voltage Bias

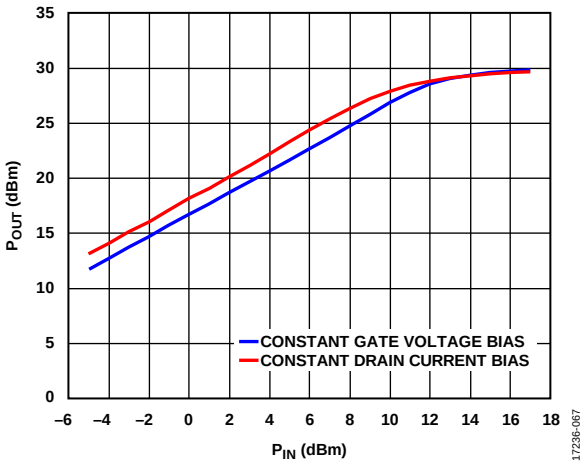


Figure 64. P_{OUT} vs. P_{IN}, V_{DD} = 5 V, Frequency = 32 GHz, Constant Current Bias and Constant Voltage Bias

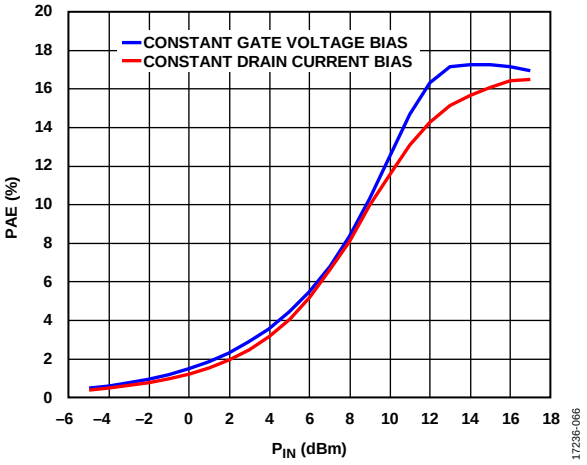


Figure 65. PAE vs. P_{IN}, V_{DD} = 5 V, Frequency = 32 GHz, Constant Current Bias and Constant Voltage Bias

MOUNTING AND BONDING TECHNIQUES FOR MILLIMETER WAVE GAAS MMICS

Attach the die directly to the ground plane with conductive epoxy (see the Handling Precautions section, Mounting section, and Wire Bonding section for instructions).

Microstrip, 50 Ω transmission lines on 0.127 mm (5 mil) thick alumina, thin film substrates are recommended to send the RF to and from the chip. Raise the die 0.075 mm (3 mil) to ensure that the surface of the die is coplanar with the surface of the substrate.

Place the microstrip substrates as close to the die as possible to minimize ribbon bond length. Typical die to substrate spacing is 0.076 mm to 0.152 mm (3 mil to 6 mil). To ensure wideband matching, a 15 fF capacitive stub is recommended to be placed on the PCB board before the ribbon bond. See Figure 67 and Figure 68 for details.

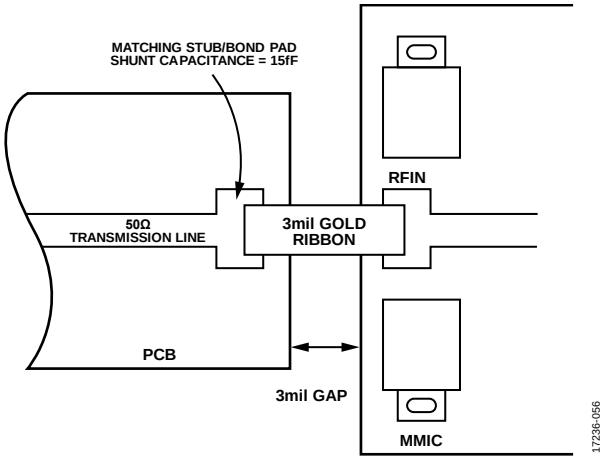


Figure 67. High Frequency Input Wideband Matching

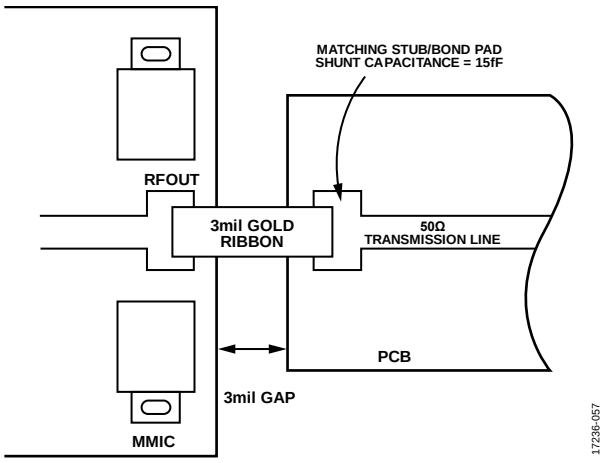


Figure 68. High Frequency Output Wideband Matching

Handling Precautions

To avoid permanent damage to the die, follow these storage, cleanliness, static sensitivity, transient, and general handling precautions:

- Place all bare die in either waffle or gel-based ESD protective containers and then seal the die in an ESD protective bag for shipment. After the sealed ESD protective bag is opened, store all die in a dry nitrogen environment.
- Handle the chips in a clean environment. Do not attempt to clean the chip using liquid cleaning systems.
- Follow ESD precautions to protect against ESD strikes.
- When the bias is applied, suppress instrument and bias supply transients. Use a shielded signal and bias cables to minimize inductive pickup.
- Handle the chip along the edges with a vacuum collet or with a sharp pair of tweezers. The chip surface has fragile air bridges and must not be touched with a vacuum collet, tweezers, or fingers.

Mounting

Before the epoxy die is attached to the ADPA7002CHIP, apply a minimum amount of epoxy (must order separately) to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip after it is placed into position. Cure the epoxy per the schedule of the manufacturer.

Wire Bonding

RF bonds made with 0.003 inch × 0.0005 inch gold ribbon are recommended to be used with the RF ports. These bonds must be thermosonically bonded with a force between 40 *g* to 60 *g*. DC bonds of 0.001 inch (0.025 mm) in diameter, thermosonically bonded, are recommended for bond wire connections. Create ball bonds with a force between 40 *g* to 50 *g*, and wedge bonds with a force between 18 *g* to 22 *g*. Create all bonds with a nominal stage temperature of 150°C. Apply a minimum amount of ultrasonic energy to achieve reliable bonds. Keep all bonds as short as possible, less than 12 mil (0.31 mm).

Alternatively, short (≤3 mil) RF bonds made with two 1 mil wires can be used in place of the gold ribbon.

OUTLINE DIMENSIONS

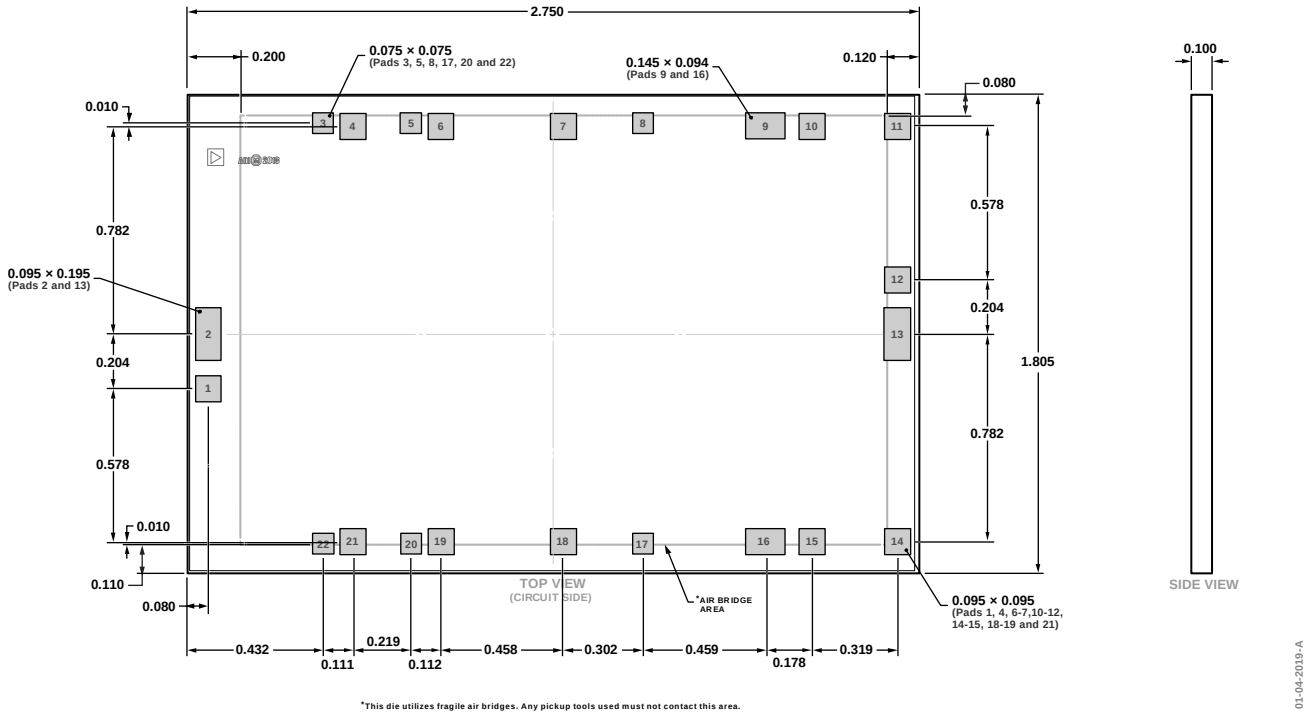


Figure 69. 22-Pad Bare Die [CHIP]
(C-22-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADPA7002CHIP	−55°C to +85°C	22-Pad Bare Die [CHIP]	C-22-3
ADPA7002C-KIT	−55°C to +85°C	22-Pad Bare Die [CHIP]	C-22-3

[1] The ADPA7002C-KIT is a sample order of two devices.