

DIFFERENTIAL OUTPUT SILICON OSCILLATOR

Features

- Quartz-free, MEMS-free, and PLL-free all-silicon oscillator
- Any output frequencies from 0.9 to 200 MHz
- Short lead times
- Excellent temperature stability (±20 ppm)
- Highly reliable startup and operation
 - High immunity to shock and vibration
- Low jitter: <1.5 ps rms
- 0 to 85 °C operation includes 10-year aging in hot environments
- Footprint compatible with industrystandard 3.2 x 5.0 mm XOs
- CMOS, SSTL, LVPECL, LVDS, and HCSL versions available
- Driver stopped, tri-state, or powerdown operation
- RoHS compliant
- 1.8, 2.5, or 3.3 V options
- Low power
- More than 10x better fit rate than competing crystal solutions



1. Inclusive of 25 °C initial frequency accuracy, operating temperature range, supply voltage change, output load change, first-year aging at 25 °C, shock, vibration, and one solder reflow.

2. Inclusive of 25 °C initial frequency accuracy, operating temperature range, supply voltage change, output load change, ten-year aging at 85 °C, shock, vibration, and one solder reflow.

3. See "AN409: Output Termination Options for the Si500S and Si500D Silicon Oscillators" for further details regarding output clock termination recommendations.

4. $V_{TT} = .5 \times V_{DD}$.

5. $V_{TT} = .45 \times V_{DD}$.

Parameters	Condition	Min	Тур	Max	Units
	LVPECL	—	34.0	36.0	mA
	Low Power LVPECL	_	19.3	22.2	mA
	LVDS	_	14.9	16.5	mA
	HCSL	_	25.3	29.3	mA
	Differential CMOS(3.3 V option, 10 pF on each output, 200 MHz)	_	33	36	mA
Supply Current	Differential CMOS(3.3 V option, 1 pFon each output, 40 MHz)	_	16	_	mA
	Differential SSTL-3.3	_	24.5	27.7	mA
	Differential SSTL-2.5		24.3	26.7	mA
	Differential SSTL-1.8	_	22.2	25	mA
	Tri-State		9.7	10.7	mA
	Powerdown		1.0	1.9	mA
Output Symmetry	V _{DIFF} = 0	46 – 13 ns/T _{CLK}	—	54 + 13 ns/T _{CLK}	%
	LVPECL/LVDS		—	460	ps
Rise and Fall Times (20/80%) ³	HCSL/Differential SSTL		_	800	ps
	Differential CMOS, 15 pF, ≥80 MHz		1.1	1.6	ns
LVPECL Output Option	Mid-level	V _{DD} – 1.5	—	V _{DD} – 1.34	V
(DC coupling, 50 Ω to V _{DD} – 2.0 V) ³	Diff swing	.720	_	.880	V _{PK}
Low Power LVPECL Output Option	Mid-level		N/A	—	V
(AC coupling, 100 Ω Differential Load) ³	Diff swing	.68	-	.95	V _{PK}
LVDS Output Option (2.5/3.3 V)	Mid-level	1.15		1.26	V
$(R_{TERM} = 100 \Omega \text{ diff})^3$	Diff swing	0.25	—	0.45	V _{PK}
LVDS Output Option (1.8 V)	Mid-level	0.85	—	0.96	V
$(R_{\text{TERM}} = 100 \ \Omega \ \text{diff})^3$	Diff swing	0.25	_	0.45	V _{PK}
	Mid-level	0.35		0.425	V
HCSL Output Option ³	Diff swing	0.65	—	0.82	V _{PK}
	DC termination per pad	45	-	55	Ω
CMOS Quitaut Valtage ³	V _{OH} , sourcing 9 mA	V _{DD} – 0.6	—	—	V
CMOS Output Voltage	V _{OL} , sinking 9 mA	_	—	0.6	V
SSTI 1.9 Output Valtage ⁴	V _{OH}	V _{TT} + 0.375	—	—	V
SSTE-1.8 Output Voltage	V _{OL}	_	—	V _{TT} – 0.375	v
SSTL 2.5 Output Valtage ⁴	V _{OH}	V _{TT} + 0.48	—	—	V
SSTL-2.5 Output Voltage	V _{OL}	_	—	V _{TT} – 0.48	v
	V _{OH}	V _{TT} + 0.48	—	—	V
SSTE-3.3 Output Voltage	V _{OL}	— — V _{TT} -0		V _{TT} – 0.48	v
Powerup Time	From time V _{DD} crosses min spec supply	_	_	2	ms
OE Deassertion to Clk Stop			—	250 + 3 x T _{CLK}	ns
Return from Output Driver Stopped Mode			-	250 + 3 x T _{CLK}	ns
Return From Tri-State Time		—	—	12 + 3 x T _{CLK}	μs

Notes:

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2. Inclusive of 25 °C initial frequency accuracy, operating temperature range, supply voltage change, output load change, ten-year aging at 85 °C, shock, vibration, and one solder reflow.

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Parameters	Condition	Min	Тур	Max	Units
Return From Powerdown Time		_	-	2	ms
Poriod litter (1-sigma)	Non-CMOS	—	1	2	ps RMS
Penod Siller (T-sigma)	CMOS, C _L = 7 pF	_	1	3	ps RMS
Integrated Phase litter	1.0 MHz – min(20 MHz, 0.4 x F _{OUT}),non-CMOS	_	0.6	1	ps RMS
integrated i hase sliter	1.0 MHz – min(20 MHz, 0.4 x F _{OUT}),CMOS format	_	0.7	1.5	ps RMS

Notes:

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3. See "AN409: Output Termination Options for the Si500S and Si500D Silicon Oscillators" for further details regarding output clock termination recommendations.

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Package Specifications



Table 1. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max	
A	0.80	0.85	0.90	
A1	0.00	0.03	0.05	
b	0.59	0.64	0.69	
D	3.20 BSC.			
е	1.27 BSC.			
E	4.00 BSC.			
L	0.95 1.00 1.0		1.05	

Table 2. Pad Connections

1	OE
2	NC—Make no external connection to this pin
3	GND
4	Output
5	Complementary Output
6	VDD



Table 3. Tri-State/Powerdown/Driver Stopped Function on OE (3rd Option Code)

	Α	В	С	D	E	F
Open	Active	Active	Active	Active	Active	Active
1 Level	Active	Tri- State	Active	Power- down	Active	Driver Stopped
0 Level	Tri- State	Active	Power- down	Active	Driver Stopped	Active







CCCCC = mark code TTTTTT = assembly manufacturing code YY = year WW = work week

Figure 2. Top Mark



Environmental Compliance

Parameter	Conditions/Test Method
Mechanical Shock	MIL-STD-883, Method 2002.4
Mechanical Vibration	MIL-STD-883, Method 2007.3 A
Resistance to Soldering Heat	MIL-STD-202, 260 C° for 8 seconds
Solderability	MIL-STD-883, Method 2003.8
Damp Heat	IEC 68-2-3
Moisture Sensitivity Level	J-STD-020, MSL 3

Ordering Information

The Si500D supports a variety of options including frequency, output format, supply voltage, and tristate/powerdown. Specific device configurations are programmed into the Si500D at time of shipment. Configurations are specified using the figure below. Silicon Labs provides a web-based part number utility that can be used to simplify part number configuration. Refer to www.silabs.com/SiliconXOPartnumber to access this tool. The Si500D XO series is supplied in a ROHS-compliant, Pb-free, 6-pad, 3.2 x 4.0 mm package. Tape and reel packaging is available as an ordering option.





DOCUMENT CHANGE LIST

Revision 0.2 to Revision 0.3

- Revision B to Revision C updated in Ordering Information
- 0 to 85 C° Operating Temperature Range option added

Revision 0.3 to Revision 1.0

- Clarified SSTL specifications.
- Revised Differential CMOS supply current values.
- Clarified Differential CMOS supply current loading conditions.

Revision 1.0 to Revision 1.1

- Updated Ordering information for ±250 ppm from 0 to +85 °C.
- Updated jitter from 1.5 ps to 1.5 ps rms.
- Updated operating temperature to include extended commercial at 0 to +85 °C.
- Updated features to include LVPECL, LVDS, and HCSL.





Disclaimer

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